Pulsed Characterization of Charge-trapping Behavior in High-$\kappa$ Gate Dielectrics

Yuegang Zhao, Keithley Instruments, Inc.
Chadwin D Young, Rino Choi, and Byoung Hun Lee, SEMATECH High-$\kappa$ Material Research

This article discusses the nature of the charge trapping and the limitation of DC characterization techniques in quantifying trapped charge. Then, it describes an ultra-fast pulse I-V technique for characterizing the intrinsic (“trap free”) performance of high-$\kappa$ gate transistors that exhibit the fast transient charging effect (FTCE).

Development of High-$\kappa$ Gates for Advances CMOS Devices

High dielectric constant (high-$\kappa$) materials, such as hafnium oxide (HfO$_2$), zirconium oxide (ZrO$_2$), alumina (Al$_2$O$_3$), and their silicates, have drawn a great deal of attention in recent years for potential use as gate dielectrics in advanced CMOS processes [1]. With high dielectric constants, gate dielectrics can be made thicker than SiO$_2$ while achieving the same capacitance. The result is leakage current that can be lower by as much as several orders of magnitude. However, there are still technical challenges to overcome, such as $V_t$ instability [2-4], carrier channel mobility degradation [5-9], and long-term device reliability [10-13].

One of the important issues preventing implementation of high-$\kappa$ gates is the trapping of charges in the pre-existing traps inside these dielectrics [14-15]. When the transistor is turned on, some of the channel carriers will be accumulated in the gate dielectric due to the vertical electrical field, resulting in a shift of threshold voltage and a reduction in drain current. Fully understanding charge-trapping and these related mechanisms is the key to understanding channel mobility degradation and device reliability problems. However, traditional DC testing techniques may not accurately characterize these mechanisms.

Limitation of DC Characterization Techniques

As charges are trapped in the gate dielectric, the threshold voltage of the transistor increases due to the built-in voltage in the gate capacitor; therefore, the drain current decreases. It appears that charge trapping and de-trapping times strongly depend on the composition of the gate stacks, i.e., physical thickness of the interfacial SiO$_2$ layer and high-$\kappa$ film, as well as process techniques [16-18]. The time scale varies from several microseconds to tens of milliseconds [19]. The de-trapping of the charges is also strongly gate voltage and polarity dependent.

The wide dynamic range of charge trapping, and the voltage dependent trapping and de-trapping, make it very difficult to use one type of characterization technique (especially a DC technique) to get a complete picture of what is going on inside the stacked gate dielectric. For example, commonly used methods employ a double sweep in either DC $V_{gs}$-$I_d$ or high frequency C-V measurements. These techniques involve ramping gate voltage back and forth while drain current or gate capacitance is measured. If hysteresis is seen on the resulting I-V or C-V curves, it is a clear indication of charge trapping inside the gate stacks.

The issue with this technique is that the hysteresis is strongly dependent on measurement time. The hysteresis measured in the DC I-V test could be different from that in a C-V test, because the time taken for each measurement may be dramatically different. This is illustrated by dual sweep C-V measurements taken at different speeds (Figure 1). Test speed is strongly dependent on instrumentation and not easily controlled. Even if it were, there is no model to quantify how much charge is really trapped in the gate during the test; i.e., hysteresis cannot quantify the amount of charge trapped, since a significant portion of the fast transient trapping could be lost in the DC measurement.

Another method involves DC stress voltage to inject charges intentionally into the gate, then the use of C-V or I-V method to
measure the flat band voltage or threshold voltage shift [20]. The amount of charge trapped can be calculated based on this formula:

\[ Q_{\text{trap}} = C_{\text{gate}} \cdot \Delta V_{\text{fb}} \text{ or } Q_{\text{trap}} = C_{\text{gate}} \cdot \Delta V_{1}. \]

The issue with this technique is the transition period between DC stress and I-V or C-V measurement, when typically there is no applied voltage, or voltage is very low compared to the stress condition. When stress voltage is off, the charges trapped in the gate can de-trap in as little as tens of microseconds. So, only a fraction of the total trapped charges are measured due to the relaxation effect, resulting in an overly “optimistic” view of the film’s quality.

**Ultra-short Pulse Characterization Techniques**

Better methods have been developed over the past few years [3, 4, 19, 21] for capturing the fast transient behavior of charge trapping. Figure 2 shows two different test configurations for a Single Pulse Charge Trapping (SPCT) measurement. In both setups a pulse is applied to the gate of the transistor while its drain is biased at a certain voltage. The change in drain current, resulting from the gate pulse, appears on the digital oscilloscope.

The key to using SPCT is to look at charge trapping and de-trapping within a single, well-configured gate pulse (Figure 3). The pulse usually starts in a position that discharges the gate capacitor before the voltage ramp begins. This is to clean up any residual charges trapped in the gate. Then, during the rise time of the voltage ramp, the corresponding drain current response is captured, allowing a \(V_{g}-I_{d}\) curve to be formed.

If the pulse rise time is fast enough that there is no charge trapping, then the \(V_{g}-I_{d}\) curve represents the transistor’s intrinsic behavior, free from error due to spurious charge-trapping effects [16]. During the plateau of the pulse, the transistor is turned on, and some of the channel carriers might be trapped in the gate, which changes the threshold voltage and causes the drain current to drop. During the fall time of the pulse, another \(V_{g}-I_{d}\) curve is formed, but with the charge-trapping effect that should be measured.

**Figure 4a** shows an example of a pulse I-V measurement with different pulse speeds using setups from **Figures 2a** and **2b** respectively. A DC I-V curve is overlaid for comparison. There is hysteresis with
the slower pulse due to charge trapping. By using the faster pulse, hysteresis is eliminated because there’s insufficient response time for charges to be trapped.

Slower pulse measurements should only be used for high-κ devices with relatively low charge-trapping effects. Although the hysteresis of a slower pulse I-V curve can quantify charge trapping better than a DC method, results must be interpreted with caution, since de-trapping effects are influenced by the specific structure of the gate stack and the pulse fall time. Also, when two traces in the tr and tf portions are not parallel, it is difficult to define the point at which hysteresis is measured.

An alternative approach is to plot pulse $I_d$ versus time (Figure 4b). An evaluation of the pulse width portion of $I_d$ (where $I_d$ degrades) can be used to quantify trapped charge [15, 16]. Still, to ensure negligible charge trapping during the entire pulse, one can use a fast pulse with short rise and fall times. This can be achieved easily with the ultra-short-pulse test system in Figure 2b. It produces $I_d-V_g$ values by using a single pulse per point of less than 100ns.

**Benefits of Short Pulse Characterization**

Since there is much less charge-trapping effect with very short pulse widths, the drain current measured is higher than under DC conditions (red curve, Figure 4a). This results in a higher predicted channel carrier mobility when pulse I-V data are used to generate a model, which is more representative of transistors that are switching very fast (i.e., those that will not experience full charge-trapping effects). Another advantage of the ultra-short pulse system is that the pulse I-V measurements, with pulse widths on the order of nanoseconds, can be performed very easily and results can be compared to a DC measurement without resetting the system hardware or moving the wafer to another station. Such a comparison is shown in Figure 5.

Drive current measured using the pulse I-V technique can be significantly higher than DC due to the lack of charge-trapping effects. This illustrates the close-to-intrinsic performance of transistors with high-κ gate dielectrics, and ultimately demonstrates the advantage of the ultra-short pulse I-V technique.

Because of complications associated with trying to characterize charge-trapping effects for transistors with different functionalities, including high frequency operation, the best solution for modeling engineers is to use instrumentation and a test configuration that avoids artifacts associated with DC or slower pulse measurements. The ultra-short pulse measurement technique provides a better depiction of real device performance [22], so the resulting models help optimize designs for actual operating conditions.

Process engineers also need these pulse measurement techniques to characterize and track improvements in their continuing efforts to improve film quality and remove charge-trapping degradation. Finally, an understanding of the intrinsic behavior of high-κ gate dielectric devices is key to understanding the physics of charge trapping.

![Figure 4. Single Pulse Charge Trapping measurements: (a) the ultra-short ramped pulse $I_d-V_g$ and slow "single pulse" pulse with hysteresis (DC result is shown as a reference), and (b) corresponding slow pulse versus time illustrating an alternative approach to determine the degradation of $I_d$.](image1)

![Figure 5. Overlay of ramped pulse I-V and DC I-V measurements on NMOSFET with high-κ (HfO2) gate dielectric: (a) DC and pulsed $Id-Vg$ measurement at linear region, (b) DC and pulsed $Id-Vd$ measurement. Short pulse parameters allowed close-to-intrinsic drive current to be measured and compared to the DC measurement.](image2)
and de-trapping. This physical-based understanding leads to the correct extrapolation of device lifetime.

**Sources of Error**

Although ultra-short pulse measurements are a powerful technique, recognize that speed characteristics are in the radio frequency (RF) domain. Therefore, it is easy to introduce measurement errors if the test system is not optimized for high bandwidth. There are three main sources of errors: signal losses due to cables and connectors, losses due to device parasitics, and contact resistance.

Signal losses due to cables and connectors, as well as contact resistance effects, can be calibrated out using a transistor with a SiO₂ gate, where there is no charge-trapping effect. The pulse I-V curve should overlay the DC I-V curve precisely once the calibration is complete.

However, device parasitics, usually parasitic capacitance between pad contacts, cannot be easily removed. This will reduce the pulse current from the drain terminal. This problem can be designed out by using RF-compatible transistor structures (Ground-Signal-Ground), and by increasing pad pitch so that capacitance between the pads is small enough not to affect pulse current measurements.

**Conclusion**

DC characterization techniques are inadequate for capturing the dynamic nature of charge trapping in high-k gate stack structures. Pulse I-V is a powerful technique that allows characterizing transistors with high-k gate stacks in a trap-free environment that permits assessing their intrinsic qualities. When current is measured in a shorter time than that associated with the charge-trapping time scale, improved intrinsic transistor characteristics can be achieved, including a drive current that is significantly higher than that measured with traditional DC I-V techniques.

**References**


May 2006

Pulsed Characterization of Charge-trapping Behavior in High-$\kappa$ Gate Dielectrics