# Memory Testing Solutions

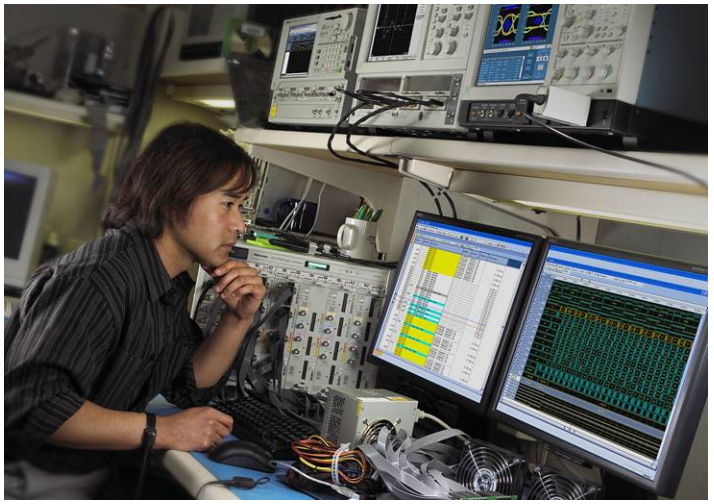
## Fast and Accurate Testing Solution to Resolve Your Memory Design Challenges

Application Fact Sheet

Continual demand for memories to be larger, faster, lower powered and physically smaller is driving the advancement of SDRAM technology. Tektronix' powerful and comprehensive test instrument portfolio for SDRAMs, memory controllers, DIMMs, computer motherboards and embedded systems will help you resolve design challenges quickly and efficiently.

**Memory Testing Challenges:**

| | |
|---|---|
| Digital Validation and Debug | ▪ Read and write data analysis<br>▪ Export data to simulation programs and other ATE<br>▪ SDRAM initialization analysis<br>▪ SDRAM commands sequences and timing analysis<br>▪ Data valid windows analysis with high resolution timing<br>▪ Time correlated memory analysis with system-level visibility of other buses |
| Electrical Validation and Debug | ▪ Address and command signal integrity<br>▪ Address and command timing analysis<br>▪ Clock, strobe and data signal integrity<br>▪ Clock, strobe and data timing analysis<br>▪ MCH to DRAM and system debugging<br>▪ Ref clock parametrics and analysis<br>▪ Ref clock DLL performance |
| Signal Path Characterization | ▪ Cross talk (single-ended and differential)<br>▪ Trace impedance (single-ended and differential)<br>▪ Trace length (single-ended and differential) |





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### Digital Validation and Debug

**TLA Series Logic Analyzers with Nexus Technology Memory Supports**

- Up to 20 ps timing resolution on all channels, all the time
- SDRAM protocol violation analysis
- Selective clocking stores useful data in the logic analyzer
- Complete system visibility with digital/analog correlation
- Data valid window analysis for setting sample point positions
- No preprocessor is required
- Industry leading high resolution timing

### Electrical Validation and Debug

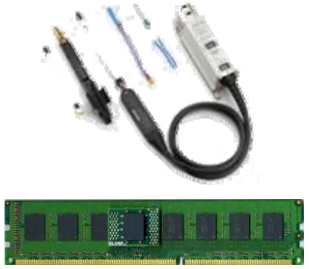
**DPO/DSA/MSO Series Oscilloscopes and Analysis Software**

- Support for multiple DDR standards (DDR1, DDR2, DDR3, GDDR3, LPDDR, LPDDR2, custom rates, and more)
- Built-in clock, strobe and data JEDEC compliance measurements
- SDRAM eye diagram with strobe information for read or write cycles
- Advanced measurement debug capabilities with DPOJET jitter and eye analysis tools
- Command bus triggering and decoding for complete system insight including logic qualified triggering using MSO Series
- Automatic read and write bursts identification with Advanced Search and Mark

### Signal Path Characterization

**DSA Series Sampling Oscilloscopes and Application Software**

- TDR impedance measurements and S-parameter characterization of the PCB traces
- Emulate the channel effect on jitter and noise using the channel's TDR/TDT or Touchstone® (S-parameter) description
- Over 70 GHz of sampling bandwidth and the lowest jitter floor



### SDRAM Probing Solutions

**TriMode Probes, Interposers, and Mid-Bus Probes**

- Wide selection of TriMode™ probe tips provide quick and easy attachment, improved usability and low cost per solder point
- Multiple connection solutions, including BGA/slot interposers, mid-bus probes, and instrumented DIMMs
- Eliminate double probing with iCapture™ multiplexing to achieve simultaneous digital and analog acquisition through a single probe connection



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