High-speed Interconnects

Characterization and Measurement–Based Modeling

Tektronix

Enabling Innovation

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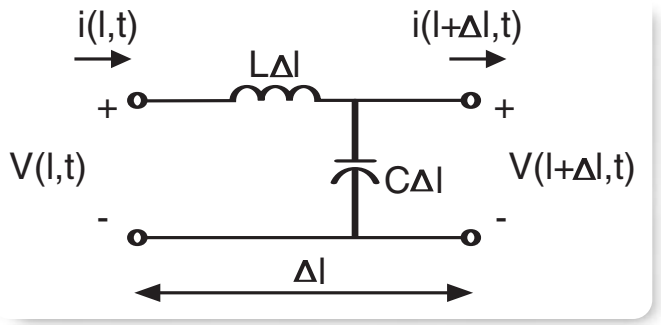
Electrical Characteristics of Interconnects

As the performance requirements for modern computer and communications systems grow, the demand for high speed interconnects increases as well. Multi-gigabit speeds are supported by standard communication technologies, with the signal s rise times being as fast as 35ps (10-90%). At these speeds, cables, connectors, vias and traces on printed circuit boards (PCBs) behave as distributed elements, or transmission lines. Moreover, reflections due to impedance mismatch, signal s rise time degradation due to the interconnect losses, and crosstalk due to coupling are typical signal integrity problems that system-level designers encounter in their work. Therefore, to accurately predict the propagation of the signals in their designs, engineers need to determine the electrical characteristics and to build reliable models of the interconnect structures.

Depending on the signal s speed and the device s physical properties, any electrical interconnect can fall into a low-loss or high-loss category. Interconnects that carry slow signals may have relatively ideal properties. On the other hand, faster signals, propagating the same interconnect, have greater frequency content and require consideration of non-ideal interconnect effects. The loss mechanism is more easily understood by analyzing circuit models for transmission lines. The following subsections will describe ideal and lossy transmission lines concepts in more detail.



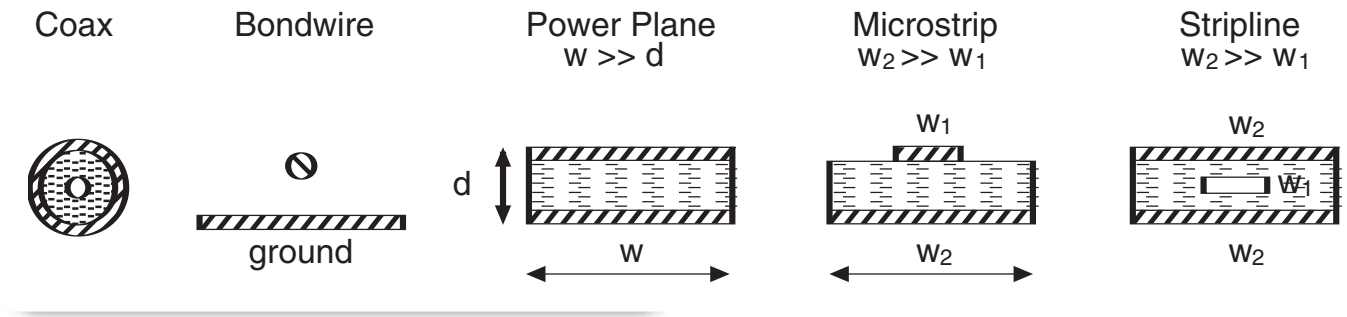
▶ **Figure 1.** *Circuit model for a short segment of the ideal transmission line. Conductor and dielectric losses are ignored.*

Ideal Transmission Line

In order to understand important characteristics of interconnect structures it is imperative to start from the general representation of the ideal transmission line model. The ideal transmission line does not exhibit losses associated with conductors and dielectrics of the mediums that carry such signals. Thus, an ideal transmission line can be described as a distributed parameter network consisting of capacitors and inductors to represent interactions due to electric and magnetic fields. A short sub-segment of the ideal transmission line can be modeled using a circuit shown in Figure 1. Circuit representation of the transmission line allows deriving partial differential equations which are generally called telegrapher s equations. A solution of these equations in terms for propagating voltages and currents, allows deriving important characteristics of the ideal transmission line, such as characteristic impedance and time delay.

For the single ideal conductor, the characteristic impedance, Z_0, is described by the following formula:

$$Z_o = \sqrt{L/C} \qquad (1)$$



▶ **Figure 2.** *Cross-sectional views of some typical interconnects.*

where L and C are inductance and capacitance of the line per unit length respectively. It is important to note that increase in the inductance per unit length leads to the increase of characteristic impedance, and the increase of the capacitance causes the decrease of the characteristic impedance. L and C values and their ratio can be controlled by the geometry and material properties of the interconnect. Time delay of the ideal transmission line can be expressed in terms of inductance and capacitance per unit length as:

$$t_d = \sqrt{L \cdot C} \qquad (2)$$

Real Interconnects

Real interconnects are fabricated using materials that exhibit losses. Figure 2 shows typical cross-sections of different interconnects. The interconnect structures consist in general combinations of different types of interconnects, and each transition among them contribute to the reflections. Geometrical configurations and material properties of these structures affect the distribution of electric and magnetic (EM) fields. The EM field interactions in their turn completely govern electrical performance of the device which can be described mathematically by a set of so called Maxwell equations. Therefore, the choice of materials and geometry for interconnects is critical for minimizing signal integrity problems. In this sub-section we will concentrate on losses, and the reflections will be discussed in the section True Impedance Profile.

Conductor[1] and dielectric losses are two major loss contributors in the interconnect structures. The conductor loss originates from a finite conductivity of the medium used to fabricate a conductor, while the dielectric loss is a result of the displacement currents in the insulator material. The best performance is expected from the air dielectric, all other materials contribute to the dielectric losses. Conductor and dielectric losses are frequency dependent and normally increasing with the increase of the operational frequency. In typical interconnects, the conductor loss dominates at the lower frequencies while the dielectric loss becomes more pronounced at the higher frequencies.

[1] Conductor loss is the loss that is typically associated with metals that constitute the conductors; this loss is often referred as "metal" loss.

The equivalent circuit that shows both metal and dielectric losses is shown in Figure 3. This representation differs from Figure 1 by having extra resistive term in series with the inductor and conductive term in parallel with the shunt capacitor. Therefore, the classic equation (1) for the characteristic impedance of a transmission line in presence of losses changes to:

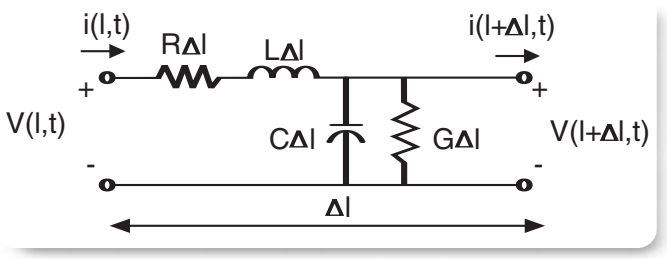
$$Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \qquad (3)$$

where R and G are resistance of transmission line conductor and conductance of the dielectric per unit length respectively, and ω is operational frequency in rad/sec.

Time delay formulation (2) under presence of the losses consequently changes to the following equation:

$$t_d = \sqrt{(R + j\omega L)(G + j\omega C)} \qquad (4)$$

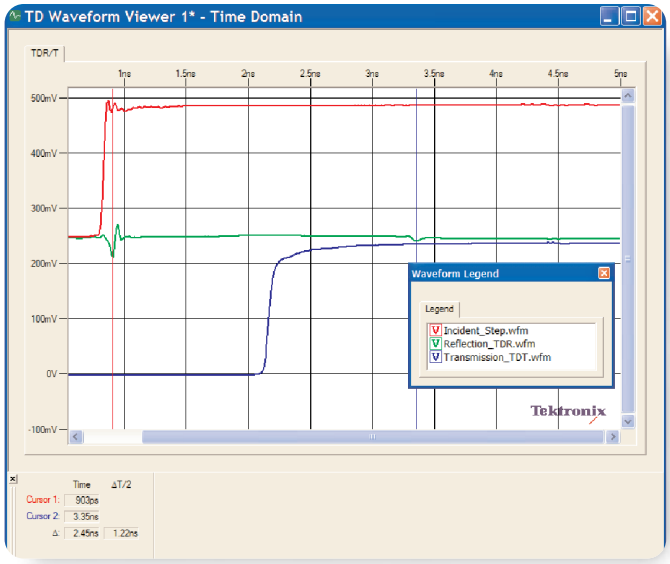
Quick analysis of the equations (3) and (4) shows that loss in the transmission lines not only slows down signals propagation, but also causes frequency dependency of the characteristic impedance Z_0. Moreover, both



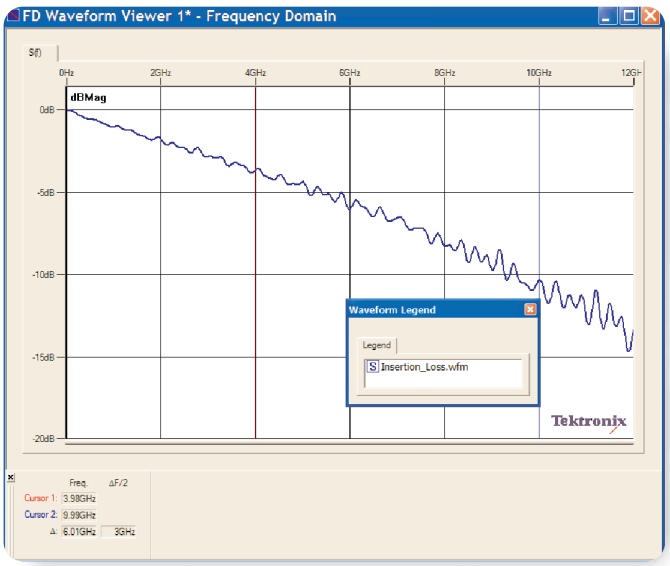
▶ **Figure 3.** *Equivalent circuit model for a lossy transmission line segment includes conductor resistance and dielectric conductance, which may be frequency dependent. Δl is the length of the transmission line segment.*

R and *G* may vary with frequency. Inductive and capacitive parts may vary with frequency as well, but as we will see, one can account for it in the resistive terms.

The loss parameters described in this section can be extracted from the measurement data and then be used in SPICE circuit simulators to model lossy transmission line behavior. This measurement-based extraction approach is usually done using optimization of predefined values and implemented in some modeling applications such as Tektronix IConnect® software.



▶ **Figure 4a**



▶ **Figure 4b**

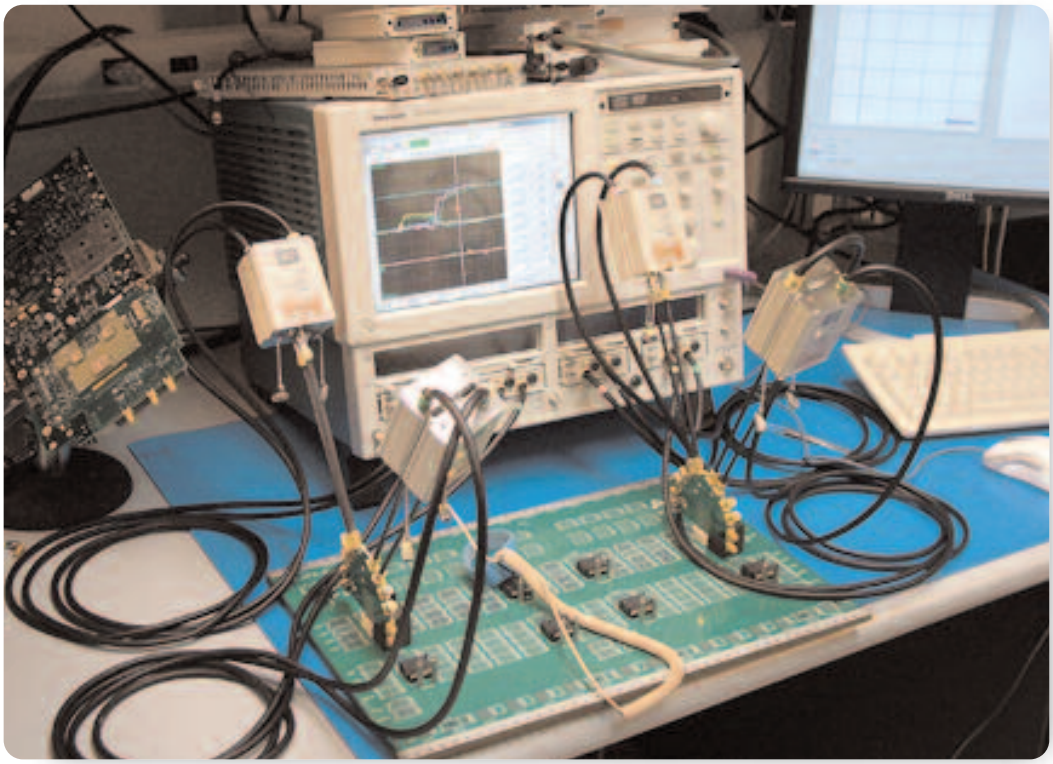
Time (a) and frequency (b) domain representation of the losses for a 50 ohm stripline fabricated on FR4 material. Signal's rise time after the transmission through the interconnect is much slower. Frequency domain plot shows increasing losses by decreasing behavior of the insertion loss as the operational frequency increases.

In practical terms interconnect losses can be observed and measured in time and in frequency domains. When a step signal with certain rise time is applied to the interconnect structure at the transmitter s end, its transition time degrades by the time it reaches the receiver s end. Therefore, if someone measures a signal s rise time before entering interconnect and after exiting it, the rise time values will be different. This can be observed in Figure 4a, where both incident and transmitted steps are displayed for an interconnect that is made of a strip line fabricated using copper on FR4 material. In frequency domain the interconnect losses will result in decreasing behavior of the insertion loss parameter which is related to the ratio of the transmitted wave over the incident wave. The corresponding plot for the same interconnect is shown in Figure 4b.

Basics of TDR/T measurements

Time Domain Reflectometry (TDR) has traditionally been used for locating faults in cables. A failure analyst can use TDR impedance measurements to locate faults very accurately and quickly by sending a voltage step and observing time domain reflected waveform from the failing device. Moreover, TDR allows determining the physical nature of the failure by comparing the impedance changes of the reflected waveform.

Time domain sampling oscilloscopes employ samples to extend the range of the conventional oscilloscope to measure high frequency signals. With current technologies developed at Tektronix, measurements of signals as high as 70 GHz can be done. The instruments detect a repetitive waveform, and work on the principle of taking a sample once per cycle, over several cycles, with each sample point being shifted from the previous point. The complete picture of the waveform is stored, and can be displayed as a stationary signal.



▶ **Figure 5.** *TDR measurements of a gigabit backplane with DSA8200 sampling oscilloscope. The high-speed sampling modules of the instrument are connected to the backplane's daughter cards using semi rigid coaxial cables.*

Currently, high performance TDR instruments, coupled with add-on analysis tools, are commonly used as the tool of choice for failure analysis and signal integrity characterization of boards, packages, sockets, connectors, cables and other interconnects at gigabit speeds. Based on the TDR impedance measurements, the designer can perform signal integrity analysis of a system s interconnect, and the performance of digital system as the whole, can be predicted accurately.

The TDR instrument can be connected to the device under test (DUT) via cables, probes or test fixtures. Figure 5 shows TDR connections to the DUT for differential crosstalk measurements of a gigabit backplane. Time domain step with fast rise time is applied to the main differential lane, and the reflected response is measured as TDR, while the transmitted response is measured as TDT (time domain transmission); the TDT response measured at the adjacent traces shows signal coupling due to crosstalk. Typical numbers for the rise time that can be delivered to the DUT vary for different vendors, and the numbers within 10-45 ps can be easily achievable.

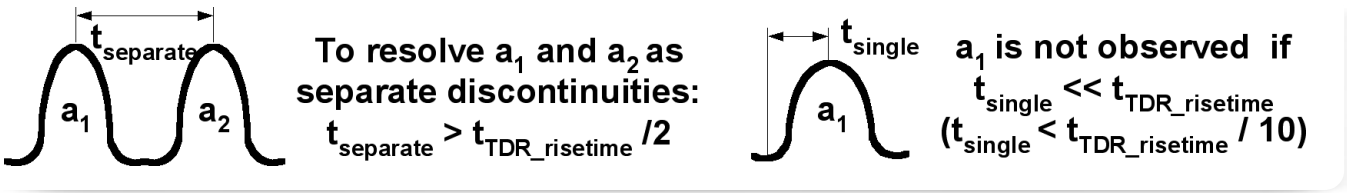
▶ **Figure 6.** *Differential probe P80318 by Tektronix, Inc. The probe uses advantage of virtual ground plane in differential signaling to eliminate the need for ground connection.*

The measurement instrument with faster rise time provides wider measurement bandwidth. However, with the faster TDR system rise times, the DUT traces may exhibit losses that are not present under normal operating conditions for the DUT. In addition, the impedance that the lumped discontinuities present to the test signal is dependent on the highest frequency present in the test signal. The relationship between the signal s rise time and the equivalent 3 dB bandwidth can be approximated using the following expression:

$$f \approx 0.35 / t_{rise} \quad (5)$$

Where t_{rise} is the signal s rise time, f is the frequency at which the step response rolls off by 3 dB, and 0.35 comes from the single-pole exponential decay assumption [1].

Therefore, to ensure that this bandwidth and fast rise time can be delivered to the DUT, an engineer must use high-quality cables, probes, and fixtures, since these cables, probes and fixtures can significantly degrade the rise time of the instrument, reduce the resolution, and decrease the impedance measurement accuracy. In a TDR probe, both a signal and a ground contact are normally required during the measurement. The only exception to this rule occurs when the response is measured using a differential step. Such measurements can be performed using a so-called differential probe similar to the one shown in Figure 6.



▶ **Figure 7.** *TDR resolution rules of thumb, in order to observe two discontinuities as separate ones, the measurement system rise time has to be at least twice as fast as the distance between them.*

When performing TDR measurements it is important to understand that the time or spatial resolution depends on the measurement signal rise time. The faster signal s rise time, the finer features of the DUT someone will be able to resolve. Nevertheless, the issues of TDR resolution are often misunderstood or misrepresented, because the TDR resolution is believed to be completely governed by the following rule of thumb. Two small discontinuities, such as two vias in a PCB, can still be resolved as two separate ones, as long as they are separated by at least 1/2 the TDR rise time as illustrated in Figure 7.

If these two vias are not separated by half the TDR rise time, they will be shown by TDR as a single discontinuity. Assuming we use good cables, probes, fixtures, and we can deliver the full 30-40 ps rise time of the instrument to the discontinuities in question, the minimal physical separation between these vias will be 15-20 ps. For FR4 board material with dielectric constant E_r=4, this results in 2.5 - 3 mm (0.1) resolution. Often this number (or other similar calculation) is quoted as the TDR resolution limit.

However, in real-life situation, the designer typically is looking to observe or characterize a single discontinuity, such as a single via, or a single bondwire in a package, rather than separate several of such vias or bondwires. In this case the designer is to observe discontinuities of 1/10 to 1/5 of the TDR rise time, bringing the numbers above to 5 ps or less than 1 mm (25 milliinches) range.

Furthermore, there are well developed relative TDR procedures for observing and characterizing even smaller discontinuities. For signal integrity modeling and lumped interconnect analysis, there are JEDEC standard procedures for package characterization, allowing the designer to measure sub-millimeter capacitive and inductive elements in 100 fF and 200-300 pH range (3). For failure analysis applications, there are well-established procedures utilizing golden device comparisons, where the measured DUT is compared with a known response from a good device [4], [5].

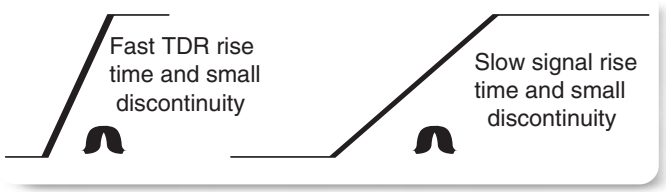
Taking this discussion further, practically all modern high-speed digital standards and applications — from Gigabit Ethernet to Infiniband — still have rise times which are slower than the 30-40 ps rise times of the TDR. Since TDR waveforms show the designer how a certain discontinuity would exhibit itself in the signal path, then if the discontinuity does not cause a reflection of fast TDR signal, it will have even less effect on the slower real signal propagating through this discontinuity. Therefore, if the fast TDR rise time does not allow the designer to observe a certain discontinuity, then an even slower real signal will now show it either as illustrated by Figure 8.

The bottom line is that the engineer has to understand goals of characterization before performing the measurements. For example if the primary goal is to do failure analysis techniques then the faster rise time is the better. On the other hand if the primary goal is to do interconnect modeling, then the responses can be filtered down to the desired rise time.

Even the best TDR cables and probes will degrade the rise time of the signal measured on the TDR oscilloscope. The delivered rise time, $t_{measured}$, measured at the end of the instrument s probes or fixtures is determined as follows:

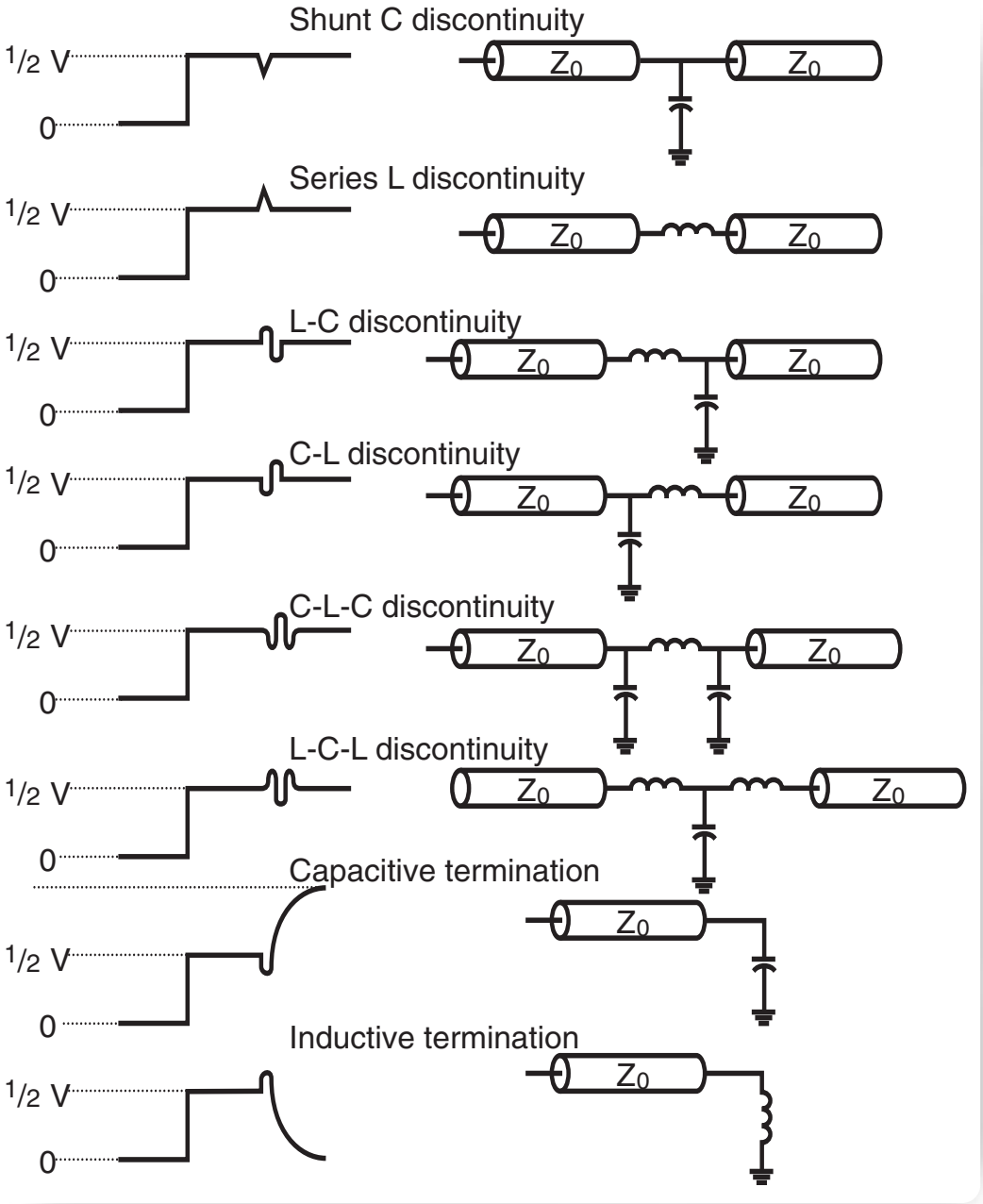
$$t_{measured} = \sqrt{t_{TDR}^2 + 2 \cdot \left(\frac{0.35}{f_{3dB}} \right)^2} \qquad (6)$$

where t_{TDR} is the rise time measured on the TDR scope with no cable connected, and f_{3dB} is the 3 dB bandwidth of the cable and probe. The factor of two in this equation is due to the fact that the signal has to take a roundtrip through the cable before it is observed and measured on the oscilloscope. Specifying a cable with a 3 dB bandwidth (f_{3dB}) of about 10 GHz for the scope with its own rise time of 30 ps, will result in the rise time at the cable end of about 58 ps. Specifying 3 dB bandwidth of 17.5 GHz will give the rise time end of the cable of about 40 ps.



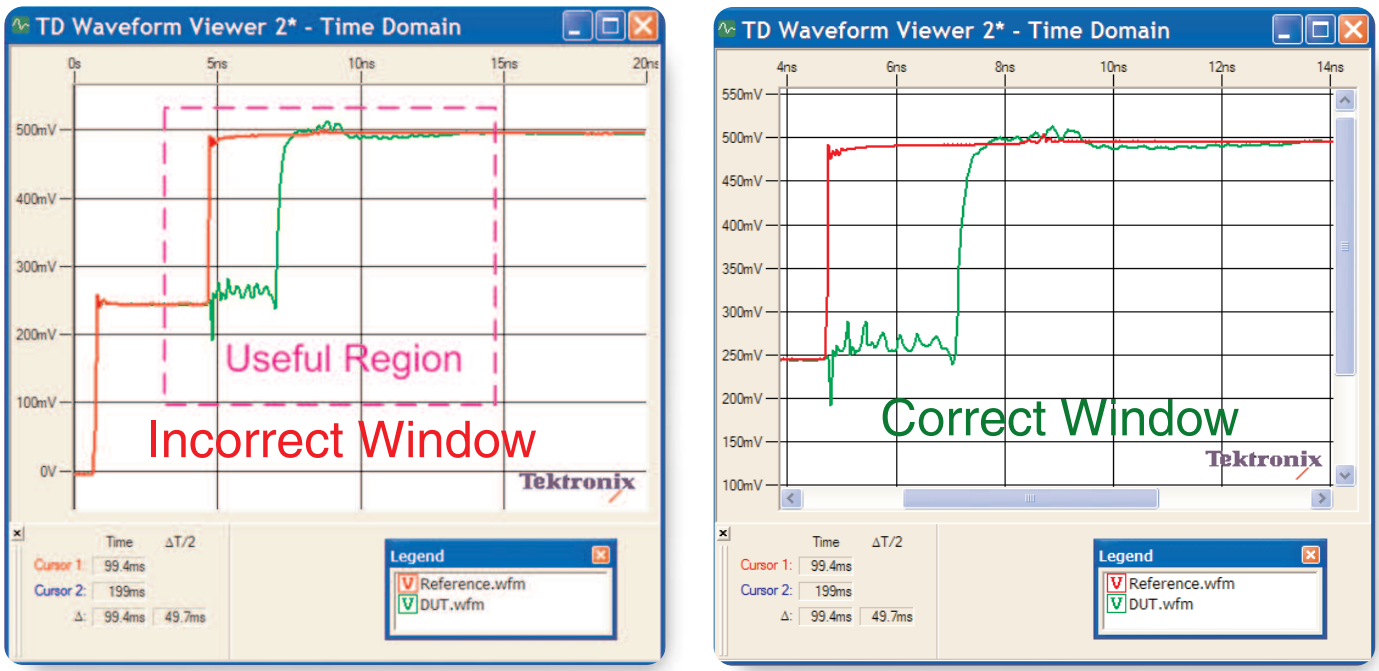
► **Figure 8.** *If the fast rise TDR time does not reflect from a certain discontinuity (left), then a slower signal in a real application will not reflect from it either; the signal will not be affected by this discontinuity.*

TDR waveform allows making a conclusion not only about the locations of the discontinuities at the transmission line but also about their types. Formula 1 shown in the first section shows that the increase of the characteristic impedance of the transmission line indicates the increase of inductance, whereas, the decrease of the impedance may indicate the increase of the shunt capacitance. For example, an engineer can, without difficulty, recognize a “dip“ in a TDR waveform as a shunt capacitance, and a “spike“ as a series inductance. Any L and C combination can also be represented as shown in Figure 9. Hence, a simple reflected voltage signature provides the easy approach to define circuit models for interconnects.



▶ **Figure 9.** *Visual lumped (LCR) interconnect analysis using TDR. Left column represent a TDR voltage waveform, and the right column correspond to the circuit model that can be applied to the particular discontinuity.*

This approach, however, needs to be carefully applied. For example, a series C or a shunt L, will represent a high-pass filter for the TDR signal, and the resulting reflection from the elements beyond such series C or shunt L can not be interpreted without prior knowledge of the DUT topology. Multiple reflections may also affect the accuracy by introducing "artificial" inductors and capacitors. In this case the impedance peeling algorithm that will be discussed in the following sections needs to be applied.



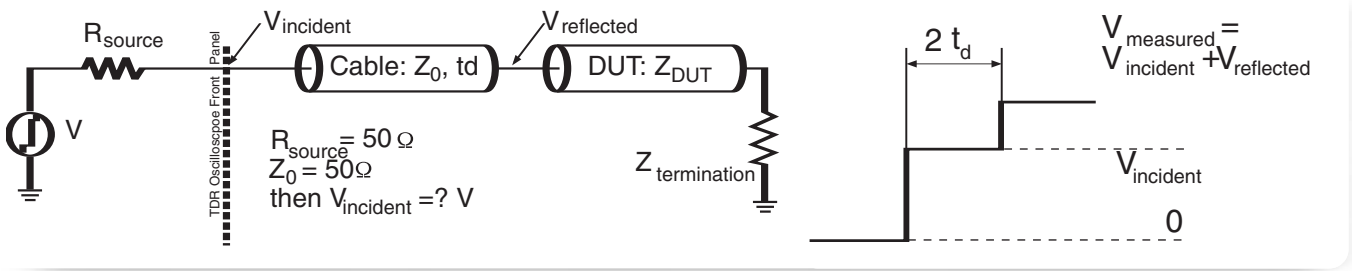
▶ **Figure 10.** *Proper windowing of the TDR waveform for further analysis in IConnect TDR software. The properly windowed waveform will exclude the first transition, corresponding to the interface between the TDR sampling head to the cable, but will keep the window sufficiently long to allow all the reflections corresponding to the DUT, to be included in the window.*

Good Measurement Practices

When using a TDR oscilloscope, it is important to follow good measurement practices. This allows obtaining a quality measurement data that can be used in impedance calculations, failure analysis or in signal integrity modeling applications. The instrument should be turned on and its internal temperature should be allowed to stabilize for 20-30 minutes before performing any measurements. Calibration, compensation and normalization for the instrument must be performed regularly, as specified by the instrument manufacturer. The internal instrument temperature must be within the specified range from the calibration points for the given instrument.

Special care needs to be taken in regards of high frequency connectors used in the measurements. They should be inspected and cleaned regularly because a bad connector can cause damage. Connector mating should be done with fingers; a torque wrench is to be used only at the last half turn. Difficulties with mating a connector indicate that the connector is dirty or damaged. The connectors can be cleaned with cotton swabs and isopropyl alcohol. To ensure repeatability of the measurements, use a calibrated torque wrench whenever possible.

To maximize the resolution of the scope, in particularly in the time axis, it is important to zoom in on the DUT — but at the same time to allow a window that is sufficiently long to include all the reflections related to the DUT. The window that is too short may prevent the designer from obtaining complete and accurate information about the DUT. When the designer intends to perform true impedance profile analysis, as implemented in IConnect TDR software, it is important to window out the transition related to the sampling head to the cable interface, and focus on the DUT portion of the waveform as shown in Figure 10.



▶ **Figure 11.** *TDR oscilloscope block diagram. The signal is sent to the DUT and the reflection provides important information about the DUT.*

True Impedance Profile

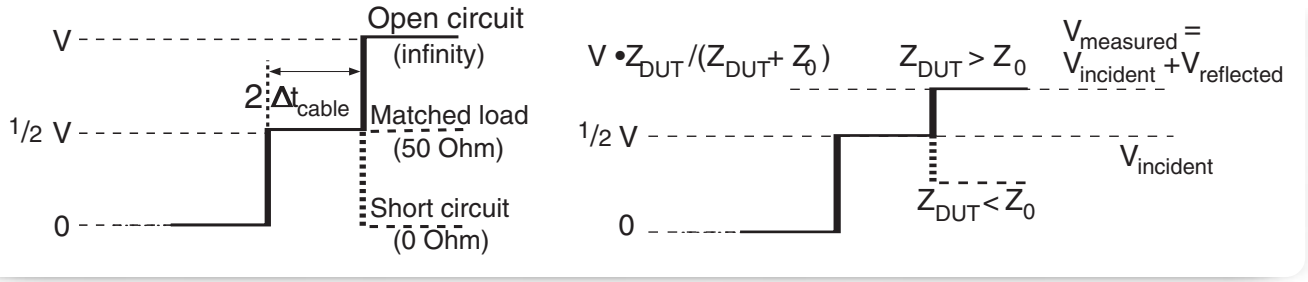
The multi gigahertz bandwidth and the internal source sets the TDR aside from any other oscilloscope in a totally separate class, making it a high-frequency impedance and network[2] characterization tool. The block diagram of the test setup for the single-ended configuration is shown in Figure 11.

The oscilloscope step generator sends a step-like stimulus to the DUT. The signal is reflected from the DUT, and based on this reflection, an engineer can analyze the impedance, delay and other characteristics of the DUT. Now we will consider how to utilize the impedance measurements of the DUT.

Single Discontinuity Case

Equivalent resistance of the TDR source R_{source} defines the characteristic impedance of the measurement system. Since for high-performance TDR instruments available today R_{source} is 50 ohm, using non-50 ohm cables and probes will produce reflections that may confuse results. Unlike with a regular oscilloscope, no active probes or resistor divider probes are allowed for use with TDR. However, the fact that the measurement system has to maintain 50 ohm characteristic impedance does not mean that the DUT may not be non-50 ohm. Non-50 ohm impedances, such as 28 ohm in the case of Rambus 75 ohm in case of cable TV, can be measured quite accurately.

[2] The term "network" is used here to describe a potentially complicated mixture of cables, board traces, connectors, sockets and IC packages.



▶ **Figure 12.** *Typical waveform shapes. Z_0 is the characteristic impedance of the TDR measurement system (50 ohm), and Z_{DUT} is the impedance of the DUT.*

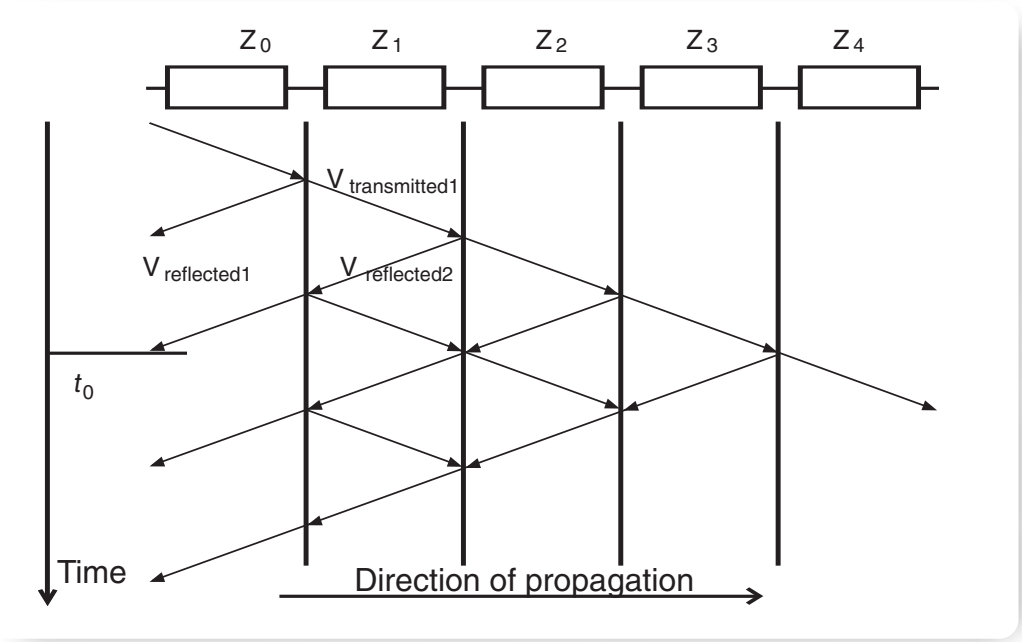
Because of the resistor divider effect between the 50 ohm resistance of the source and the 50 ohm characteristic impedance of the cable used to connect the instrument to the DUT, initially only $^1/_2$ of the TDR source voltage V of the TDR reaches the DUT as shown in Figure 12. Then, if nothing is connected to the cable (open circuit condition), after the round trip delay through the cable, the waveform reaches the full incident voltage magnitude. If a shorting block is connected to the cable, thus creating a short circuit condition, the waveform will go to 0 volts. If a 50 ohm termination is connected ("matched load"), then the waveform will stay at the $V_{incident}$ level, equal to $^1/_2$ V. The TDR signature for different levels of the DUT s impedance is shown in Figure 12. The right part of the figure shows that there is more impedance resolution in the lower range of the TDR (from the matched to the short), than it is in upper range (from matched case to the infinity).

Time information in TDR signature is given in terms of the round trip delay. This applies not only to the cable interconnecting the TDR oscilloscope to the DUT, but also to all delay measurements on the DUT itself. In order to obtain accurate delay readout, the designer has to divide the measured delay by 2. When the voltage reflected from the DUT arrives back to the oscilloscope, it is added to the incident voltage on the oscilloscope to produce the measured voltage value $V_{measured}$. Then, many TDR oscilloscopes use the following equations to convert the voltage, which the oscilloscope measures, to impedance and reflection coefficient:

$$V_{reflected} = V_{incident} \frac{Z_{DUT} - Z_0}{Z_{DUT} + Z_0} \quad (7)$$

$$\rho = \frac{V_{reflected}}{V_{incident}} = \frac{Z_{DUT} - Z_0}{Z_{DUT} + Z_0} \quad (8)$$

$$Z_{DUT} = Z_0 \cdot \frac{1+\rho}{1-\rho} = Z_0 \cdot \frac{V_{incident} + V_{reflected}}{V_{incident} - V_{reflected}} = Z_0 \cdot \frac{V_{measured}}{2 \cdot V_{incident} - V_{measured}} \quad (9)$$



▶ **Figure 13.** *Lattice diagram of TDR waveform propagating through a complex DUT with multiple impedance discontinuities. The superposition of primary reflections at each layer and multiple secondary or "ghost" reflections between layers, makes it difficult to determine the impedance of each layer in the DUT.*

where ρ is the reflection coefficient, and the other notations used here have been described above. This equation is accurate only for a single discontinuity; multiple reflections require application of another approach to determine the accurate impedance readouts.

For a simple DUT, such as a test coupon on a PCB or a cable, the equations (7) - (9) work quite well. However, in real life, engineers have to deal with more complex structures. These may include such structures as board traces that are interconnected by vias between different layers of a board and by connectors between different boards. A good example of this is a backplane with daughter-cards. Traces on different board layers can have different impedances, and vias and connectors constitute inductive and capacitive discontinuities that distort the signal propagating through interconnects. Such complex structures result in multiple reflections occurring in the system at each impedance discontinuity. The resulting superposition of real and multiple "ghost" reflections in the system makes it difficult, if not impossible, to apply the equations directly.

The multiple-reflection effects are illustrated by the lattice diagram in Figure 13. Even for a simple test coupon, an SMA connector that serves as an interface to the board trace can create a situation where superposition of multiple reflections may result in insufficient accuracy in determination of the coupon's impedance.

The true impedance profile can be computed, however, from the TDR profile measured with a TDR oscilloscope using an impedance peeling algorithm, also known as an inverse scattering algorithm [3], [4]. From the lattice diagram on Figure 13, it is clear that equation (9) can be applied to the reflection at the interface between Z_0 and Z_1 in order to compute the impedance of layer 1:

$$Z_1 = Z_0 \cdot \frac{1+\rho_{01}}{1-\rho_{01}} = Z_0 \cdot \frac{V_{incident1}(1)+V_{reflected1}(1)}{V_{incident1}(1)-V_{reflected1}(1)} \qquad (10)$$

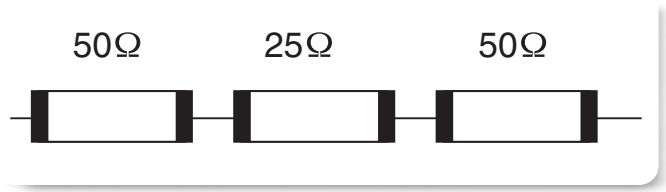
Where the subscript 01 refers to the reflection at the impedance discontinuity between layers 0 and 1.

The reflected waveform at time t_0 is defined by the reflection between layers 1 and 2 and but also by the reflection and transmission between layers 0 and 1. The reflected waveform amplitude at time t_0 can be computed as:

$$V_{reflected}(2) = \tau_{01}^2 \cdot \rho_{12} \cdot V_{incident1}(1) + \rho_{01} \cdot V_{incident1}(2) \qquad (11)$$

where τ_{01} is the transmission coefficient at the interface between layers 0 and 1, defined as $\tau_{01} = 1+\rho_{01}$. From this equation, ρ_{12} can be determined unambiguously, and the impedance at layer 2 can then be found using equation (9) above.

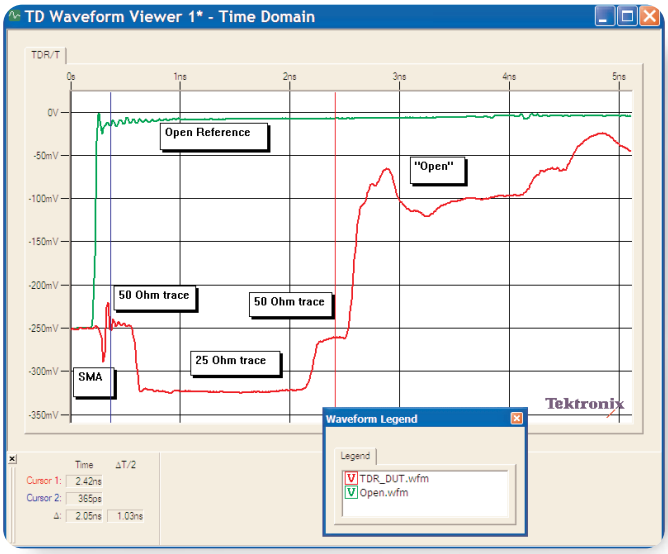
$$Z_2 = Z_1 \cdot \frac{1+\rho_{12}}{1-\rho_{12}} \qquad (12)$$



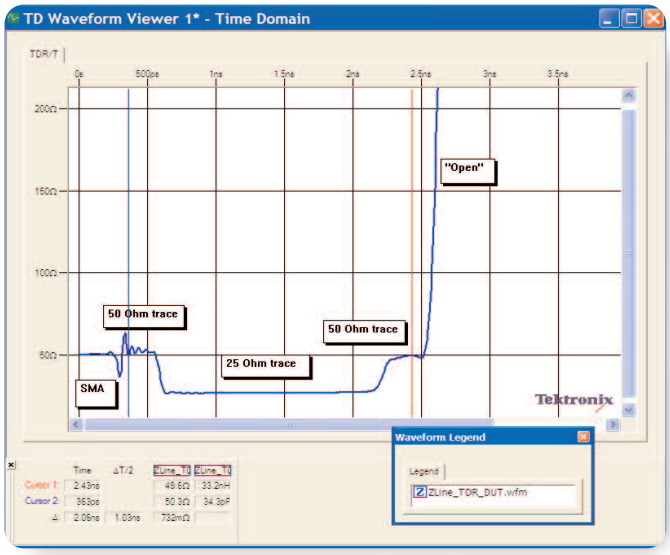
▶ **Figure 14.** *Topological description of a test device. A 25 ohm FR4 board microstrip trace is surrounded by two 50 ohm traces.*

This computational procedure can be applied to the measured waveform, consequently peeling layers of impedance. As a result, impedance at each layer can be computed to form the true impedance profile of the DUT. The algorithm for computing the true impedance profile, often referred to as the "peeling" or "inverse scattering" algorithm, is implemented in IConnect software from Tektronix.

Once the impedance profile has been computed, a board designer can obtain direct readouts of impedance values for all sections of the microstrip board trace under test, or any given DUT. As an example, a 25 ohm (nominal) board trace surrounded by two 50 ohm traces has been characterized using the impedance peeling algorithm (Figure 14). Standard SMA connectors have been used to interface from the board to the TDR measurement system. The software computes true impedance profile based on TDR data acquired with the DSA8200 or similar equivalent time sampling oscilloscope. It is also possible to convert frequency domain measurements performed with a vector network analyzer (VNA) into time and use peeling, however, in this case the resolution will be limited by the bandwidth of the measurement.



▶ **Figure 15.** *Time domain measurement of the microstrip shown in Figure 14. Note that the second 50 ohm portion of the microstrip is not at 250 mV level which indicates the effect of multiple reflections.*



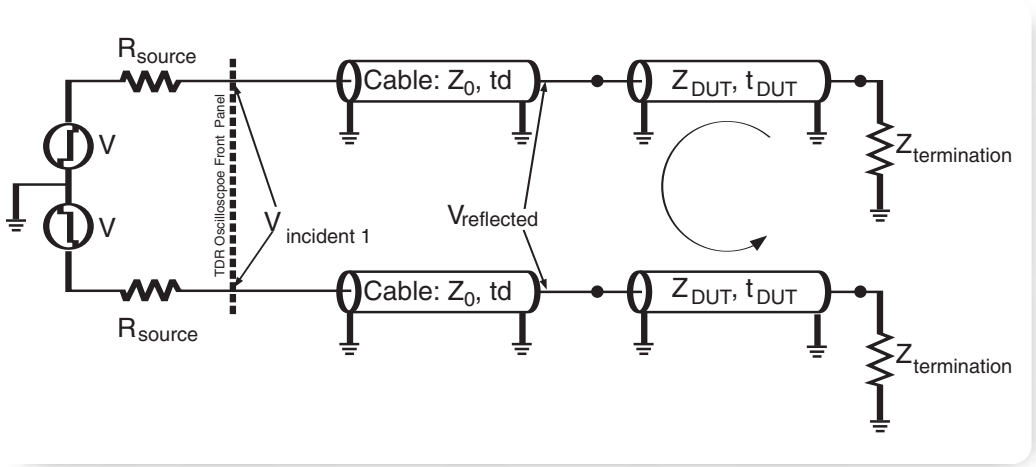
▶ **Figure 16.** *Accurate impedance profile of the microstrip shown in Figure 14. Note that the second 50 ohm portion of the microstrip is now at 50 ohm level which shows accurate impedance readout.*

To compute the impedance profile waveform, both the incident and reflected waveform must be known. The reflected waveform can be computed based on TDR measurements of the DUT. The incident waveform, on the other hand, can de determined in several ways. The simplest is to compute it from an acquired reference short or open waveform, where a short or an open termination is connected at the interface between the instrument cables and the DUT, in place of the DUT. A short termination typically has less reactance (an open-ended coaxial cable can have significant fringing capacitance), and is the preferred method of acquiring the reference waveform. From TDR measurements of the DUT and the reference waveform shown in Figure 15, the software will compute the true impedance profile, using the impedance peeling algorithm described.

The true impedance waveform computed using this approach is shown in Figure 16. It is clear that the impedance profile accurately depicts major sections of the 50-25-50 ohm trace. The last 50 ohm section of the microstrip measured using formula 9 measures 44 ohms, whereas the value obtained using a peeling algorithm is 49 ohms.

Coupled Interconnects

As the complexity of the circuit board grows it becomes more difficult to achieve reliable common ground, which provides a return path for the current. The differential signaling scheme using coupled interconnects is commonly used to overcome this difficulty by providing a virtual signal ground. Other important reasons for the wide acceptance of the differential coupled lines in the gigabit rate designs are benefits of increased immunity to the common noise and reduced electromagnetic interference (EMI) between devices.



► **Figure 17.** *Differential TDR block diagram. Using this setup a device under test (DUT) can be characterized in terms of even and odd modes of signal propagation.*

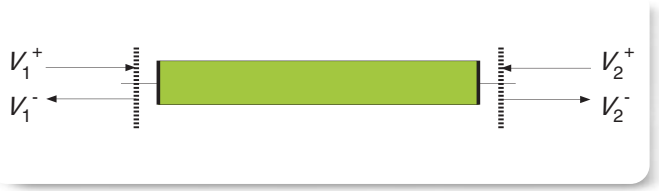
A coupled structure could be fully described by two modes of propagation: even mode and odd mode. When signaling is performed with one of these modes, the signal in a two-signal-line differential pair propagates undistorted [6]. Since the system's noise has common component, the odd mode or differential signaling is used to transmit data. Each line in the odd mode of propagation carries a single bit of data of the same amplitude but with opposite polarity. When the signal is subtracted at the receiver's side, the common noise components are ideally canceled out.

Differential TDR measurements are an important capability that the TDR instruments provide, since most of the modern signaling schemes and standards are differential — whether it is USB2.0, Firewire, Infiniband, Rapid I/O, SCSI, FibreChannel, Gigabit Ethernet, or Sonet — thus requiring differential impedance measurements. In addition, differential TDR is very useful for crosstalk characterization, whether it is crosstalk between two single-ended traces or crosstalk between differential pairs.

The block diagram of the test setup for the differential configuration is shown in Figure 17. This setup requires two sampling heads as opposed to one in the single-ended setup. The TDR instrument, such as the DSA8200, provides up to 8 single ended or 4 differential channels, allowing the designer to look at the crosstalk between up to 4 differential pairs, making TDR the most capable high-frequency differential instrument currently available.

The TDR de-skew capability ensures that both signals in a differential pair reach the DUT traces at the same time, and allows to correct for delay differences between the cables, probes and fixtures. If the TDR is not properly de-skewed, the resulting skew can produce significant inaccuracies in differential impedance measurements and differential line modeling[3]. It may also result in the increased amount of time jitter for the eye diagram measurements.

[3] Note, however, that since TDR displays the round trip delay, and for best accuracy the designer needs to make sure that the signals reach the DUT (one-way trip!), not come back to the oscilloscope, at the same time, the designer needs to use the TDR source delay adjustment to adjust for half of the observed delay, and then use the acquisition skew adjustment to account for the second half of the observed delay. Please refer to your TDR oscilloscope manual for further details.



▶ **Figure 18.** *Sij parameter is the ratio of the reflected (or transmitted) wave at port j to the incident wave at port .*

Frequency Domain from Time Domain Measurements

S-parameters Theory

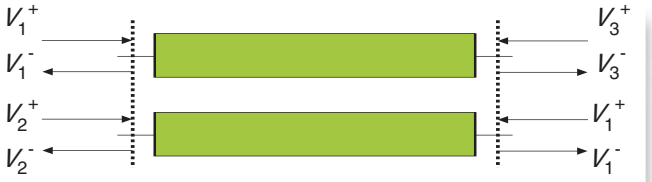
S-parameters are defined in terms of incident and reflected waves at each port. Each Sij parameter is the ratio of the reflected (or transmitted) wave at port j to the incident wave at port i.

The generalized term for reflection or transmission is "scattering." If we make an assumption that the power transmitted is given by $\frac{1}{2}$ $|V_i^+|^2$, then the voltages at each port can be defined as $V=V^+ + V^-$ and currents as $I=I^+ + I^-$. For a reciprocal junction (such as an interconnect) the scattering matrix is symmetrical, i.e. $S_{21}=S_{12}$.

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \quad (13)$$

For a four port, the picture is a little more complicated, even though a 4-port is a direct extension of a 2-port definition.

Most S-parameter measurements in digital design are differential. As a result, what really is of interest to digital engineers are the differential and common mode, not single ended measurements. Differential measurements are performed between the lines, whereas common mode measurements are performed from the lines, tied together, to ground.



$$\begin{bmatrix} V_1^- \\ V_2^- \\ V_3^- \\ V_4^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ V_3^+ \\ V_4^+ \end{bmatrix}$$

▶ **Figure 19.** *For a four port, more voltage and current values are involved in computing the S-parameter matrix, and the matrix itself is 4x4 in dimension*

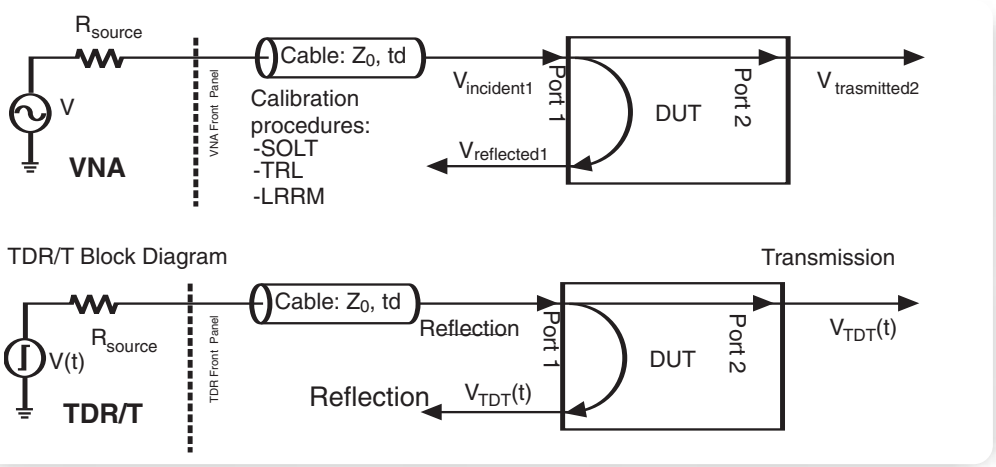
		Differential	Common
Response	Differential	S_{dd}	S_{dc}
	Common	S_{cd}	S_{cc}

▶ **Figure 20.** *Differential stimulus and differential response define the differential S-parameter quadrant etc.*

In practical terms, the type of stimulus and response defines the type of S-parameters we are looking at. Differential stimulus and differential response define the differential S-parameter quadrant, common mode stimulus and response define the common mode quadrant, differential stimulus and common mode response define the differential-to-common mode conversion mixed-mode quadrant, and common mode stimulus and differential response define common-to-differential mode conversion mixed-mode quadrant.

The resulting S-parameters matrix looks as follows:

$$\begin{bmatrix} V_{d1}^- \\ V_{d2}^- \\ V_{c1}^- \\ V_{c2}^- \end{bmatrix} = \begin{bmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{c11} & S_{cc12} \\ S_{cd21} & S_{cd22} & S_{cc21} & S_{cc22} \end{bmatrix} \begin{bmatrix} V_{d1}^+ \\ V_{d2}^+ \\ V_{c1}^+ \\ V_{c2}^+ \end{bmatrix} \quad (14)$$



► **Figure 21.** *Conceptual block diagram of TDR-based TDNA system vs. VNA. The main conceptual difference is in the use of a wide-band step-like source for TDNA vs. a narrow band sine-wave generator for VNA.*

S-parameters are relevant in different degree to digital design. Differential S-parameter quadrant relates to direct degradation of bandwidth and BER/jitter. Common mode explains skew and ground bounce problems. Mixed mode illustrates EM interference (EMI, differential-to-common mode) and EM susceptibility (EMS, common-to-differential); however, a time domain view of the same data produces much more intuitive results when looking for sources of EMI and EMS. Crosstalk, on the other hand, is a form of insertion loss (S_{21}), except that it is insertion loss between lines which do not have direct connection from.

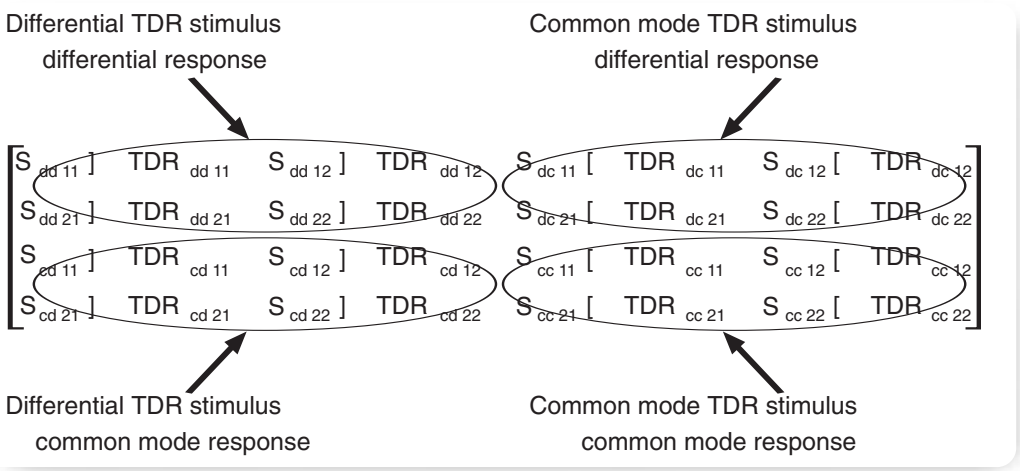
S-parameters Measurements

Time domain reflectometry (TDR) instruments, from which the serial data network analysis (SDNA) approach originates, were initially introduced for fault location in long electrical cables and then quickly found their way into interconnect characterization and signal integrity work, where the intuitive and visual nature of TDR allowed the digital designers to quickly gain insight into their interconnect performance. Differential TDR functionality has existed for many years, and it allows the TDR instruments to assist designers with differential interconnect characterization.

Currently, Tektronix sampling oscilloscope can provide multi-port single-ended or true differential TDR measurement capability. Software tools for extracting and validating interconnect models from measurements and for computing frequency domain S-parameters from time domain data, such as IConnect TDR software, expands the versatility of the TDR instrument even more. The simplicity of the reference plane calibration and fixture deembeding attracts more and more engineers to use this technique for interconnect and termination characterization.

Time domain network analysis (TDNA) calibration and measurement routines, designed to enhance the accuracy of TDR and TDT (time domain transmission) measurements in a manner similar to that of VNA calibration, yielding data in both time and frequency domain, have been reported [7]-[9] and implemented in tools such as MultiCal software from United States National Institute of Standards and Technology (NIST). The full calibration brought the accuracy of TDNA to the level similar to that of network analyzers.

TDNA has been studied extensively by the NIST and various research institutions in the USA and abroad, and has been commercialized by a number of products. Conceptually, the similarity between frequency domain network analysis (FDNA) as done by vector network analyzers (VNA) and TDNA is evident even from the observation of the measurement block diagrams shown in the Figure 21.

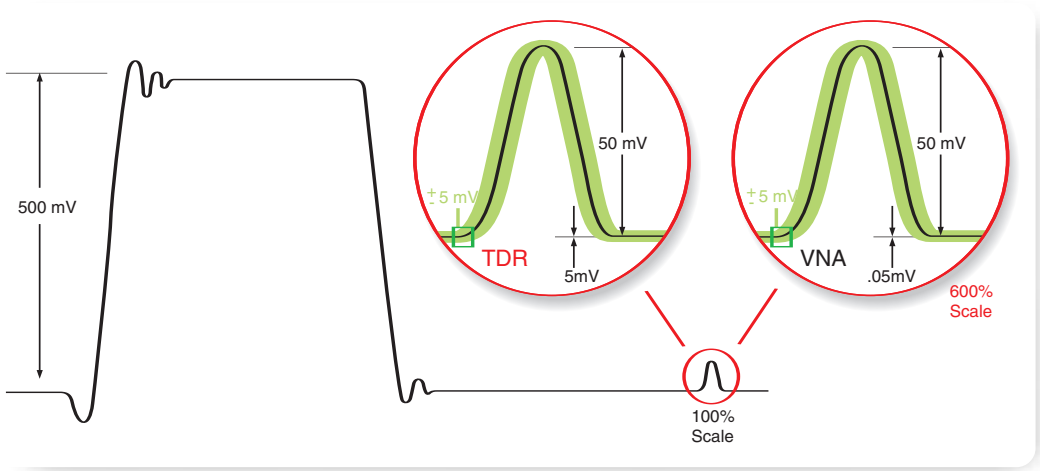


▶ **Figure 22.** *Computations of mixed-mode S-parameter matrix using TDNA technique..*

The main conceptual difference is in the use of a wide-band step-like source for TDR/T vs. a narrow band sine-wave generator for VNA. Additionally, TDR/T is a transient measurement (all transitions are observable) whereas a VNA is a steady-state measurement — all transitions are lumped together, and the measurement is performed at a single frequency, with narrowband filtering employed to minimize the effects of noise. The correlation between the elements of the differential S-parameter matrix and the corresponding TDR measurements are shown in Figure 22.

Since the VNAs were developed to test microwave designs and targeted such applications as microwave filters and mixers, the measurements traditionally require high dynamic range. The need for extremely high dynamic range resulted in devolping some very advanced calibration procedures (such as Short-Open-Load-Thru, SOLT, or Thru-Reflect-Line, TRL), and the overall design of the instrument targeted towards this very high dynamic range, not ease of use. The frequency domain has become the domain of choice for microwave designs, and thus the FDNA is a traditional approach for microwave designers. Ironically, the calibration procedures that make FDNA very accurate, also make a VNA instrument much more difficult and very time-consuming to perform the required tests — very undesirable qualities in particular when production testing is involved.

TDNA was developed as an extension of TDR technology which is intuitive to the digital designers. The conversion of TDR into frequency domain S-parameter data using Fast Fourier Transformation (FFT) is an intuitive and straightforward process as well. Even though it is possible to apply advanced calibration such as SOLT and TRL to TDNA to improve its accuracy, these procedures would make TDNA measurements much less easy and intuitive. Even without these calibration procedures, the dynamic range of TDNA is well into -50 to -60 dB range, which is more than adequate for a typical measurement in digital design or signal integrity, as shown in Figure 23.



▶ **Figure 23.** *Illustration of comparison of the accuracy that can be attained with a TDR of 60 dB dynamic range and a VNA with 80 dB dynamic range. TDR provides sufficient accuracy for the measurements.*

In serial data design the need for S-parameter measurements is driven primarily by the need to characterize the frequency domain behavior of interconnect channel, and by compliance testing requirements in many standards. The need to look at both time and frequency domains for compliance testing resulted in evolving of TDNA into serial data network analysis (SDNA). The compliance testing requirements typically limit the measurements to about -30 dB (-26 dB frequency domain crosstalk for SATA), and the channel analysis does not require any more than -40 dB in measurement capability in most of the cases which makes time domain sampling oscilloscope the best choice for such measurements.

To illustrate the sufficiency of the SDNA's dynamic range for the majority of serial data measurements, let s consider a typical example that a user faces when performing design validation and compliance testing. A discontinuity size that a designer has to pay attention to is normally above 10% of the signal, which is translated to 50 mV or 20 dB for 500 mV signal level. A typical accuracy requirement for this type of the measurements is 10% of the discontinuity size (5mV for the signal specified). This adds another 20 dB to the dynamic range requirement and results in 40 dB of the total required accuracy. The SDNA dynamic range of 60 dB is translated into 0.5 mV, and a VNA measurement of 80 dB is translated into 0.05 mV. Hence, both measurements are well within the accuracy requirements. The graphical comparison of the TDR and VNA measurements is illustrated in Figure 23 where the required accuracy level is shown by green lines and achievable accuracy is shown by the black lines of different thickness.

The dynamic range of SDNA is improved by increasing number of points and number of averages in the time domain acquisition window; more averaging and larger number of points play the same role as narrow band filtering of the signal in FDNA.

$$DR(N, N_{avg}) = DR(N_0, N_{avg0}) \cdot \sqrt{\frac{N}{N_0}} \cdot \sqrt{\frac{N_{avg}}{N_{avg\,0}}} \qquad (15)$$

This equation illustrates that it is highly recommended to use the maximum number of acquisition points and maximum practical number of averages before the measurement begins to take an unacceptably long time. Additionally, a longer acquisition window reduces dynamic range. The user is, therefore, advised to make the window long enough to capture all transitions, but no longer than necessary.

Overall, the correlation between FDNA and TDNA has been studied extensively and accepted as more than adequate by many standard groups. The reader, however, is certainly encouraged to perform his/her own correlation study.

Combined with substantially lower cost of the typical SDNA system, the SDNA solution provides an excellent easy to use solution for doing standard compliance tests.

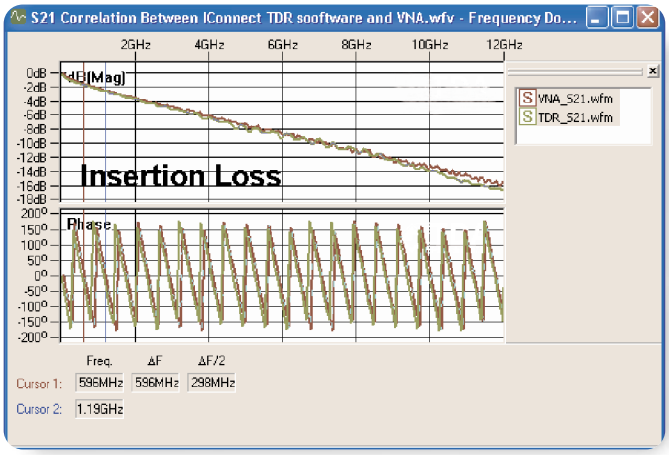
Another important point is that the compliance test point for many standards is defined in such a way that the fully mated connector must be part of the compliance test. Compliance test point is defined so as the fully mated connector must be included in the passive physical layer measurement. The standard connector receptacle must be de-embedded, excluding the connector mated on the board. Even though it is not an impossible task to perform with a VNA, it adds yet another layer of complexity to the VNA measurements. At the same time with SDNA, the ease of calibration (only a "short," "open" or "thru" reference is required) allows to de-embed the standard connector receptacle very easily, providing additional advantage to the SDNA approach.

Modeling of System Performance Based on TDR/T Measurements

SPICE modeling of passive interconnects with IConnect

The measurement-based interconnect modeling approach employs the Measure-Model-Verify philosophy; a prototype is measured using TDR techniques, and based on the acquired data, an equivalent SPICE circuit model can be created. The model is verified through simulation, with the same excitation and terminations used for simulation and measurement. The simulated and measured waveforms are then compared, and the model is verified and adjusted if necessary.

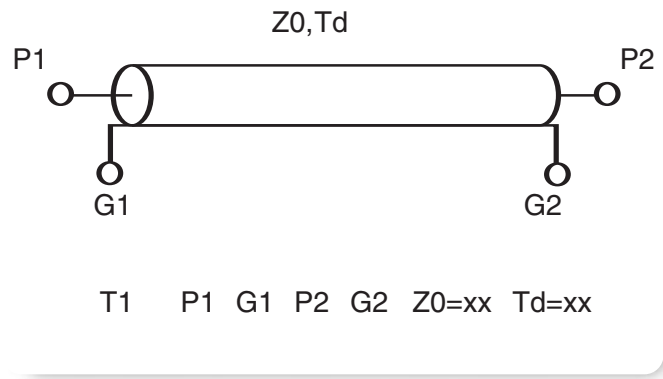
This measurement-based approach does not contradict the design approach that utilizes analytical tools, such as electromagnetic field solvers. If the component



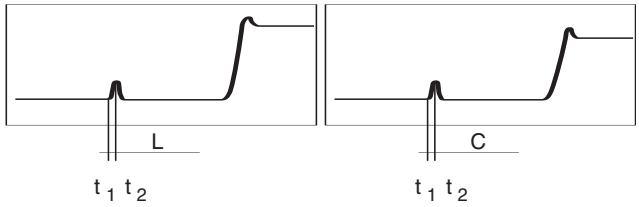
▶ **Figure 24.** *Typical correlation with a vector network analyzer (VNA).*

design is based on an electromagnetic field solver analysis, a prototype must still be fabricated. At this point, the prototype must be carefully characterized and accurate models for the prototype generated. In this case the Measure-Model-Verify approach can be used to ease the modeling work and create an accurate prototype model from measurements. If the measurement-based model differs from the original analytical model, then the difference between assumptions in the field solver and the measurement reality must be reconciled and the model representing the prototype, as it will be used in the actual system, must be defined.

In the previous sections we considered general characteristics of interconnects and found two major factors that contribute to signal integrity problems such as reflections and losses and considered two simple models that can represent an interconnect is circuit simulators. Both of these components can be successfully modeled using the Measure-Model-Verify philosophy. The loss model can be extracted from transmission data, and impedance discontinuities causing reflections can be extracted from the time domain reflection data. The following sections provide description of those techniques in more detail.



▶ **Figure 25.** *SPICE circuit representation and the net list line of the lossless transmission line model. Nodes G1 and G2 are connected to ground when a single-ended configuration is used.*



▶ **Figure 26.** *Inductive spike and capacitive dip on the impedance profile waveform.*

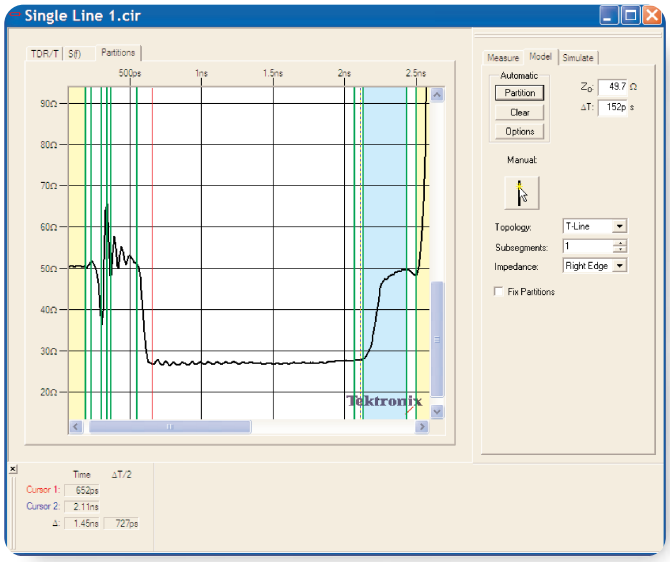
Z-line

In the *True Impedance Profile* section we described that peeling algorithm applied to the TDR waveform allows to obtain accurate impedance readout. The impedance profile by itself is a model consisting of small, equal-length sections of ideal transmission lines. This model, however, is too complicated to be used in the circuit simulators directly and needs to be simplified by partitioning. This partitioning can be done by approximating the beginning of each discontinuity and assigning the characteristic impedance and time delay values at the time when the next discontinuity is seen. All of these operations are conveniently implemented in Single Line or Symmetric Coupled Line modelers of the IConnect software. The Symmetric Coupled line is used to model a four-port coupled transmission line models whereas the single line is used to model a two port device. Dependently on the shape and duration of each discontinuity, different types of the models can be assigned. These types of the models can be distributed, such as transmission lines, or lumped, such as ideal inductors, capacitors, or resistors.

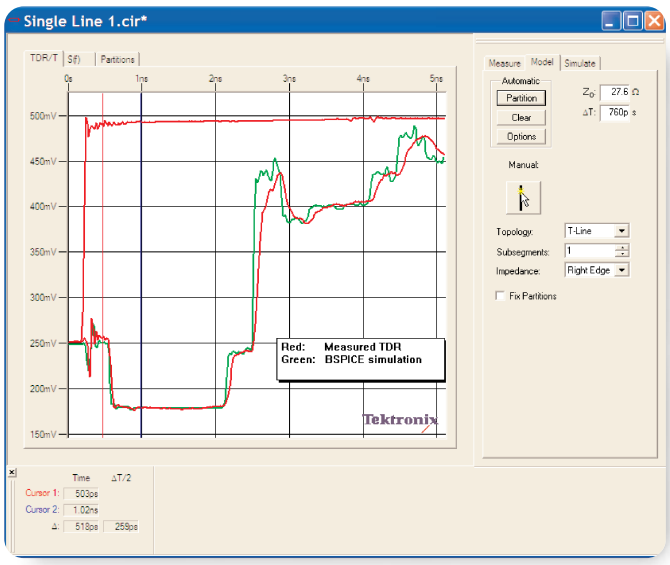
The distributed models describe transmission line properties of interconnects such as characteristic impedance and time delay. These values are used in SPICE simulators to define a lossless transmission line model shown in Figure 25. This model has four nodes and takes into account both characteristic impedance (Z0) and propagation delay (Td) values. In a single ended configuration, nodes G1 and G2 are normally connected to ground. In a coupled configuration, these nodes can be used as a connection to other lines in order to simulate coupling. This model can also be expressed in terms of short sections of ideal transmission lines, similar to the model shown in Figure 1.

When time delay of interconnect is short compared to the signal's rise time, Td value approaches zero. This means that the ideal transmission line model can not only be replaced with a lumped element inductive or capacitive model, but also that the inductance and capacitance can be modeled using lossless transmission lines of the very short length.

The lumped element modeling approach is used to model small features with sizes in order of five or six times smaller than the rise time of the signal used for the data transmission. The values for the series inductance and shunt capacitance can be determined directly from the true impedance profile. An inductive discontinuity is represented on a TDR waveform as a spike above the impedance of the surrounding lines, whereas a capacitive discontinuity will be represented as a dip in the impedance profile waveform, as illustrated in Figure 26.



▶ **Figure 27.** *Single Line modeler window of IConnect with partitions set to define sub-segments of a microstrip model. The topology for each partition can be defined in terms of T-lines or lumped element components.*



▶ **Figure 28.** *Correlation of SPICE model with the measurement data, SPICE circuit components are computed from the true impedance profile.*

The corresponding values for inductance and capacitance can be computed using this equation[10], [11].

$$C = \frac{1}{2} \cdot \int_{t_1}^{t_2} \frac{1}{Z(t)} dt \qquad L = \frac{1}{2} \cdot \int_{t_1}^{t_2} Z(t) dt \qquad (16)$$

where L and C are inductive and capacitive approximations of the discontinuities on the transmission line, t_1 and t_2 are the limits of the integration, and Z(t) is the time function of the true impedance profile.

In the Single Line modeler, the calculated impedance profile waveform is partitioned and appropriate circuit topologies are selected for each partition. The segments of constant impedance are evidently the transmission lines on the board, whereas the dips and peaks in the waveform are the capacitive and inductive discontinuities. On the true impedance profile waveform, the board designer can zoom in on the part of the DUT that needs to be modeled, without running the risk of having multiple reflection effects distort the impedance of the DUT in that section of the trace. Unessential information, such as reflections at the connector-to-board interface, can be windowed out during the modeling session. Figure 27 illustrates modeling partitions assigned for the impedance profile of the structure shown in Figure 15.

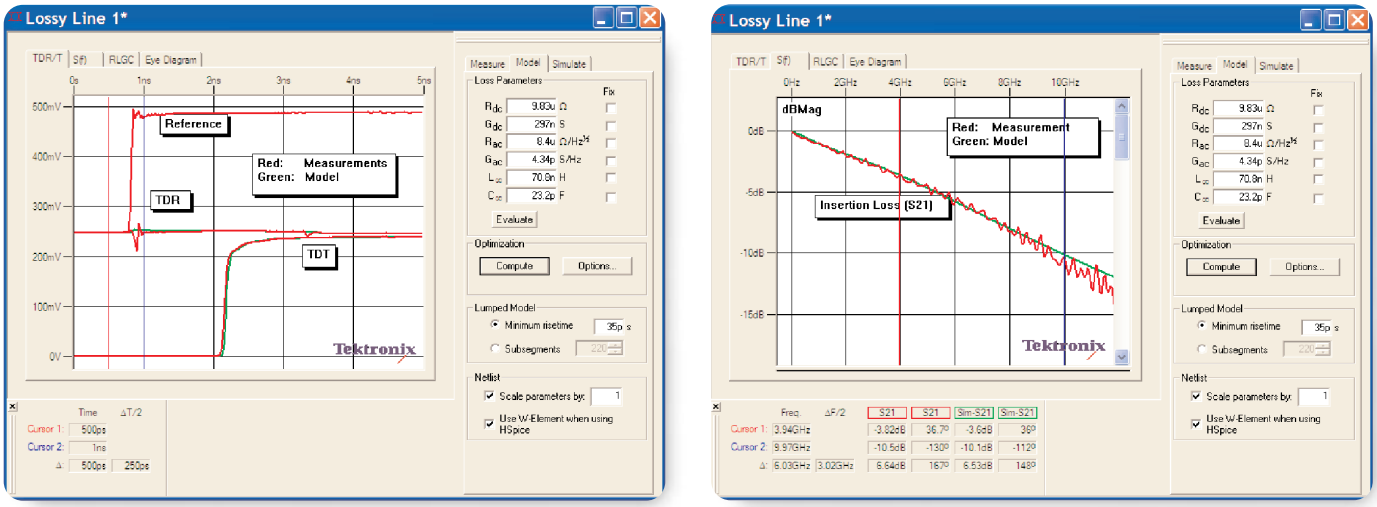
Once an engineer has segmented the impedance profile waveform, IConnect software automatically computes the impedances and propagation delays for the lines on the board and values for capacitive and inductive discontinuities. The created model is then verified with the measurement by using SPICE circuit simulator. The output of the simulation is then compared side-by-side with the measurements of the same structure. Figure 28 shows excellent correlation of the generated model with the measurement data.

Lossy line

From the knowledge about loss mechanisms that we gained in this paper, we conclude that if we can determine R and G, we get the complete high frequency dispersion picture for our interconnect. A simple approach appears to be to use the equations given in that section, or one of the many powerful electromagnetic field solvers on the market, and compute those parameters based on the theoretical data. The problem with this approach, however, is that we all know that accurate information about the dielectric constant, magnetic permittivity, resistivity and often the exact geometry of the transmission line on the board is not easily available. Without such information, any loss parameter extraction will provide inaccurate data and will not be useful for circuit simulations.

A more practical approach is to use TDR/T measurements and extract the loss parameters using IConnect TDR software lossy line modeling function. With IConnect lossy line model extraction, we start with TDR and TDT measurements on the test vehicle, and fit the value of characteristic impedance Z_0, time delay t_d, R and G to the measured data. IConnect software provides a direct integrated interface to simulation tools and allows the designer to run the SPICE simulation on the extracted data, and obtain an automatic comparison between the simulation and the previously measured TDR/T data. This is an easier and more intuitive approach for a digital designer than extracting these parameters from frequency domain measurements.

The first step in the extraction process is to acquire a reference open waveform by taking a TDR of a test fixture or test probe disconnected from the device under test (DUT). If the quality of the open reference is poor and losses in the fixtures, probes and cables are high, it may be difficult to extract the interconnect loss accurately. Therefore, a designer must pay careful attention to the fixtures, probes and cables used in the measurement process. These fixtures and probes ought to be either de-embedded or allow the designer direct access to the DUT. Such de-embedding is relatively easy to use with a TDR oscilloscope. The next step is to measure TDR and TDT data for the DUT. Good repeatability between the reference measurement and the DUT measurement is very important when extracting losses.

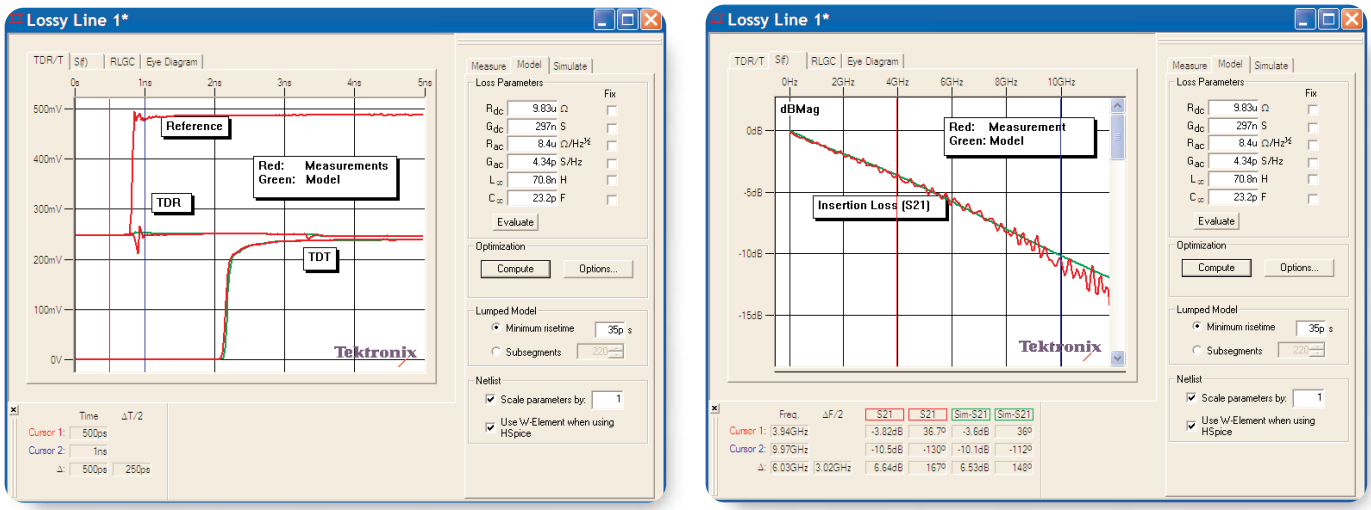


▶ **Figure 29.** *A uniform lossy transmission line model generated for a 50 ohm stripline fabricated on FR4 material. Figure on the left shows time domain correlation, and the figure on the right shows frequency domain correlation up to 12 GHz.*

As an example we will extract a uniform lossy transmission line model for the same stripline structure that we discussed in section *Real Interconnects*. After the measured reference, reflection, and transmission waveforms are loaded into the modeler tool, the model is extracted and optimized automatically to obtain the best possible fit in terms of time- and frequency-domain correlation as shown in Figure 29. Loss input fields allow to input different loss factors and to observe their effect on the overall model performance. Since the created SPICE model is a uniform lossy transmission line model, the small reflections caused by the SMA connectors are ignored in the optimization process.

Behavioral Models

The Z-line-based and lossy line models considered in the previous sections are commonly referred as "topological" models because a user applies certain assumptions based on the previous knowledge of device geometry and physical properties. The topological models have one-to-one correlation between the model components and the physical interconnect structure. Such model can include frequency dependent losses and resonances, and they are most convenient for troubleshooting the causes of signal integrity problems because once the model is generated, a user can easily change the model s parameters to observe the effect of such change on the overall model performance in time and in frequency domains. However, in some cases it is difficult to generate a topological model, and so-called behavioral model becomes handy.



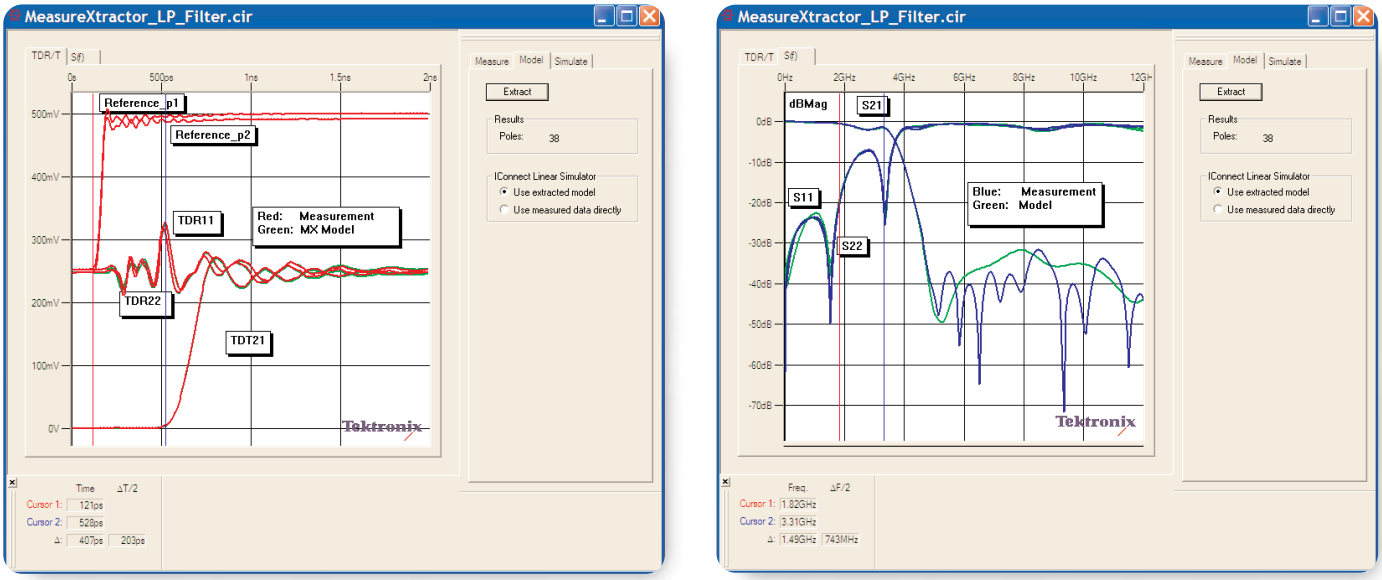
▶ **Figure 30.** *Time and frequency domain correlation of a MeasureXtractor model for a low-pass filter. Both insertion (S21) and return losses (S11 and S22) are accurately modeled.*

Behavioral models usually provide a better overall time- and frequency- domain match, especially in the cases when the user does not have a good insight into the device topology. The behavioral models sometimes are referred to as “black-box“ models, because a user cannot use them to trouble-shoot pieces of the overall interconnect link. However, because the algorithms for these models are fully automated, they provide better model extraction efficiency — and sometimes faster simulation time. They are more convenient for quickly creating a model for a component that does not have a supplier-provided model, but that can be easily measured — and this measurement converted into a behavioral model. IConnect s MeasureXtractor modeling tool is capable of generating two or four port behavioral model for various types of interconnects, terminations, and passive devices. The passivity and causality of such models is guaranteed through the use of a special built-in algorithm.

Consider a modeling example of a low pass filter fabricated on FR4 material. Generating a topological model described in the previous section would be difficult due to the presence of both losses and reflections in the DUT’s response. MeasureXtractor, however, easily generates the SPICE model, which shows excellent correlation in both time and frequency domains as shown in Figure 30.

Generating Composite Models

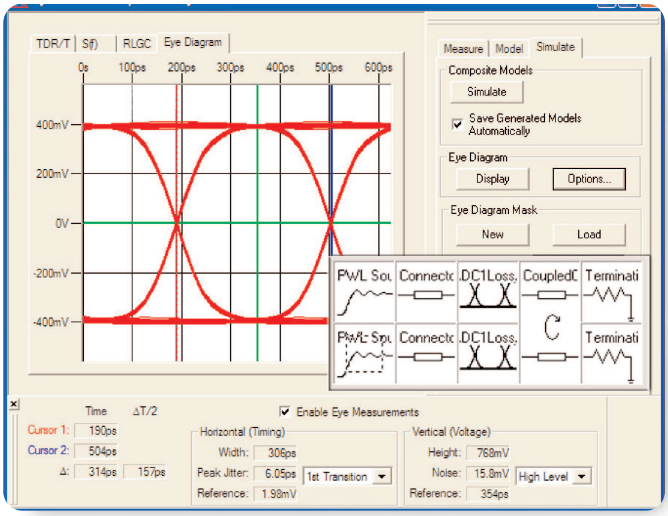
When an engineer needs to generate a SPICE model for a more complicated link, such as the gigabit backplane shown in Figure 5, both reflections and losses need to be considered. In this case it might be desired to generate a composite model that will include a combination of lossy line and Z-line models. If it is desired to model both even and odd modes of propagation, coupled line modeling capabilities of IConnect can be used. Hence, from the observation of modeling structure a user decides the most appropriate model components and generate respective sub circuits for each component. For instance, to generate a model for a daughtercard, an engineer has to consider different models for the connectors and the traces, and desides to model the connectors with single and coupled Z-line based models, and the traces with lossy line models.



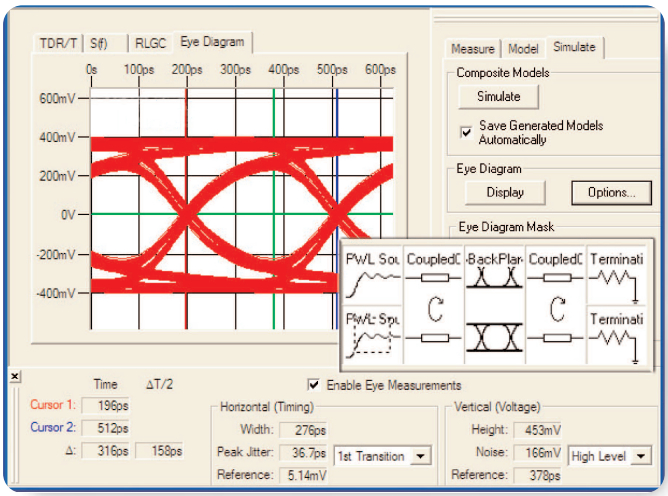
▶ **Figure 31.** *Model topology and a correlation between the circuit model simulated with HSPICE and measured data for the backplane assembly. Each box of the model topology represents a sub-circuit of the composite model. Signal rise time is 80 ps (20-80%).*

After the models obtained for the daughter card and backplane are verified with the circuit simulator of choice, the models could be assembled in one composite. During the assembly process the length of the symmetric coupled lossy line model can be scaled down to account for the length of elements inserted in the circuit model. Figure 31 shows the resulting circuit model topology for a complete backplane assembly. Each box represents the sub-circuit of the composite model. The model simulation reveals excellent correlation between the measured and modeled values for both even and odd modes of excitation.

It is often desirable to analyze the effects of different parts of the backplane on the eye diagram. The topological model is perfectly suitable for such analysis because it allows acquiring transmission waveforms at the different stages of the circuit topology. Once a good correlation with the actual measurement is obtained, an engineer can remove or add different design components, and approximate an eye diagram without using a pattern generator. For example, to approximate the eye diagrams for the daughtercard and the backplane, the user can simulate one transmission waveform for the daughtercard and the connector, and the other with only the backplane and two connectors at the ends. Then the saved transmission waveforms could be used to generate eye diagrams.



▶ **Figure 32.** *Eye diagram generated at 3.2 Gbit/s and 80 ps (20-80%) rise time for the for the daughtercard model only. Eye opening is 768 mV and 306 ps, and peak-to-peak jitter is 6.05 ps.*



▶ **Figure 33.** *Eye diagram generated at 3.2 Gbit/s and 80 ps (20-80%) rise time for the backplane model only. Eye opening is 453 mV and 276 ps, and peak-to-peak jitter is 36.7 ps.*

Eye diagrams generated with this approach are shown in Figures 32 and 33. They indicate that the main contributor to the eye diagram closure is a backplane structure with its connectors. The daughtercard alone produces an eye opening of 768 mV and 306 ps, and peak-to-peak jitter is 6.05 ps for the eye diagram generated at 3.2 Gbit/s and 80 ps (20-80%) rise time, while the backplane model generates an eye opening of 453 mV and 276 ps, and peak-to-peak jitter is 36.7 ps at the same conditions.

Conclusion

As modern signaling standards push digital designs to the gigahertz and gigabit ranges, interconnect performance becomes the key factor in enabling reliable system operation. Signal integrity issues such as reflections, crosstalk, frequency dependent transmission line loss and dispersion can significantly degrade system performance and reliability. Ability to measure, simulate, and accurately predict the effect of these signal integrity issues is critical to achieving a working design, and this ability is contingent on the designer's ability to obtain accurate measurement-based interconnect models for each part of the interconnect link — from the driver chip, through the package into the daughtercard; through a high-speed backplane connector to the backplane, and to the cable interconnect between subsystems.

The critical role in meeting design or complaince play tools that a designer is using in his or her work. Tektronix sampling oscilloscope, probes, and modeling software help to achieve the most efficient results in fast evolving world of digital communications making them indispensible tools for every engineer.

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