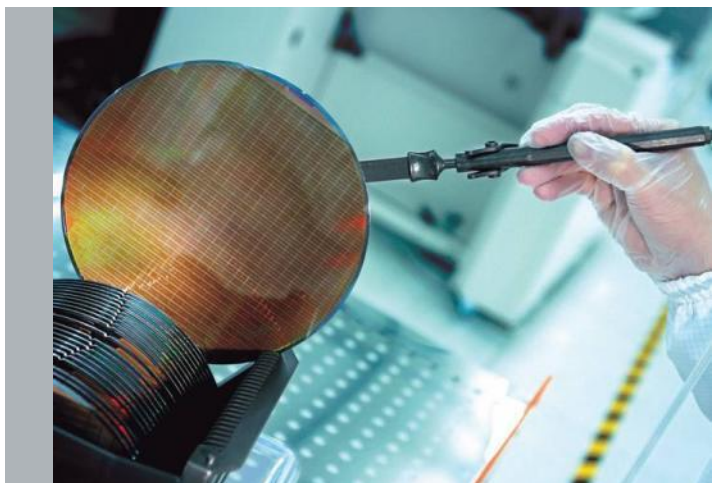


# 高速串行测试方案介绍

泰克华南区技术支持工程师 余岚



**Tektronix**<sup>®</sup>

# High-Speed Serial Data Test Solutions

Design

Verification

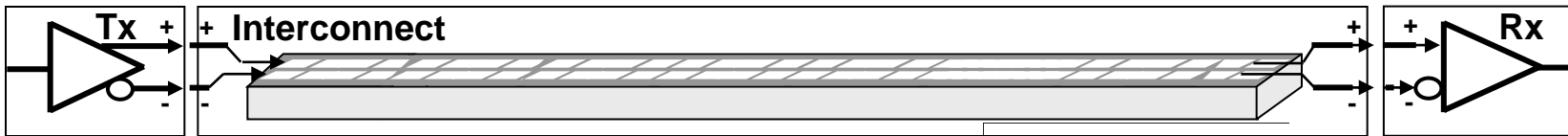
Compliance Test



GbE DisplayPort

HDMI™

MHL ...



Real-time Scopes



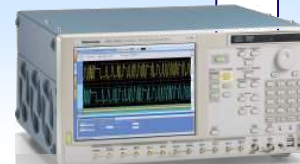
System Integration  
Digital Validation & Debug

Logic Analyzers



Transmitter Testing

Receiver Test  
Margin  
Testing



Arbitrary Waveform Generator

Probing  
Fixtures



Interconnect Test

Sampling Scopes

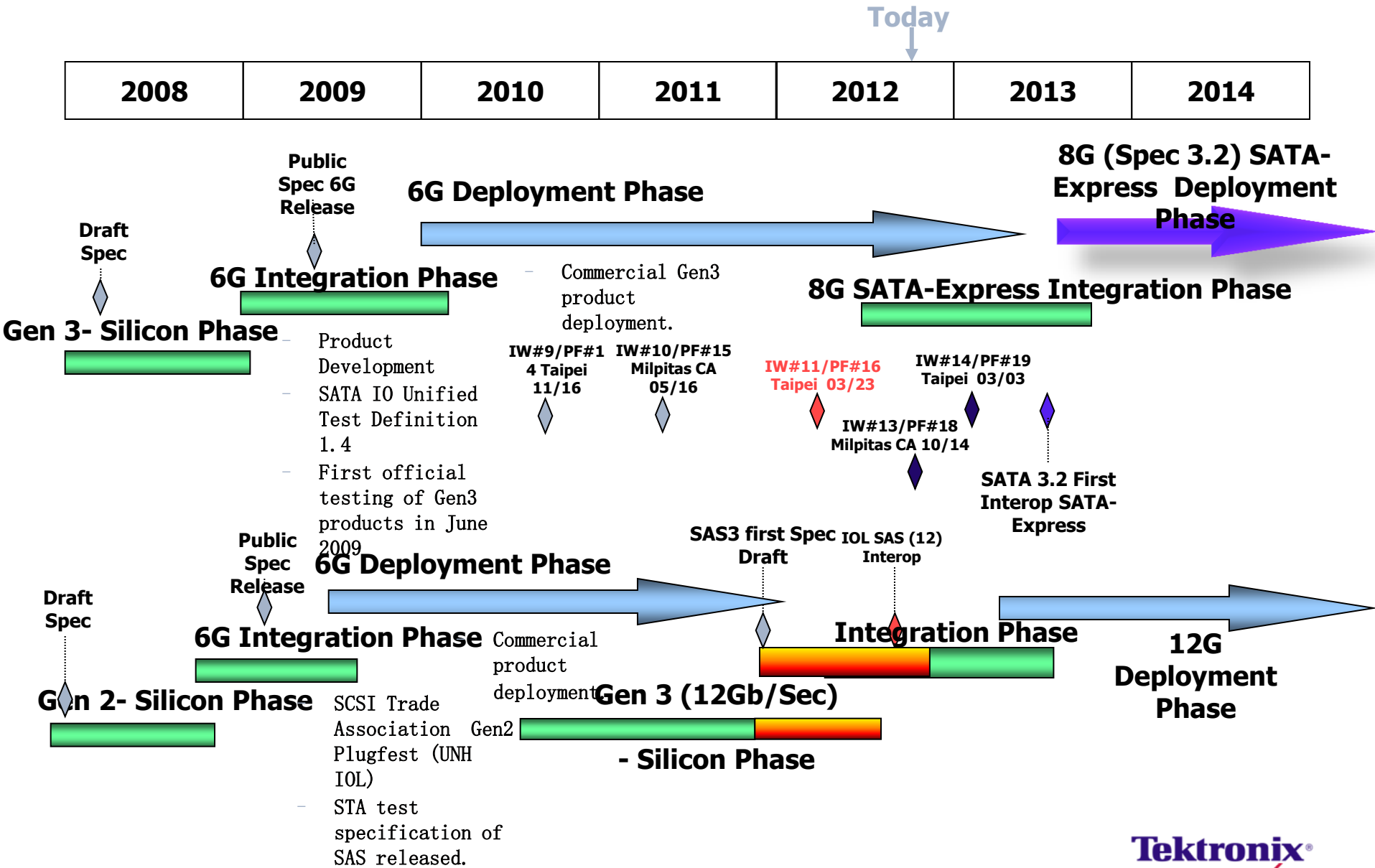


Compliance Test

Compliance Test Software



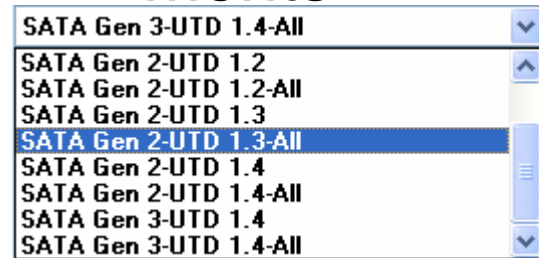
# Storage Timelines and Solutions Development



# SATA UTD 1.4 TSG/PHY/OOB Measurements

Drive : PHY-TSG-OOB SATA Gen 3-UTD 1.4-All

Select	Test Name
<input checked="" type="checkbox"/>	Informative-df/dt Measurement
<input checked="" type="checkbox"/>	Informative-Eye diagrams
<input checked="" type="checkbox"/>	OOB01-OOB Signal Detection Threshold
<input checked="" type="checkbox"/>	OOB02-UI During OOB Signaling
<input checked="" type="checkbox"/>	OOB03-COMINIT_RESET and COMWAKE Transmit Burst Length
<input checked="" type="checkbox"/>	OOB04-COMINIT_RESET Transmit Gap Length
<input checked="" type="checkbox"/>	OOB05-COMWAKE Transmit Gap Length
<input checked="" type="checkbox"/>	OOB06-COMWAKE Gap Detection Windows
<input checked="" type="checkbox"/>	OOB07-COMINIT Gap Detection Windows
<input checked="" type="checkbox"/>	PHY01-Unit Interval
<input checked="" type="checkbox"/>	PHY02-Frequency Long Term Stability
<input checked="" type="checkbox"/>	PHY03-Spread-Spectrum Modulation Frequency
<input checked="" type="checkbox"/>	PHY04-Spread-Spectrum Modulation Deviation
<input checked="" type="checkbox"/>	TSG01-Differential Output Voltage-Option 1
<input checked="" type="checkbox"/>	TSG01-Differential Output Voltage-Option 2
<input checked="" type="checkbox"/>	TSG02-Rise-Fall Time
<input checked="" type="checkbox"/>	TSG03-Differential Skew
<input checked="" type="checkbox"/>	TSG04-AC Common Mode Voltage
<input checked="" type="checkbox"/>	TSG05-Rise-Fall Imbalance
<input checked="" type="checkbox"/>	TSG06-Amplitude Imbalance
<input checked="" type="checkbox"/>	TSG09-TJ at Connector, Clock to Data, fBAUD-500
<input checked="" type="checkbox"/>	TSG10-DJ at Connector, Clock to Data, fBAUD-500
<input checked="" type="checkbox"/>	TSG11-TJ at Connector, Clock to Data, fBAUD-500
<input checked="" type="checkbox"/>	TSG12-DJ at Connector, Clock to Data, fBAUD-500
<input checked="" type="checkbox"/>	TSG13-Transmit Jitter
<input checked="" type="checkbox"/>	TSG14-TX Maximum Differential Voltage Amplitude
<input checked="" type="checkbox"/>	TSG15-TX Minimum Differential Voltage Amplitude
<input checked="" type="checkbox"/>	TSG16-Tx AC Common Mode Voltage



- Different test program and degrees of regression testing user selectable.
- Debug and diagnostic tools (Informative measurements)
- Updated SATA Gen3 measurements
  - **New OOB patterns**
  - TSG ECN additions

# SATA/SAS TSB/PHY/OOB



Select Standard	Select Device	Select Test Suite	Version
<input type="radio"/> Serial ATA	<input checked="" type="radio"/> Drive	<input checked="" type="radio"/> PHY-TSG-00B	SAS 2.0
<input checked="" type="radio"/> SAS		<input type="radio"/> Rx-Tx	

**Drive : PHY-TSG-00B SAS 2.0**

Select	Test Name
<input checked="" type="checkbox"/>	Test 5.2.4 - TX SSC DFDT (Informative)
<input checked="" type="checkbox"/>	Test 5.3.1 - TX Physical Link Rate Long Term Stability
<input checked="" type="checkbox"/>	Test 5.3.2 - TX Common Mode RMS Voltage Limit
<input checked="" type="checkbox"/>	Test 5.3.3 - TX Common Mode Spectrum
<input checked="" type="checkbox"/>	Test 5.3.4 - TX Peak-to-Peak Voltage
<input type="checkbox"/>	Test 5.3.5 - TX VMA and EQ
<input checked="" type="checkbox"/>	Test 5.3.6 - TX Rise and Fall Times
<input checked="" type="checkbox"/>	Test 5.3.7 - TX Random Jitter (RJ)
<input checked="" type="checkbox"/>	Test 5.3.8 - TX Total Jitter (TJ)
<input checked="" type="checkbox"/>	Test 5.3.9 - TX Waveform Distortion Penalty (WDP)

**Configure**

**Show MOI**

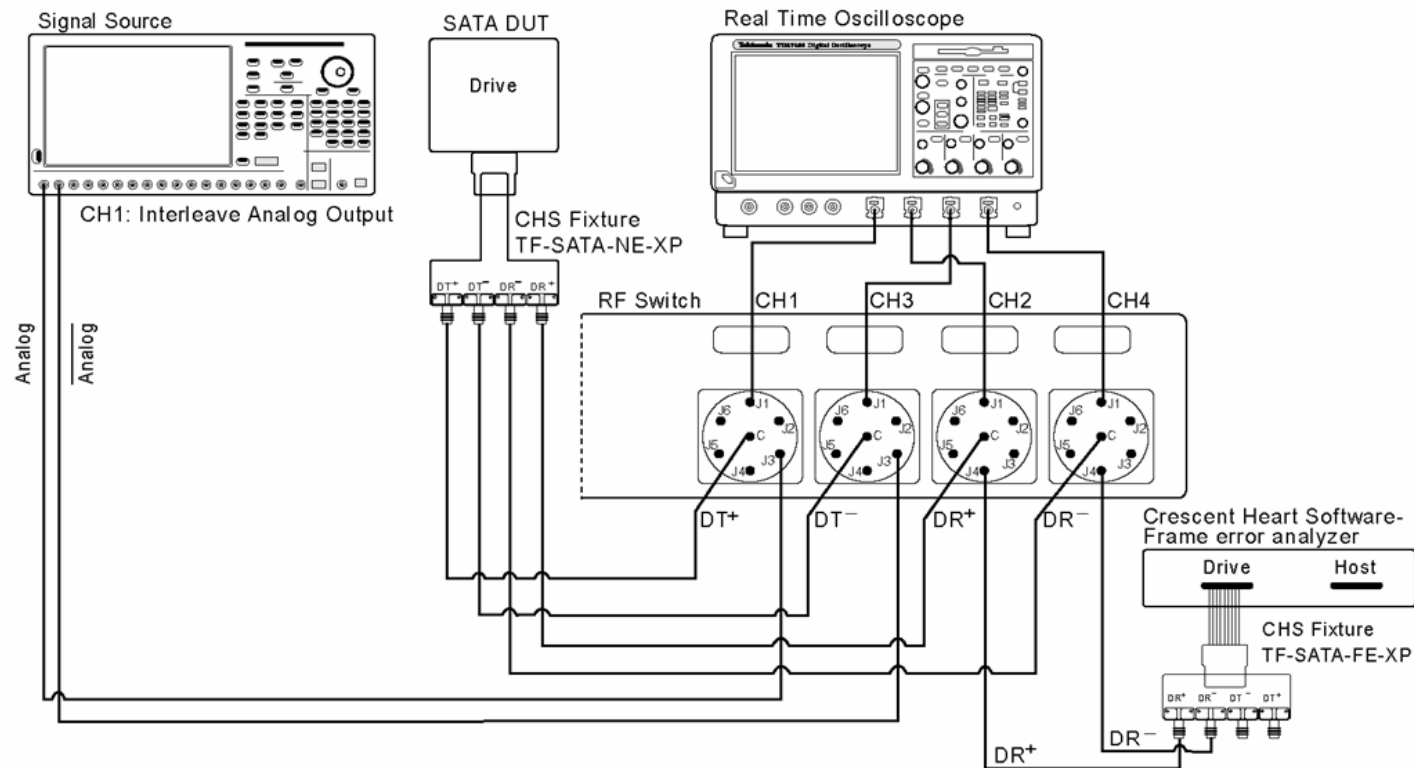
**Show Schematic**

**Select All**

**Select Required**

**Deselect All**

# SATA/SAS TSG/PHY/OOB test connection



# SATA/SAS: test Report

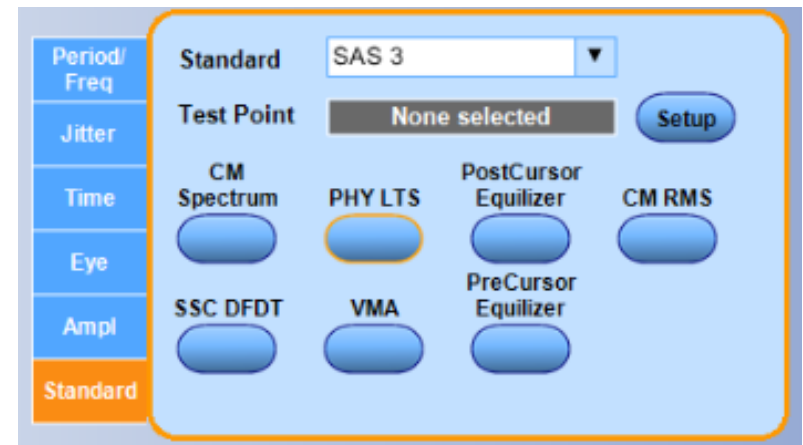
Test Name	Test Details			Low Limit	Measured Value	High Limit	Margin	Units	Test Result
	Pattern Name	Interface Speed	Measurement Details						
<a href="#">Test 5.2.1-TX SSC Modulation Type</a>	HFTP	6.0Gb/s	Center-spread SAS	-NA-	SSC ON	-NA-	-NA-	-NA-	Pass
<a href="#">Test 5.2.2-TX SSC Modulation Frequency</a>	HFTP	6.0Gb/s	SSC Modulation Frequency	>= 30	30.0000	<= 33	0 , 3	KHz	Pass
	HFTP	6.0Gb/s	Min SSC Modulation Frequency	>= 30	29.9992	<= 33	Informative		Informative
	HFTP	6.0Gb/s	Max SSC Modulation Frequency	>= 30	30.0011	<= 33	Informative		Informative
<a href="#">Test 5.2.3-TX SSC Modulation Deviation and Balance</a>	HFTP	6.0Gb/s	Max Deviation	-NA-	-2199.6500	-NA-	-NA-	ppm	Informative
	HFTP	6.0Gb/s	Min Deviation	-NA-	2200.0074	-NA-	-NA-		Informative
	HFTP	6.0Gb/s	Avg Deviation	>= -350	0.1787	<= 350	350.1787, 349.8213		Pass
	HFTP	6.0Gb/s	Deviation asymmetry	-	0.3574	<= 288	287.6426		Pass
<a href="#">Test 5.2.4-TX SSC DFDT (Informative)</a>	HFTP	6.0Gb/s	df/dt	>= -850	-380.3082	<= 850	Informative	ppm/us	Informative
<a href="#">Test 5.3.1-TX Physical Link Rate Long Term Stability</a>	HFTP	6.0Gb/s	Mean Period	> -100	-2.1050	< 100	Informative	ppm	Informative
	HFTP	6.0Gb/s	Min Period	> -100	2200.0074	< 100	Informative		Informative
	HFTP	6.0Gb/s	Max Period	> -100	-2199.6501	< 100	Informative		Informative
Test 5.3.2-TX Common Mode RMS Voltage Limit	CJTPat-Gen 2	6.0Gb/s	Common-mode RMS voltage at IT (mV)-SAS 2.0	-	42.9927	< 30	12.9927	mV	Fail
<a href="#">Test 5.3.3-TX Common Mode Spectrum</a>	CJTPat-Gen 2	6.0Gb/s	Common-mode spectrum (dBmV) at 100MHz-SAS 2.0	-	-33.5589	< 12.7	46.2589	mV	Pass
	CJTPat-Gen 2	6.0Gb/s	Common-mode spectrum (dBmV) at first harmonic-SAS 2.0	-	16.7701	< 26	9.2299		Pass
	CJTPat-Gen 2	6.0Gb/s	Common-mode spectrum (dBmV) at second harmonic-SAS 2.0	-	-9.8586	< 30	39.8586		Pass
Test 5.3.4-TX Peak-to-Peak Voltage	D30.3-Gen 2	6.0Gb/s	Peak to Peak voltage (mVppd)-SAS 2.0	> 850	1240.0000	< 1200	390 , 40	mV	Fail
Test 5.3.5-TX VMA and EQ	D30.3-Gen 2	6.0Gb/s	Transmitter equalization (dB)-SAS 2.0	> 2	2.0684	< 4	Informative	dB	Pass
Test 5.3.6-TX Rise and Fall Times	D10.2	6.0 Gb/s	Rise time in ps	>= 41.6	55.7616	-	14.1616	ps	Pass
	D10.2	6.0 Gb/s	Fall time in ps	>= 41.6	55.3999	-	13.7999		Pass
Test 5.3.7-TX Random Jitter (RJ)	D24.3-Gen 2	6.0Gb/s	Rj before CIC	-	0.7069	<= 25	24.2931	ps	Pass
	D24.3-Gen 2	6.0Gb/s	Rj after CIC	-	0.5321	<= 25	24.4679		Pass



# SAS-3 12Gbps PHY Transmitter Solution – Option SAS3

- Support per SAS-3 Spec 23Apr2012

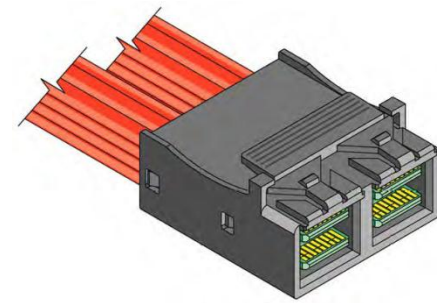
Tests	Base Measurement
TX SSC Modulation Type	DPOJET
TX SSC Modulation Frequency	DPOJET
TX SSC Modulation Deviation and Balance	DPOJET
TX Peak to Peak Voltage	DPOJET
TX Rise/Fall Time	DPOJET
TX Random Jitter	DPOJET
TX Total Jitter	DPOJET
TX SSC DFDT	Custom
TX Physical Link Rate Long Term Stability	Custom
TX Common Mode RMS Voltage	Custom
TX Common Mode Spectrum	Custom
TX VMA and EQ	Custom
TX SAS Eye Opening	Custom
Pre Cursor Equalization	Custom
Post Cursor Equalization	Custom



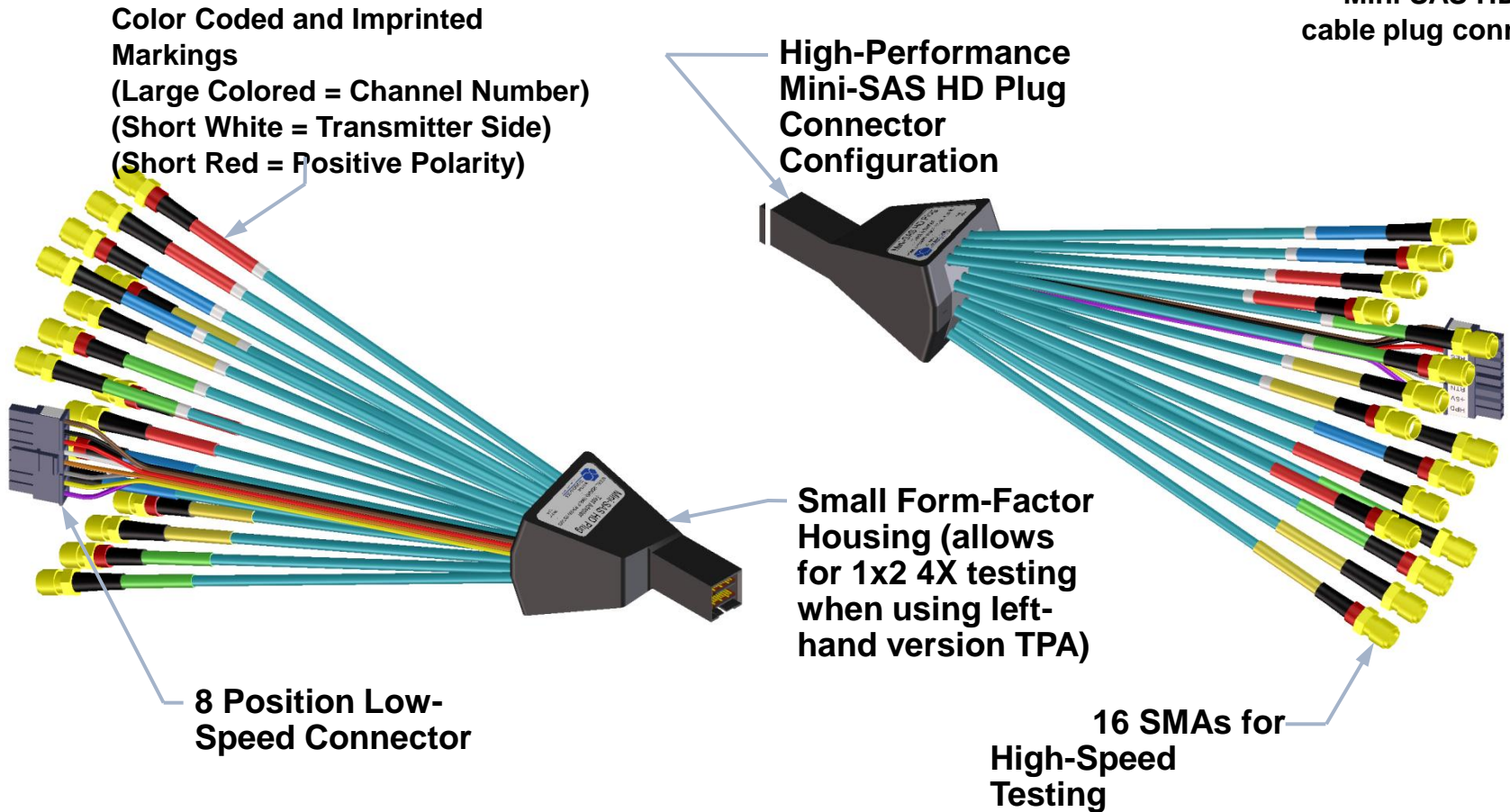
\* SAS3 Eye measurement to be added



# Mini-SAS HD Plug Test Adapters



Mini SAS HD 8i  
cable plug connector



Color Coded and Imprinted  
Markings  
(Large Colored = Channel Number)  
(Short White = Transmitter Side)  
(Short Red = Positive Polarity)

High-Performance  
Mini-SAS HD Plug  
Connector  
Configuration

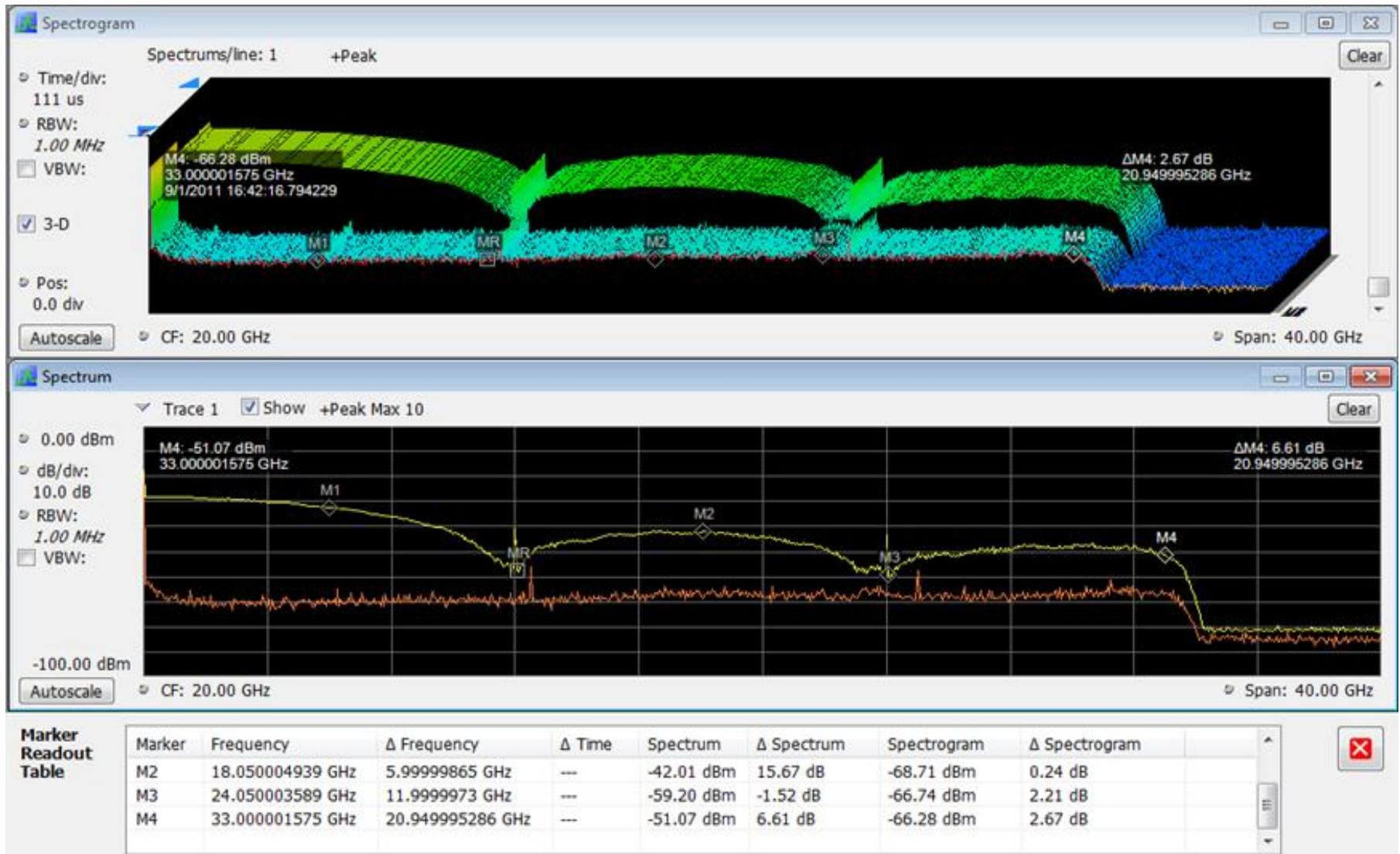
Small Form-Factor  
Housing (allows  
for 1x2 4X testing  
when using left-  
hand version TPA)

8 Position Low-  
Speed Connector

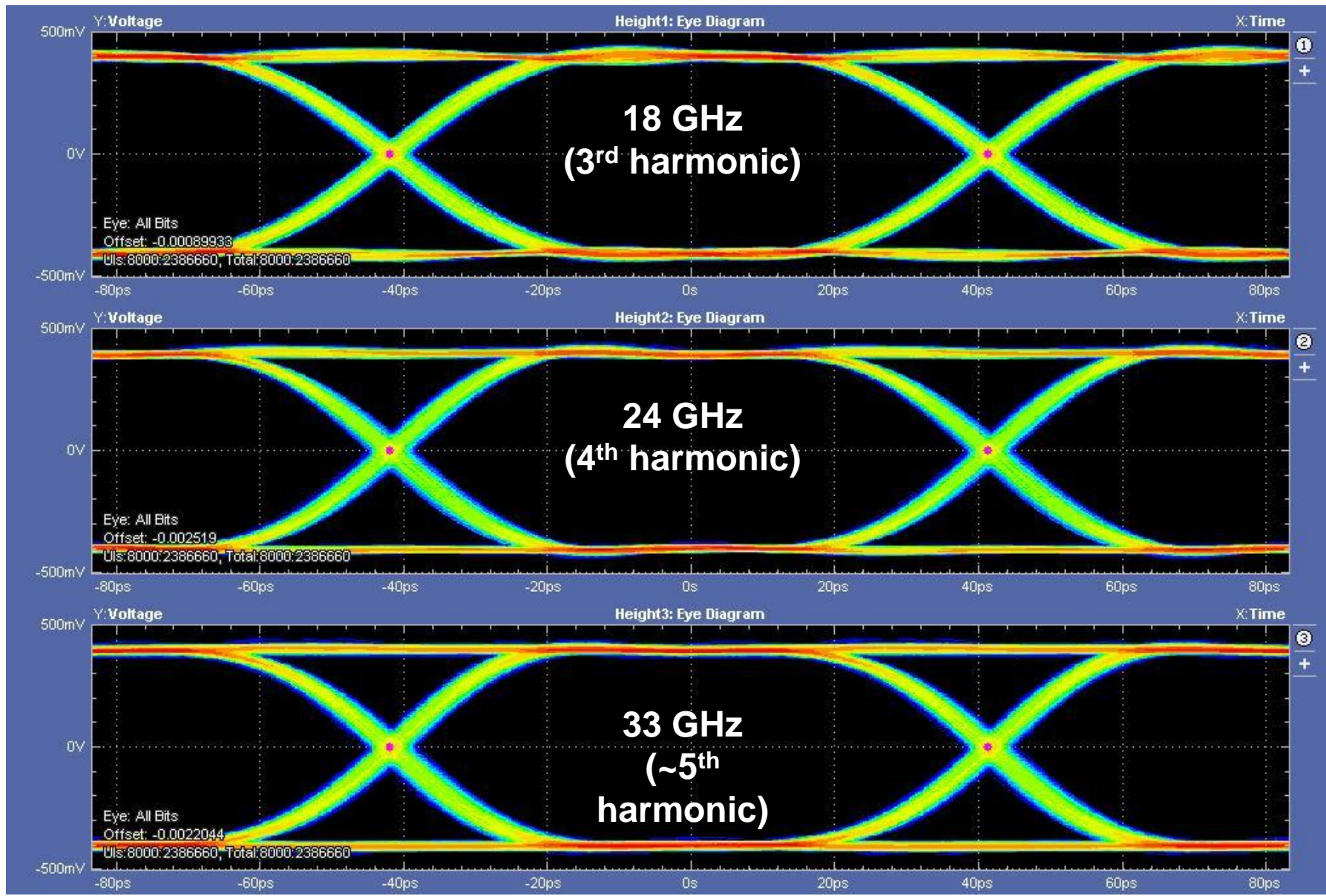
16 SMAs for  
High-Speed  
Testing

# Bandwidth Considerations

## SAS 12G NRZ Power Spectrum



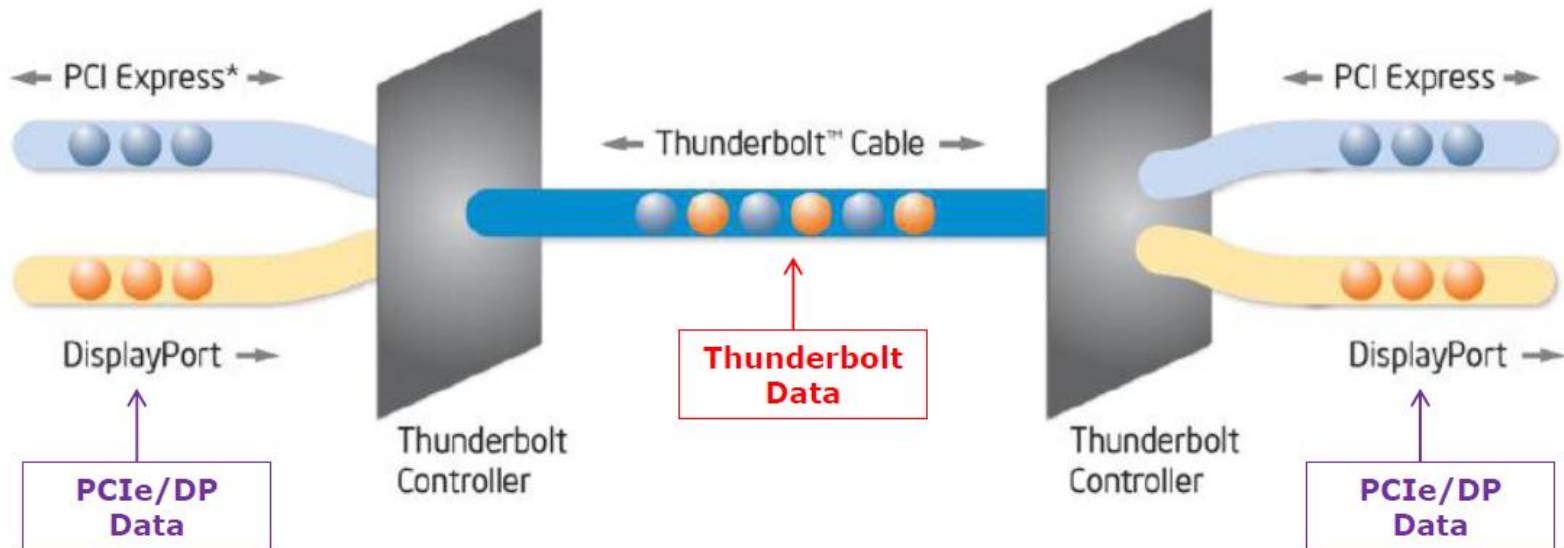
# 12G PRBS from BERT (20ps 20-80% Tr)





# Thunderbolt Overview

- High Speed Data Bus for PC's
  - Brought to market by Intel/Apple in 2011
  - Interoperable with DisplayPort
- Thunderbolt signaling is dual NRZ (64/66b Encoded)
  - 10.3125 Gb/s data rate
  - It utilizes SFP+ technology with 2 diff Tx and Rx pairs.

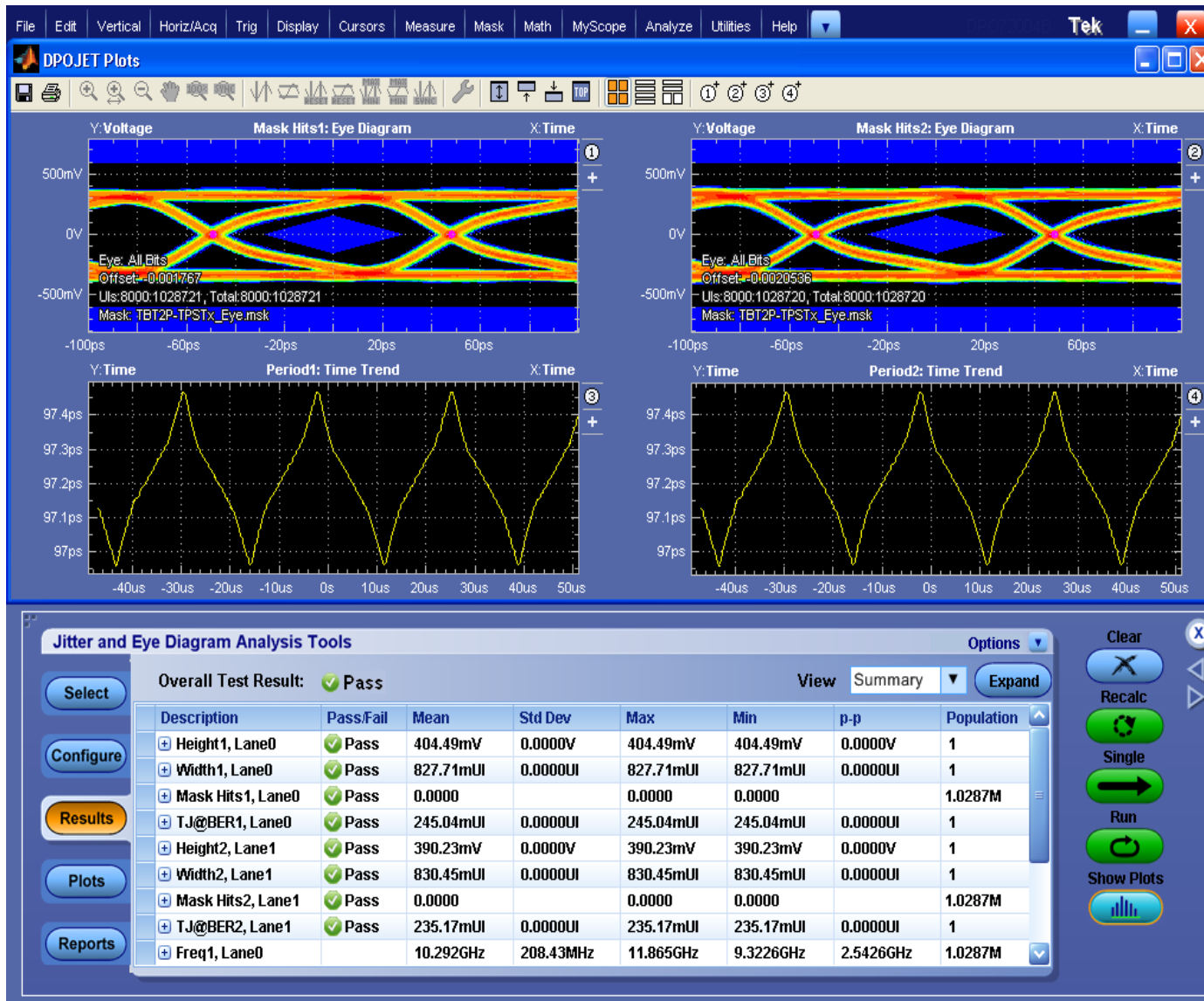


# Thunderbolt Transmitter Test Overview

- All measurements are near end with Fixtures fully de-embed.
- Requires DisplayPort 1.2 conformance testing
- **Source Test Suite**
  - PHY1.1 – Transition Timing
  - PHY1.2 – Intra-Pair Skew
  - PHY1.3 – AC Common Mode RMS
  - PHY1.4 – AC Common Mode Peak
  - PHY1.5 – Eye Height
  - PHY1.6 – Eye Width
  - PHY1.7 – Max Differential Voltage
  - PHY1.8 – Total Jitter at 10-12 BER
  - PHY1.9 – Unit Interval
  - PHY1.10 – SSC Modulation Frequency
- **DUT Configuration**
  - 1. **Bit Rates: (DP1.2) + 10.3125Gb/sec**
  - 2. **Patterns: 8 1's8 0's, PRBS-9, PRBS-11 and PRBS-31**
  - 3. **SSC (Spread Spectrum): On/Off**

# Thunderbolt Transmitter Testing

## Fully supported in Tektronix's current solutions



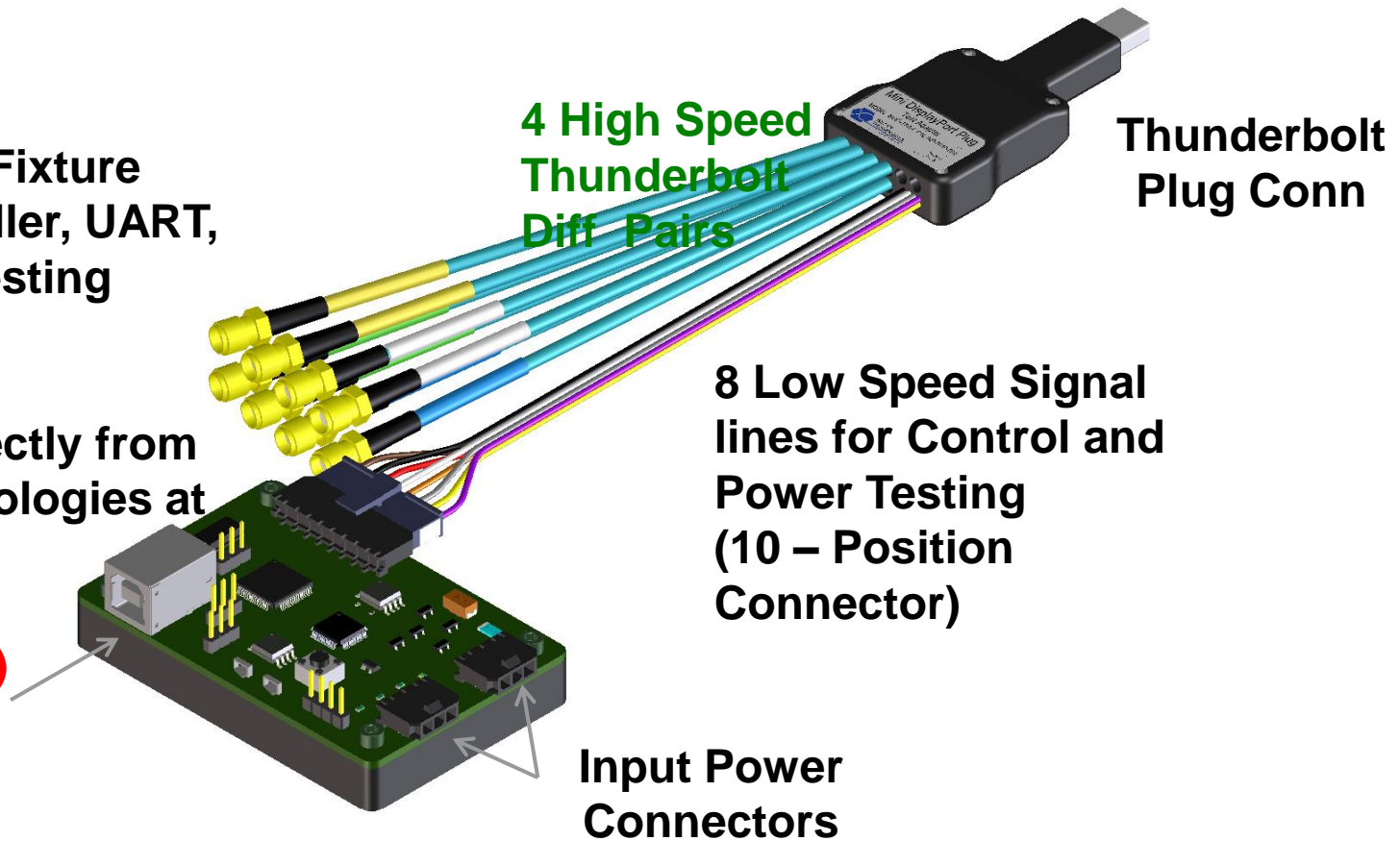
# Thunderbolt Test Connectivity

- The Digital Port Micro is responsible for Test Pattern and general state control, as well as error polling in the DUT.

Thunderbolt Fixture  
Micro Controller, UART,  
and Power Testing  
Board:

Available directly from  
Wilder Technologies at  
part number..

**640-0503-000**  
**(TBT-TPA-UH)**  
USB to PC  
Connection  
for Control



4 High Speed  
Thunderbolt  
Diff Pairs

Thunderbolt  
Plug Conn

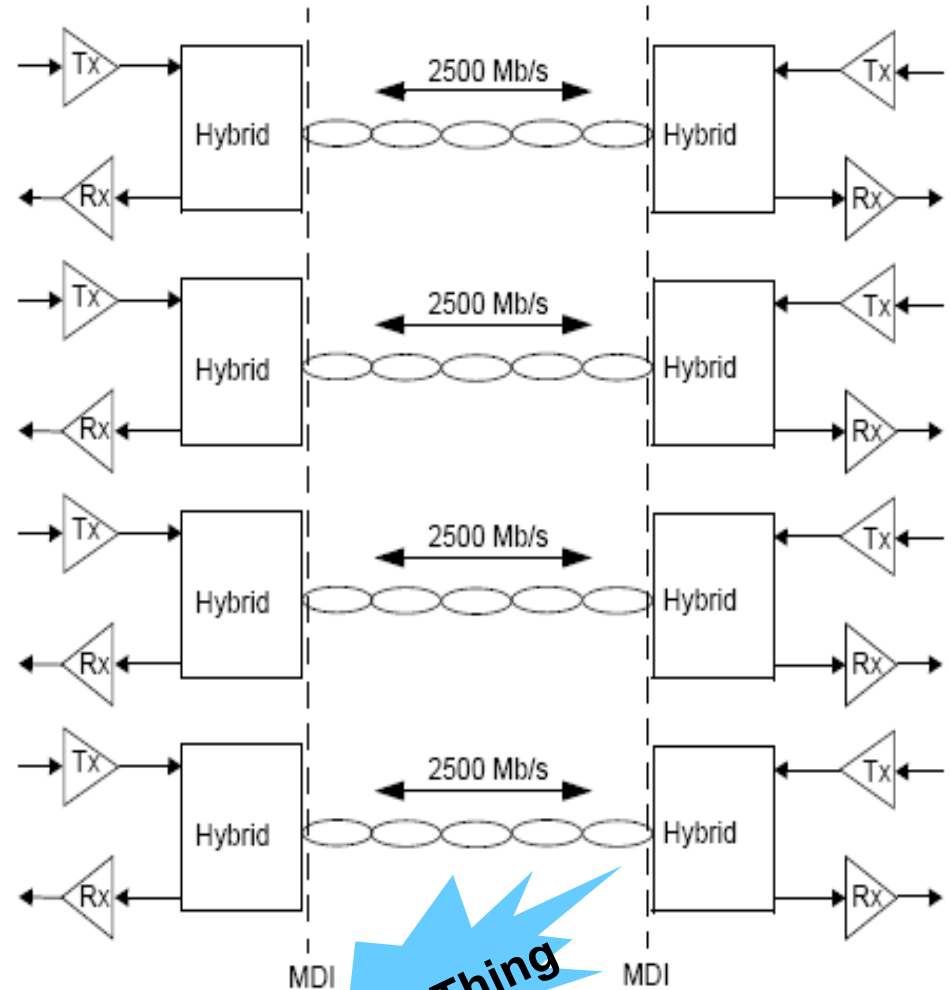
8 Low Speed Signal  
lines for Control and  
Power Testing  
(10 – Position  
Connector)

Input Power  
Connectors



# 10GBASE-T - Overview

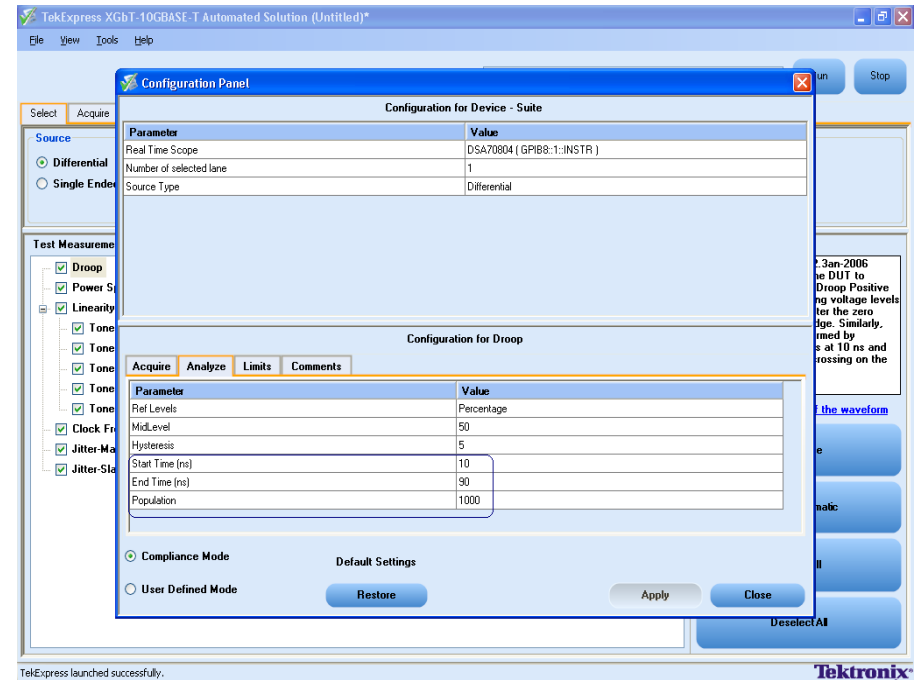
- **10GBASE-T provides 10 gigabit/second connections over unshielded or shielded twisted pair cables, over distances up to 100 m. 2.5Gbps per lane (A, B, C & D)**
- **Baseband 16-level PAM signaling with a modulation rate of 800 Msymbols per second is used on each of the wire pairs.**
- **Supports full duplex operation only**
- **Compatibility of Auto Negotiation enabled to also operate 10/100/1000 BASE-T**
- **Supports a BER of less than or equal to  $10E-12$  on all supported distances and Classes**
- **Provides a cost advantage over fiber**



**Next Big Thing**

# Maximum Output Droop

- **Purpose** - To verify that the transmitter output level does not decay faster than the maximum specified rate.
- The resulting magnitude of both the positive and negative droop shall be less than 10%.
- Flexibility to test beyond compliance – XGbT provides the flexibility to perform testing beyond what is specified in IEEE standard 802.3an-2006. It helps users to analyze their PHY in addition to compliance tests.
- Configure the DUT for Test Mode 6 operation
- IEEE standard 802.3an-2006, sub clause 55.5.3.1



# XGbT - Report

- TEKEXP software provides summary-reporting capability of all lanes in .mht (HTML) format with pass/fail status.
- A detailed report of each lane's performance including test configuration details, waveform plots, and margin analysis is also produced by XGbT providing more insight into compliance efforts underneath the XGbT standard.
- Report also provides additional details like calibration status, scope model, probe model, software version etc

The screenshot displays the TekExpress XGbT-10GBASE-T Automated Solution software interface. The window title is "TekExpress XGbT-10GBASE-T Automated Solution (Untitled)\*". The interface includes a menu bar (File, View, Tools, Help), a toolbar with "Run" and "Stop" buttons, and a "DUT ID" field containing "DUT001". Below the toolbar are tabs for "Select", "Acquire", "Analyze", and "Report". The main content area shows the "TekExpress Automation Framework" logo and the title "XGbT Signal Characteristics Test Report".

Key parameters displayed include:

- DUT ID: DUT001
- Date/Time: 7/8/09 11:40
- Device Type: Transmitter
- Execution Time: 32 Min
- Compliance Mode: True
- Overall Test Result: Pass
- Scope Model: DSA70804
- Scope Serial Number: Q435
- Scope FW Version: 4.3.3.ACHLLESBUILD.12
- Calibration Status: PASS,PASS
- TekExpress Version: 1.3.4.125
- XGbT Version: 0.8.1.3

The report is for "Lane-A" and contains a table with the following data:

Test Name	Measurement Details	Limit1	Measured value	Limit2	Units	Test Result	Compliance Mode	Execution Time	Comment
Clock Frequency	Clock Frequency	-50.00	1.85	50.00	ppm	Pass	TRUE	2 Min	
Drop	Drop Positive	0.00	1.74	10.00	%	Pass	TRUE	2 Min	Vhigh = 1.011V
	Drop Negative	0.00	1.96	10.00		Pass			Vhigh = -989.2mV
Linearity	Linearity Tone-1	54.50	63.41	0.00	dBm	Pass	TRUE	0 Min	IMD
	Linearity Tone-2	50.30	63.85	0.00		Pass			IMD
	Linearity Tone-3	45.40	60.89	0.00		Pass			IMD
	Linearity Tone-4	41.60	58.37	0.00		Pass			IMD
	Linearity Tone-5	38.50	54.61	0.00		Pass			IMD

At the bottom of the interface, there are navigation buttons for "Report Summary", "Lane A", "Lane B", "Lane C", and "Lane D". A status bar at the very bottom indicates "TekExpress launched successfully." and the Tektronix logo is visible in the bottom right corner.

# TF-XGbT Test Fixture

- The XGbT test fixture provides easy access to the 10GBASE-T Electrical signals to perform conformance testing and device characterization as described in of IEEE 802.3an-2006 sub-clause 55.5.3 & 55.8.2.1. This fixture is used with the Tektronix's XGbT- 10GBASE-T Automation Solution to provide fast and accurate design debugging and validation. XGbT fixture covers all seven measurements including Jitter Slave and MDI Return Loss



Fig 1: XGbT Test Fixture main board

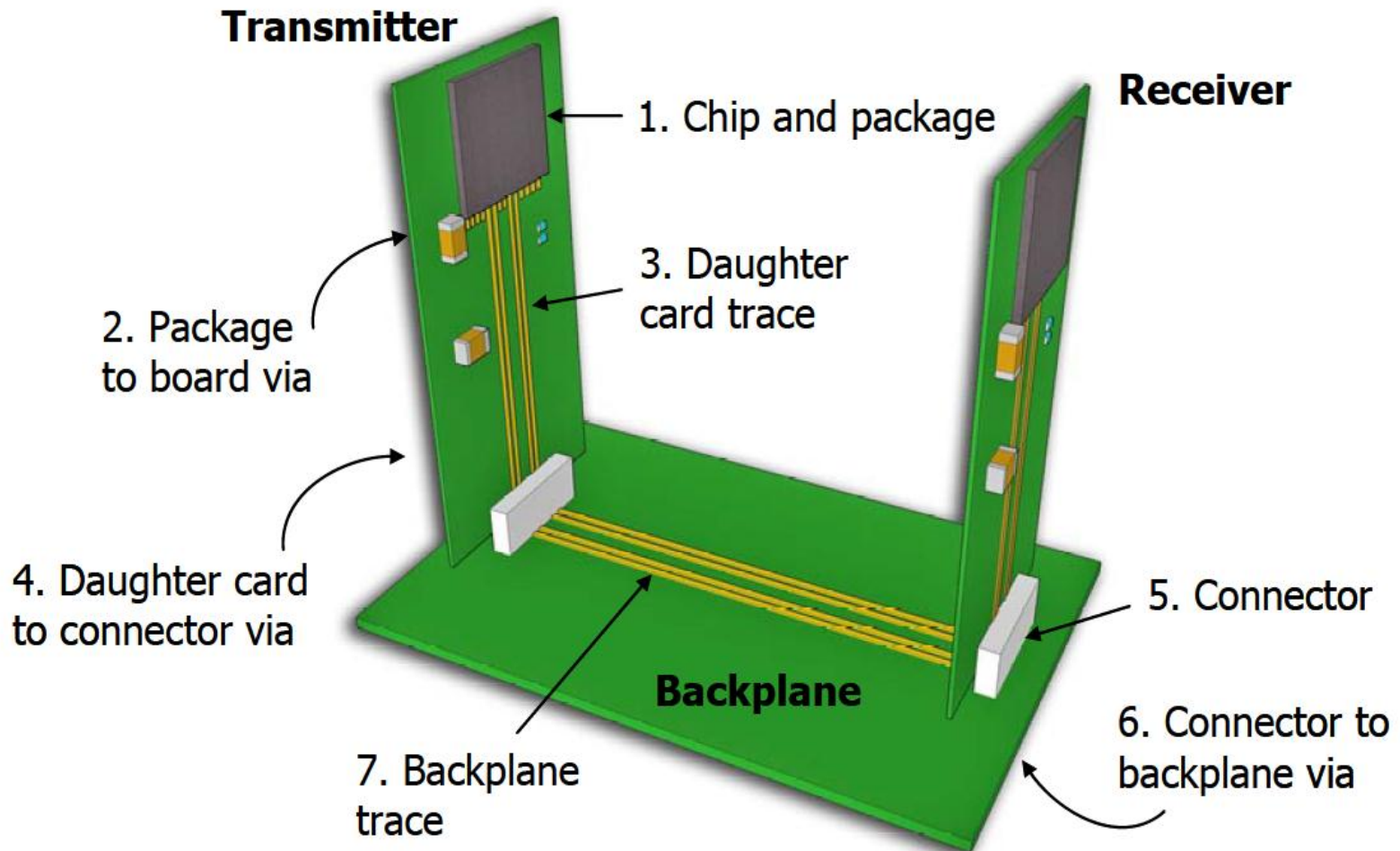


Fig 2: Calibration Board



Figure 3: RJ45 Shielded Patch cord

# 10G-KR Typical Backplane Ethernet

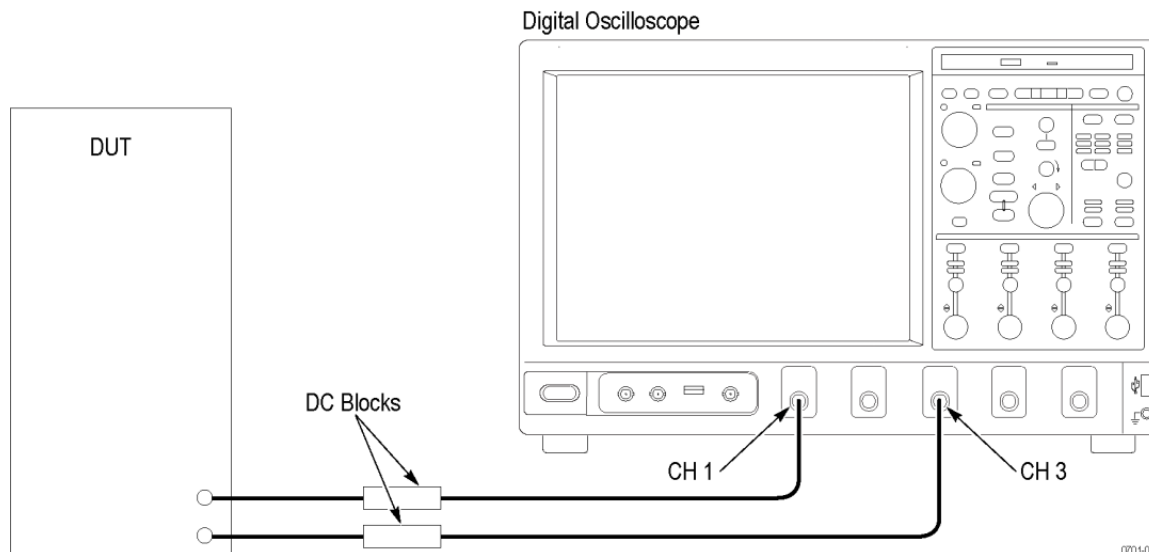
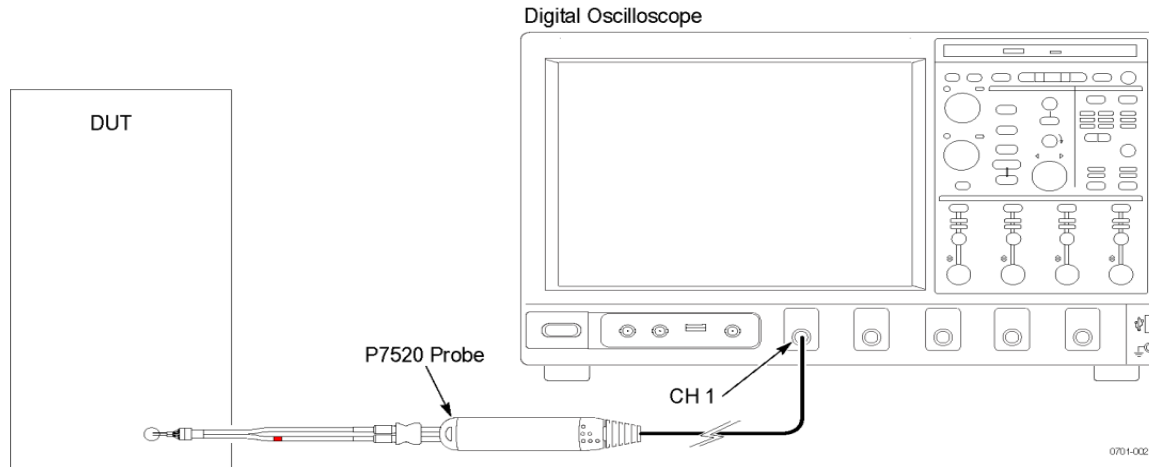


# 10G-KR自动化测试软件

The screenshot displays the TekExpress 10G-KR (Evaluation Version) software interface. The main window title is "TekExpress 10G-KR (Evaluation Version) - (Untitled)\*". The interface is divided into several sections:

- Left Sidebar:** Contains navigation buttons for "Setup", "Status", "Results", and "Reports". A vertical progress indicator shows the current step is "2 Test Selection", with "DUT", "Acquisitions", and "Preferences" also marked as completed.
- Top Bar:** Includes an "Options" dropdown menu and a close button (X).
- Device Information:** Shows "Device : Source : CTS 0.9".
- Test Selection List:** A list of tests under the "10GKR" category, all of which are checked. The selected tests are:
  - Test 72.7.1.3\_Signaling speed
  - Test 72.7.1.4\_Differential peak-to-peak output voltage (max)
  - Test 72.6.5\_Differential peak-peak output voltage (max) with Tx disa
  - Test 72.7.1.4\_Common-mode voltage limits
  - Test 72.7.1.7\_Transition time
  - Test 72.7.1.8\_Max output jitter (peak-peak)
  - Test 72.7.1.10\_Transmitter output waveform characteristics
  - Test 72.7.1.11a\_Output waveform coefficient update
  - Test 72.7.1.11b\_Output waveform coefficient status
- Test Description:** A text area showing the description for the selected test: "The 10GBASE-KR signaling speed shall be 10.3125 GBd ± 100 ppm." Below this are "Schematic" and "Configure" buttons.
- Right Side:** Features a "Start" button (green with a refresh icon) and a "Pause" button (grey with a pause icon).
- Bottom Bar:** Displays the "Tektronix" logo and a "Status Ready" indicator.

# Testing connection for 10G-KR



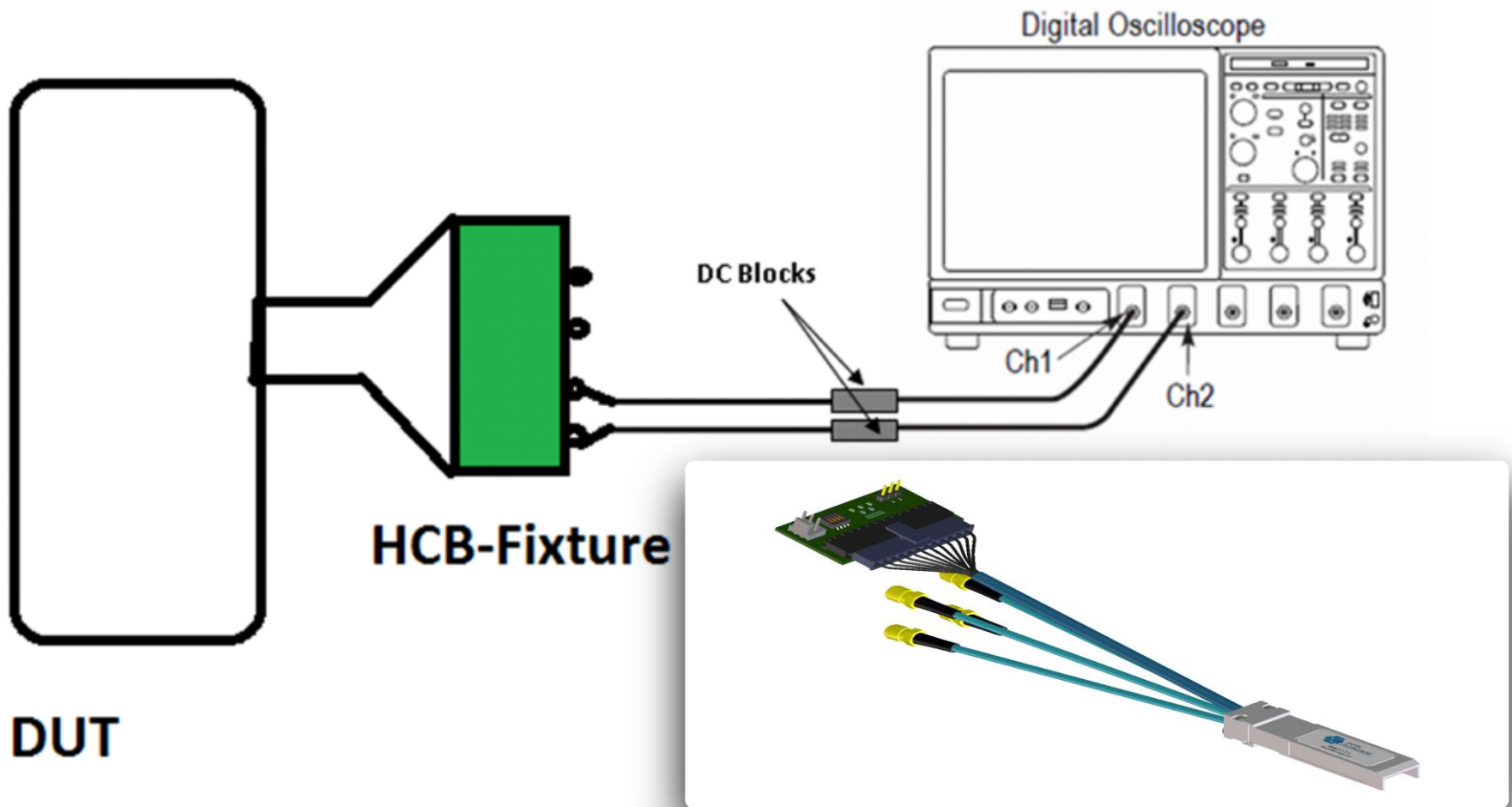


# Tektronix SFP-TX – Automation & DPOJET Option

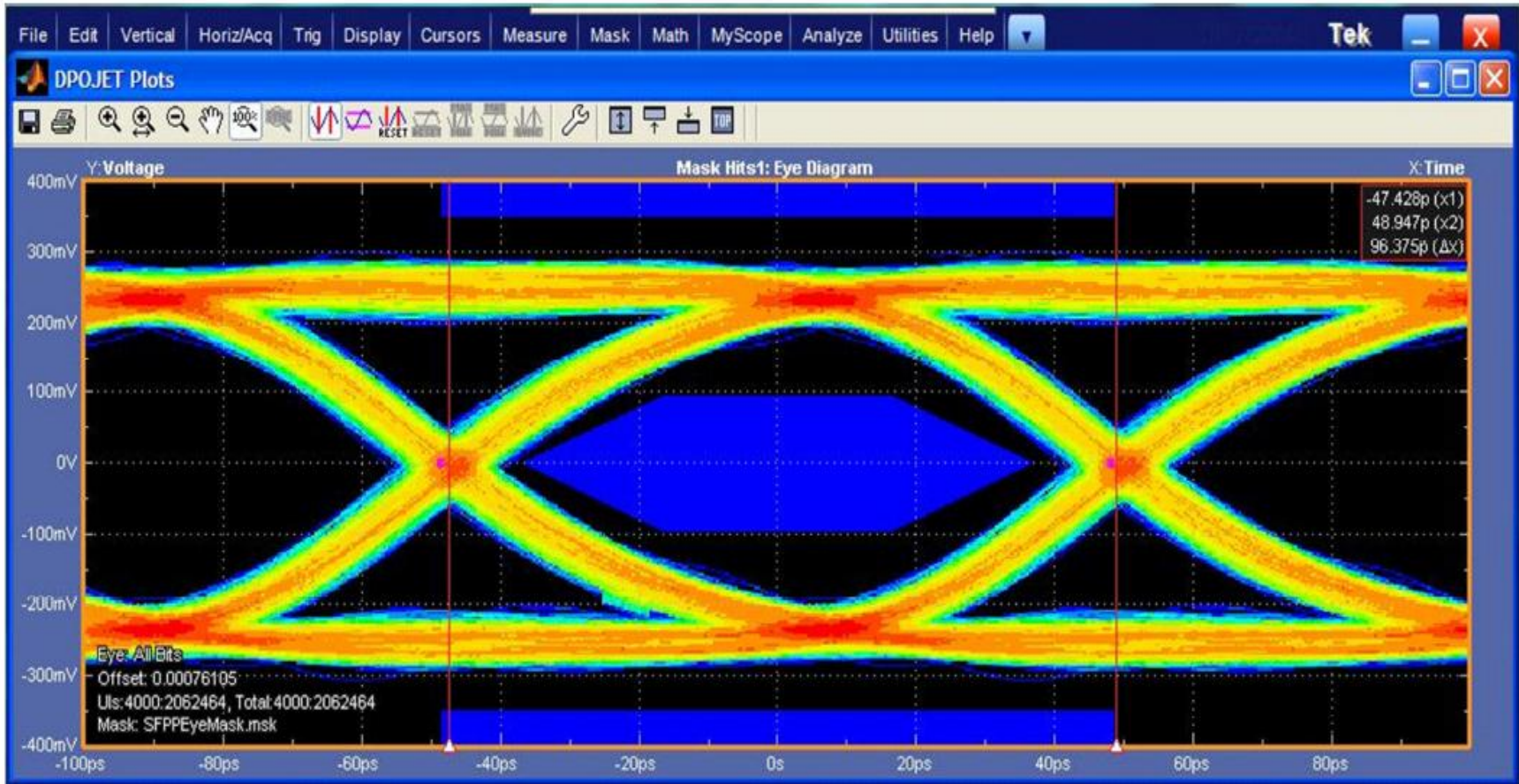
SL No.	Measuremnts	Signal Type Recommended	Limit			
			Min	Target	Max	Units
Host Transmitter output electrical Specifications:						
1	Single Ended Output Voltage Range	PRBS31	-0.3		4	V
2	Output AC Common Mode voltage (RMS)	PRBS31			15	mV(RMS)
Host Transmitter Jitter and Eye Mask specifications						
3	Crosstalk source rise/fall time (20%-80%) (Tr, Tf)	8180		34		ps
4	Crosstalk source amplitude (p-p differential)	8180		1000		mV
5	Signal rise/fall time (20%-80%) (Tr, Tf)	8180	34			ps
6	Total Jitter (p-p) (Tj)	PRBS31			0.28	UI(p-p)
7	Data Dependent Jitter (p-p) (DDJ)	PRBS9			0.1	UI(p-p)
8	Data Dependent Pulse Width Shrinkage (p-p) (DDPWS)	PRBS9			0.055	UI(p-p)
9	Uncorrelated Jitter (RMS) (UJ)	PRBS9			0.023	UI(p-p)
10	Transmitter Qsq	8180	50			
11	Eye mask hit ratio(Mask hit ratio of 5x10-5)	PRBS31	X1=0.12UI, X2=0.33UI, Y1=95mV, Y2=350mV			
Host Transmitter output specifications for Cu (SFP+ host supporting direct						
12	Voltage Modulation Amplitude (p-p)	8180	300			mV
13	Transmitter Qsq Output AC Common Mode voltage	8180	63.1			
14	Output AC Common Mode Voltage	PRBS31			12	mV(RMS)
15	Host Output TWDPc	PRBS9			10.7	dBc

The image displays two screenshots of the Tektronix software interface. The top screenshot shows a signal waveform with a menu open, highlighting the 'Jitter and Eye Analysis (DPOJET)' option. The bottom screenshot shows the 'TekExpress SFP+ Tx - (Untitled)' configuration window. This window includes a 'Test Selection' list with various specifications checked, such as 'SFF-8431 Table 11 Output Electrical Specifications at B', 'Crosstalk Source Rise/Fall Time (20%-80%)', and 'SFF-8431 Table 33 Output Specifications at B for Cu'. A 'Test Description' section provides details on how the rise/fall time is measured.

# SFP test connection



# SFP Eye Mask hit ratio :less than 5E10-5



# Tektronix Solutions for PCI Express 3.0 Measurements

- Introducing option PCE3 for DSA/DPO/MSO70K Scopes
- Support for NEW Base Spec measurements
- Support for CEM Specification
- Supports all versions of PCI Express

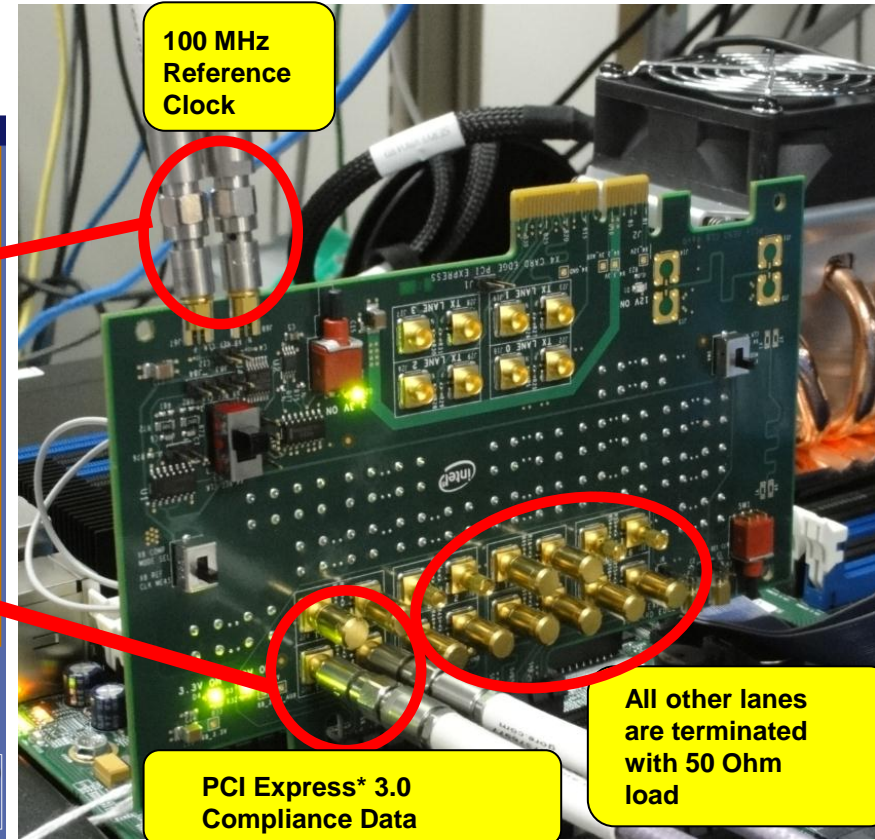


The screenshot shows the "Jitter and Eye Diagram Analysis Tools" panel with a table of test results. The overall test result is "Pass".

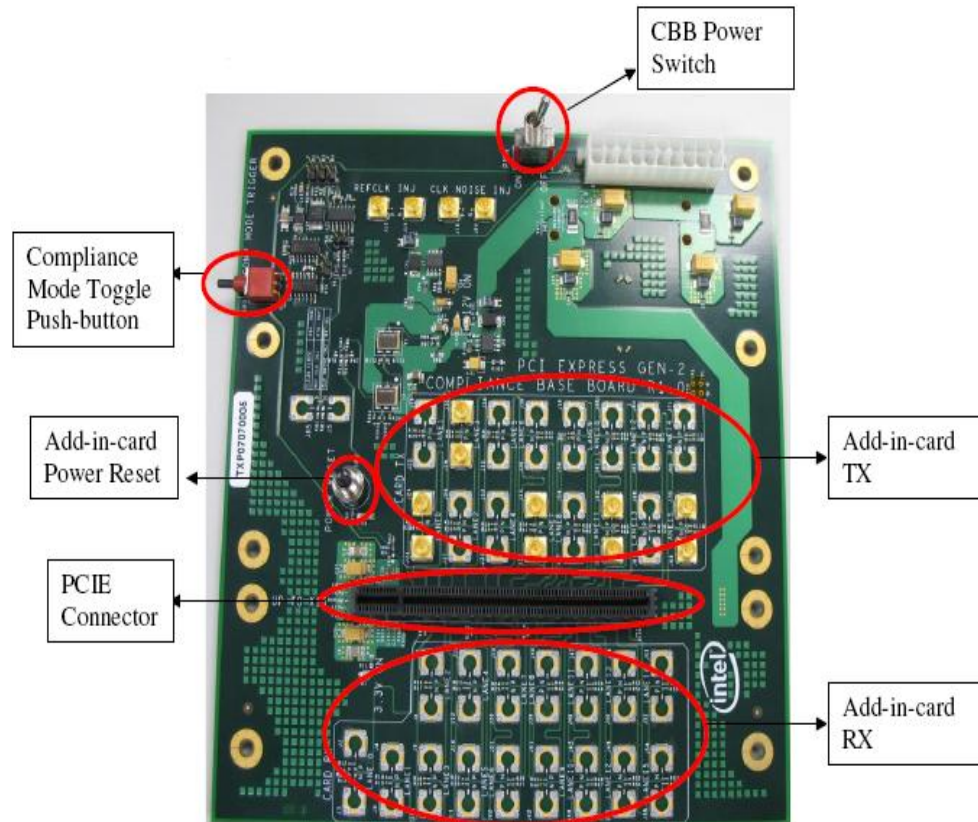
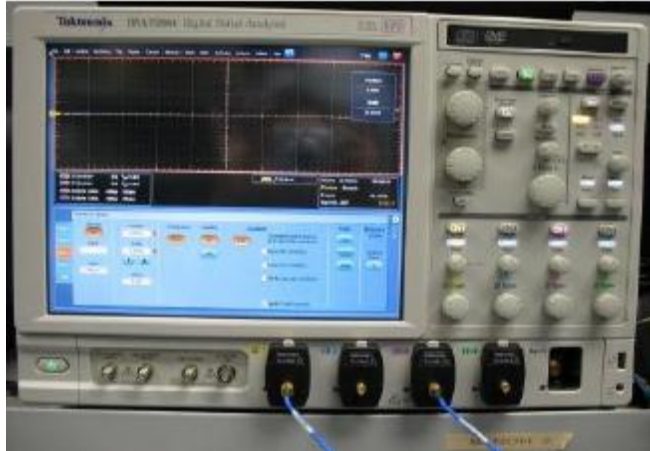
Description	Pass/Fail	Mean	Std Dev	Max	Min	p-p	Population
V-TX-FS-NO-EQ, Ma...	Pass	1.0157V	1.4688mV	1.0196V	1.0116V	8.0250mV	341
V-TX-EIEOS-FS, Ma...	Pass	959.37mV	3.0854mV	970.50mV	950.92mV	19.575mV	2730
T-TX-UTJ, Math1	Pass	7.2816ps	0.0000s	7.2816ps	7.2816ps	0.0000s	1
T-TX-UDJDD, Math1	Pass	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	1
T-TX-DDJ, Math1	Pass	12.072ps	0.0000s	12.072ps	12.072ps	0.0000s	1
T-TX-UPW-TJ, Math1	Pass	8.8315ps	0.0000s	8.8315ps	8.8315ps	0.0000s	1
T-TX-UPW-DJDD, M...	Pass	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	1
Eye Diagram, Math1	Pass	677.15mV	0.0000V	677.15mV	677.15mV	0.0000V	1
UI, Math1	Pass	125.00ps	1.8156ps	134.59ps	116.46ps	18.132ps	1.6000M



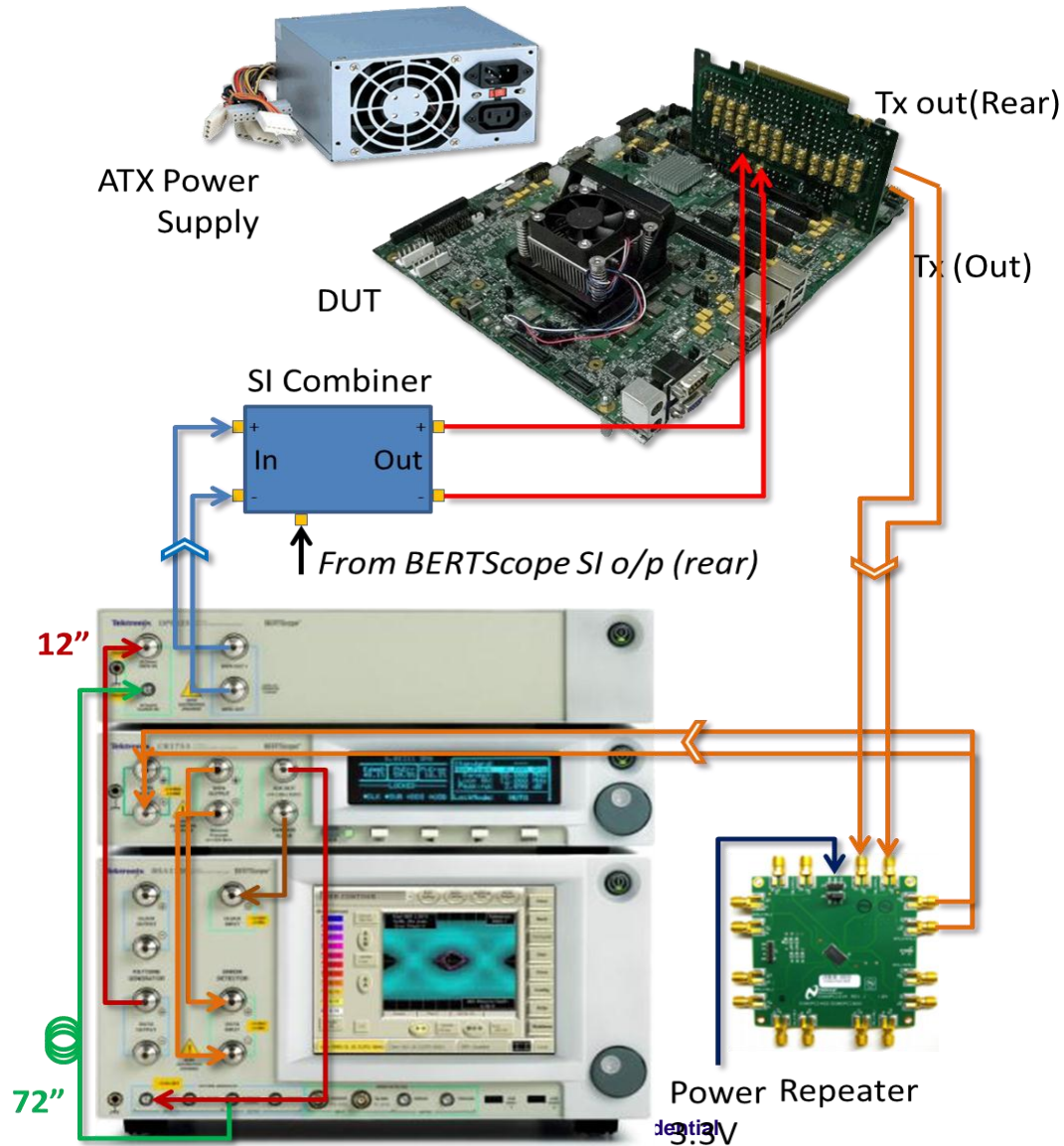
# PCIe Dual-Port TX Measurement Example for System



# PCIE TX Measurement Example for Add-in Card



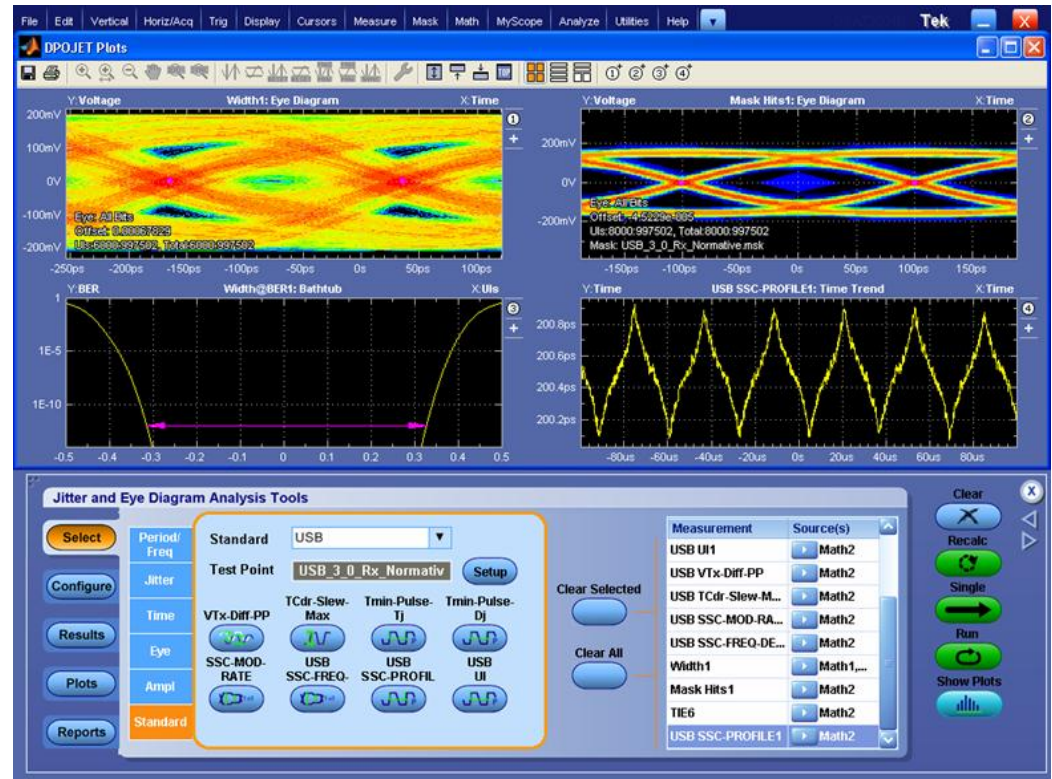
# RX Measurement Example for Host





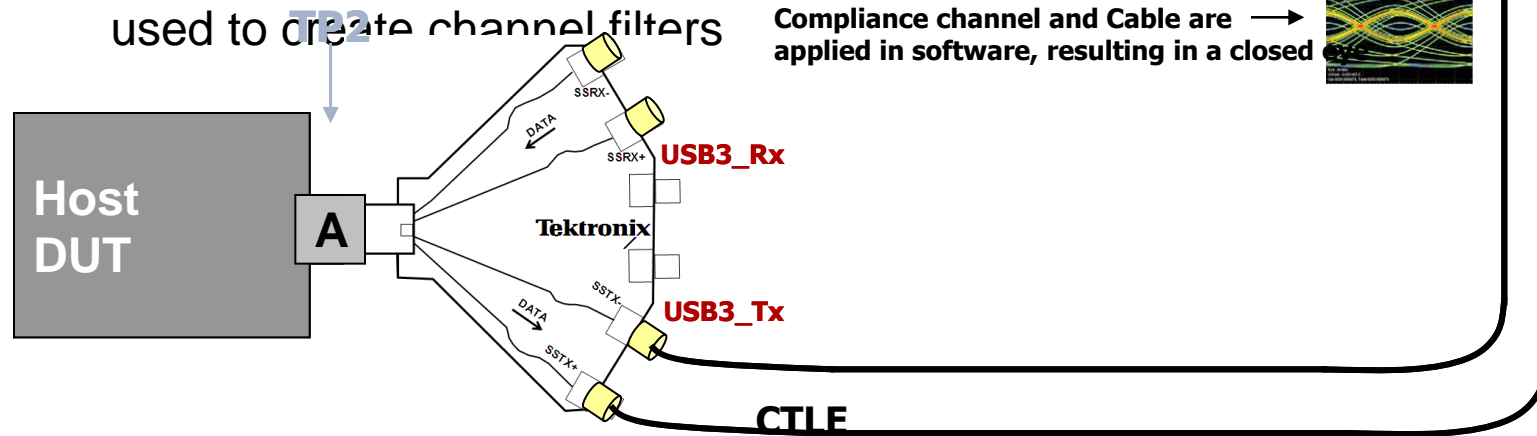
# USB 3.0 Transmitter Measurement Overview

- Voltage and Timing
  - Eye Height
  - Pk to Pk Differential Voltage
  - RJ
  - DJ
  - TJ
  - Slew Rate
  
- Low Frequency Periodic Signaling (LFPS)
  - Pk to Pk Differential Voltage
  - Rise / Fall Time
  - AC Common Mode
  - tBurst
  - tRepeat
  - tPeriod
  
- SSC
  - Modulation Rate
  - Deviation



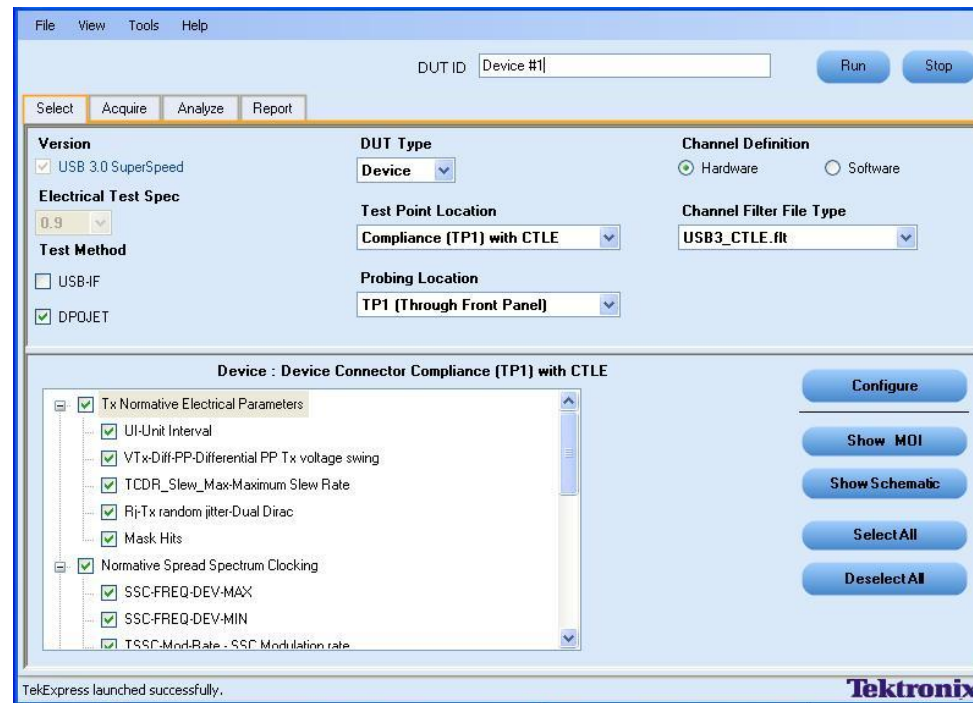
# Transmitter Compliance Test Setup

- USB-IF or Tektronix fixtures can be used
  - Test configuration is the same
- Compliance channel and 3 meter cable are emulated in software
  - Compliance sparmeters were used to create channel filters

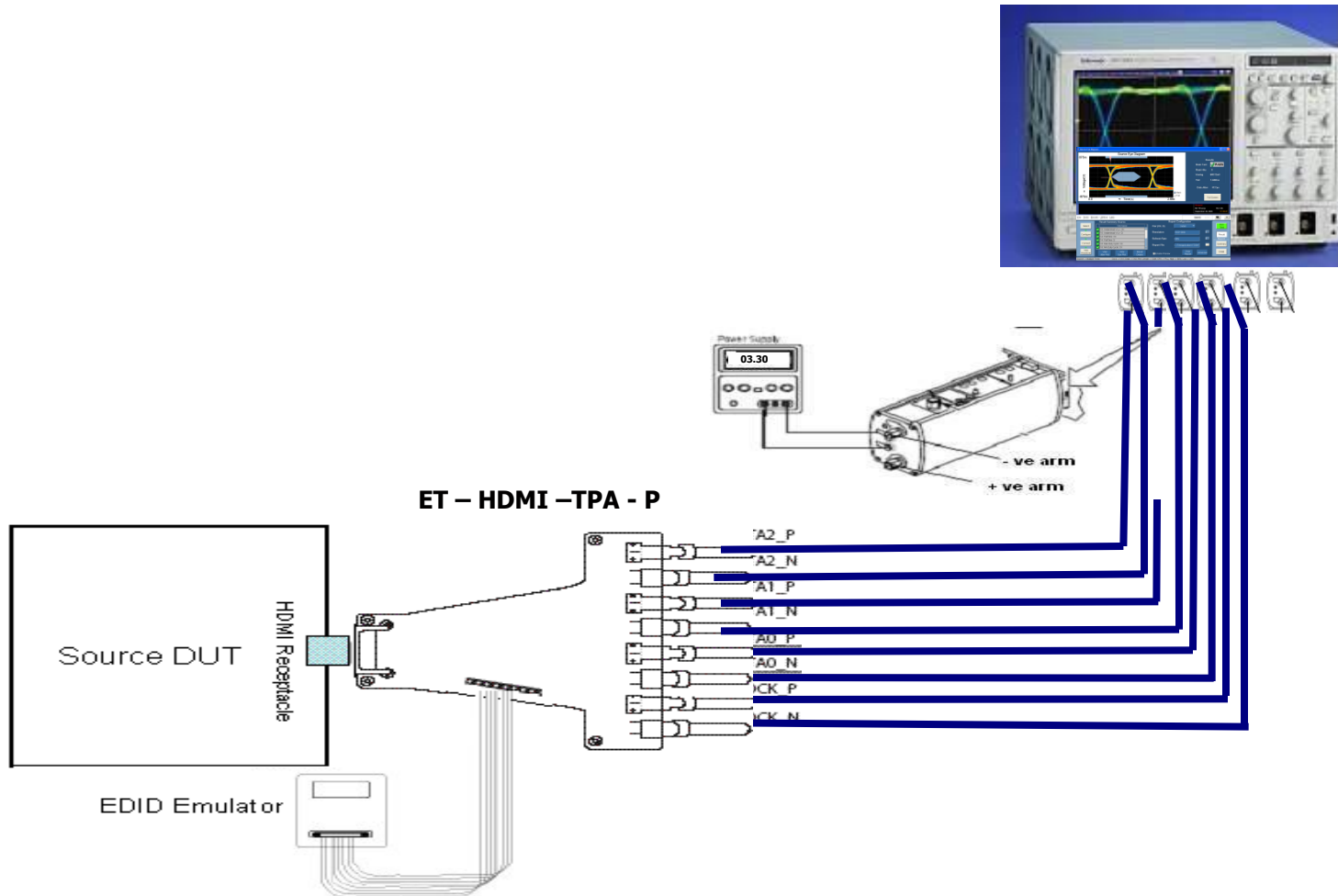


# USB 3.0 Compliance and Automation

- Complete Automation of USB 3.0 Measurements with TekExpress
- No need to learn technology specific software applications- TekExpress is a Common Framework from Serial Applications including SATA, USB, DisplayPort, HDMI, and Ethernet
- TekExpress utilizes DPOJET USB 3.0 Specific algorithms making it easy to move from compliance to DPOJET for debug

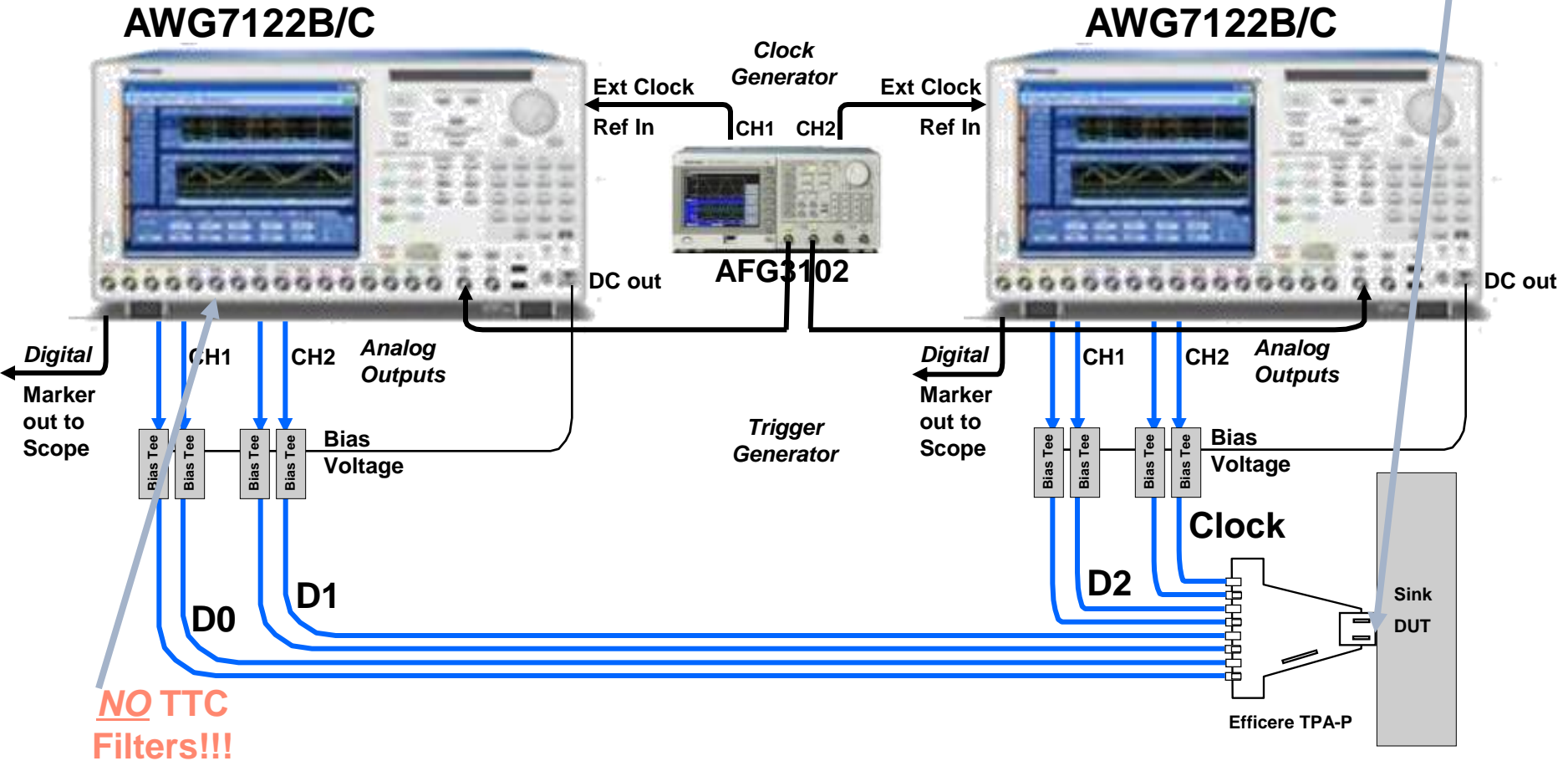


# HDMI 测试方案-源端

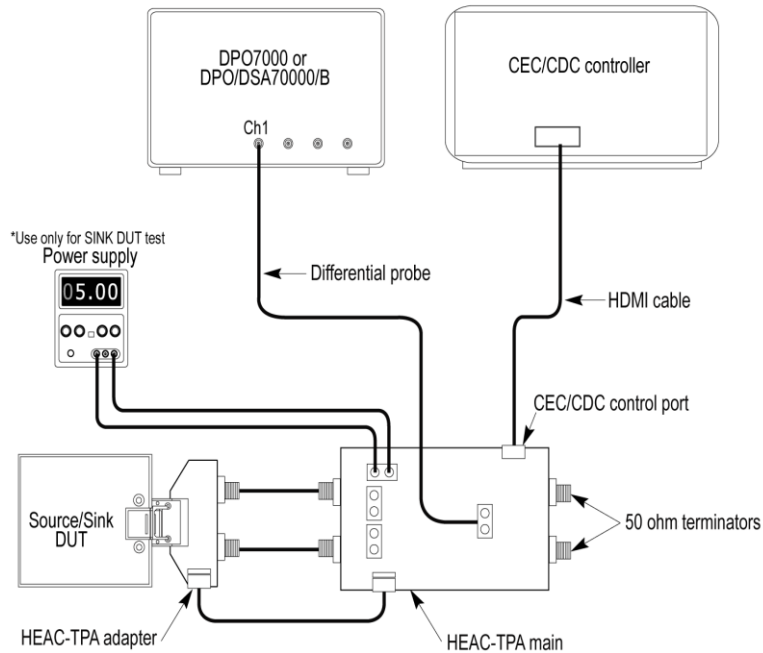


# HDMI 测试方案-接收端(TV/Monitor)

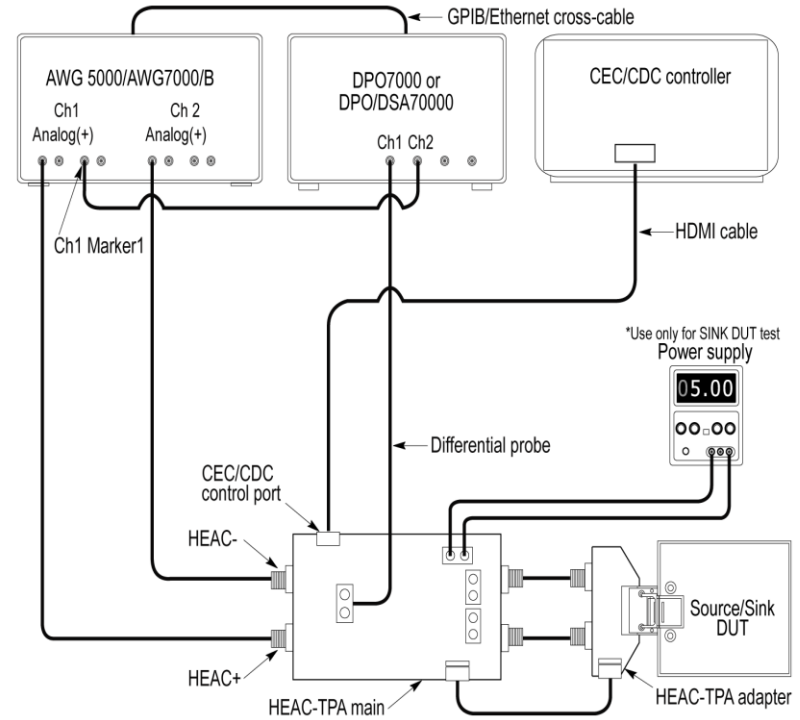
**NO Cable Emulator!!!**



# HDMI 1.4 HEAC Solution Configuration



**Tx Test Setup**



**Rx Test Setup**



# HEAC Software

**TekExpress HEAC Automated Solution (Evaluation Version) (Untitled)\***

File View Tools Help

DUT ID:  Run Stop

Select Acquire Analyze Report

**Select Device**

- HEAC-Transmitter
- HEAC-Receiver

**Select Test Suite**

- Differential-Rx
- CommonMode-Rx
- SingleMode-Rx

**Version**

CTS 1.4

DUT IP Address

Auto Detect MAC Address

**HEAC-Receiver : Differential-Rx CTS 1.4**

Select	Test Name
<input checked="" type="checkbox"/>	Receiver Performance - Nominal Response
<input checked="" type="checkbox"/>	5.16 Receiver Performance - Amplitude
<input checked="" type="checkbox"/>	5.16 Receiver Performance - Clock Frequency
<input checked="" type="checkbox"/>	5.16 Receiver Performance - Common mode
<input checked="" type="checkbox"/>	5.16 Receiver Performance - Signal Source Impedance
<input checked="" type="checkbox"/>	5.16 Receiver Performance - Worst Case Cable

**Test Description**

This optional test verifies the receiver capability to respond to nominal amplitude, clock frequency and

Configure

Show Schematic

Select All

Deselect All

TekExpress launched successfully. **Tektronix**



# MHL Compliance Software for Automated Tx Tests: Option MHD

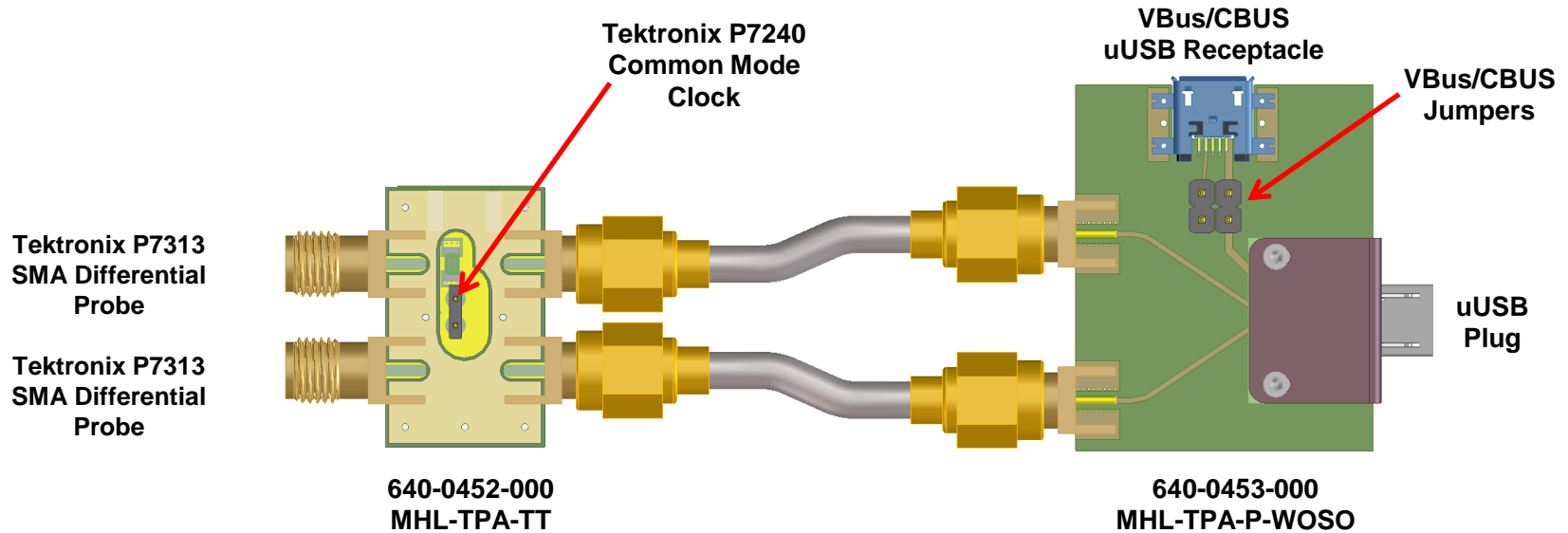
The screenshot displays the TekExpress MHL software interface. The main window is titled "MHL Physical Layer Solution : MHL Transmitter : Spec 1.0". On the left, a vertical navigation bar shows three steps: "1 DUT" (checked), "2 Test Selection" (highlighted), and "3 Acquisitions". Below this are buttons for "Setup", "Status", "Results", and "Reports". The central area contains a tree view of test items, all of which are checked:

- MHL Clock
  - 3.1.1.7 Common-mode Rise and Fall Times-TR\_CM, TF\_CM
  - 3.1.1.10 MHL Clock Duty Cycle 24-Bit or Packed Pixel Mode
  - 3.1.1.11 MHL Clock Jitter
- MHL Data
  - 3.1.1.2 Single-ended High Level Voltage-VSE\_HIGH
  - 3.1.1.3 Single-ended Low Level Voltages-VSE\_LOW
  - 3.1.1.4 Differential Output Swing Voltage-VDF\_SWING
  - 3.1.1.5 Common-mode Output Swing Voltage-V\_CMSWING
  - 3.1.1.6 Differential Rise and Fall Times-TR\_DF, TF\_DF
  - 3.1.1.8 Differential Intra-Pair Skew-TSKEW\_DF
  - 3.1.1.12 MHL Data Eye Diagram

At the top right of the main window are buttons for "Deselect All", "Select Required", and "Select All". Below the tree view is a "Test Description" section with a text area and "Schematic" and "Configure" buttons. On the right side of the interface are "Start" and "Pause" buttons. At the bottom left, the status bar shows "Tektronix Status Ready" with a green progress indicator. At the bottom right, there are "Adv Setup" and "DPOJET" buttons.



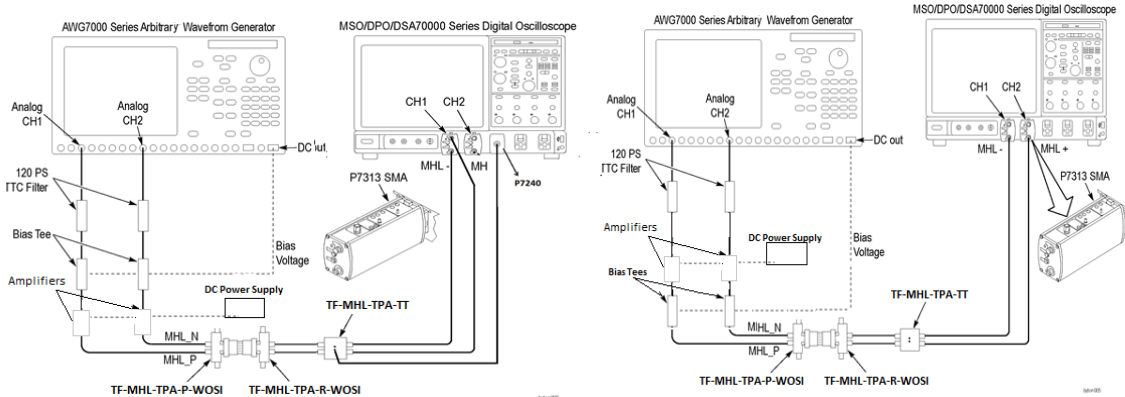
# Wilder Fixtures: Tektronix MHL Source Testing Setup



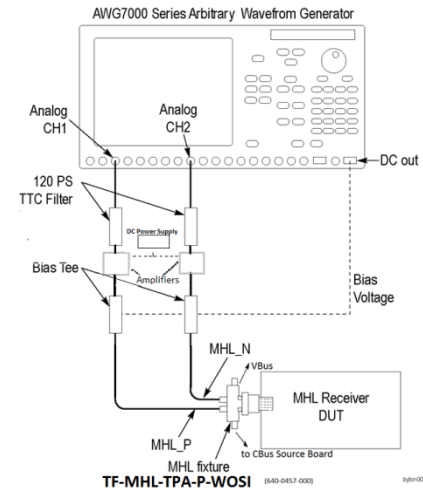
# Tektronix MHL Solution Setup: Simple and Easy Sink and Dongle Min/Max Testing -2

## Setup based on Direct Synthesis Capability of AWG7122C Series

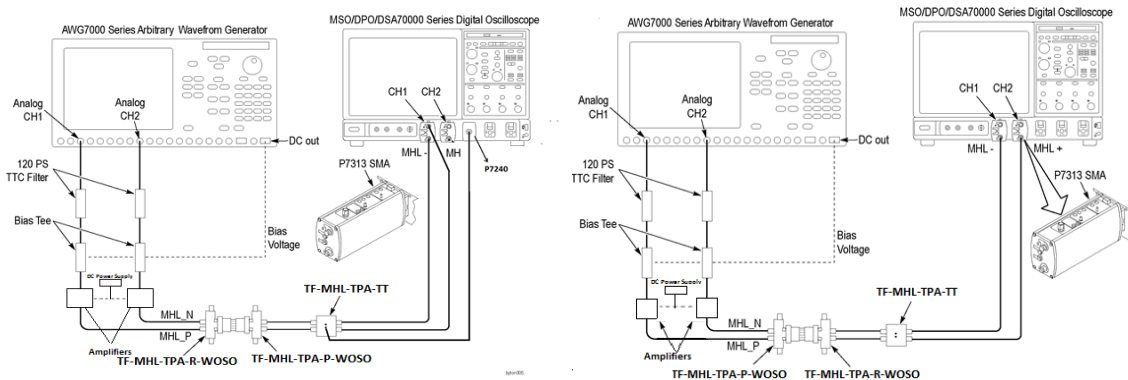
### AWG Sink Min/Max Signal ( CM,SE and Diff) Verification Using Real Time Oscilloscope



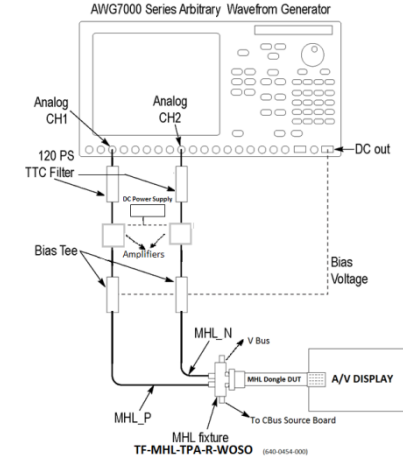
### Test Setup for Sink Min/Max Tests



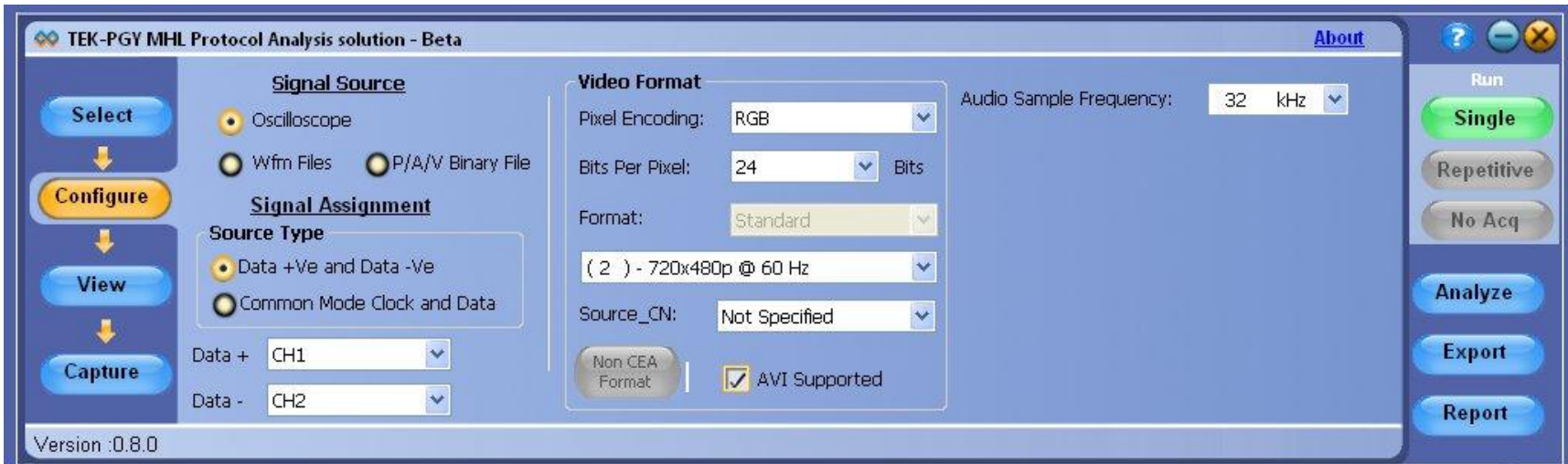
### AWG Dongle Min/Max Signal ( CM,SE and Diff) Verification Using Real Time Oscilloscope



### Test Setup for Dongle Min/Max Tests



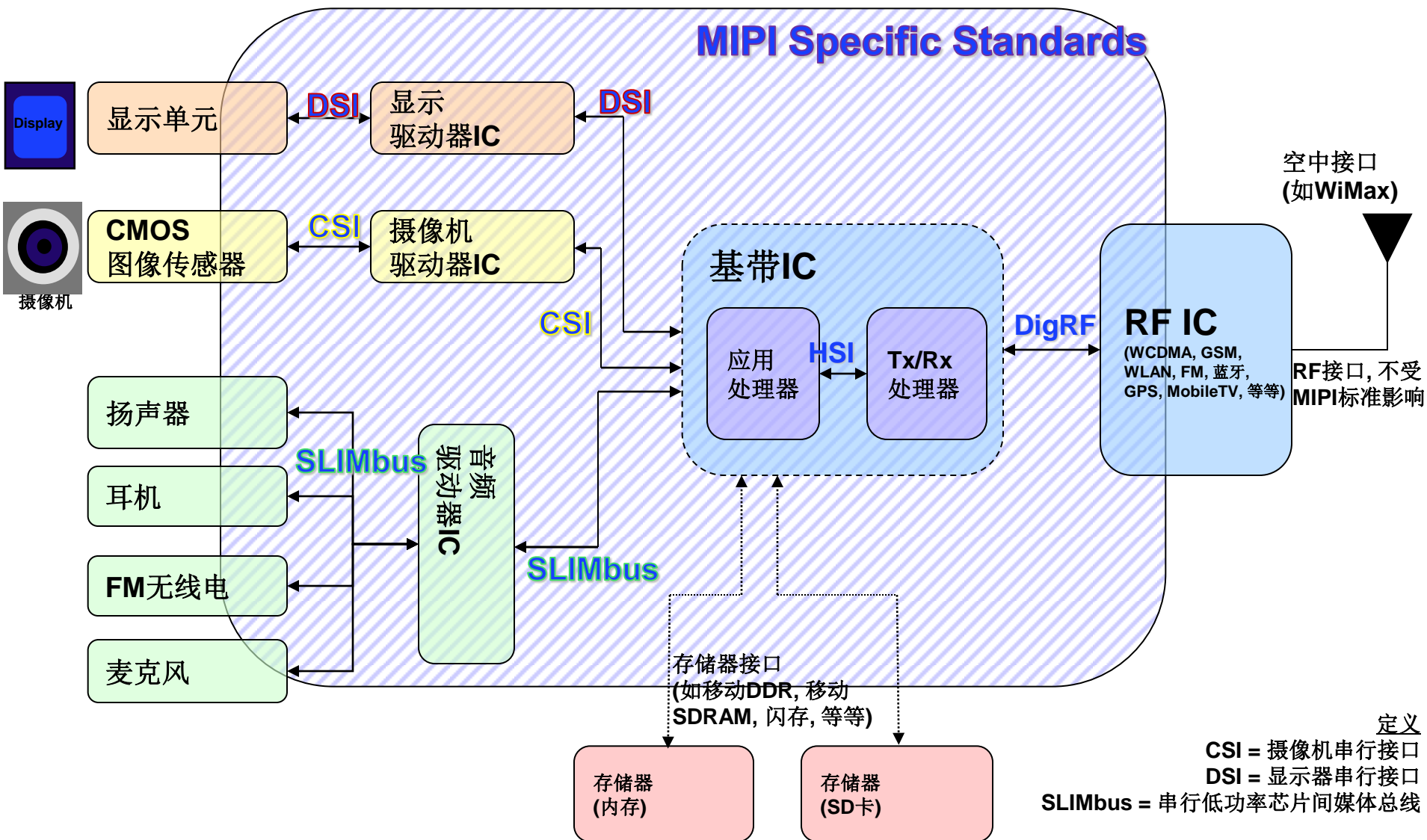
# Tektronix MHL Protocol Analyzer





# MIPI标准概述

## 移动终端方框图实例



# D-PHY Tx测试解决方案 – 续

## ■ 示波器

- 推荐: **DPO7354或DPO/DSA/MSO70404/B**
  - 用来测量规范 $\pm 5\%$ 误差范围内的上升时间(150ps)
  - 如果不考虑上升时间的测试, 可以使用DPO7254

## ■ 探头

### - 探头考虑因素

- 同时测量单端性能和差分性能
- 动态范围必须 $>1.2V$
- 探头衰减要达到最小
  - 1X最好, 2.5X或5X也行

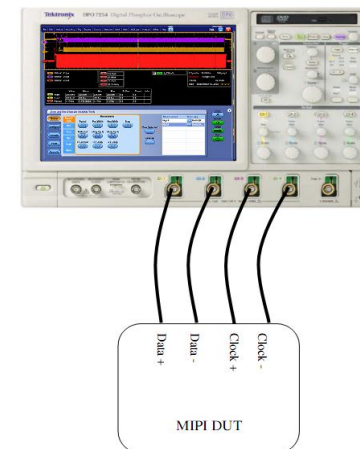
### - 推荐:

- **DPO7000**采用四只**TAP3500**; **MSO/DPO/DSA70000/B**采用四只**P7240**
- (Ch1: D+), (Ch2: D-), (Ch3: Clk+), (Ch4: Clk-)
- TAP2500也适合低数据速率的DUT

### - 也可以使用:

#### - 焊接式探头

- **DPO7000**采用**TDP3500**, **70000**系列采用**P73xx**
- (Ch1: D+, Gnd), (Ch2: D-, Gnd), (Ch3: Clk+ & Clk-)



# New Opt.D-PHYTX

## ■ Opt.D-PHYTX : D-PHY Automated Solution

- TekExpress option for Fully-Automated testing
- Automation similar to Opt.USB-TX
- Provides Conformance and Characterization Testing
- Based on D-PHY Base Spec v1.0 and UNH's Conformance Test Suite v0.98.
- Runs on DPO7000, DPO/DSA/MSO70000/B Series oscilloscopes

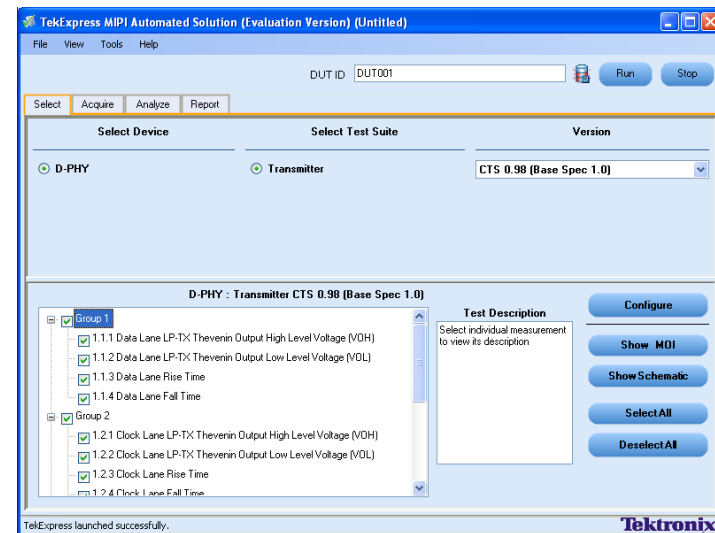
## ■ Opt.TEKEXP is Pre-Requisite

## ■ Differentiation

- Un-parallel Automation (Auto-Cursors/ Regions)
- For Conformance testing to Latest CTS (v0.98)
- Based on Latest Base spec (v1.0)

## ■ Value proposition

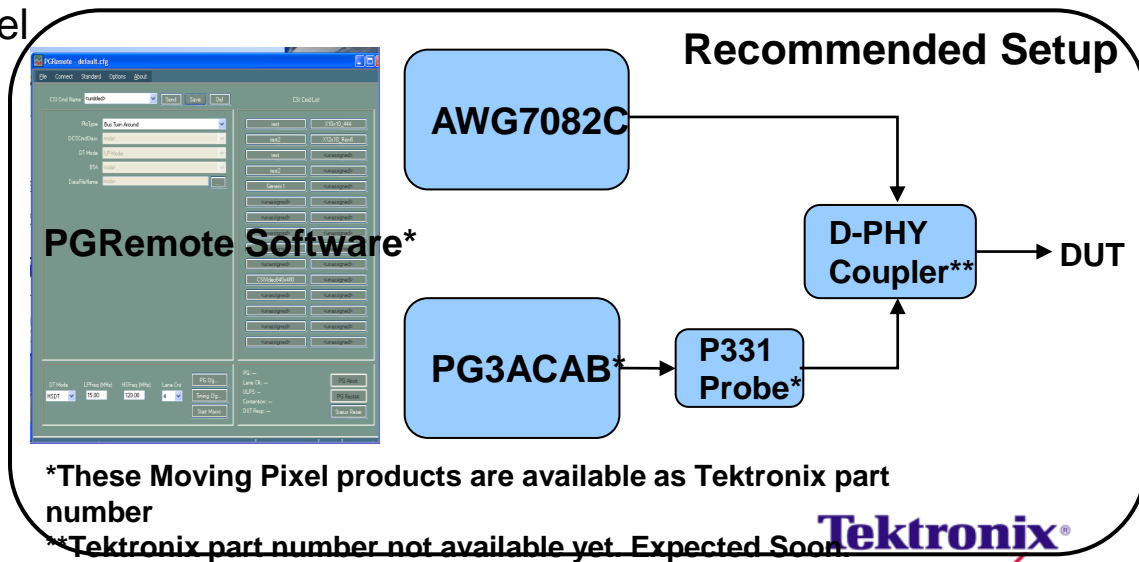
- Custom-limits/ Limits-Editing on the fly
- Test Reports
  - Zoom-in waveform captures at the Cursors/ Regions
  - Pass/Fail Summary with Margin details
- Tek 3.5GHz scope is the minimal configuration for accurate testing
  - i.e. unlike Agilent 4G scope at entry-level



# D-PHY Rx : Test Solution Overview

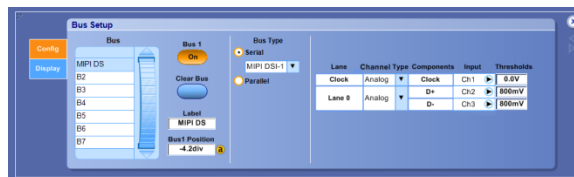
Simple, Quick, Easy and Re-usable

- 100% Coverage to Rx CTS
  - Meets all the requirements in UNH-IOL CTS document (v0.98)
- Quick and Easy setup
  - No complex VXI system, just stand alone instruments, and a probe.
- Cost effective solution
  - 70% Lower list price vs Competition
- Re-usable for Protocol tests
  - PG3A is the Only 4 channel solution for CSI & DSI test
- PG3A Pattern Generator
  - Controls clock and signaling to establish link with DUT
  - Adjusts voltage levels, packet type, etc to stress test receiver
- AWG7082C Generator
  - Adds jitter and interference to the D-PHY signals



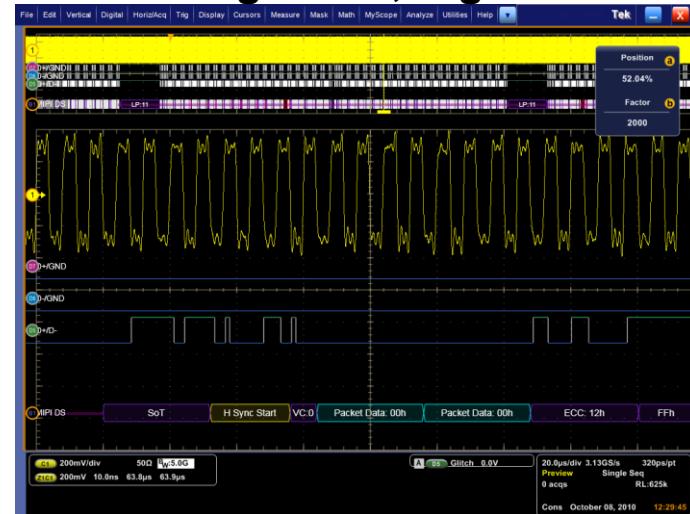
# D-PHY Decode: Opt.SR-DPHY for DSI/ CSI-2 Decode Simultaneous Acquisition

- Probe using Analog, Digital or Mixed Channels
- Simultaneous probing of DSI & CSI using MSO channels
- Working on multi-lane support, using high performance MSO digital channels
- Supported on all 7KC, 70KC and MSO70K scopes. (**Win7-OS only**)
  - Option key bit #25
- Software installed as part of TekScope firmware v6.1.2.4 or later.
  - Browse to TekScope Menu --> Vertical --> Bus Setup --> Select Bus Type as Serial--> Select MIPI DSI or CSI from the drop down list.



Probe using Mixed Channels

## Analog Clock, Digital Data

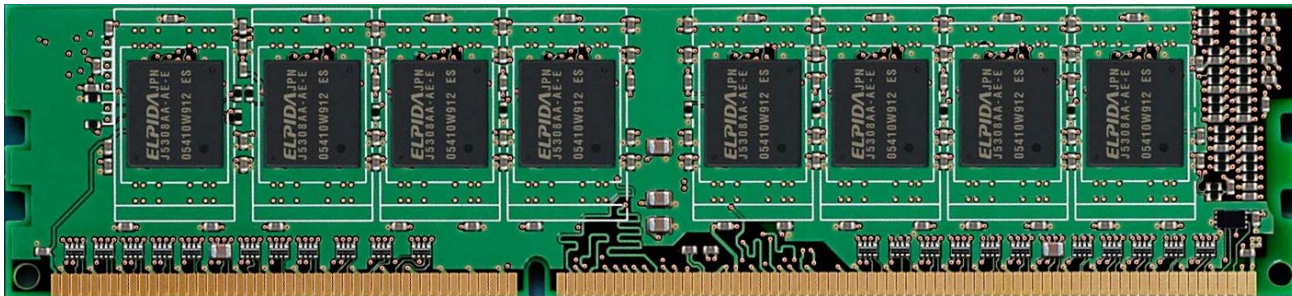


Digital Clock, Analog Data

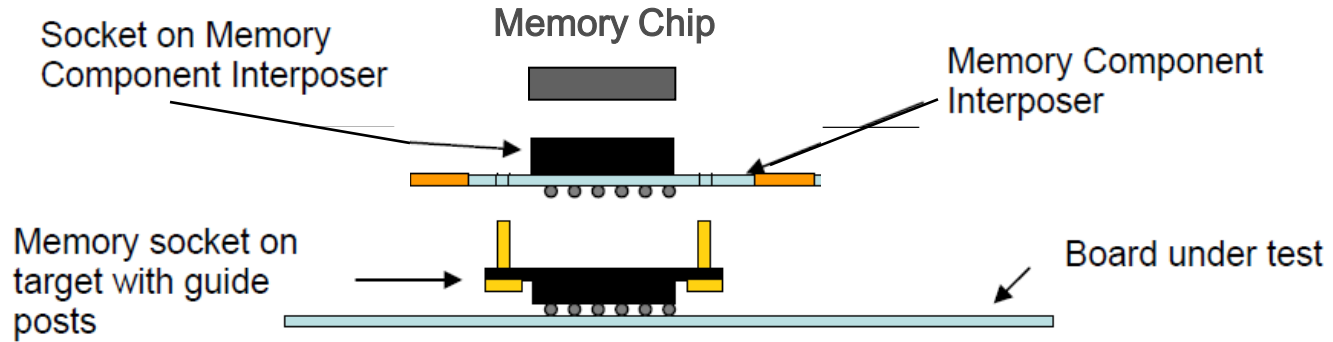


# Memory Technology – Quick Overview

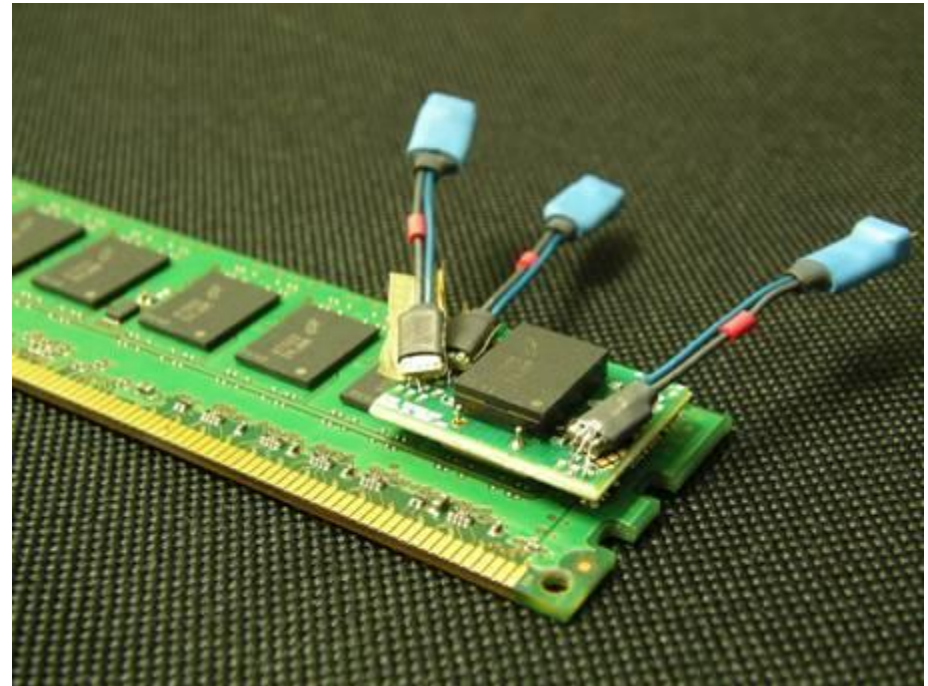
- DRAM - dominant memory technology
  - Computer system memory
    - Server, desktop, laptop
    - Dynamic, volatile memory, plug-in DIMMs
  - Embedded systems
    - Cell phones, printers, cars
    - Fixed memory configuration
  - DRAM driven by faster processors, faster data rates
    - DDR3 now available at 1600 (1.6Gb/s) data rates
    - DDR3 2000 emerging soon (overclocked)
- DRAM variants
  - LPDDR – Low Power DDR
    - Power savings for portable computing
  - GDDR – Graphic DDR
    - Optimized for Speed - faster access



# Installation Process



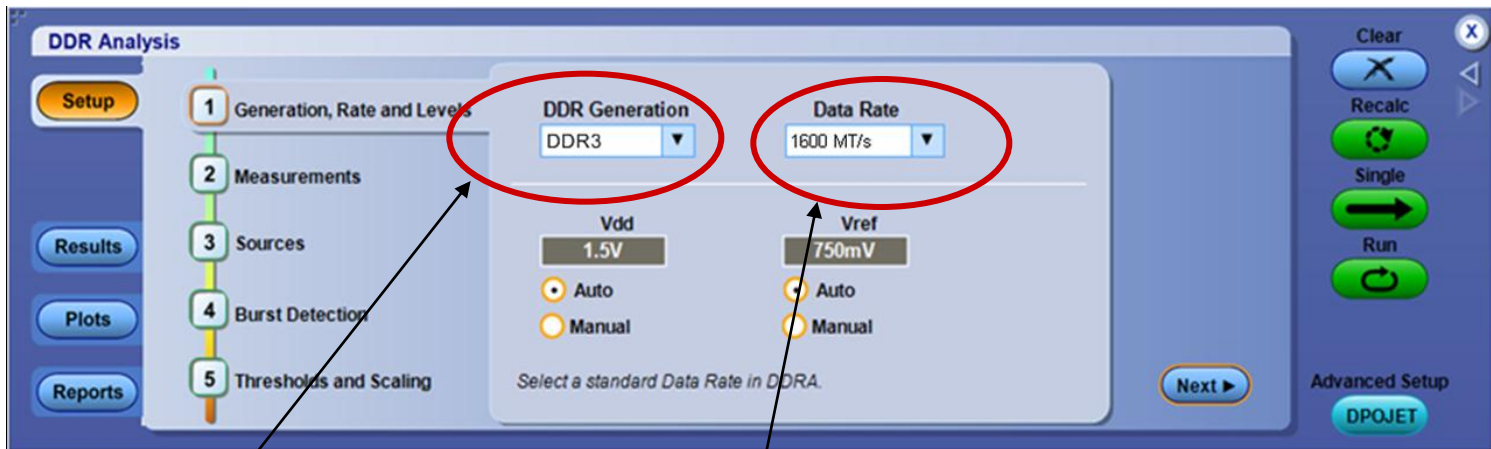
# BGA Chip Interposer for Oscilloscopes



- Available in socket and solder-in versions
  - Socket design allows for multiple chip exchanges
  - Solder-in best for single use
- Recommended probes: P7500 Series
  - P7504, P7506, P7508, P7513A
  - 020-3022-00 TriMode solder tips for Nexus Interposer

# Automated Test Setup

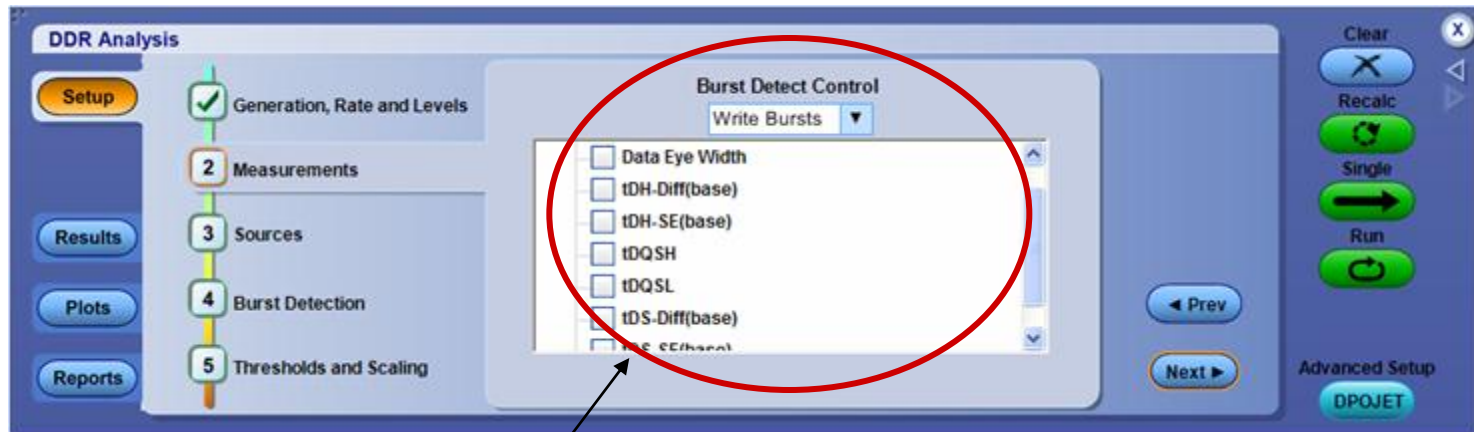
## Step #1



Select DDR Generation

Select DDR Rate

## Step #2



Choose measurements (Read / Write / CLK / Addr & Command)



# Effective Reporting / Archiving

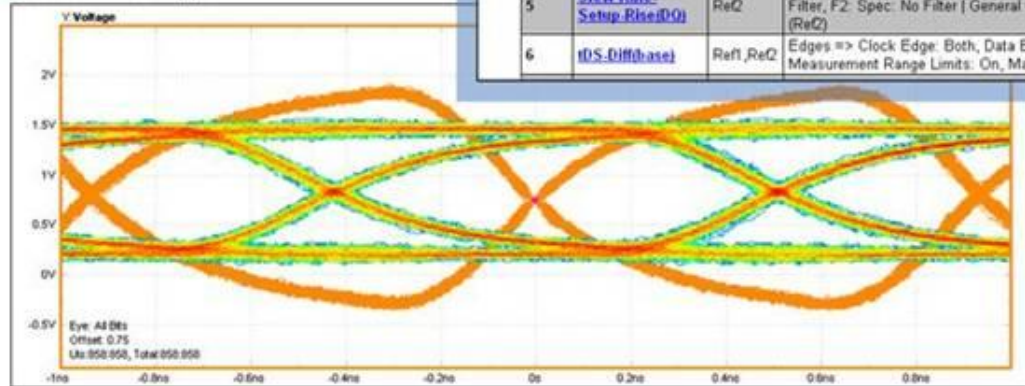
Measurement	tDOSH
Source1	DQS(Ref1)
	Value High Limit Low Limit Pass Fail
Min	928.86ps 1.8150ns 843.75ps Pass
Max	974.29ps 1.8150ns 843.75ps Pass


#### Pass/Fail Information

Measurement	tDOSL
Source1	DQS(Ref1)
	Value High Limit Low Limit Pass Fail
Min	900.00ps 1.8150ns 843.75ps Pass
Max	940.44ps 1.8150ns 843.75ps Pass

#### Plot Images

##### Measurement Plot(s)




  
Enabling Innovation

October 16, 2009 10:17:54 AM

### Jitter and Eye Diagram Analysis Tools : Measurement Report

- Configuration
  - Setup Configuration
    - Oscilloscope Version 4.3.6 Build 5
    - DPOJET Version 2.4.0 Build 41
    - Status Pass
- Measurement Configuration
 

Index	Measurement	Source(s)	Others
1	<a href="#">Data Eye Height</a>	ReQ,Ref1	Bit Config => Bit Type: All Bits   Clock Recovery => Method: Explicit Clock - Edge, Clock Source: Ref1, Clock Edge: Both, Clock Multiplier: 1, Clock Offset Selection Type: Manual, Clock Offset: 469.04ps; Recalculation Type: When required   General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Source Name: DQ(ReQ), DQS(Ref1)
2	<a href="#">Slew Rate Hold-Fall(DQ)</a>	ReQ	Edges => From Level: High, To Level: Mid, Slew Rate Technique: DDRSlewrateTechnique   Filters => F1: Spec: No Filter, F2: Spec: No Filter   General => Measurement Range Limits: Off, Max: 0s, Min: 0s, Custom Source Name: DQ(ReQ)
3	<a href="#">Slew Rate Hold-Rise(DQ)</a>	ReQ	Edges => From Level: Low, To Level: Mid, Slew Rate Technique: DDRSlewrateTechnique   Filters => F1: Spec: No Filter, F2: Spec: No Filter   General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Source Name: DQ(ReQ)
4	<a href="#">Slew Rate Setup-Fall(DQ)</a>	ReQ	Edges => From Level: Mid, To Level: Low, Slew Rate Technique: DDRSlewrateTechnique   Filters => F1: Spec: No Filter, F2: Spec: No Filter   General => Measurement Range Limits: Off, Max: 0s, Min: 0s, Custom Source Name: DQ(ReQ)
5	<a href="#">Slew Rate Setup-Rise(DQ)</a>	ReQ	Edges => From Level: Mid, To Level: High, Slew Rate Technique: DDRSlewrateTechnique   Filters => F1: Spec: No Filter, F2: Spec: No Filter   General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Source Name: DQ(ReQ)
6	<a href="#">tDS-Diff/base</a>	Ref1,ReQ	Edges => Clock Edge: Both, Data Edge: Both   Filters => F1: Spec: No Filter, F2: Spec: No Filter   General => Measurement Range Limits: On, Max: 938ps, Min: 0s, Custom Source Name: DQS(Ref1), DQ(ReQ)



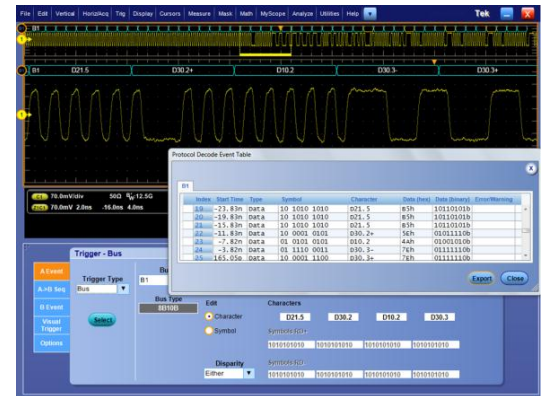
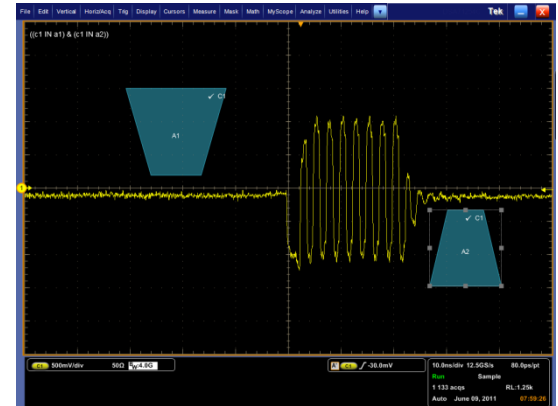
# Automatically isolate & mark all read or write bursts

- Easily Identify, mark & measure all Read / Write bursts
  - Scroll through marked reads / writes across the entire waveform record
  - Measurements performed on ALL reads/writes



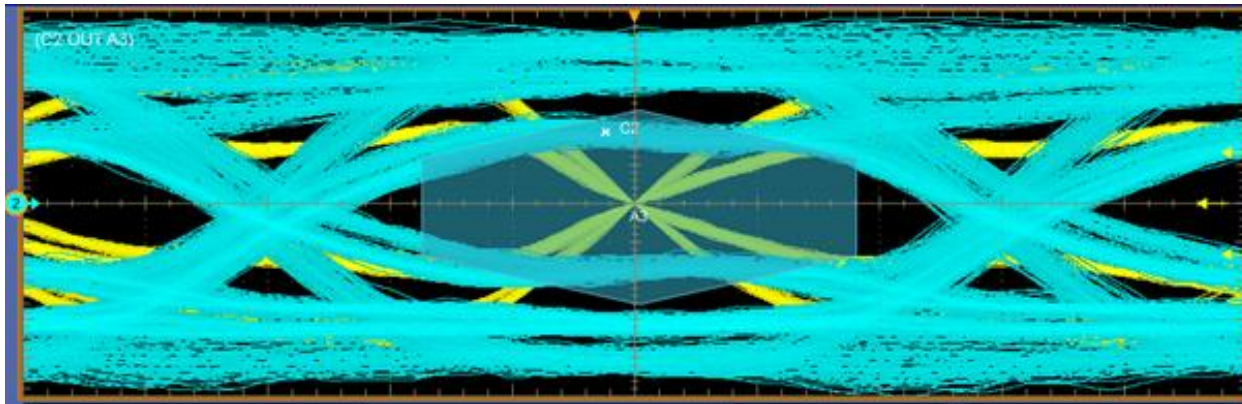
# Visual Trigger and Serial Decode

- Next generation designs have less margin and additional analysis must be done to pinpoint in on pattern dependent issues
  - **NEW!** Visual Trigger qualifies hard to define trigger events
    - 8 customizable shapes for capture of real signal behaviors
- Electrical and Logic layer are merging and requires simultaneous analog and protocol views
  - **NEW!** 8b/10b Serial Decode
    - Trigger or Search on decoded traffic
    - Compare to analog views to speed up time to answer



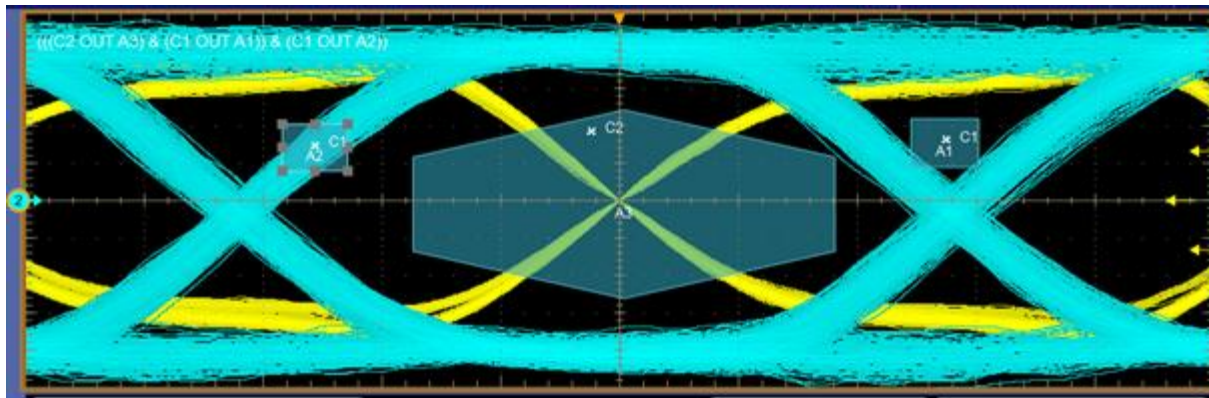
# Triggering Techniques for Debugging DRAM

- **Challenge: Dual-Rank System**
  - **Need to Isolate & Measure a Single Rank**
  - **Difficult to isolate data bursts from one rank only**



# Triggering Techniques for Debugging DRAM

- **‘Visual’ Trigger Used to Qualify One Rank**
  - Visual area (“keep-out” region) used to exclude low-amplitude signals
  - Eliminates lower-amplitude data bursts from rank 2



“After” gating with visual trigger

# High-Speed Serial Data Test Solutions...

Design

Verification

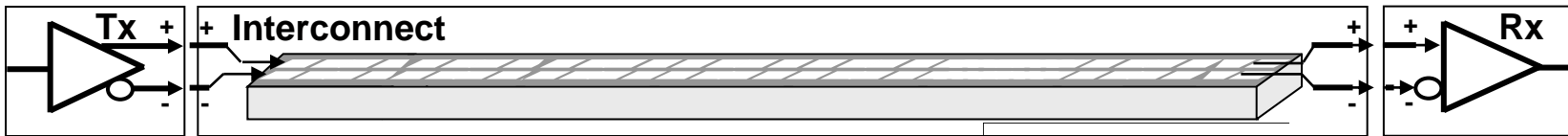
Compliance Test



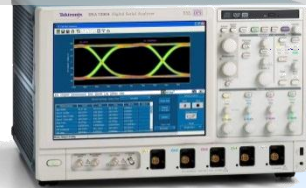
GbE DisplayPort

HDMI™

MHL ...



Real-time Scopes



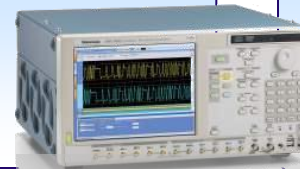
System Integration  
Digital Validation & Debug

Logic Analyzers



Transmitter Testing

Receiver Test  
Margin  
Testing



Arbitrary Waveform Generator

Probing  
Fixtures



Sampling Scopes

Interconnect Test

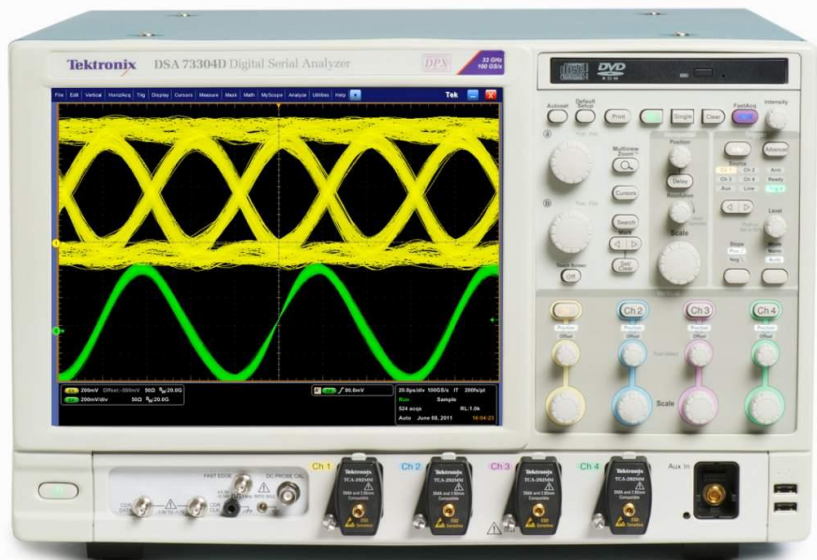
Compliance Test

Compliance Test Software





# DPO/DSA70000D 系列



1. 10 TS/s等效采样率
2. 输入灵敏度达到6.25mV/div
3. 低本底噪声和抖动
4. 大于300,000 wfms/sec 的最高波形捕获率

型号	带宽	采样率	存储深度 (最大)	上升时间
DPO/DSA73304D	33GHz(2Ch) 23GHz(4Ch)	100GS/s(2Ch) 50GS/s (4Ch)	250Mb	9ps
DPO/DSA73254D	25GHz(2Ch) 23GHz(4Ch)	100GS/s(2Ch) 50GS/s (4Ch)	250Mb	12ps

# DPO/DSA70000C 系列



型号	带宽	采样率	存储深度(标配)	上升时间
DPO/DSA72004C	20GHz(2Ch) 20GHz(4Ch)	100GS/s(2Ch) 50GS/s (4Ch)	10Mb/31.25Mb	14ps
DPO/DSA71604C	16GHz(2Ch) 16GHz(4Ch)	100GS/s(2Ch) 50GS/s (4Ch)	10Mb/31.25Mb	17ps
DPO/DSA71254C	12.5GHz(2Ch) 12.5GHz(4Ch)	100GS/s(2Ch) 50GS/s (4Ch)	10Mb/31.25Mb	22ps
DPO/DSA70804C	8GHz(2Ch) 8GHz(4Ch)	25GS/s(2Ch) 25GS/s (4Ch)	10Mb/31.25Mb	34ps
DPO/DSA70604C	6GHz(2Ch) 6GHz(4Ch)	25GS/s(2Ch) 25GS/s (4Ch)	10Mb/31.25Mb	45ps
DPO/DSA70404C	4GHz(2Ch) 4GHz(4Ch)\	25GS/s(2Ch) 25GS/s (4Ch)	10Mb/31.25Mb	68ps

# MSO70000C 高性能混合信号示波器

业内领先的配有高性能数字通道的实时示波器

高性能

▪ **20G带宽模拟通道**  
4个通道

▪ **80ps** 数字定时分辨率  
▪ **20 ps** 模拟定时分辨率

▪ **16 数字通道**  
连同4个模拟通道  
组成的采集系统

▪ **深存储**  
▪ 对于模拟和数字通道全部为**250M/ch**

▪ **事件触发能力**  
隔离定位偶发的故障

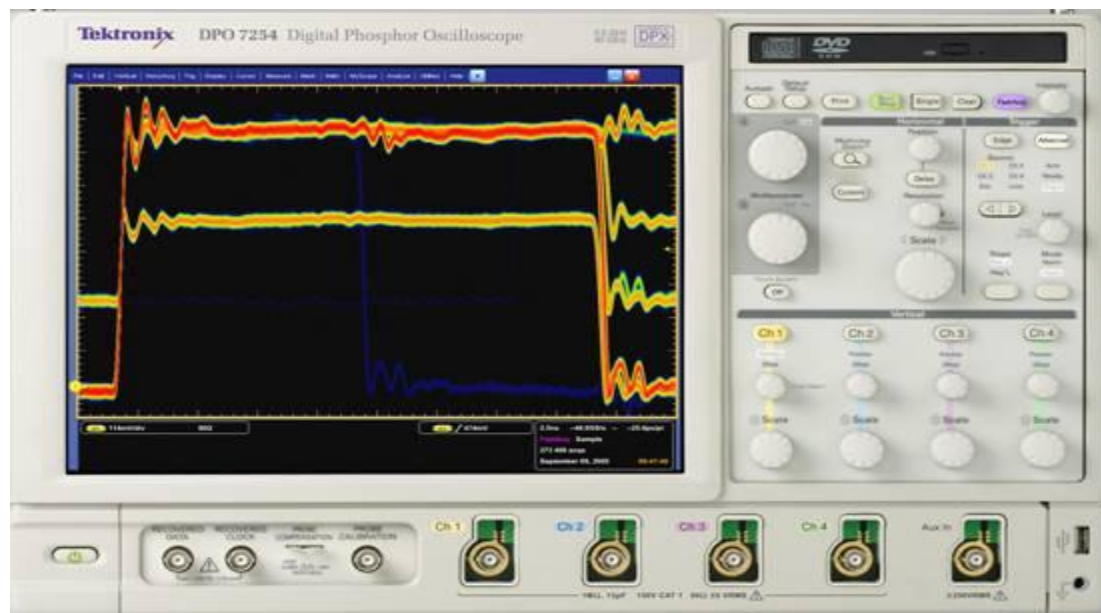
**iCapture™** 同时进行模拟数字时间相关调试

▪ **新数字逻辑探头**  
提供高信号保证度  
以及最小的负载

集成了并行总线、  
**I2C、SPI**解码功能



# DPO7000 系列



型号	带宽	采样率	存储深度(标配)	波形捕获率
DPO7054C	500MHz	10GS/s(1Ch) 5GS/s (2Ch) 2.5GS/s (2Ch)	10Mb/20Mb/40Mb	>250,000
DPO7104C	1GHz	20GS/s(1Ch) 10GS/s (2Ch) 5GS/s (2Ch)	10Mb/20Mb/40Mb	>250,000
DPO7254C	2.5GHz	40GS/s(1Ch) 20GS/s (2Ch) 10GS/s (2Ch)	10Mb/20Mb/40Mb	>250,000
DPO7354C	3.5GHz	40GS/s(1Ch) 20GS/s (2Ch) 10GS/s (2Ch)	10Mb/20Mb/40Mb	>250,000

# MSO/DPO5000系列示波器

	MSO5204 DPO5204	MSO5104 DPO5104	MSO5054 DPO5054	MSO5034 DPO5034
带宽	2 GHz	1 GHz	500 MHz	350 MHz
模拟通道	4			
数字通道 <sup>1</sup>	16 (仅 MSO 型号) <sup>1</sup> , 带有新 P6616 16 通道数字探头			
模拟采样率	10 GS/s (1 或 2 通道); 5 GS/s (全部通道)		5 GS/s (全部通道)	
数字采样率	500 MS/s 数字 Main, 16.5 GS/s 数字 MagniVu™			
模拟记录长度 (最大/全部通道)	标配: 25M/12.5M 可选: 50M/25M、125M/50M、250M/125M 带 Wave Inspector 导航		标配: 12.5M 可选: 25M、50M、125M 带 Wave Inspector 导航	
数字记录长度	标配: 12.5M; 可选最大 40M			
波形捕获率	> 250,000 个波形/秒			
分段存储器	FastFrame™			
串行触发和解码	可选: I <sup>2</sup> C, SPI, RS-232/422/485/UART, USB, CAN/LIN <sup>2</sup>			
分析	标配: 高等数学、FFT、53 项自动测量、波形柱状图、OpenChoice™、NI SignalExpress™ 可选: 功率、抖动/眼图、以太网和 USB 2.0 一致性、极限和模板测试、DDR <sup>3</sup>			
标配模拟探头	(4) TPP1000 – 1 GHz、3.9pf、10X 无源探头 (1 和 2 GHz 型号) (4) TPP0500 – 500 MHz、3.9pf、10X 无源探头 (350 和 500 MHz 型号)			
计算平台	Intel Core2 Duo 处理器带 4GB RAM, 运行 Windows 7 64 位操作系统			
标配 I/O	(6) USB 主机、USB 设备、LAN (LXI Class-C)、视频输出、参考时钟输入、辅助 (Aux) 输出、音频、可移除硬盘驱动器			
显示屏	10.4 英寸 XGA 触摸屏			

注 1: DPO 型号可现场升级到 MSO 功能

注 2: 通过 VNA 软件支持 CAN/LIN

注 3: 1 GHz 和 2 GHz 型号可获得 DDRA



# MDO4000系列混合域示波器(数字,模拟,射频一体化)



- 多达21条通道  
支持复杂调试
- 内置频谱分析仪
- 时间相关的模拟、数字与RF

型号	模拟通道	模拟带宽	数字通道	RF通道	RF频率范围
MDO4054-3	4	500 MHz	16	1	50 kHz – 3 GHz
MDO4054-6	4	500 MHz	16	1	50 kHz – 6 GHz
MDO4104-3	4	1 GHz	16	1	50 kHz – 3 GHz
MDO4104-6	4	1 GHz	16	1	50 kHz – 6 GHz

# DSA8300 采样示波器

- 光信号测试
- 电信号测试
- 阻抗测试
- S参数测试

DSA8300 / Option	Description
DSA8300	Digital Signal Analyzer mainframe
Opt. ADTRIG	Add Advanced Trigger (required for JNB or JNB01)
Opt. JNB	Add 80SJNB Essentials
Opt. JNB01	Add 80SJNB Advanced
Opt. JARB	Add 80SJARB (included in JNB & JNB01)
Opt. ICMX	Add IConnect with Measurement Extractor
Opt. ICON	Add IConnect Signal Integrity Software
Opt. SPAR	Add IConnect S-parameter and Z-line



# DSA8300采样示波器-光信号测试模块



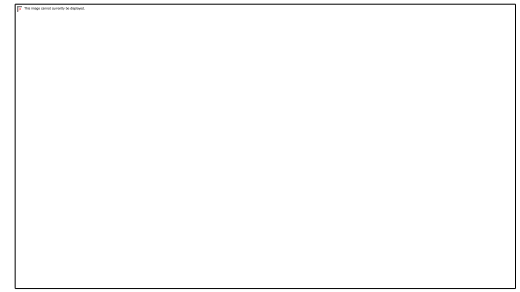
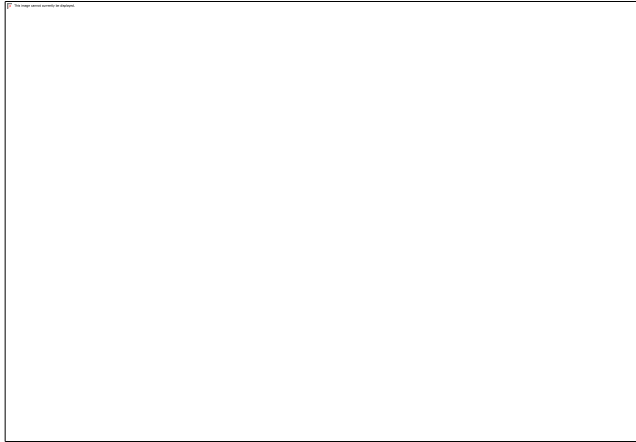
## Multi-mode, Broad Wavelength (750 - 1650 nm) Modules

80C07B	Supports rates to 2.7 Gb/s, high sensitivity, optional integrated clock recovery
80C08C	Supports all of the 8/10 Gb/s applications, high sensitivity, optional integrated clock recovery, optional Integrated CR
80C12B <b>New</b>	Supports rates from 155 Mb/s – 11.3 Gb/s, high sensitivity - data pick-off for external CRU e.g. CR125A
80C14 <b>New</b>	Supports rates from 8.5 Gb/s – 14.063 Gb/s, high sensitivity – data pick-off for external CRU e.g. CR175A

## Single-mode, Long Wavelength (1100 - 1650nm) Modules

80C11	Optical bandwidth to 30GHz, supports 10Gbit/s up to 14G+ standards, optional Integrated CR
80C25GBE	Focused product that supports (4 x 25 Gb/s) emerging 100 Gb/s Ethernet standards
80C10B	Optical bandwidth to 80GHz, supports all 40 and 100 Gb/s (4 x 25 Gb/s) standards, optional CR trigger pickoff for e.g. CR286A CRU

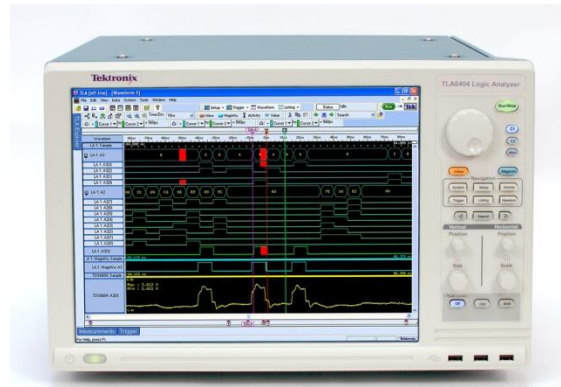
# DSA8300采样示波器-电信号测试模块



Electrical Modules	Channels	Vertical Resolution	Bandwidth	Risetime (10%-90%)	Monolithic or Remote
80E02	1	16 bits	50 GHz	7 ps	Monolithic
80E03	2	16 bits	20 GHz	17.5 ps	Monolithic
80E06	1	16 bits	70+ GHz	5 ps	Monolithic
80E07	2	16 bits	30 GHz	11.7 ps	Remote (2 meter)
80E09	2	16 bits	60 GHz	5.8 ps	Remote (2 meter)

Electrical and TDR Acquisition Modules

# 逻辑分析仪系列TLA6400



## ■ TLA6400 Series LA

*Replaces TLA5000 & TLA6200 products*

- TLA6401 34 ch
- TLA6402 68 ch
- TLA6403 102 ch
- TLA6404 136 ch

## ■ P5900 Series Probes

- P5910 17 ch GP
- P5934 34 ch Mictor
- P5960 34 ch DMAX



# 逻辑分析仪系列TLA6400

Models	Channels (per module)	State Clock Rate	Record Length (Full CH)	Timing	MagniVu™ Timing
TLA6401	32	333 MHz (std) 667 MHz (opt)	2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb	1.6 GS/s (all ch) 3.2 GS/s (1/2 ch)	40 ps (25 GS/s) 128 Kb
TLA6402	68	333 MHz (std) 667 MHz (opt)	2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb	1.6 GS/s (all ch) 3.2 GS/s (1/2 ch)	40 ps (25 GS/s) 128 Kb
TLA6403	102	333 MHz (std) 667 MHz (opt)	2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb	1.6 GS/s (all ch) 3.2 GS/s (1/2 ch)	40 ps (25 GS/s) 128 Kb
TLA6404	136	333 MHz (std) 667 MHz (opt)	2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb	1.6 GS/s (all ch) 3.2 GS/s (1/2 ch)	40 ps (25 GS/s) 128 Kb
TLA6404GSA	136	333 MHz (std) 667 MHz (opt)	2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb	1.6 GS/s (all ch) 3.2 GS/s (1/2 ch)	40 ps (25 GS/s) 128 Kb

# 逻辑分析仪TLA7000系列

- TLA7012 Portable Mainframe  
支持2模块的主机(272通道)
- TLA7016 Benchtop Mainframe  
支持6模块的主机(支持136X6=816通道)



# TPI4000 系列协议分析仪

## TPI4202

- Portable
- Two Card Slots
- Built-in screen and keyboard



## TPI4208

- 4U Rackmount
- 2 Card Slots



# TPI4000 系列

## 一台仪器可以支持多种协议

- Fibre Channel
  - FICON, AS1760, ASM, FC-AE-1553, others
- Ethernet
  - iSCSI, FCoE, TCP/IP, IPv6, iFCP, AFDX, ARINC664, TTE, others
- Serial Front Panel Data Port (Serial FPDP)
- Serial Attached SCSI (SAS)
- Serial ATA (SATA)
- Common Public Radio Interface (CPRI)
- Serial RapidIO (SRIO)

# BSA误码仪系列



误码仪主机  
BSA260C  
BSA175C  
BSA125C  
BSA850V



时钟恢复模块  
CR286A  
CR125A



- 预加重模块
- DPP125



**BA1500/1600**  
• **Basic BERT & Scope**

- 26G
- 17.5G
- 12.5G
- 8.5G

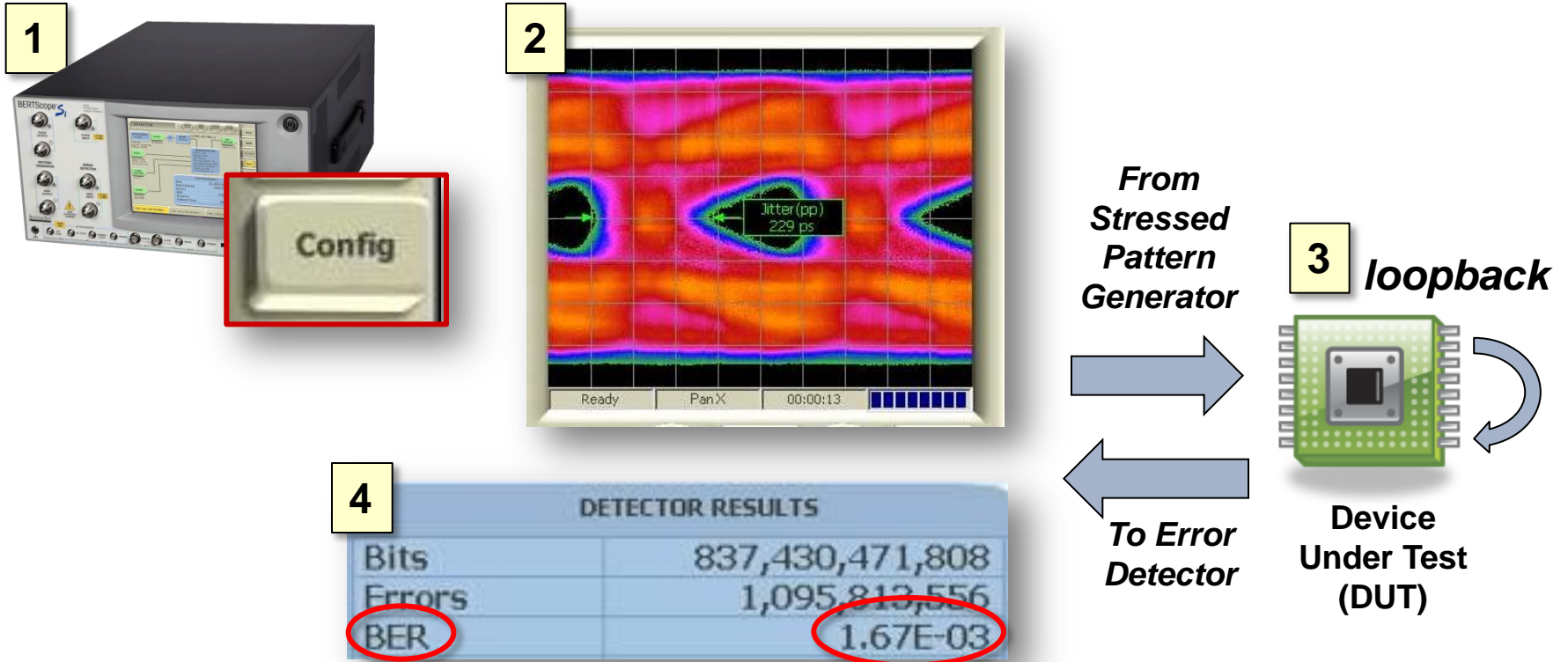
- 28.6G
- 17.5G
- 12.5G

- 12.5G

- 1.5G/1.6G



# 接收端抖动容限测试



# 任意波形发生器 AWG5000C/7000C系列

## AWG5000C

- ▶ 600MS/s and 1.2 GS/s models
- ▶ 2 and 4 channels
- ▶ 14 bit vertical resolution
- ▶ 4 or 8 markers
- ▶ Sequencing, Sub-sequencing & Dynamic Jump capability
- ▶ 28 bit digital output option on 2 channel models



## AWG7000C

- ▶ 8 GS/s and 12 GS/s
- ▶ 1 and 2 channels
- ▶ Optional 16 & 24 GS/s interleaving on the 2 channel 8 & 12 GS/s models
- ▶ 10/8 bit vertical resolution
- ▶ 2 or 4 markers
- ▶ Sequencing, Sub-sequencing & Dynamic Jump capability

