Validating and Debugging DDR2, DDR3 SDRAM Designs
- Comprehensive Test solution from Analog to Digital Validation for All DDR Versions

name
title
Memory Design and Validation

### Chip/Component Design
- Precise understanding of circuit behavior under range of conditions
- Margin testing

### System Integration
- Signal integrity and timing analysis, discovery of issues under nominal conditions
- Debug interoperability issues

### Embedded Systems
- Easy test setup
- Quick pass/fail results
DDR Test Challenges

- Signal Access & Probing
  - Easy-to-use / reliable connections
  - Bandwidth & Signal Integrity
  - Affordable

- Isolation of Read/Write bursts
  - Triggering or Post-Processing

- Complexity of JEDEC Conformance Tests
  - Parametric timing/amplitude measurements
  - Vref / Vih / Vil, Derating

- Results Validity / Statistics

- Effective Reporting / Archiving

- Advanced Analysis
  - Characterization
  - Debug
Fast & Accurate instrument solutions

DDR, DDR2 & DDR3 SDRAM Solutions

Signal Path Characterization and Circuit Board Verification
DSA Sampling Oscilloscopes
Verify correct design and circuit board performance

Analog & Electrical Debug
DPO/DSA real time scopes & software
Signal integrity measurements

Digital Validation & Debug
TLA Logic Analyzers with Nexus & FuturePlus
Technology memory supports
Verify and debug command sequence, timing, data, and more

SDRAM Probing Solutions
Easy and reliable physical connection with minimal loading
Tektronix DDR Test Solutions

Path Characterization & Circuit Board Verification

**DDR**
- 266MHz
- 333MHz
- 400MHz

**DSA8200 sampling oscilloscope**

**Analog Validation & Debug**

**DSA70000 Probing and measurement Software**

**Digital Validation & Debug**

**TLA7000, Memory support and probing solutions**

**DDR2**
- 400MHz
- 533MHz
- 667MHz
- 800MHz
- 1066MHz

**DSA8200 sampling oscilloscope**

**TLA7000, Memory support and probing solutions**

**DDR3**
- 800MHz
- 1066MHz
- 1333MHz
- 1600MHz
- 1867MHz

**DSA8200 sampling oscilloscope**

**TLA7000, Memory support and probing solutions**
Problem: verify correct design and performance

Path Characterization & Circuit Board Verification

Characterize board/DIMM with TDR and S-Parameters
Frequency-domain characterization of reflections and loss in a network

Quantitative insight into the causes of signal integrity problems

Measurements:
- Impedance measurements
- Insertion & Return Loss
- Frequency domain crosstalk
Verify correct design and circuit performance

Path Characterization & Circuit Board Verification

**DSA8200 Sampling Oscilloscope with TDR and S-parameter generation software**

**Performance**
- Over 70GHz sampling bandwidth & lowest Jitter floor
- Improved impedance measurement accuracy and resolution (Z-Line)
- 1M record length enables measurements of long interconnects at higher frequency

**Efficiency & Simplicity**
- Emulate channel effect on jitter & noise using TDR/TDT or S-parameter description
- Automated procedures minimize errors & reduce test time
- Complete analysis tasks in minutes not hours
Tektronix DDR Test Solutions

Path Characterization & Circuit Board Verification

**DDR**
- 266MHz
- 333MHz
- 400MHz

**DSA8200 sampling oscilloscope**

**DDM**
- 400MHz
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- 800MHz
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Analog Validation & Debug

**DSA70000 Probing and measurement Software**

Digital Validation & Debug

**TLA7000, Memory support and probing solutions**

Path Characterization & Circuit Board Verification

**Analog Validation & Debug**

**Digital Validation & Debug**
DDR Analog Validation & Debug – Tektronix Solutions

Signal Access - Probing
- Requires easy but reliable physical connectivity
  - access to various measurement points on DRAM or Memory
- Requires maximum signal integrity
  - sufficient performance for signal speeds

Signal Acquisition
- Automatically trigger and capture DDR signals
  - Identify and trigger directly on DQ, DQS in real-time to isolate Reads/Writes
  - Automatically set voltage levels and data rates
- Capture long time duration at high resolution
  - Direct connection to DPOJET for signal analysis

Signal Analysis
- DDRA – Automated setup, read/write burst detection, JEDEC pass/fail meas.
- DPOJET – The most powerful Jitter, Eye and Timing analysis tool
  - Time, Amplitude, Histogram, measurements
  - Advanced Jitter, Eye diagram measurements and Pass/Fail testing
  - Many display and plotting options
  - Report generator
Leading Connectivity

Signal Access Complexity

- Higher Data Rates Drive Probe Connection Complexity
  - Higher data rate = less margin
  - Higher signal fidelity requirements
  - Component geometries shrinking
  - Fine pitch pin spacing of <20 mils
  - Fewer & nearly inaccessible test points

- Key Applications: Validation, Debug & Troubleshooting
  - Semi-permanent & reliable fine pitch solder down connections for repeatable system validation
  - Mobile probing without compromise for debug & troubleshooting requirements
  - Low cost leave-behind solder points for less critical measurements
Signal Access

- Computer Systems use standardized DIMM’s for which several probing solutions are available
- Memory in Embedded Designs is usually directly mounted on the PCB
- All DDR2 & DDR3 Components use BGA Packages
- Probing a BGA package is Difficult
  - Unable to probe at the Balls of the Device

Signal Access Solutions
- Component Interposers
- Direct Probing
- Analog Probing
  - DQ, DQS, Clock
- Digital Probing
  - Address
  - Command
  - Power, Reset, and Reference
Analog Solder-In Probing Solutions

P7500 Series Tri-Mode Probes

Socket Cable 020-2954-xx

TriMode Micro-Coax Tip 4GHz

P75TLRST Solder Tip up to 20GHz
BGA Chip Access For DDR2, DDR3

- Unique, reusable socket design allows for multiple chip exchanges
- Nexus DDR Interposers sold by Tektronix
  - DDR2 and DDR3 versions
  - X4/x8, x16 pins
  - Socket and solder models
Leading Connectivity

Soldering Probe Tips – Example

- A – Tip with long wires
- B – Wires cut short
- C – Back side of tip
- D – Tip covered with anti-static tape

- E – Solder placed on signal vias
- F – Tip soldered to vias and secured with tape
Leading Connectivity

Soldering Probe Tips – Example (cont’d)

- A - Tip wires in via and ready for soldering

- B - Tip soldered to board

- All tips soldered to DDR Component Interposer
  - 5 signals of interest
  - A4, CK0, DQ0, DQS0, and CS2
  - Minimized wire length for best signal fidelity
Mixed Analog and Digital Validation

- **P6780 Active Differential Logic Probe**
  - 16 channel + 1 Clock Qualifier (CQ)
  - 2.5 GHz bandwidth with low loading (<0.5pf)
  - Small form factor for high density circuit access

- **P6717 Single-Ended Logic Probe**
  - 16 channel + 1 CQ
  - > 350 MHz bandwidth
  - General purpose mixed signal applications

- **iCapture on MSO70000**
  - Route digital signal through analog system
  - Removes need for double-probing
iCapture™ - One Connection for Analog and Digital

- **Industry’s only** single probe connection for analog and digital
  - Measurement flexibility while preserving signal access
  - No need to reconfigure probing

- Quickly route any digital channel to any analog channel – *Simultaneously*
  - See both digital and analog views of the same signal
  - Validate signal connection, logic threshold
  - Check signal integrity, improve timing resolution
Read/Write Burst Identification

- Locate the right kind of bursts (read vs write)
- Locate the precise edges of each burst
- Refine burst identity based on other criteria (rank, secondary bus state, etc)
## Symbol Files for Bus Decoding

### Basic Command Bus
(CS, RAS, CAS, WE)

<table>
<thead>
<tr>
<th>Command</th>
<th>Command Name</th>
<th>Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODE_REG</td>
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<td>0000</td>
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<tr>
<td>REFRESH</td>
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<td>PRECHARGE</td>
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### JEDEC Command Truth Table
(CKE, CS, RAS, CAS, WE, MRS, BA0/1, Address)

<table>
<thead>
<tr>
<th>Command</th>
<th>CKE#</th>
<th>CS#</th>
<th>RAS#</th>
<th>CAS#</th>
<th>WE#</th>
<th>BA0</th>
<th>BA1</th>
<th>BA3</th>
<th>A12/BC#</th>
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</tbody>
</table>
Burst Identification using Command Bus

- Using bus state, specific transactions can be isolated
  - For example, locate only Reads from a specific memory rank
  - Advanced Search & Mark is used for fine burst positioning
Measurement Setup

- JEDEC Standards specify measurements & methods
Automated Test Setup

Step #1

Select DDR Generation

Select DDR Rate

Step #2

Choose measurements (Read / Write / Clock)
Source and Level Selection

Step #3

Identify scope input channels for DQS, DQ, CLK

Optional Chip Select qualifier

Step #4

Let DDRA set Read/Write Burst Detect Levels automatically, or customize if needed
Threshold and Auto Scaling

Step #5

Let DDRA set Measurement Ref Levels automatically (per JEDEC), or customize if needed.
Comprehensive Measurement Support

Option DDRA supports a broad range of JEDEC-specified measurements for DDR, DDR2, DDR3, LPDDR, LPDDR2

- Example measurements list for DDR2:
  - tCK(avg)
  - tCK(abs)
  - tCH(avg)
  - tCH(abs)
  - tCL(avg)
  - tCL(abs)
  - tHP
  - tJIT(duty)
  - tJIT(per)
  - tJIT(cc)
  - tERR(02)
  - tERR(03)
  - tERR(04)
  - tERR(05)
  - tERR( 6 - 10 per)
  - tERR(11 - 50 per)
  - tDQSH
  - tDS - diff (base)
  - tDS - SE (base)
  - tDS -diff - DERATED
  - tDS -SE - DERATED
  - tDH - diff (base)
  - tDH - SE (base)
  - tDH -diff - DERATED
  - tDH -SE - DERATED
  - tDIPW
  - tAC - diff
  - tDQSCCK -diff
  - tDQSCCK - SE
  - tDQSQ - diff
  - tDQSQ - SE
  - tQH
  - tDQSS
  - tDSS
  - tDSH
  - tIPW
  - tIS (base)
  - tIH (base)
  - tIS - DERATED
  - tIH - DERATED
  - Vid - diff (AC)
  - Vix (AC) - DQS
  - Vix (AC) - CLK
  - Vox (AC) - DQS
  - Vox (AC) - CLK
  - Input Slew-Rise (DQS),
  - Input Slew-Fall (DQS),
  - Input Slew-Rise (CLK),
  - Input Slew-Fall (CLK),
  - AC - Overshoot Amplitude - diff
  - AC -Undershoot Amplitude - diff
  - AC - Overshoot Amplitude - SE
  - AC - Undershoot Amplitude - SE
  - Data Eye Width
Measurement De-rating

- JEDEC stipulates de-rating of DDR2 and DDR3 pass / fail limits for Setup & Hold measurements based on signal slew rate*
- Option DDRA automatically calculates slew rates and applies the appropriate de-rating values to the measurement limits.

- \( t_{DS} \) - diff (base)
- \( t_{DS} \) - diff - DERATED
- \( t_{DS} \) - SE (base)
- \( t_{DS} \) - SE - DERATED
- \( t_{DH} \) - diff (base)
- \( t_{DH} \) - diff - DERATED
- \( t_{DH} \) - SE (base)
- \( t_{DH} \) - SE - DERATED
- \( t_{IS} \) (base)
- \( t_{IS} \) - DERATED
- \( t_{IH} \) (base)
- \( t_{IH} \) - DERATED

* JESD79-2E, JESD79-3C specifications
Results and Statistical Validity

- To have confidence in your test results, you need 100’s, 1000’s or even more observations of each measurement.
- As a practical matter, measurement throughput is essential.
Beyond DDRA: Other Tektronix Scope DDR Debug Tools

- Fastest way to solve sophisticated Memory signaling issues
  - Superior real-time insight into the complex DDR2/DDR3 signaling
    - DPX (FastAcq) and Pinpoint Triggering gives you “the power to see what others can’t”
    - FastAcq shows any disparities on strobe/data – like infrequent glitch on Write data. You can choose to display consecutive eyes on the data only (w/o showing the strobe information)
Tektronix DDR Test Solutions

Path Character. & Circuit Board Verification

- DDR
  - 266MHz
  - 333MHz
  - 400MHz
  - DSA8200 sampling oscilloscope

- DDR2
  - 400MHz
  - 533MHz
  - 667MHz
  - 800MHz
  - 1066MHz
  - DSA8200 sampling oscilloscope

- DDR3
  - 800MHz
  - 1066MHz
  - 1333MHz
  - 1600MHz
  - 1867MHz
  - DSA8200 sampling oscilloscope

Analog Validation & Debug

- DSA70000 Probing and measurement Software

Digital Validation & Debug

- TLA7000, Memory support and probing solutions

DDR
- 266MHz 333MHz 400MHz
DDR2
- 400MHz 533MHz 667MHz 800MHz 1066MHz
DDR3
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Path Character. & Circuit Board Verification

Analog Validation & Debug

Digital Validation & Debug

Tektronix Innovation Forum 2010
Digital Design and Validation

- Additional Visibility Needed
  - Data flow in and out of memory
  - Timing across many channels - all strobes and clock.
  - Data flow to/from a processor and memory

- Identify bus/system level issues
  - Protocols Sequences & Timing
  - Memory system power up initialization protocols & timing
  - DRAM Mode register settings
  - Refresh operations
  - Time Correlation with other system buses
  - Time Correlation with Oscilloscope waveforms
Performance
- Sufficient performance for all DDR signal speeds
- Preservation of frequency components
- Preservation of timing
- Minimizes effects of reflections
- Lowest probe loading in industry <0.5pF

Connectivity
Wide Range of probes for all DDR2/3 speeds – up to DDR3-1867
- NEXVu instrument DIMMs – only for Tektronix Logic Analyzers
  - Enhanced JEDEC layout DIMMs to include logic analyzer probing very close to the SDRAM
- DIMM Interposers
- BGA Memory Component Interposers that use Innovative Socket Design
- Direct probing to circuit board
Write Data Strobes Skew Analysis
Logic Analyzer MagniVu 20 ps (50 GS/s) timing resolution
Digital Validation & Debug

Data Acquisition

• Acquisition
  – 1.4 Gb/s data, 1.4GHz clock, 64Mb, Full Channel
  – 2.8 Gb/s data, 1.4GHz clock, 128Mb, Half Channel
  – Simultaneous timing & state acquisition
    • MagniVu 20ps (50GHz) timing resolution @ 128K record length

• Triggering
  – 16 state IF-THEN-ELSE trigger state machine
  – 24 word recognizers

• Module
  – 136 channel module
  – Merge with other modules
  – Uses P68xx and P69xx probes
  – Uses TLA7016 and TLA7012 mainframes

The only Logic Analyzer module fast enough to address all DDR3 speeds
DDR3 Enhanced Analysis Tools

DDR3 Sample Point Analysis Tool
- Helps to easily and quickly setup the Logic Analyzer for Acquiring the DDR data
- Optimally Adjusts the Threshold on the DQS and DQ Channels
- Determines the best sample point for each data group

DDR3 Protocol Violation Tool
- Quickly Identifies Protocol Violations
- Gives Global view of the DDR Bus Activity across the Entire LA Memory
- Navigates the user to the protocol errors in the listing or waveform window
DDR3 Sample Point Finder (SPF) Software

Select module that is connected to the interposer.

Auto runs the analyzer to acquire the desired number of read and write transactions.

Identify Support Package:
- Apply single threshold as starting point.
- Personality file for different DDR3 Raw cards, pinouts or unique system requirements.
- See results of multi-threshold old run.

Setup for min, max threshold along with increments.

Number of commands analyzed.

Select the Read or Write data.

Cancel test at any time.

Single button to apply all sample points and set all thresholds.

Blue area is data transitions.

White area is stable data.

Sample Point, Red is suggested and Green is current.

Personality file for different DDR3 Raw cards, pinouts or unique system requirements.
Digital Validation & Debug
Data Analysis

TLA7000 Series & Nexus & FuturePlus Memory support:

- Extensive Analysis capability enabled by exceptional timing resolution (MagniVu)
  - SDRAM initialization, commands, sequence and timing analysis
  - Read and Write Data analysis
  - Complete system visibility, directly transfer signals to an oscilloscope \textit{without the need of double probing}

Nexus & FuturePlus Memory support

- Protocol analysis features automates the analysis of DDR2 and DDR3 to quickly and easily identify protocol violations
- Provision of easy to read DDR symbols
- Decode of DDR/2/3 SDRAM command signals into mnemonics.

\textit{Tektronix + Nexus & FuturePlus = the world’s leading DDR3 test solution}
**Digital Validation & Debug**

### Data Access - Probing
- Requires reliable physical connectivity with minimal loading
  - Interposers
  - Instrument DIMMs
  - Direct probing to circuit board
- Requires maximum signal integrity

### Data Acquisition
- **NEW** DDR probing solution
- **NEW** DDR3 Logic Analyzer module
- The only Logic Analyzer fast enough to capture all DDR3 speeds
- Timing resolution high enough for thorough debugging
- Trigger state machine flexible enough to trigger only on relevant events
- Channel count scalable and high enough to capture all required signals
- Scalable and time correlated system for cross bus analysis

### Data Analysis
- **NEW** Memory support packages
- Verify and debug memory system operation
  - Data valid windows
  - Read/Write data operation
  - DDR commands and mode register initialization
- Quickly and easily identify protocol violations
**Fast & Accurate instrument solutions**

**DDR, DDR2 & DDR3 SDRAM Solutions**

**Signal Path Characterization and Circuit Board Verification**

**DSA Sampling Oscilloscopes**
Over 70GHz of sampling bandwidth & the lowest Jitter floor

Emulate the channel effect on jitter & noise using channels’ TDR/TDT or Touchstone® (S-parameter) description

TDR impedance measurements & S-parameter characterization of the PCB traces

**Analog & Electrical Debug**

DPO/DSA real time scopes & software

Pinpoint triggering on DDR reads & writes

Automatic detection of voltage levels & data rates

Automated clock jitter measurements based on JEDEC specification

SDRAM eye diagram measurements for read or write cycles

**Digital Validation & Debug**

TLA Logic Analyzers with Nexus & FuturePlus Technology memory supports

Only solution available to capture and analyze all DDR3 speeds

Up to 20 ps timing resolution on all channels, all the time

Selective clocking only stores useful data

Complete system visibility with digital/analog correlation

**SDRAM Probing Solutions**

Active differential oscilloscope probes

Slot interposers

Midbus probes

Instrumented DIMMs

Oscilloscopes can either use direct probing or probing via the logic analyzer with logic analyzer probes

*The world’s leading DDR3 test solution*
## Digital Validation and Debug

### DDR SDRAM Memory Support

<table>
<thead>
<tr>
<th></th>
<th>DDR</th>
<th>DDR2</th>
<th>DDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Analyzer Mainframe</td>
<td>TLA7102 Portable or TLA7016 Benchtop</td>
<td>TLA77AA4</td>
<td>TLA7BB4</td>
</tr>
<tr>
<td>Logic Analyzer Module**</td>
<td>TLA7AA4</td>
<td></td>
<td>TLA7BB4</td>
</tr>
<tr>
<td>Test Fixture/Support Package</td>
<td>Nexus Technology NEXVu &amp; FuturePlus System DDR Support</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Probing</td>
<td>Tektronix midbus probes or Nexus &amp; FuturePlus slot interposer and instrumented DIMMs</td>
<td></td>
<td>P6960HCD (&gt;1500MT/s) or NEX-PRB1XL (&lt; 1500MT/s)</td>
</tr>
</tbody>
</table>
## Analog Validation and Debug

### DDR SDRAM Memory Support

<table>
<thead>
<tr>
<th></th>
<th>LPDDR2</th>
<th>DDR2</th>
<th>GDDR3 DDR3*</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Oscilloscope</strong></td>
<td>DPO/DSA70404B or MSO70404 or higher</td>
<td>DPO/DSA70604B or MSO70604 or higher</td>
<td>DPO/DSA70804B or MSO70804 or higher</td>
</tr>
<tr>
<td><strong>Probing</strong></td>
<td></td>
<td></td>
<td>P7300 or P7500 Series Differential Probes</td>
</tr>
<tr>
<td><strong>Analysis Software</strong></td>
<td>DDR Analysis (DDRA), Advanced Search &amp; Mark (ASM), DPOJET Jitter/Eye Analysis (DJA)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Command Bus Triggering/Decode iCapture (Analog Mux)</strong></td>
<td>MSO70404 or higher</td>
<td>MSO70604 or higher</td>
<td>MSO70804 or higher</td>
</tr>
</tbody>
</table>

*Additional speeds supported with custom clocking selection in analysis software*
# Should I use a Logic Analyzer, MSO, or Digital Oscilloscope?

<table>
<thead>
<tr>
<th>Applications</th>
<th>TLA7000 Logic Analyzer</th>
<th>MSO70000 MSO</th>
<th>DPO/DSA70000B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full digital system visibility</td>
<td>Debugging high-speed events in a mixed signal environment</td>
<td>Debug &amp; measurements to 20 GHz</td>
<td></td>
</tr>
<tr>
<td>Processor bus validation</td>
<td>High-speed timing analysis and Debug</td>
<td>High speed transceiver analysis/characterization, Physical layer analysis</td>
<td></td>
</tr>
<tr>
<td>Full System (CPU, mem., I/O) visibility</td>
<td>High Speed FPGA or Embedded Memory interfaces</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory bus protocol verification</td>
<td>Memory bus analog verification</td>
<td>Memory bus analog verification</td>
<td></td>
</tr>
<tr>
<td>DDR2/DDR3 Debug</td>
<td>DDR2/DDR3 Debug</td>
<td></td>
<td></td>
</tr>
<tr>
<td>System validation</td>
<td>HSS Phy layer, characterization &amp; debug</td>
<td>High speed validation and margin analysis</td>
<td></td>
</tr>
<tr>
<td>Low-speed serial/parallel (command) bus correlated to high-speed signals (data/strobe/clock)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>State and Timing analysis (sync &amp; async sampling), Correlated Analog + Digital with iView</td>
<td>Timing Analysis, Correlated Analog + Digital validation</td>
<td>Timing Analysis, Analog characterization</td>
<td></td>
</tr>
<tr>
<td>Powerful, complex, 16-stage trigger equations, Memory bus disassembly</td>
<td>Hardware-based bus triggering, Bus/State qualified signal integrity</td>
<td>Single stage trigger for finding analog faults and logic patterns</td>
<td></td>
</tr>
<tr>
<td>Hundreds of channels</td>
<td>4 analog + 16 digital channels</td>
<td>4 analog</td>
<td></td>
</tr>
</tbody>
</table>
Summary – World’s Best DDR Test Solution

**COMPLETE**
- Provides total validation and characterization and full measurement support
- DDR1/2/3, LP-DDR1/2 and GDDR3 support in one tool
- Partnership with Nexus & FuturePlus provides most complete protocol and probing support

**Performance**
- Based upon highest performing oscilloscopes, Logic Analyzers and software analysis tools
- TriMode probing enables three
- Read/Write burst identification on all bursts
- Automated setup with JEDEC pass/fail limits

Comprehensive Test from Analog to Digital Validation for All DDR Versions

DDRA Validation Software
- DPO/DSA70000B Series Oscilloscopes
- P7500 Series TriMode Probes
- TLA7BBx Logic analyzer module for DDR
Resources

- What equipment do I need to test DDR?
  
  *Tektronix Knowledge Center:* [www.tektronix.com/memory](http://www.tektronix.com/memory)

- How can I learn more about DDR testing?
  
  *DDR Application Note:* [www.tektronix.com/ddr](http://www.tektronix.com/ddr)

  *Memory Implementers Forum:* [www.memforum.org](http://www.memforum.org)

- *JEDEC:* [www.jedec.org](http://www.jedec.org)