Link Analysis and Interconnect/Cable Testing for High Speed Serial Standards
Agenda

- Serial Data Network and Link Analysis Applications
  - Serial Data Network Analysis and Cable Testing
  - Serial Data Link Analysis and Jitter, Noise and BER Measurements
  - Summary
High Speed Serial Test Challenges

- Design Verification Compliance Test
- Simulation
- Signal Integrity: Eye and Jitter Analysis, Characterization & Validation
- System Integration: Digital Validation & Debug
- Data Link Analysis: Digital validation & Debug
- Transmitter Test: Eye and Jitter Analysis, Characterization & Validation
- Receiver Test
- Compliance Testing
- Interconnect Test & Link Analysis

Transaction Layer
- Data Link Layer
- Physical Layer
- Logical Sub-block
- Electrical Sub-block

Diagrammed components include Tx (transmitter), path, Rx (receiver), and various logical and electrical sub-blocks.
Market Dynamics

- 2nd & 3rd Gen HSS standards deploying
- Faster data rates and low level signals
- Understanding HF losses is critical

<table>
<thead>
<tr>
<th>Standard</th>
<th>Data Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>SATA Gen III</td>
<td>6 Gb/s</td>
</tr>
<tr>
<td>SATA Gen II</td>
<td>3 Gb/s</td>
</tr>
<tr>
<td>PCI Express 1.0</td>
<td>2.5 Gb/s</td>
</tr>
<tr>
<td>PCI Express 2.0</td>
<td>5 Gb/s</td>
</tr>
<tr>
<td>DisplayPort</td>
<td>2.7 Gb/s</td>
</tr>
<tr>
<td>HDMI 1.3</td>
<td>0.75 Gb/s to 2.25 Gb/s</td>
</tr>
<tr>
<td>FC 1, 2, 4 Gb/s</td>
<td>1 Gb/s to 4.25 Gb/s</td>
</tr>
<tr>
<td>FB-DIMM II</td>
<td>4.8-9.6 Gb/s</td>
</tr>
<tr>
<td>FibreChannel</td>
<td>4.25-8.5 Gb/s</td>
</tr>
<tr>
<td>10GE Ethernet</td>
<td>10.3125 Gb/s</td>
</tr>
</tbody>
</table>
Serial Data Network Analysis Application

- Time and frequency domain analysis, compliance testing of differential interconnects for data rates from 1 Gb/s to 10 Gb/s, and beyond

- Needs:
  - Accurate and repeatable impedance and S-parameter measurement results
  - Validate design performance
  - Verify standards compliance
  - Minimize test cost
  - Minimize test time

- Traditional S-parameter measurement methods – Vector Network Analyzers

- Modern S-parameter measurements – using TDR
Design Dynamics: Interactions Between Tx and Channel

Transmitter Analysis
- Jitter separation
- Noise separation
- Eye Contour and BER Eye

Network Analysis
- Characterization of the network (channel) through TDR and S-Parameters
- Impedance measurements
- Insertion & Return Loss
- Cross Talk characterization
Emerging Serial Data Link Analysis Application

- Traditional measurement techniques are inadequate – e.g., measuring transmitter or receiver alone is insufficient
- Must understand interactions between transmitter, channel, and receiver
- Equalization employed to compensate for signal loss at speeds >2.5 Gbs
- Must understand pre-emphasis effects at the transmitter output
- Need to understand effects of measurement systems (e.g., probing)
- Channel performance does not easily scale with transmitter/receiver performance
- Spread Spectrum Clocking (SSC) is emerging in low-cost standards

Complete Link Needs to be Considered – Need for Serial Data Link Analysis
Agenda

✓ Serial Data Network and Link Analysis Applications

⁻ Serial Data Network Analysis and Cable Testing
  ▪ Serial Data Link Analysis and Jitter, Noise and BER Measurements
  ▪ Summary
Network Characterization: Time-Domain Reflectometry (TDR)

Common TDR Measurements:
- Impedance
- Delay
- Intra-pair skew
- Inter-pair skew
Network Characterization: S-Parameters

Frequency-domain characterization of reflections and loss in a network

Quantitative insight into the causes of signal integrity problems

Common S-parameter Measurements:
- Differential return loss
- Differential insertion loss
- Frequency domain crosstalk
Dynamic Range for Insertion Loss and Return Loss

-70 dB at DC, -40 dB at 50 GHz

Best dynamic range with:
- More points
- More averages
- Shorter acquisition window

Dynamic range for insertion loss \( (S_{21}) \) is a thru measurement without connection between ports

Dynamic range for return loss \( (S_{11}) \) is a reflection measurement of a precision 50 Ohm termination
TDR-VNA S-parameter Correlation (40GHz)
HDMI Cable Example (with VNA correlation, 5 GHz)
<table>
<thead>
<tr>
<th>Standard</th>
<th>Data Rate</th>
<th>TDR</th>
<th>Required Frequency Domain Measurements</th>
<th>Lowest Measurement Level</th>
<th>Measurement Bandwidth Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>SATA Gen 2</td>
<td>3 Gb/s</td>
<td>★</td>
<td>★</td>
<td>-26 dB</td>
<td>100 MHz to 5 GHz</td>
</tr>
<tr>
<td></td>
<td>2.5 Gb/s</td>
<td>★</td>
<td>★</td>
<td>-10 dB</td>
<td>500 MHz to 3.75 GHz</td>
</tr>
<tr>
<td></td>
<td>3.4 Gb/s</td>
<td>★</td>
<td>★</td>
<td>-54 dB&lt;sup&gt;1&lt;/sup&gt;</td>
<td>100 MHz to 2.5 GHz</td>
</tr>
<tr>
<td></td>
<td>0.75 Gb/s to 4.25 Gb/s</td>
<td>★</td>
<td>-</td>
<td>-30 dB</td>
<td>300 kHz to 4.125 GHz</td>
</tr>
<tr>
<td></td>
<td>1 Gb/s to 4.25 Gb/s</td>
<td>★</td>
<td>★</td>
<td>-20 dB</td>
<td>100 MHz to 8 GHz</td>
</tr>
<tr>
<td></td>
<td>5 Gb/s</td>
<td>★</td>
<td>-</td>
<td>-8 dB</td>
<td>100 MHz to 3.2 GHz</td>
</tr>
<tr>
<td></td>
<td>2.5 Gb/s</td>
<td>★</td>
<td>-</td>
<td>-10 dB</td>
<td>Up to 1.25 GHz</td>
</tr>
<tr>
<td></td>
<td>3.125 Gb/s</td>
<td>★</td>
<td>★</td>
<td>-32 dB</td>
<td>100 MHz to 2 GHz</td>
</tr>
</tbody>
</table>

<sup>1</sup>-54 dB at low frequency only, well within the performance range of 80E10
Real Advantages vs Perceived Issues
TDR-Based Solution vs. VNA

- **TDR-Based Solution Advantages:**
  - Ease of calibration, and consequently...
    - Fast throughput
    - Ease of use
    - Easy fixture de-embedding – critical for compliance testing
  - 25%-35% lower cost for differential serial data application requirements

- **Perceived Issues w/TDR-Based Solution**
  - Lower dynamic range
    - Up to 70dB for TDR-based vs. up to 100 dB for traditional VNA
    - 70dB is perfectly suitable for serial data applications
      - typical measurement is in -10 to -40dB range
IConnect® Software Unique Capabilities

- Automated data collection using scripts for SDNA
  - For serial data standards – or Touchstone output

- Eye diagram – including crosstalk effects and equalization
  - Standard-defined compliance testing and channel analysis

- Complete channel simulation using Link Simulator
  - *Measurement based, no Spice models required*
  - Combine 5 backplanes and 5 cables and choose the best performing combination in minutes instead of hours or days
  - Not for Tx/Rx simulation

- EZ Z-line UI for efficient fault isolation
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The Case for Jitter Analysis

- The case for Jitter analysis has been accepted industry wide
  - Separating jitter into its constituent components provides increased precision and insight into root cause of BER performance
The Cause for **Jitter** and **Noise** and BER Analysis

- BER of a link is limited by just Jitter
  - Jitter separation leads to insight into root cause
  - BER extrapolations and bathtub curves are accurate

- Sometimes it is **noise** that dominates the BER
  - Jitter separation provides very little insight into root cause of BER performance

- Often it is limited by both Jitter and Noise
  - Jitter separation provides only a limited answer

- 80SJNB: Jitter and Noise Separation and Accurate BER Extrapolation
More Accurate BER Analysis

More Accurate Eye Contour and BER Extrapolation

Jitter Separation

Bit Error Ratio (BER)

Total Jitter (TJ)

Random Jitter (RJ)

Deterministic Jitter (DJ)

Periodic Jitter (PJ)

Data Dependent Jitter (DDJ)

Duty-Cycle Jitter (DCD)

Noise Separation

Total Noise (TN)

Random Noise (RN)

Deterministic Noise (DN)

Periodic Noise (PN)

Data Dependent Noise (DDN)

80SJNB the FIRST oscilloscope solution to TOTAL BER analysis!
The Breakthrough in Serial Data: PDF Eye, BER Eye

- Jitter and Noise separation provides crucial new understanding of a data link’s BER
  - Statistical Eye diagrams describing the probability of the signal across the eye
  - Jitter-only solution do not give accurate BER predictions
80SJNB Advanced Jitter, Noise and BER Analysis Software

Jitter and Noise Results

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TJ @ BER</td>
<td>Total jitter @ BER</td>
</tr>
<tr>
<td>RJ</td>
<td>Random jitter</td>
</tr>
<tr>
<td>RJ (h)</td>
<td>Horizontal component of random jitter</td>
</tr>
<tr>
<td>RJ (v)</td>
<td>Vertical component of random jitter</td>
</tr>
<tr>
<td>RJ (δ-δ)</td>
<td>Random jitter computed in the dual Dirac model</td>
</tr>
<tr>
<td>DJ</td>
<td>Deterministic jitter</td>
</tr>
<tr>
<td>DDJ</td>
<td>Data dependent jitter</td>
</tr>
<tr>
<td>DDPWS</td>
<td>Data Dependent Pulse Width Shrinkage</td>
</tr>
<tr>
<td>DCD</td>
<td>Duty cycle distortion</td>
</tr>
<tr>
<td>DJ (δ-δ)</td>
<td>Deterministic jitter computed in the dual Dirac model</td>
</tr>
<tr>
<td>PJ</td>
<td>Periodic jitter</td>
</tr>
<tr>
<td>PJ (h)</td>
<td>Horizontal component of periodic jitter</td>
</tr>
<tr>
<td>PJ (v)</td>
<td>Vertical component of periodic jitter</td>
</tr>
<tr>
<td>EOH @ BER</td>
<td>Horizontal eye opening @ specified BER</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RN</td>
<td>Random noise</td>
</tr>
<tr>
<td>RN (v)</td>
<td>Vertical component of random noise</td>
</tr>
<tr>
<td>RN (h)</td>
<td>Horizontal component of random noise</td>
</tr>
<tr>
<td>DN</td>
<td>Deterministic noise</td>
</tr>
<tr>
<td>DDN1</td>
<td>Data dependent noise on logical level 1</td>
</tr>
<tr>
<td>DDN0</td>
<td>Data dependent noise on logical level 0</td>
</tr>
<tr>
<td>PN</td>
<td>Periodic noise</td>
</tr>
<tr>
<td>PN (v)</td>
<td>Vertical component of periodic noise</td>
</tr>
<tr>
<td>PN (h)</td>
<td>Horizontal component of periodic noise</td>
</tr>
<tr>
<td>EOV @ BER</td>
<td>Vertical eye opening @ specified BER</td>
</tr>
</tbody>
</table>
80SJNB Results Overview

Computed Horizontal and *Vertical* Bathtub, BER-Eye view, Contours view, and others.

Whatever should be measured, plot or calculated – if its serial data 80SJNB has the answer.
The Foundation for Serial Data Link Analysis

- Serial Data Link Analysis
  - Combined transmitter & channel analysis for virtual view at the receiver
  - Impairment compensation with Equalization and Emphasis

Builds on and incorporates:

- Transmitter Characterization
  - Jitter separation
  - Noise separation
  - Eye Contour and BER Eye

- SDNA For Channel Characterization
  - Impedance measurements
  - Insertion & Return Loss
  - Cross Talk characterization
## Pre-/De-Emphasis, Equalization, & SSC in High Speed Standards

<table>
<thead>
<tr>
<th></th>
<th>Data rate [Gbps]</th>
<th>Pre-/De-emphasis in Tx</th>
<th>Equalization: FFE only:</th>
<th>FFE/DFE:</th>
<th>Spread Spectrum Clocking (SSC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SATA Gen 2</td>
<td>3</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SATA Gen 3</td>
<td>6</td>
<td>★</td>
<td>★ Opt.</td>
<td>-</td>
<td>★</td>
</tr>
<tr>
<td>PCI Express 1.0</td>
<td>2.5</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>★</td>
</tr>
<tr>
<td>USB 3.0</td>
<td>5</td>
<td>★</td>
<td>-</td>
<td>-</td>
<td>★</td>
</tr>
<tr>
<td>FibreChannel</td>
<td>&lt;4.25</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>FibreChannel</td>
<td>8.5</td>
<td>★</td>
<td>★</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>XAUl</td>
<td>3.125</td>
<td>★</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>10GE Ethernet LRM</td>
<td>10.3125</td>
<td>-</td>
<td>★</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>(Multi-mode fiber)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10GE Ethernet KR</td>
<td>10.3125</td>
<td>★</td>
<td>★</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>(backplane)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFP+ Interconnect</td>
<td>8G, 10G</td>
<td>★</td>
<td>★</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
One High Performance Oscilloscope Does not Fit All High-End Applications

Real-time Scopes
The most versatile tool for all areas of high-speed digital and analog applications

Sampling Scopes
For applications that place top priority on waveform precision
Serial Data Link Analysis Tool for DSA8200

- Characterization of the channel (network)
- Characterization of the transmitter
- Emulation of the waveform at the receiver; output to simulation software
- Closed loop analysis and correction, from transmitter to receiver

Most Complete SDLA Solution In the Industry
- 8.5 Gb/s Signal Without Equalization…
- … and with FFE/DFE Equalization
80SJNB Equalization, Channel Emulation

- Emulate channel effects using Touchstone S-parameter or TDR/T data
- Max FFE taps – 100
  - FFE taps per UI – 1, 2, 5, 10
- Max DFE taps – 40
- Ability to “Autoset Taps” to minimize noise
- Delay FFE filter using “FFE Reference Tap”
- “Rise Time Selector” to emulate effects of DFE path
  - Defines a Gaussian filter
  - $T_{rise}$ defaults to 20% of UI
Introducing Serial Data Link Analysis for DSA/DPO70000

- Characterization of the transmitter
- Emulation of the waveform at the receiver; including effects of the channel and equalization
- Remove the effects of the test fixture

Complete SDLA Solution for Real Time
Precise – Insightful - Flexible
De-embed test fixture (probing) on DSA/DPO70000

- When measuring the signal, the fixture impacts the result
- What does the signal look like at the Tx, without fixture?

- Measure the Fixture (with TDR, VNA, etc) and generate the S parameters: *S1p (S21), *S2p or *S4p (SE or Diff)
- In SDLA: Select “Fixture”. Import the S parameter file. Select a reasonable filter bandwidth (for the inversion)
- Debug the results created in frequency and time domain

Note: Model does not support return loss
De/Pre-emphasis – add/ remove emulation

- When measuring the signal after the emulated channel
- What would the signal look like at the Rx, with Emphasis?

- Transmitter equalization
  - Pre/De-emphasis.
  - Enter the dB
- See the results in frequency and time domain for debug
Rx Equalization Emulation with FFE and DFE

- What would the signal look like at the Rx, with Equalization?
- When measuring the signal after the emulated channel

- Supports FFE and DFE.
- DFE has 3 modes of operation: Adapt from provided taps, Adapt from automatically generated taps, do not adapt.
- Same Clock recovery as DPOJET
- Slicer controls
- Support training sequence
- Create Ref waveforms to plot into Eye diagrams in DPOJET
Agenda

✓ Serial Data Network and Link Analysis Applications
✓ Serial Data Network Analysis and Cable Testing
✓ Serial Data Link Analysis and Jitter, Noise and BER Measurements

Summary
Serial Data Network and Link Analysis Toolset

TDR/TDT/IConnect for Serial Data Network Analysis
- 50 GHz TDR/TDT system and S-Parameter measurements, highly accurate impedance and loss measurements
- Up to 1M record length

80SJNB – Jitter Noise, BER and Link Analysis
- Advanced Transmitter Analysis with SSC support
- “Complete Link” – channel embedding/de-embedding, equalization (FFE/DFE)
- Separation of Jitter & Noise into deterministic & random components at the comparator
- Eye contour and BER eye calculations at the comparator

Serial Data Link Analysis for DSA/DPO70000
- DFE/FFE Equalization algorithms correlated to industry references
- Time and Frequency plots to verify S-parameters translation
- Equalization with 3 modes of adaptation that can learn from a known pattern, a random pattern or traffic or can be pre-configured