PCI Express 3.0 – Physical Layer Solutions
Sarah Boen
PCI Express 3.0 Technology Timeline

<table>
<thead>
<tr>
<th>Year</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
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</tbody>
</table>

- **Estimated Date**
- **Released Date**

*Base Spec*
- 0.5 Release
- 0.7
- 0.9
- 1.0

*CEM Spec*
- 0.5 Release
- 0.7
- 0.9
- 1.0

*Test Spec*
- 0.3 Release
- 0.5
- 0.7
- 0.9
- 1.0

- **Integration Phase**
  - Product Development
  - PCI-SIG Tool Development
  - CEM Spec Development

- **Deployment Phase**
  - FYI Testing
  - 6 Month FYI Testing

All information in this presentation is based on 1.0 Base Specification

Tektronix Involved in PCIe EWG, CEM, and SEG Working Groups
### PCI Express 3.0

#### Trends and Implications

**Industry/Technology Trends**

- 8GB/s using the same board material (FR4) and connectors results in increased channel loss.
- Probing access at the transmitter pins is typically not available.
- Receiver equalization can only compensate for channel loss.
- Receiver Testing is a requirement and is critical to ensure system interoperability.
- Energy efficiency (Lower mW/ Gb/s).

**Implications**

- Link Analysis - de-embedding, embedding, and RX equalization is required post process.
- Closed data eyes requiring new techniques for transmitter and receiver equalization.
- Higher data rate signals have less margin - requires de-embedding for base specification measurements.
- New Jitter Separation Measurements are required.
- Back channel negotiation to equalize the receiver.
- Link training and power management continue to be the most difficult logic layer challenges.
Transmitter PHY Layer Analysis for PCIe 3.0
PCIe 3.0 Transmitter Compliance Testing

- Compliance testing is based on the Compliance Test Specification, which is under development
- New compliance 128b/130b data pattern
- Three Tests
  - Electrical: Eye Height and Width must pass one pre-set value
  - Preset Test: all Pre-sets are tested to be within their limits
  - Transmitter Equalization Test: Verify the transmitter will respond to equalization change requests
- Measurements are taken after the Compliance channel and RX Equalization using the Compliance Base or Load Board
Transmitter Equalization For Compliance

- Transmitter equalization now requires pre-shoot in addition to de-emphasis to compensate for channel loss
- Transmitters must support all defined presets and a subset for low swing devices
- Presets are toggled on the CLB or CBB the same way as Gen 2 CLB/CBB

<table>
<thead>
<tr>
<th>Preset Number</th>
<th>Preshoot (dB)</th>
<th>De-emphasis (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P4</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>P1</td>
<td>0.0</td>
<td>-3.5 ± 1 dB</td>
</tr>
<tr>
<td>P0</td>
<td>0.0</td>
<td>-6.0 ± 1.5 dB</td>
</tr>
<tr>
<td>P5</td>
<td>3.5 ± 1 dB</td>
<td>0.0</td>
</tr>
<tr>
<td>P6</td>
<td>3.5 ± 1 dB</td>
<td>-3.5 ± 1 dB</td>
</tr>
<tr>
<td>P7</td>
<td>3.5 ± 1 dB</td>
<td>-6.0 ± 1.5 dB</td>
</tr>
<tr>
<td>P6</td>
<td>1.9 ± 1 dB</td>
<td>0.0</td>
</tr>
<tr>
<td>P6</td>
<td>2.5 ± 1 dB</td>
<td>0.0</td>
</tr>
<tr>
<td>P3</td>
<td>0.0</td>
<td>-2.5 ± 1 dB</td>
</tr>
<tr>
<td>P2</td>
<td>0.0</td>
<td>-4.4 ± 1.5 dB</td>
</tr>
<tr>
<td>P10</td>
<td>0.0</td>
<td>See Note 2</td>
</tr>
</tbody>
</table>
Transmitter Compliance Preset Test

- Validate Vb, De-Emphasis and Preshoot for each Preset are within spec limits
Add-In Card Compliance Signal Acquisition and Processing

Signal Acquired from Compliance Board

Embed the Add-In Card Compliance Channel

Closed Eye due to the Channel

Apply the Base Specification CTLE + DFE for Long Channel

Open Eye for Measurements

System Board Eye Limits

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{TXS}</td>
<td>50</td>
<td>1200</td>
<td>mV</td>
</tr>
<tr>
<td>V_{TXS_d}</td>
<td>50</td>
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<td>mV</td>
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<tr>
<td>T_{TXS}</td>
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<td>41.25</td>
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Add-In Card EyeLimits

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
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<td>50</td>
<td>1200</td>
<td>mV</td>
</tr>
<tr>
<td>V_{TXA_d}</td>
<td>50</td>
<td>1200</td>
<td>mV</td>
</tr>
<tr>
<td>T_{TXA}</td>
<td></td>
<td>41.25</td>
<td>ps</td>
</tr>
</tbody>
</table>

1 Measurement Limits Under CEM Review
Serial Data Link Analysis for PCIe Compliance Measurements

- De-embed cables / fixtures
- Embed the effects of the channel
- Equalize the waveform using CTLE, FFE, and/or Dfe
Embed Compliance Channel

- Verify the channel attenuation
  - Based on the PCIe 3.0 Add-In Card Compliance Channel, 10dB attenuation is expected on high frequency bits (4Ghz for PCIe Gen 3)
Validate Channel Embedding on Scope Waveform

- Based on the Insertion Loss Plot, we expect a 10dB loss at the fundamental frequency of 4Ghz.
  - This equates to approx. 68% reduction in the high frequency content of the signal (\(\text{lin} = 10^{\frac{\text{db}}{20}}\), so \(10^{\frac{-10}{20}} = .316\))

- This can be easily verified on the scope waveform by doing a quick check using cursor measurements
Validate Channel on Scope Waveform

- Next measure the vertical amplitude after the channel (approx. 140mV)
- SDLA has automatically applied the channel filter to Math 4
Receiver Equalization

- PCIe reference equalizer is CTLE and 1 Tap DFE
  - CTLE – one Zero and Two Poles
  - DFE – 1 Tap (-30/30mV tap value)
- Equalizer is optimized on the CTLE + DFE tap value that results in the best eye area
  - 7dB Adc settings are shown in the example below
Automated Receiver Optimization

- Manually optimizing over 7 CTLE settings is time consuming
- Optimization is automated with SDLA
- Optimization is done on a short record across all settings, the setting with the best eye opening is then computed and measurements can be taken
Verifying Effects of RX Equalizer

- Low frequency bits are attenuated based on the optimal CTLE setting
- Example below shows plot of -8dB Adc
  - Low frequency bits should be attenuated by ~60%
- DFE will result in an increase of eye opening based on the tap value setting
Validate Equalizer: Analyze Raw Waveform

- On the scope, use cursors to measure the low frequency content of the signal on the acquired waveform (Math 1)
- In this example the low frequency content of the waveform is approx. 615mV
Validate Equalizer: Analyze Waveform After CTLE

- Based on the CTLE that was applied, we expect a 60% attenuation in the low frequency content after the CTLE.
- This can quickly be verified, note the low frequency amplitude is approx. 240mV.
Validate Equalizer: Analyze DFE

- The DFE will open the eye by twice the tap value
- PCIe uses a 1 tap DFE, meaning that the previous bit will determine if change of the current bit.
- The table below outlines the change based on the 20mV Tap

<table>
<thead>
<tr>
<th>Previous Bit</th>
<th>Current Bit</th>
<th>Change</th>
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<tr>
<td>0</td>
<td>1</td>
<td>20mV</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>-20mV</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>No Change</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>No Change</td>
</tr>
</tbody>
</table>
Validate Equalizer: Analyze DFE

- DFE will open the eye by approx 2 times the tap value
- High frequency signal before DFE is 126mV and after 166mV, which is 2 times the tap value of 20mV
CEM Measurements with Optimized RX Settings

- CEM measurements can be quickly done with pre-defined setup files in DPOJET
- Simultaneous assessment of the signal at each point during the post processing stage
Testing Beyond Compliance

- What happens if a measurement fails SigTest?
- Could it be the channel?
  - Measurements can be taken before the channel to evaluate results
  - Different channel models can be created using Serial Data and Link Analysis
- How does the optimized RX setting compare to other settings?
  - Easily compare the results of multiple Equalization settings
- Does deeper analysis of the waveform need to be done?
  - PCIe specific measurements can be taken in Tektronix' measurement system DPOJET
  - Determine if data dependent, uncorrelated or pulse width jitter is in spec
  - Measurements filters and settings can be adjusted to get to root cause, but remember you must pass SigTest to be certified for compliance
- Is the TX compliant?
  - NEW PCIe 3.0 base spec measurements are available to verify TX compliance
Base Specification Transmitter Measurements

- Base Specification Measurements are defined at the pins of the transmitter
- Signal access at the pins is often not assessable
- De-embedding is required to see what the signal look liked at the pins of the TX, without the added effects of the channel
- Sparameters are acquired on the replica channel
De-embedding Considerations

- De-embedding amplifies high frequency noise, thus requiring a bandwidth filter
  - This also impacts the required bandwidth for a RT Scope
  - Bandwidth is dependent on board material

- Successful de-embedding starts with good quality board design and S-Parameter data
  - Matched impedance, low loss structures
  - No gain, significant resonances, or large dips

- Quality of de-embedding
  - Eye height and jitter
  - Signal to Noise Ratio
Verification of De-embedding Results

- Best to have original signal at the TX pins
- Embed the sparameter representing the test fixture
- De-embed the sparameter representing the test fixture
- Compare the waveform as acquired from the DUT directly with the fixture embedded in the original waveform
  - Captured Waveform (White), Channel Embedded in Direct Waveform (Yellow)
De-Embedding Results

- Good correlation is shown below- verify rise time, pre-shoot/under-shoot, ripples
- Signal at TX pins – white
- Signal at TP1 – blue
- Signal after de-embedding from TP1 – Red
Further Analysis on Gen 3 Measurements

- Acquired Signal (Left)
- De-embedded Signal (Center)
- Signal at TX Pins (Right)
- All Gen 3 Base Spec Measurements done on de-embedded waveform
NEW PCI Express Base Specification Measurements

- Voltage
- Package Loss
- Transmitter Equalization
- Jitter
Transmitter Equalization Measurements

VTX-BOOST-FS / VTX-BOOST-RS

- What’s new for Gen 3.0
  - De-Emphasis (Va) and pre-shoot (Vc)
  - Transmitters must support 11TX equalization pre-sets

- The high frequency nature of 8.0 GT/s signaling makes measurement of single UI pulse heights impractical due to attenuation by the package and breakout channel
  - Amplitude measurements are taken on low frequency waveforms (64 ones/ 64 zeros in the compliance pattern) using last few UI of each half period
  - Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

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</tr>
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<td>0.0</td>
<td>-3.5 \pm 1 dB</td>
</tr>
<tr>
<td>P0</td>
<td>0.0</td>
<td>-6.0 \pm 1.5 dB</td>
</tr>
<tr>
<td>P9</td>
<td>3.5 \pm 1 dB</td>
<td>0.0</td>
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<td>P8</td>
<td>3.5 \pm 1 dB</td>
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<td>See Note 2.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Preset Number</th>
<th>De-emphasis (dB) (20 \log_{10}(Vb/Vb(i)))</th>
<th>Preshoot (dB) (20 \log_{10}(Vb/Vb(i)))</th>
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<td>N/A</td>
</tr>
<tr>
<td>P1</td>
<td>P1/P4</td>
<td>N/A</td>
</tr>
<tr>
<td>P0</td>
<td>P0/P4</td>
<td>N/A</td>
</tr>
<tr>
<td>P9</td>
<td>N/A</td>
<td>P4/P9</td>
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<tr>
<td>P8</td>
<td>P8/P6</td>
<td>P3/P6</td>
</tr>
<tr>
<td>P7</td>
<td>P7/P5</td>
<td>P2/P7</td>
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<td>P4/P5</td>
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<td>N/A</td>
<td>P4/P6</td>
</tr>
<tr>
<td>P3</td>
<td>P3/P4</td>
<td>N/A</td>
</tr>
<tr>
<td>P2</td>
<td>P2/P4</td>
<td>N/A</td>
</tr>
<tr>
<td>P10</td>
<td>P10/P4</td>
<td>N/A</td>
</tr>
</tbody>
</table>
Transmitter Voltage Measurements

**VTX-EIEOS-FS / VTX-EIEOS-RS**

- **Launch Voltage of Electrical Idle Exit Ordered Set**
- **Required to ensure that the RX can properly detect an exit from electrical idle**
- **Taken on a pattern of eight ones followed by eight zeros repeated 128 times included in the compliance pattern**
  - Taken on the middle five UI to reduce attenuation effects of the channel
- **VTX-EIEOS-FS - Full Swing Signaling**
  - Measured by Preset 10
- **VTX-EIEOS-RS – Reduced Swing Signaling**
  - Measured by Preset 1
Package Loss Measurements

PS21

- Can be taken at TP1 while capturing silicon package loss and drive characteristics, but due to the high frequency content of the 1010 pattern the measurement must be de-embedded back to the TX pins
- Measured by comparing 64 zeros and 64 ones PP voltage against a 1010 pattern
- Measured with de-emphasis and pre-shoot set to 0 at the end of each interval to minimize ISI and low frequency effects
Transmitter Jitter Measurements

- Necessary to take transmitter jitter measurements with all lanes operating in order to capture crosstalk effects
- Measurements are taken at TP1 and de-embedded back to the pins of the TX
- Necessary to separate uncorrelated and data dependent jitter in order to ensure that jitter that can be recovered is not budgeted as uncorrelated jitter

<table>
<thead>
<tr>
<th>Jitter measurements</th>
<th>Data Dependent Jitter</th>
<th>Uncorrelated Jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cause</td>
<td>Due to package loss and reflections (dynamics in the channel, ISI)</td>
<td>Uncorrelated - PLL jitter, crosstalk, noise conversion (amplitude to phase)</td>
</tr>
<tr>
<td>How to compensate</td>
<td>Can be reduced by equalization</td>
<td>Difficult to remove (better components, layout)</td>
</tr>
</tbody>
</table>
Transmitter Jitter Measurements: Data Dependent Jitter

**TTX-DDJ**

**DDJ Measurement Process**

- Measurement taken on multiple repeats of the compliance pattern using a 1\textsuperscript{st} order CDR function representing a high pass filter
- A PDF is created for each edge crossing of the compliance pattern
- DDJ is calculated as the difference of the mean of each PDF and the recovered clock edge
- Measurement is defined as the absolute value of \( DDJ(\text{max}) - DDJ(\text{min}) \)
Uncorrelated Jitter Example

**TTX-UTJ / TTX-UDJDD**

- DDJ is removed from the PDF of each edge
- Data is converted to Q-Scale
- Uncorrelated Deterministic Jitter Dual Dirac (UDJDD)
  - Accounts for Periodic Jitter and Crosstalk
    Convert the PDF to Q-Scale
- Random Jitter is implied by subtracting UDJDD from UTJ

![Diagram of TTX-UTJ and TTX-UDJDD derivation](image)
Uncorrelated Total and Deterministic PWJ

TTX-UPW-TJ / TTX-UPW-DJDD

• Pulse Width Jitter
  – Addresses lone bits that are attenuated the most in lossy channel and could likely cause bit errors
• DDJ is removed to accurately quantify PWJ
• Calculate edge-to-edge jitter
• Construct Q-scale PDF curve and Extrapolate to BER = 10^{-12} (Q= 7.03) to determine Uncorrelated Pulse Width Jitter (containing F/2 or Odd/Even Jitter) and Deterministic Pulse Width Jitter
• Final measurements are calculated by looking at the left hand side of the PDF curve
Tektronix Solutions for PCI Express 3.0 Measurements

• Visibility
  – Tektronix is the only scope vendor that provides visibility of the link at multiple test points.
  – Unlike other solutions Tektronix provides a complete set of Base Specification measurements with associated plots for characterization, debug, and analysis
  – Complete insight into all possible equalization settings for comparison and debug

• Flexibility
  – Customers can quickly verify their measurements with different configuration settings, unlike other solutions
  – Other solutions are targeted at compliance, however, with DPOJET customers can quickly debug root cause of problems in a standard specific environment

• Compliant
  – Equalization follows the requirements in the specification, unlike other vendors who have a single methodology for applying a DFE
Receiver PHY Layer Analysis for PCIe 3.0
Tektronix BSA85C Bit Error Rate Tester
Agenda

1. Introduction

2. Stressed Eye
3. Beyond Compliance
4. Receiver Test Demonstration

PCI Express is a trademark of PCI-Sig, www.pcisig.com
USB is a trademark of USB-IF, www.usb.org
Introduction

- Latest Generation Computer Standards have some **common trends**.
- We’ll use **PCI Express Gen 3** as our main example.
- **Similar themes** are emerging in other new standards such as IEEE 100GbE etc.
Introduction - Basics

At the simplest level, receiver testing is composed of:

1. Send **impaired signal** to the receiver under test.

2. The **receiver decides** whether the incoming bits are a one or a zero.

3. The chip **loops back** the bit stream to the transmitter.

4. The **transmitter sends out** exactly the bits it received.

5. An **error counter** compares the bits to the expected signal and looks for mistakes (errors).

- Pattern Generator
- Stress
- Error Counter
PCI Express 3.0 Equipment Setup

- Product: Silicon, Host, and AIC solutions from the BERTScope portfolio
- Industry Knowledge: Participation in standards meetings
- Technical Expertise: Plugfest, Intel testing events

Host Testing

Add-in Card Testing

OEM Host Equipment List

- BSA85C
- DFF125B
- CR125A
- DM Interference Combiner
- CLB/CBB
- RT Scope with latest SGTEST version
- Repeater board for long channel Tx
- SMA-SMP right angle cables (Rosenberger L71-456-102-3808)
Agenda

1. Introduction

2. Stressed Eye
   - Changing Test Signal Recipes
   - Channel Considerations
   - Calibration Challenges

3. Beyond Compliance
Receiver Testing (a.k.a “Jitter Tolerance”) Review

- Test receiver for error free operation (0 BER) while stressed with input jitter/impairments.
- Calibrated jitter/stress is added to Pattern Generator (PG), output is increased until receiver experiences bit errors, or test limit is reached.
- Test often repeated at another jitter frequency, results are plotted.
Test receiver for error free operation (0 BER) while stressed with input jitter/impairments.

Calibrated jitter/stress is added to Pattern Generator (PG), output is increased until receiver experiences bit errors, or test limit is reached.

Test often repeated at another jitter frequency, results are plotted.

- Stress recipe varies by standard. In theory it emulates the system impairments for the expected use.
- Higher data rates mean closed eyes and crosstalk are bigger issues.
PCI Express Gen 3 uses a long circuit board channel that closes the eye, and two forms of vertical eye closure ("Interference").

(Taken from PCI Express Base Spec, Figure 4-71)
PCle Gen 3 Stress Recipe
- Channel

- Depending upon Host or Add-in Card, different test fixtures/combinations are used.

- ISI is large enough to mean the Eye is closed at the receiver.
PCIe Gen 3 Stress Recipe
- Calibration

Post-processing by software. Several complex elements are accommodated in software including the IC package and elements within the IC including the equalizer.

This is still in flux – Correlation work ongoing between simulation and direct measurement and analysis techniques. Being refined at Plugfests.
PCIe Gen 3: Example Add-In Card Stress Calibration

To RT Scope for calibration

Last Cal. details being refined. This setup being successfully used at Plugfests.
Base Spec calibration recommendation

- SigTest or DPOJET
  - PCI-SIG group methodology
  - Repeatable
  - Easy to understand
  - Used for Tx testing
Loopback – PCIe 3

• PCIe 3 loopback is more complicated.
  1. **Speed negotiation** – natively 2.5GT/s, needs to negotiate up to 8GT/s
  2. **Equalization negotiation** – receiver controls transmitter pre-emphasis and find optimum Tx & Rx settings – 500ns compliance response time limit
  3. **Setting of device into Loop**
     • Initially “brute force” with static patterns
     • Now **compliant state machine**

• Feedback from Plugfests is that Add-In Card manufacturers aren’t implementing equalization negotiation yet. Instead test with limited number of pre-emphasis presets (3)
Agenda

1. Introduction
2. Stressed Eye

3. Beyond Compliance

When a Device Fails… What Next?
Beyond Compliance
BERTScope = Debug/Characterization

1. Click a control button in the UI
2. Adjust
3. Changes happen instantly

- You may need to try lots of different signal conditions
- May want to monitor BER while changing stress conditions on the fly
Beyond Compliance
The BERTScope Analysis Tools

- Besides being a BERT, the BERTScope’s “Scope” functionality brings benefits that complement those of the Tektronix scopes
- Analysis tools are full featured and easy to use
  - Frees up the scope for other tasks
  - Eye diagram for quick diagnosis of synchronization and BER failure issues
  - Debug challenging signal integrity problems
    - Error Location Analysis
    - Pattern Capture
    - Jitter Map
    - BER Contour
Summary

- Higher speeds on cheap channel materials causing closed eyes from ISI and crosstalk

- Increased use of equalization forcing changes in testing: speed, equalization negotiation & Tx control

- Test signal is changing:
  - Vertical eye closure
  - Closed eye
  - Calibration is evolving

- Attaining Loopback is often problematic.

- Returned signal is often also a closed eye, meaning eye needs opening before error counting
Extensive application information at:

www.tek.com

PCI Express : PCI-Sig, www.pcisig.com
Important Resources

• **Complete Solutions Available on** [www.tek.com](http://www.tek.com)
  - Solutions available today for PCIe 1.0, 2.0, 3.0 Transmitter, Receiver, PLL Loop bandwidth and Protocol Testing

• **Support & Resource Links**
  - Recommended Equipment Configurations
    
    [www.tek.com/serial_data](http://www.tek.com/serial_data)
  - Access to new PCE3 Software Downloads & Free Trial
    
    [www.tek.com/software](http://www.tek.com/software) (search for PCE3)
  - PCI Express Base Specification (members only)
    