Debugging and Compliance Testing of Serial Designs
Agenda

- High Speed Serial Data Fundamentals
  - Introduction
  - Architecture and common elements
  - Performance requirements
  - Filtering/Equalization
  - Probing/Signal Access

- Signal Integrity
  - Signal Loss
  - Crosstalk
  - Jitter
  - Noise

- Compliance Testing
  - Technology Timeline
  - Toolset

- Summary
**High Speed Serial: Defined**

- Fast serial buses are replacing many parallel buses
  - Fast serial signals were found mostly in Telecom and Datacom industries. They now span several industries including Computer, Consumer, Government, and even Automotive.
  - *High Speed Serial* applications range from hundreds of MHz to tens of GHz: these speeds span the Tektronix performance and high bandwidth products.
PCI Express Example of Increase in Data Rate From Parallel to Serial Evolution

- Going from parallel PCI bus to one-lane of PCI Express

**PCI at 33 MHz**

- Verifying clean transitions
- Measuring setup and hold times

**PCI Express Gen II at 5 Gbps**

- 300 bits in same interval
- Recovering spread spectrum clock embedded in data
- Sorting transition, non-transition bits for mask test
- Jitter <30 ps

*Unit Intervals*
The Industry Today

Data capacities are increasing...

- This drives a need for faster transport systems
- Complexity/cost of parallel systems drives serial systems
- Commercial state-of-the-art parallel is about 3GT/s
- Commercial state-of-the-art serial is between 6.25Gb/s and 8Gb/s
- Highest electrical data rates are about 10.25Gb/s in specialized backplanes (but 25Gb/s-40Gb/s MLT-3 being studied)
The Basic Blocks of the Serial DATA Link

**Transmitters**
- Differential Transmitter

**Interconnects (paths)**
- Dual-coax differential cable
- Twisted-pair differential cable
- Coupled-pair traces on **circuit board** (backplanes)

** Receivers **
- Differential Receiver
Common Elements of High Speed Serial

- Differential Signaling
- TMDS or LVDS
- Embedded Clocks
- 8b/10b Encoding
- Typical Measurements
  - Jitter
  - Eye Diagram
  - Rise/Fall Times
  - Bit Rate
  - Differential Amplitude
  - AC/DC Common Mode Voltages
- While many elements are common across different standards, there are variations from one standard to the next.
Embedded Clock

Differential serial data is sent **without any clock** signal across the interconnect to the receiver.

A clock is “recovered” from the incoming data at the receiver through a **clock and data recovery** circuit (CDR).
A Real Life Example: PCI Express

Figure 4-50: Refclk Transport Delay Paths for a Common Refclk Rx Architecture
High Speed Serial Test Challenges

Design

Verification

Compliance Test

Simulation

System Integration
Digital Validation & Debug

Data Link Analysis
Digital validation & Debug

Transmitter Test
Eye and Jitter Analysis
Characterization & Validation

Receiver Test

Compliance Testing

Interconnect Test & Link Analysis

Transaction Layer

Data Link Layer

Physical Layer

Logical Sub-block

Electrical Sub-block
Gigabit Data Rates Require High-Bandwidth Test

<table>
<thead>
<tr>
<th>Serial Bus Data Rate</th>
<th>Fundamental Frequency</th>
<th>3&lt;sup&gt;rd&lt;/sup&gt; Harmonic</th>
<th>5&lt;sup&gt;th&lt;/sup&gt; Harmonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 Gb/s (PCI-Express)</td>
<td>1.25 GHz</td>
<td>3.75 GHz</td>
<td>6.25 GHz</td>
</tr>
<tr>
<td>3.0 Gbps (SATA II)</td>
<td>1.5 GHz</td>
<td>4.5 GHz</td>
<td>7.5 GHz</td>
</tr>
<tr>
<td>3.125 Gbps (XAUI)</td>
<td>1.56 GHz</td>
<td>4.69 GHz</td>
<td>7.81 GHz</td>
</tr>
<tr>
<td>4.25 Gb/s (Fibre Channel)</td>
<td>2.125 GHz</td>
<td>6.375 GHz</td>
<td>10.625 GHz</td>
</tr>
<tr>
<td>4.8 Gb/s (FBD)</td>
<td>2.4 GHz</td>
<td>7.2 GHz</td>
<td>12.0 GHz</td>
</tr>
<tr>
<td>5.0 Gb/s (PCI-Express 2.0)</td>
<td>2.5 GHz</td>
<td>7.5 GHz</td>
<td>12.5 GHz</td>
</tr>
<tr>
<td>6.0 Gb/s (SATA III)</td>
<td>3.0 GHz</td>
<td>9.0 GHz</td>
<td>15.0 GHz</td>
</tr>
<tr>
<td>6.25 Gb/s (2x XAUI) (CEI)</td>
<td>3.125 GHz</td>
<td>9.375 GHz</td>
<td>15.625 GHz</td>
</tr>
<tr>
<td>6.4 Gb/s (Front Side Bus)</td>
<td>3.2 GHz</td>
<td>9.6 GHz</td>
<td>16.0 GHz</td>
</tr>
<tr>
<td>8.0 Gb/s (Front Side Bus)</td>
<td>4.0 GHz</td>
<td>12.0 GHz</td>
<td>20.0 GHz</td>
</tr>
<tr>
<td>8.0 Gb/s (PCI-Express 3.0)</td>
<td>4.0 GHz</td>
<td>12.0 GHz</td>
<td>20.0 GHz</td>
</tr>
</tbody>
</table>

- GHz bandwidth performance ensures optimal signal integrity
- Ensures complete testing of design margins
- Tektronix DSA72004 is the only 20 GHz real-time scope to support next generation signal capture to the 5th harmonic

**Measurement System Bandwidth Required**

<table>
<thead>
<tr>
<th>DUT Signal Rise/Fall time (20%-80%)</th>
<th>10% Accuracy</th>
<th>5% Accuracy</th>
<th>3% Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 ps</td>
<td>8.0 GHz</td>
<td>9.6 GHz</td>
<td>11.2 GHz</td>
</tr>
<tr>
<td>40 ps</td>
<td>10.0 GHz</td>
<td>12.0 GHz</td>
<td>14.0 GHz</td>
</tr>
<tr>
<td>30 ps</td>
<td>13.3 GHz</td>
<td>16.0 GHz</td>
<td>18.7 GHz</td>
</tr>
<tr>
<td>20 ps</td>
<td>20 GHz</td>
<td>24 GHz</td>
<td>28 GHz</td>
</tr>
</tbody>
</table>
Instrument Selection for High Speed Serial Data

- **5th Harmonic Performance**
  - 30ps transition times up to 10Gb/s
    - 20GHz scope is sufficient

- **Four Channel Sample Rate**
  - Emerging Standards will make this a requirement
  - ‘Dual Port’ on PCI-E and QuickPath for example
  - DisplayPort x4 Bus

- **1 Million UI Jitter Requirement**
  - Jitter numbers do not converge with short records unless multiple phase continuous acquisitions are taken
  - 1 Million UI gives 1ps repeatability

- **Equalization/Filtering/DFE**
  - Electrical Reference Receivers

- **Signal Access and Probing**
  - Low loading
  - Common Mode/Differential

> 5Gb/s Signals
Tektronix Arbitrary Filter Design

- Virtual Test Points
  - Channel embed/de-embed
  - Fixture/cabling removal
  - Probe inaccessible test points

- Noise reduction (Bandwidth Dial)

- Continuous Time Linear Equalizer (CTLE)

hc(t) \rightarrow \text{MyFilter.flt}
USB3.0 Transmitter Compliance Example

- Compliance Pattern (near end) with reference channels (FrontPanel, Cable)
  - Eye closed at ‘Far End’
- Rx Equalizer (CTLE converted to FIR Filter)
  - Provides almost 8 dB boost around 4 GHz

![Diagram of the transmission channel setup with reference channels and measurement tool.](image1)

![Graph showing frequency response and eye diagram before and after CTLE.](image2)
TriMode Probing

- TriMode, with a single probe-DUT connection, allows:
  - Traditional differential measurements: V+ to V-
  - Independent single ended measurements on either input
    - V+ with respect to ground
    - V- with respect to ground
  - Direct common mode measurements: \((V+) + (V-)/2\) with respect to ground

- Serial Data standards such as PCI Express, Serial ATA, etc require both differential and maximum permissible common mode voltage limit measurements. Requires two separate probes – Until Now!
Before TriMode Probing
1 Probe for Differential
2 Probes for SE and Common Mode
or
1 Probe Soldered and Re-soldered 3 times
2 Probes for Common Mode

After TriMode Probing
1 Probe and 1 setup for Differential, SE and Common Mode
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High Speed Serial Interconnect: Loss

The faster the data rate and the longer the Interconnect, then the more loss in the signal

Clean, open, logical 1 & 0 at launch from transmitter

Smeared edges at end of long interconnect. Logical 1 & 0 can be hard to distinguish at end of long interconnects; (this is often called a "closed eye")

Fast, sharp, edges at transmitter launch

Reference Maxim Note HFDN-27.0 (Rev. 0, 09/03)
High Speed Serial: Crosstalk
In many cases there are multiple “Lanes” of serial data

Serial data can be a single differential signal…

…but generally there are multiple “lanes” of serial data running side by side; these can CROSSTALK with each other.
Jitter Defined

- What is jitter?
  - ITU Definition of Jitter: “Short-term variations of the significant instants of a digital signal from their ideal positions in time”

*Jitter is a major signal integrity problem at high speed data rates*
Jitter is caused by many things…

- **Thermal noise**
  - Generally Gaussian
  - External radiation sources
  - Like background conversations…random and ever changing

- **Injected noise (EMI/RFI) & Circuit instabilities**
  - Usually a fixed and identifiable source like power supply and oscillators
  - Will often have harmonic content
  - Transients on adjacent traces
  - Cabling or wiring (crosstalk)

- **PLL’s problems**
  - Loop bandwidth (tracking & overshoot)
  - Deadband (oscillation / hunting)

- **Transmission Losses**
  - There is no such thing as a perfect conductor
  - Circuit Bandwidth
  - Skin Effect Losses
  - Dielectric Absorption
  - Dispersion – esp. Optical Fiber
  - Reflections, Impedance mismatch, Path discontinuities (connectors)
Random Jitter

- Jitter of a random nature has Gaussian distribution
- Histogram (estimate) ↔ pdf (mathematical model)
- Peak-to-Peak = … unbounded!
Deterministic Jitter

- Deterministic jitter has non-Gaussian distribution and is bounded.
- Histogram = pdf (close enough)
Periodic Jitter

- TIE vs. time is a repetitive waveform
- Equivalent to Frequency Modulation (FM)
Duty Cycle Distortion

- Asymmetrical rise-time vs. fall-time
- Non-optimal choice of decision threshold

Well, ALMOST never a dual-Dirac histogram!
Inter-Symbol Interference

- ISI or DDj or PDj – used interchangeably
- How a pattern effects subsequent bits
  - Due to transmission line effects, reflections, etc.
**DDJ – Data Dependent Jitter**

- **Other Causes?**
  - State Dependent DDJ
    - FPGA Design
    - FPGA Power Dist.
    - Board Power Dist.
  - Pattern Dependent DDJ
    - ISI
    - Reflections
  - Sub Rate DDJ
    - Clock Multipliers
    - Serializers

- *This list is just to get you thinking, and is by no means intended to be complete…*
Bit Error Rate (BER), Total Jitter (Tj)

- **BER: Bit Error Rate/Ratio**
  - Method to describe expected or measured data stream error rate or ratio of good bits to bad bits.
  - Example: In $10^{12}$ Bits, only one error is allowed => BER = $10^{12}$

- **Total Jitter (Tj)**
  - Jitter at a specified BER to describe expected or measured data stream error rate or ratio of good bits to bad bits.
  - Tj is generally known as “Jitter @ BER”
  - Example: Tj @ $10^{12}$ => The total jitter measured at $10^{-12}$ bit error ratio
Real-Time Rj/Dj in a Nutshell

- Start with
  - TIE
  - PLL TIE

- Perform FFT
  - Determine frequency and pattern rate
  - Sum pattern related bins
  - Sum unrelated periodic bins
  - Measure RMS of remaining bins
  - Estimate BER
Total Jitter @ BER

pdf: \( T_j = D_j \otimes R_j \) (convolution)

option b: \( Pk-Pk: T_j = (N \times R_j) + D_j \), where \( N \) is a factor for BER …
Real World

- Sometimes the BER of a communications link is limited by just Jitter *(horizontal problems)*
  - Jitter separation leads to insight into root cause
  - BER extrapolations and bathtub curves can be accurately calculated

- Sometimes it is **noise** that dominates the BER *(vertical problems)*
  - Jitter separation provides very little insight into root cause of BER performance

- Often it is limited by both Jitter and Noise
  - Jitter separation provides only a limited answer
Signal Analysis

Jitter Analysis

- Jitter measurement provides basis for bit error rate performance.
- Assure that signal acquisition does not significantly contribute to measured jitter.
- Jitter measurement must be made per specification – methods vary from one spec to the next. Use of proper record length, test data patterns, and clock recovery techniques critical.
- Additional jitter analysis tips and insights at [www.jitter360.com](http://www.jitter360.com)
**What tool can measure which Jitter?**

<table>
<thead>
<tr>
<th>Time Interval Error</th>
<th>Cycle-to-Cycle</th>
<th>Period</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Real-Time Oscilloscope</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Characterization and analysis of serial data jitter, clock sources, PLLs, etc.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Limitations are Frequency (or Bit Rate), Resolution (of spectra, of minute jitter, of multi-level modulation)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Real-Time Spectrum Analyzer</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Excels with complex modulations for mobiles.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Clocks, PLLs and their dynamic performance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Limitations include Span (sub-100 MHz), and bandwidth (below 10 GHz), signals with great modulation spectrum</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Equivalent-time Sampling Oscilloscope</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Best bandwidth for serial data.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Limitations include no real-time capture – repetitive patterns only, some jitter spectra aliased.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Demo: Jitter Best Practices
Setting up the scope for accurate results
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High Speed Serial Technology Deployment Timeline

- Specification Development (Promoters Group)
  - Spec v0.5
  - Test Equipment Support
  - Methods of Implementation (MOI)
- Specification Feedback/Review (Contributors Group)
  - Spec v1.0
- Logo License & Administration
  - Authorized Test Centers
SATA Compliance Testing Requirements

- Compliance measurement details outlined in “Methods of Implementation” (MOIs)

<table>
<thead>
<tr>
<th>Number of Tests</th>
<th>Performance/Complexity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gen 1</td>
<td>50</td>
</tr>
<tr>
<td>Gen 2</td>
<td>100</td>
</tr>
<tr>
<td>Gen 3 (Est)</td>
<td>150</td>
</tr>
</tbody>
</table>

This test is performed once at fastest data rate for the device.

**Test pattern(s):**
- HFTP (SSC ON)

**SATA usage model:**
- 1.5 Gbps and 3 Gbps (Gen1 and Gen2 respectively)

40 us/div (>10 SSC periods), 25 pA/pV

Record min, max frequency from results overview.
Calculate deviation: \(\frac{(\text{Nominal} - \text{Measured Mean Max Period})/\text{Nominal}}{1 \times 10^6}\) ppm.

No greater than -5000 to 5000 assuming (Nominal – Measured Max Period)/Nominal * 1e6 ppm
Compliance Testing – An *Industry* Productivity Issue

- Greater speed means greater design complexity, necessitating…

- Greater test complexity
  - More instruments, configurations, and setup time

- More tests
  - Highly specialized – e.g., SSC modulation analysis, advanced receiver testing.

- Requires highly experienced, senior users

- Can require days to perform standards compliance tests

“Banner specs are no longer the gating issue. The latest equipment provides ample raw performance. What’s needed is greater ease of use and automation.”

- Customer feedback
TekExpress® - A New Era in Standards Automation

### SIMPLE
- One-button automation
- No test script customization required
- Auto recognizes test instrumentation in local topology

### EFFICIENT
- Reduces elapsed test time
- Eliminates need for senior engineers to perform tests
- Tests run unattended
- Produces reports for compliance certification

### COMPLETE
- 100% Automation of test methods of implementation (MOI)
- Transmitter and Receiver Testing
- NI TestStand enables integration with other lab control needs
Debug and Compliance Tools

DPOJET Jitter And Eye Diagram Analysis (opt. DJA)
Eye diagram, jitter, and timing analysis for real-time oscilloscopes

DDR Memory Bus Analysis (opt. DDRA)
DDR1, LP-DDR1, DDR2, DDR3 and GDDR3 read/write qualification, debug and compliance of JEDEC measurements

DisplayPort Compliance Test Solution (opt. DSPT)
Four lane simultaneous testing, detailed test report, and margin analysis

DVI Compliance Test Solution (opt. DVI)
Automated DVI testing based on objective pass/fail detection

Ethernet Compliance Test Solution (opt. ET3)
Full PHY layer support for Ethernet variants 10BASE-T, 100BASE-TX, and 1000BASE-T

FB-DIMM Compliance Test Solution (opt. FBD)
Receiver, Transmitter and Reference clock compliance test points as per FB-DIMM standards
Debug and Compliance Tools (cont’d)

HDMI Compliance Test Solution (opt. HT3)
CTS1.2 and 1.3 Source, Cable or Sink solution

PCI Express Compliance Test Solution (opt. PCE)
Rev 1.0/1.1/2.0 CEM and System test points including Dual Port method

SATA and SAS Analysis Solution (opt. SST)
Analysis and debug of SATA/SAS transmitters and receivers

TekExpress® SATA Automated Compliance Test Software
Automated testing for SATA Gen1 and SATA Gen2 defined test suites

USB2.0 Compliance Test Solution (opt. USB)
USB compliance testing including automated probe deskew

Ultra Wideband Spectral Analysis Software (opt. UWB)
WiMedia PHY Test Spec 1.2 Analysis
High Speed Serial Test Challenges

- Design
- Verification
- Compliance Test

- Simulation
  - System Integration
    - Digital Validation & Debug
  - Transmitter Test
    - Eye and Jitter Analysis
    - Characterization & Validation
  - Interconnect Test & Link Analysis

- Data Link Layer
  - Data Link Analysis
    - Digital validation & Debug
  - Receiver Test
    - Compliance Testing

- Physical Layer
  - Transaction Layer
  - Logical Sub-block
  - Electrical Sub-block
Serial Data Debug and Validation Summary

- Pressures of cost, design and layout simplicity have made advances in bit-rates even more complex.

- The incredible complexity of systems today mandate a list of measurements for compliance which regularly number in the hundreds of tests.

- A generation of measurement tools has followed the evolution of serial architectures, giving you better tools for accelerated testing and to help you with serial measurement and compliance challenges.