Simplifying Validation and Debug of USB 3.0 Designs
- Tektronix USB Testing Solutions Introduction
Agenda

• Introduction
• USB 3.0 SuperSpeed
  – Why USB 3.0?
  – Timeline
  – Cable
  – Transmitter
  – Receiver
  – Protocol analysis
• USB 2.0
  – Introduction
  – Compliance Testing
• Wireless USB
  – Overview
  – Compliance and Debug

Disclaimer: The material and content that describes specific details of the USB 3.0 specification (and SuperSpeed logo) belong to the USB 3.0 Promoters. Tektronix is not speaking or presenting on behalf of the USB 3.0 Promoters.
USB Industry Leadership

- Tektronix 1st to market for USB 2.0
- Only approved Method of Implementation (MOI) for WiMedia PHY Leadership in USB
- Millions of certified products shipped, enabled by Tektronix USB solutions
- Tektronix is only T&M Technical Contributor in the USB 3.0 specification!
Why SuperSpeed USB?

- USB 2.0 is adequate for many products…
- Emerging applications will benefit from higher performance.
- Something faster is needed for large digital multi-media files.

**Products Requiring SuperSpeed USB**

- Source: iSuppli Corp. / Oct. 2006

**User wait time requirement is 1 1/2 minutes to synchronize**

<table>
<thead>
<tr>
<th></th>
<th>Song/Pic</th>
<th>256 Flash</th>
<th>USB Flash</th>
<th>SD Movie</th>
<th>USB Flash</th>
<th>HD Movie</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB 1.0</td>
<td>4 MB</td>
<td>5.3 sec</td>
<td>5.7 min</td>
<td>22 min</td>
<td>2.2 hr</td>
<td>5.9 hr</td>
</tr>
<tr>
<td>USB 2.0</td>
<td>256 MB</td>
<td>0.1 sec</td>
<td>8.5 sec</td>
<td>33 sec</td>
<td>3.3 min</td>
<td>8.9 min</td>
</tr>
<tr>
<td>USB 3.0</td>
<td>1 GB</td>
<td>0.8 sec</td>
<td>3.3 sec</td>
<td>20 sec</td>
<td>53.3 sec</td>
<td>70 sec</td>
</tr>
</tbody>
</table>

**Flash Application Demand 2010**

Source: USB-IF
USB 3.0 Technology Timeline & Tektronix Involvement

<table>
<thead>
<tr>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spec Release</td>
<td>Test Vendor Compliance Group Participation</td>
<td>Pil (Peripheral Interop Lab)</td>
<td>Deployment Phase</td>
</tr>
<tr>
<td>Spec Development</td>
<td>Product Development</td>
<td>USB-IF Plugfests</td>
<td></td>
</tr>
<tr>
<td>Silicon Phase</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Tektronix Test Solution Updates
- Chapter 5 - Cable
- Chapter 6 - Transmitter, Receiver, Channel
- Chapter 7 - Protocol (Partner Solution)
USB-IF Platform Interoperability Lab (PIL) Collaboration

- The PIL is available for USB developers to test host and device interoperability and ensure that devices perform correct USB 3.0 electrical and link level signaling
- Tektronix is located less than 10 miles from the PIL
- Tektronix will work with you at the PIL or local Tektronix Technology Centers
  - Contact your local Tektronix representative to schedule an appointment
High Speed Serial Test Challenges

- Design
- Verification
- Compliance Test

- System Integration
  - Digital Validation & Debug

- Data Link Analysis
  - Digital Validation & Debug

- Transmitter Test
  - Eye and Jitter Analysis
  - Characterization & Validation

- Receiver Test

- Compliance Testing

- Interconnect Test & Link Analysis

- Transaction Layer
- Data Link Layer
- Physical Layer
  - Logical Sub-block
  - Electrical Sub-block

Diagram with signal flow from Tx to Rx through path.
Differences from High-Speed Electricals

- **High-Speed**
  - 480MT/s
  - No-SSC
  - 2 wires for signaling
    - Tx and Rx use the same wire
    - 1 bi-directional link
  - DC coupled bus
  - NRZ encoding

- **SuperSpeed**
  - 5.0GT/s (10X speed increase)
  - SSC is required
  - 4 wires for signaling
    - 2 for Tx and 2 for Rx
    - Each Uni-directional
  - AC Coupled bus
  - 8b/10b Encoded (Scrambling)
USB 3.0 Key Considerations

- Receiver testing now required
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues

- Channel considerations
  - Need to consider transmission line effects
  - Software channel emulation for early designs

- New Challenges
  - 12” Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx

- Test strategy
  - Cost-effective tools
  - Flexible solutions

Figure 6-1. Super Speed Block Diagram: Physical

Source: USB 3.0 Rev 1.0 Specification
Connecting to the Device Under Test

- For Host Tx/Rx Testing
  - A Plug
  - B Receptacle + Short USB3 Cable
- For Device Tx/Rx Testing
  - A Receptacle + Short USB3 Cable
- For Cable Testing
  - A Receptacle
  - B Receptacle
  - USB 2.0 for X-Talk
- For De-Embed
  - A Receptacle mated with A Plug

World’s Only Plug Style Fixture!

Manufactured on single flat
Fixture Considerations

- Acquire signal as close to the Silicon/Connector
- Host Testing
  - A Plug
  - B Receptacle + Short USB3 Cable
- Device Testing
  - A Receptacle + Short USB3 Cable
- 13cm Cable Adds Error!
  - 7% Amplitude Loss
  - 500fs Rj
  - 2.5ps Dj
USB Characterization and Debug

Beyond Compliance

- USB 3.0 specification has informative measurements
  - Measurements at silicon pads
  - AC/DC parametric, common-mode measurements
- Complete link analysis with custom equalization functions
- De-embed fixture for accurate results
- Model channel and cable beyond required compliance reference channels
  - Worst case channel analysis
  - Cascading of S-Parameters for various interconnect topologies
- Equipment considerations
Informative Transmitter Measurements

- Measurement at Transmitter Pads Requires Tx Channel DeEmbed

**Table 6-10. Transmitter Normative Electrical Parameters**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>3.0 GTS</th>
<th>Units</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vs</td>
<td>Unit interval</td>
<td>199.94 (min)</td>
<td>200.96 (max)</td>
<td>ps</td>
</tr>
<tr>
<td>Voffset</td>
<td>Differential p-p Tx voltage swing</td>
<td>0.8 (min)</td>
<td>1.2 (max)</td>
<td>V</td>
</tr>
<tr>
<td>Vde-emphasis</td>
<td>Tx de-emphasis</td>
<td>3.0 (min)</td>
<td>4.0 (max)</td>
<td>dB</td>
</tr>
<tr>
<td>Rts/psoc</td>
<td>DC differential impedance</td>
<td>72 (max)</td>
<td>120 (max)</td>
<td>Ω</td>
</tr>
<tr>
<td>Vtrans/detect</td>
<td>The amount of voltage change allowed during Receiver Detection</td>
<td>0.5 (max)</td>
<td>V</td>
<td>Detected voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an “off” receiver’s input goes below ground. See Section 1.2.5.6 and Table 6.10 for details.</td>
</tr>
<tr>
<td>Ccoupling</td>
<td>AC Coupling Capacitor</td>
<td>75 (min)</td>
<td>200 (max)</td>
<td>nF</td>
</tr>
<tr>
<td>Tskewmax</td>
<td>Max skew rate</td>
<td>10</td>
<td>ns/ptc</td>
<td>See the jitter white paper for details on this measurement.</td>
</tr>
</tbody>
</table>

**Table 6-11. Transmitter Informative Electrical Parameters at Silicon Pads**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>3.0 GTS</th>
<th>Units</th>
<th>Normative</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tskew</td>
<td>Deterministic min pulse</td>
<td>0.95</td>
<td>Vs</td>
<td></td>
<td>Tx pulse width variation that is deterministic.</td>
</tr>
<tr>
<td>Tskew/detect</td>
<td>Tx min pulse</td>
<td>0.90</td>
<td>Vs</td>
<td></td>
<td>Min Tx pulse at 10^-12 including E1 and R.</td>
</tr>
<tr>
<td>Pre</td>
<td>Transmitter Eye</td>
<td>0.625 (max)</td>
<td>UI</td>
<td>Includes all jitter sources.</td>
<td></td>
</tr>
<tr>
<td>Pre</td>
<td>Tx deterministic jitter</td>
<td>0.19 (max)</td>
<td>UI</td>
<td>Deterministic jitter only assuming the Dual Dirac Distribution.</td>
<td></td>
</tr>
<tr>
<td>Closs</td>
<td>Tx input capacitance for return loss</td>
<td>1.25 (max)</td>
<td>pf</td>
<td>Parasitic capacitance to ground</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 6-4. Channel Models without Cable (Top) and with Cable (Bottom)**

**Source: USB 3.0 Rev 1.0 Specification**
Accurate Transmitter Characterization

Channel De-Embedding

• Measure true representation of signal at the Tx output
  – Characterize channel with TDR or Simulator
  – Import S-Parameter file
  – Create fixture de-embed filter with SDLA software

• Identify root cause failures
  – Removes fixture effects
  – Improved margin
USB Channel Modeling

- Understand transmitter margin given worst case channels
- Model channel and cable combinations beyond compliance requirements
- Easily create interconnect models with SDLA software to analyze channel effects

Figure 6-14. Tx Normative Setup with Reference Channel

USB-IF HW Channel Prototypes
Custom Equalization Analysis

- Equalizer models
  - Pole, Zero, and Frequencies for Continuous Time Linear Equalizer (CTLE)
  - Feed-Forward (FFE) and Decision-Feedback (DFE) Equalizers

\[ H(s) = \frac{A_{dc} \omega_1 \omega_2}{\omega_z} \frac{s + \omega_z}{(s + \omega_1)(s + \omega_2)} \]

- \( A_{dc} = 0.667 \)
- \( \omega_z = 2\pi(650 \times 10^6) \)
- \( \omega_1 = 2\pi(1.95 \times 10^9) \)
- \( \omega_2 = 2\pi(5 \times 10^9) \)
Transmitter Compliance Testing (Normative Testing)

Channel Embedding

- Measurements at TP1
- HW Channel Probed at TP1
  - CTLE applied in SW
- SW Channel Probed at TP2
  - CTLE combined with Channel

6.7.2 Transmitter Eye

The eye mask is measured using the compliance data pattern CD1 described in Section 6.4.4. Eye Height is measured from 10^8 UI. Jitter is extrapolated from 10^9 UI to 10^12.

Table 6-12. Normative Transmitter Eye Mask

<table>
<thead>
<tr>
<th>Signal Characteristic</th>
<th>Minimal</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Units</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Height</td>
<td>100</td>
<td>1200</td>
<td>mV</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Dc</td>
<td>93</td>
<td>ps</td>
<td>1.23</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rj</td>
<td>60</td>
<td>ps</td>
<td>1.23</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tj</td>
<td>132</td>
<td>ps</td>
<td>1.23</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Measured over 10^8 UI and extrapolated to 10^{-9} BER
2. Measured after receiver equalization function
3. Measured at end of reference channel and cables at TP1 figure 6-14

Figure 6-4. Channel Models without Cable (Top) and with Cable (Bottom)
Complete USB 3.0 Transmitter Solution

DPO/DSA70000B Series Oscilloscopes

- Tektronix Super Speed USB Fixtures
- 12.5 GHz Real-Time Scope
  - 5th Harmonic Performance
  - 50GS/s Sample Rate
  - P7313SMA Differential Probe (Optional)
- Analysis software for validation and debug
  - Serial Data Link Analysis SW (Optional)
  - DPOJET with option USB3
- Automation software for characterization and compliance
  - TekExpress with option USB-TX

TF-USB3-AB-KIT
Normative Receiver Tolerance Test

- SSC Clocking is enabled
- BER Test is performed at $10^{-10}$
- De-Emphasis Level is set to -3dB
- Voltage Level is set to 0.75V
- Each SJ term in the table below is tested one at a time after the device is in loopback mode

<table>
<thead>
<tr>
<th>Frequency</th>
<th>SJ</th>
<th>RJ</th>
</tr>
</thead>
<tbody>
<tr>
<td>500kHz</td>
<td>400ps</td>
<td>2.42ps</td>
</tr>
<tr>
<td>1MHz</td>
<td>200ps</td>
<td>2.42ps</td>
</tr>
<tr>
<td>2MHz</td>
<td>100ps</td>
<td>2.42ps</td>
</tr>
<tr>
<td>4.9MHz</td>
<td>40ps</td>
<td>2.42ps</td>
</tr>
<tr>
<td>50MHz</td>
<td>40ps</td>
<td>2.42ps</td>
</tr>
</tbody>
</table>
Normative Receiver Testing

- Receiver processes the BERT Ordered Sets using ‘built-in BERT’ feature
- Impairment at TP1
- HW Channel Attached at TP1
- SW Channel Attached at TP2

6.7.4.1 Loopback BERT

During loopback, the receiver processes the BERT ordered sets BRST, BDAT, and BERC. These ordered sets are given in Table 6-14 through Table 6-17. BRST and BDAT are looped back as received. BERC ordered sets are not looped back but are replaced with BCNT ordered sets. Anytime a BRST is received, the error count register EC is set to 0 and the scrambling LFSR is set to 0xFFFFh. Any number of consecutive BRST ordered sets may be received.

BRST followed by BDAT starts the bit error rate test. BDAT sequence is the output of the scrambler and is equivalent to the logical idle sequence. It consists of scrambled 0 as described in Appendix B. As listed in Appendix B, the first 16 characters of the sequence are reprinted here:

| FF | 17 | C0 | 14 | D2 | E7 | D2 | 62 | 72 | 8E | 28 | A6 | BE | 8D | 6F | 8D |

The receiver must compare the received data to the BDAT sequence. Errors increment the error count register (EC) by 1. EC may not rollover but must be held at FFFFh. The LFSR, as advanced once for every character except SKPs. The LFSR rolls over after 2^16 symbols. SKPs inserted or deleted as necessary for clock tolerance compensation.
Receiver Testing MOI (with SW Channel Emulation)

If DUT supports ‘Loopback BERT’

• Sequence for Initiating Loopback BERT
  – Ping.LFPS > TSEQ > TS1 > Loopback
  – BRST > Scrambled D0.0 > BERC
  – Direct Synthesis of Signal Impairments
  – Decode ‘BERC’ Signal with Scope
Receiver Test MOI (with SW Channel Emulation)

If DUT does not support ‘Loopback BERT’

- Ping.LFPS > TSEQ > TS1 > Loopback
- BRST > Scrambled D0.0 > BERC
- Direct Synthesis of Signal Impairments
- Protocol Analyzer Counts Symbol Errors

Diagram showing the setup:

- Host
- DUT
- AWG7122B
- Ellisys 280T
- USB3_Tx
- USB3_Rx
- TP2
- Rx Channel

Counts Symbol Errors

Channel ISI
SSC
Rj
Sj
Custom SSC

SerialXpress SW
SSC Slew Rate

+ df/dt  - df/dt

minimum duration df/dt

position of df/dt peak

nominal period

x %

100 %
Receiver Compliance & Margin Testing

• Early Market Automated Test Solution

Table 6.19. Input Jitter Requirements for Rx Tolerance Testing

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>f1</td>
<td>Tolerance corner</td>
<td>4.9</td>
<td>MHz</td>
</tr>
<tr>
<td>J0</td>
<td>Random jitter</td>
<td>0.0121</td>
<td>UI</td>
</tr>
<tr>
<td>J0_{pp}</td>
<td>Random Jitter peak-peak at 10^{12}</td>
<td>0.17</td>
<td>UI p-p</td>
</tr>
<tr>
<td>J1_{sin}</td>
<td>Sinusoidal Jitter</td>
<td>2</td>
<td>UI p-p</td>
</tr>
<tr>
<td>J1_{sin}</td>
<td>Sinusoidal Jitter</td>
<td>1</td>
<td>UI p-p</td>
</tr>
<tr>
<td>J2_{sin}</td>
<td>Sinusoidal Jitter</td>
<td>0.5</td>
<td>UI p-p</td>
</tr>
<tr>
<td>J3_{sin}</td>
<td>Sinusoidal Jitter</td>
<td>0.2</td>
<td>UI p-p</td>
</tr>
<tr>
<td>J4_{sin}</td>
<td>Sinusoidal Jitter</td>
<td>0.2</td>
<td>UI p-p</td>
</tr>
<tr>
<td>\text{V}_{\text{full swing}}</td>
<td>Transition bit differential voltage swing</td>
<td>0.75</td>
<td>V p-p</td>
</tr>
<tr>
<td>\text{V}_{\text{EQ level}}</td>
<td>Non transition bit voltage (equalization)</td>
<td>-3</td>
<td>dB</td>
</tr>
</tbody>
</table>

ATE (Automated Test for Excel)

USB-1F DevCon Demo - Tokyo, Japan May 20th, 2009 - NEC Electronics Booth
Tx/Rx MOI (with HW Channel Emulation)

- USB-IF ‘Compliance Channel’
- Same HW Configuration

Long Return Path a problem for External Analyzers
USB 3.0 Tx/Rx Test Equipment Considerations

- **AWG & RT Scope**
  - **Simplified Setup**
    - 2 Instruments, add Protocol Analyzer for system level test
    - 1 Fixture, 4 Cables, 4 Connectors
    - AWG7122B (Opt. 06, 08)
  - **RX Tolerance Testing**
    - Supports Silicon, Host/Device per the USB 3.0 Specification
  - **Flexible Signal Impairment Generation**
    - All required impairments are generated with the AWG using Direct Synthesis
    - Precise ISI generation for channel emulation

- **BERT & RT Scope**
  - **Complex Setup**
    - 6 Instruments, add Protocol Analyzer for system level test
    - 1 Fixture, 35 Cables/Connectors
    - BERT HW + External impairment sources
  - **RX Tolerance Testing**
    - Synchronous Clock Required, BERT method not suitable for system/device test
  - **Impairment Capabilities Limited by Hardware**
    - SSC and Sj require external equipment
    - ISI generation limited by Hardware Channels
Key Advantages of the AWG for USB Receiver Testing
AWG7000B Arbitrary Waveform Generators with SerialXpress®

- Flexibility to support all signal impairments required for jitter tolerance testing
- Model real-world complexities of SSC profiles to avoid system interoperability issues
- No tradeoffs between any signal impairments - No limitations in generating SSC and SJ at the same time
- Multiple SJ tones can be generated at one time
- Flexible ISI generation enables customers to test ISI models that exceed the test specification
  - No need to wait for USB hardware compliance channels
- Minimize time needed for re-cabling
- Improved repeatability and portability of Receiver test configurations with setup files
Cable Testing

DSA8200 Sampling Oscilloscope with IConnect®

- Test Fixtures
  - A Receptacle
  - B Receptacle
  - USB2/USB3 Connectors Available for Crosstalk measurements
- Using Sampling Oscilloscope & S-Parameter SW
- Measurements:
  - Impedance
  - Intra-Pair Skew
  - Differential Insertion Loss
  - Differential Return Loss
  - Differential Near-End Crosstalk
  - Differential Crosstalk between USB3.0 and USB2.0 Pairs
  - Differential to CM Conversion
Tektronix Partner Solution

Ellisys EX280 Explorer- USB 3.0 Analyzer/Exerciser

- Analyzer Applications
  - USB host & device monitoring
  - Performance analysis
  - Debug of drivers & software stacks
  - Link state analysis
  - Protocol errors checks

- Generator Applications
  - USB host & device emulation
  - Testing error recovery mechanisms
  - Performance stress testing
  - Compliance verification
  - Link state analysis

www.ellisys.com
USB 2.0 Compliance

Signal Quality
- Eye-Diagram testing
- Signal Rate
- End of Packet Width
- Cross-over voltage range (for LS and FS)
- JK jitter
- KJ jitter
- Consecutive jitter
- Monotonicity test (for HS)
- Rise and Fall times

Timing Measurements
- Packet Parameters
- Suspend
- Resume
- Reset from High-Speed
- Reset from Suspend
Tektronix Wireless USB Validation Solution

- Easy to setup: Automatically detect Time Frequency Codes (TFCs) and data rates from the RF waveform header
- Demodulate, Analyze and Record measurements of each packet independently
- Perform Measurements Outlined in the Wireless USB EVM Test Specification
- Industry’s only MOI (Method of Implementation) for WiMedia test!
  - WUSB EVM test is a subset of WiMedia PHY certification
Tektronix USB Solution

**Complete solution:** from PHY layer to Protocol for USB 2.0, 3.0 and Wireless USB (Only approved Method of Implementation (MOI) for WiMedia PHY Leadership in USB)

**Cost Effective:** Automation with a single box solution

**Connectivity:** Measure closest to Tx output for true performance of USB 3.0 device/host

**Flexibility:** Compliance, debug, characterization with software channel emulation

**USB leadership:**
1. Tektronix 1st to market for USB 2.0
2. Tektronix is active in USB-IF Compliance Group and USB 3.0 PIL and contributes to USB 3.0 specification (only T&M Technical Contributor in the USB 3.0 specification)
Resources

- Access to Specifications
  - Rev 1.0, http://www.usb.org/developers/docs/

- Tektronix USB Electrical PHY Tools
  - www.tektronix.com/usb
  - www.tektronix.com/software

- Ellisys Protocol Tools
  - www.ellisys.com
Enabling Innovation in the Digital Age

Accelerating Performance
Enabled by High-speed Serial Technologies