

Service Manual



HFS 9009 Stimulus System

070-8366-03

Warning

The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

Copyright © Tektronix, Inc. 1991, 1994. All rights reserved.

Tektronix products are covered by U.S. and foreign patents, issued and pending. Information in this publication supercedes that in all previously published material. Specifications and price change privileges reserved.

Printed in the U.S.A.

Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070-1000

TEKTRONIX and TEK are registered trademarks of Tektronix, Inc.

WARRANTY

Tektronix warrants that this product will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If any such product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; or c) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

THIS WARRANTY IS GIVEN BY TEKTRONIX WITH RESPECT TO THIS PRODUCT IN LIEU OF ANY OTHER WARRANTIES, EXPRESSED OR IMPLIED. TEKTRONIX AND ITS VENDORS DISCLAIM ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. TEKTRONIX' RESPONSIBILITY TO REPAIR OR REPLACE DEFECTIVE PRODUCTS IS THE SOLE AND EXCLUSIVE REMEDY PROVIDED TO THE CUSTOMER FOR BREACH OF THIS WARRANTY. TEKTRONIX AND ITS VENDORS WILL NOT BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES IRRESPECTIVE OF WHETHER TEKTRONIX OR THE VENDOR HAS ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Table of Contents

General Safety Summary	vii
Service Safety Summary	xi
Specifications	
Nominal Traits	1-1
Warranted Characteristics	1-8
Typical Characteristics	1-11
Operating Information	
Menu Selections	2-1
Resetting the HFS 9009	2-2
Setting the Time Base	2-2
The UNDO Button	2-4
Pulse Output	2-4
Theory of Operation	
Module Descriptions	3-1
Mainframe	3-1
Backplane	3-1
Power Supply	3-1
Fans	3-1
Front Panel	3-1
Cards	3-1
CPU Card	3-2
Time Base Card	3-2
Pulse Generator Cards	3-2
Data Time Generator Cards	3-3
Performance Verification	
Required Test Equipment	4-1
Test Record	4-2
Verification Sequence	4-11
Self Test	4-11
Calibration	4-12
Check Procedures	4-13
Instrument Setup	4-13
Output Level Checks (HFS 9DG1 Card Only)	4-13
Output Level Checks (HFS 9DG2 and HFS 9PG2 Cards Only)	4-16
Output Level Checks (HFS 9PG1 Card Only)	4-19
Trigger Output Level	4-21
Rise Time and Fall Time Checks (HFS 9PG1 and HFS 9DG1 Cards Only)	4-22
Rise Time and Fall Time Checks (HFS 9PG2 and HFS 9DG2 Cards Only)	4-25
Edge Placement Checks	4-27
Frequency Accuracy Check	4-31
Phase Lock Check	4-34

Adjustment Procedures

Adjustments	5-1
--------------------------	------------

Maintenance

Preventive Maintenance	6-1
Removal and Replacement	6-3
Front Panel	6-3
Front Panel Keypad and Encoder Switch	6-3
Display Module	6-4
Top Panel Circuit Board and Trim Bezel	6-5
ON/STANDBY Switch	6-5
Cards	6-6
Mainframe Top Cover	6-7
Power Supply (lower back panel)	6-8
Fans (upper back panel)	6-9
Fan (side panel)	6-9
Troubleshooting	6-11
Power-On Diagnostics	6-11
Kernel-Test Diagnostics	6-11
Controller-Test Diagnostics	6-11
Self-Test Diagnostics	6-11
Self-Test Diagnostics	6-12
Calibration	6-12
Error Indications	6-13
Bit Assignments For Diagnostic LEDs	6-13
Diagnostic Procedure	6-16

Options

Electrical Parts List

Diagrams

Block Diagram	9-1
----------------------------	------------

Mechanical Parts List

Replaceable Parts List	10-1
Parts Ordering Information	10-1
Using the Replaceable Parts List	10-2

List of Figures

Figure 2–1: HFS 9009 Mainframe, Cards, and Front Panel	2–1
Figure 2–2: MAIN MENU, SELECT, and Arrow Button Locations .	2–2
Figure 2–3: Main Menu Display	2–2
Figure 2–4: The Time Base Menu	2–3
Figure 2–5: Mode set to Auto-Burst	2–3
Figure 2–6: Controls and Connectors for the Pulse Generator, Data Generator, and Time Base Cards	2–5
Figure 6–1: Clock Distribution Cable Location	6–6
Figure 6–2: HFS 9009 Power Supply (rear view)	6–8
Figure 6–3: The Location of LEDs on the CPU Card	6–14
Figure 6–4: Bit Assignments for Diagnostic LEDs	6–15
Figure 6–5: Diagnostic Procedure Flowchart	6–17
Figure 9–1: Module Block and Interconnection Diagram	9–2
Figure 10–1: Cabinet	10–5
Figure 10–2: Front Panel	10–7
Figure 10–3: Mainframe and Chassis Parts	10–9
Figure 10–4: Power Supply and Fan Assembly	10–11
Figure 10–5: Circuit Cards	10–13

List of Tables

Table 1–1: Nominal Traits — HFS 9PG1 Output Performance	1–1
Table 1–2: Nominal Traits — HFS 9PG2 Output Performance	1–2
Table 1–3: Nominal Traits — HFS 9DG1 Output Performance	1–3
Table 1–4: Nominal Traits — HFS 9DG2 Output Performance	1–3
Table 1–5: Nominal Traits — Time Base	1–4
Table 1–6: Nominal Traits — Performance to External Frequency Reference	1–4
Table 1–7: Nominal Traits — Output Edge Placement Performance	1–5
Table 1–8: Nominal Traits — Transducer In Performance	1–5
Table 1–9: Nominal Traits — Skew Cal In Performance	1–5
Table 1–10: Nominal Traits — Trigger In Performance	1–6
Table 1–11: Nominal Traits — Trigger Out Performance	1–6
Table 1–12: Nominal Traits — Power Requirements	1–6
Table 1–13: Nominal Traits — System Memory Performance	1–6
Table 1–14: Nominal Traits — HFS 9003 Mechanical	1–7
Table 1–15: Nominal Traits — HFS 9009 Mechanical	1–7
Table 1–16: Warranted Characteristics — HFS 9PG1 Output Performance	1–8
Table 1–17: Warranted Characteristics — HFS 9PG2 Output Performance	1–8
Table 1–18: Warranted Characteristics — HFS 9DG1 Output Performance	1–8
Table 1–19: Warranted Characteristics — HFS 9DG2 Output Performance	1–9
Table 1–20: Warranted Characteristics — Time Base	1–9
Table 1–21: Warranted Characteristic — Performance to External Frequency Reference	1–9
Table 1–22: Warranted Characteristics — Output Edge Placement Performance	1–9
Table 1–23: Warranted Characteristics — Trigger Out Performance	1–10
Table 1–24: Warranted Characteristics — Power Requirements . . .	1–10
Table 1–25: Warranted Characteristics — Environmental and Safety	1–10
Table 1–26: Typical Characteristics — Time Base	1–11
Table 1–27: Typical Characteristics — HFS 9PG1 Output Performance	1–11

Table 1–28: Typical Characteristics — HFS 9PG2 Output Performance	1–12
Table 1–29: Typical Characteristics — HFS 9DG1 Output Performance	1–12
Table 1–30: Typical Characteristics — HFS 9DG2 Output Performance	1–12
Table 1–31: Typical Characteristics — Performance to External Frequency Reference	1–13
Table 1–32: Typical Characteristics — Transducer In Performance	1–13
Table 1–33: Typical Characteristics — Trigger In Performance	1–13
Table 1–34: Typical Characteristics — Trigger Out Performance ..	1–14
Table 1–35: Typical Characteristics — Power Requirements	1–14
Table 4–1: Required Test Equipment	4–1
Table 4–2: Trigger Output Level and Phase Lock Test	4–3
Table 4–3: Test Record for HFS 9DG1 Card	4–4
Table 4–4: Test Record for HFS 9DG2 Card	4–6
Table 4–5: Test Record for HFS 9PG1 Card	4–7
Table 4–6: Test Record for HFS 9PG2 Card	4–9
Table 4–7: HFS 9DG1 Output Level Checks, First Settings	4–14
Table 4–8: HFS 9DG1 Output Level Checks, Second Settings	4–14
Table 4–9: HFS 9DG1 Output Level Checks, Third Settings	4–15
Table 4–10: HFS 9DG1 Output Level Checks, Fourth Settings	4–15
Table 4–11: HFS 9DG2 and HFS 9PG2 Output Level Checks, First Settings	4–17
Table 4–12: HFS 9DG2 and HFS 9PG2 Output Level Checks, Second Settings	4–17
Table 4–13: HFS 9PG2 Output Level Checks, Third Settings	4–18
Table 4–14: HFS 9PG2 Output Level Checks, Fourth Settings	4–18
Table 4–15: HFS 9PG1 Output Level Checks, First Settings	4–19
Table 4–16: HFS 9PG1 Output Level Checks, Second Settings	4–20
Table 4–17: HFS 9PG1 Output Level Checks, Third Settings	4–20
Table 4–18: HFS 9PG1 Output Level Checks, Fourth Settings	4–21
Table 4–19: Settings for Trigger Output Check	4–22
Table 4–20: Settings for Rise Time and Fall Time Checks	4–23
Table 4–21: DSO Settings for Rise/Fall Time Checks	4–24
Table 4–22: Settings for Rise Time and Fall Time Checks	4–25
Table 4–23: DSO Settings for Rise/Fall Time Checks	4–26
Table 4–24: Settings for Edge Placement Checks	4–27
Table 4–25: Lead Delay Limits for HFS 9PG1 and HFS 9PG2	4–28

Table 4-26: Lead Delay Limits for HFS 9DG1 and HFS 9DG2	4-29
Table 4-27: Width Variance Limits for HFS 9PG1	4-29
Table 4-28: Width Variance Limits for HFS 9DG1	4-30
Table 4-29: Width Limits for HFS 9PG1 and HFS 9PG2	4-30
Table 4-30: Width Limits for HFS 9DG1	4-30
Table 4-31: Width Limits for HFS 9DG2	4-31
Table 4-32: Frequency Limits (HFS 9PG1 & HFS 9DG1)	4-32
Table 4-33: Frequency Limits (HFS 9PG2)	4-32
Table 4-34: Frequency Limits (HFS 9DG2)	4-33
Table 6-1: Results from *TST?	6-12
Table 6-2: Troubleshooting From the Error Index Code	6-16

General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

Only qualified personnel should perform service procedures.

Injury Precautions

- | | |
|---|--|
| Use Proper Power Cord | To avoid fire hazard, use only the power cord specified for this product. |
| Avoid Electric Overload | To avoid electric shock or fire hazard, do not apply a voltage to a terminal that is outside the range specified for that terminal. |
| Ground the Product | This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded. |
| Do Not Operate Without Covers | To avoid electric shock or fire hazard, do not operate this product with covers or panels removed. |
| Use Proper Fuse | To avoid fire hazard, use only the fuse type and rating specified for this product. |
| Do Not Operate in Wet/Damp Conditions | To avoid electric shock, do not operate this product in wet or damp conditions. |
| Do Not Operate in Explosive Atmosphere | To avoid injury or fire hazard, do not operate this product in an explosive atmosphere. |

Product Damage Precautions

- | | |
|-----------------------------------|---|
| Use Proper Power Source | Do not operate this product from a power source that applies more than the voltage specified. |
| Provide Proper Ventilation | To prevent product overheating, provide proper ventilation. |

Do Not Operate With Suspected Failures

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Safety Terms and Symbols

Terms in This Manual

These terms may appear in this manual:



WARNING. Warning statements identify conditions or practices that could result in injury or loss of life.



CAUTION. Caution statements identify conditions or practices that could result in damage to this product or other property.

Terms on the Product

These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product

The following symbols may appear on the product:



DANGER
High Voltage



Protective Ground
(Earth) Terminal



ATTENTION
Refer to
Manual



Double
Insulated

Certifications and Compliances

CSA Certified Power Cords CSA Certification includes the products and power cords appropriate for use in the North America power network. All other power cords supplied are approved for the country of use.

Compliances Consult the product specifications for IEC Installation Category, Pollution Degree, and Safety Class.

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone

Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power

To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On

Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This Service Manual provides you with limited service information for the HFS 9009 Precision Pulse Generator.

Use the *Specifications* section as a reference for all nominal, typical, and specified characteristics.

Use the *Operating Information* section to learn about each of the front panel controls and how to input simple settings for basic operation.

Use the *Theory of Operation* section to help you understand the operation of each of the replaceable modules in the HFS 9009.

Use the *Performance Verification* section to verify the specified performance of the instrument.

The *Adjustment Procedures* section lists the adjustment that can be made to the instrument.

Use the *Maintenance* section to learn how to perform general preventive maintenance of the instrument. Removal and replacement and troubleshooting procedures are also described in this section.

The *Options* section lists the options available from the factory. This section also describes the procedure for installing field updates to the internal programmed code of the instrument.

The *Diagrams* section describes and illustrates the major electrical sections of the HFS 9009.

The *Mechanical Parts List* section lists all of the replaceable parts and describes how to order these parts.

Notation Conventions

The following conventions are used in this manual:

- Signal names are printed in bold capital letters; for example, **SENSE IN**.
- A signal active in the low state is shown with a tilde (~) in front of the signal name; for example, **~ACFAIL**.
- Labels of front panel buttons and connectors are shown in bold capital letters; for example, **ENTER**.
- Labels of menu items are shown in mixed case bold text; for example, the Pulse menu **Amplitude** item.

Related Manuals

Refer to the *HFS 9000 User Manual* (070-8365-01) for additional operating information.

Specifications

The HFS 9000 family of high-speed logic signal source instruments have a modular architecture with factory-configurable cards. The channels are digitally synthesized from a common clock resulting in highly accurate independent placement of rising and falling edges. The instruments are optimized for digital device characterization with unique triggering capabilities and a variety of pulse outputs. The product family also features low RMS jitter, the ability to compensate for external cable skews, and an easy-to-use graphical human interface.

This section contains the complete specifications for the HFS 9000 Stimulus System and Modules. These specifications are classified as either nominal traits, warranted characteristics, or typical characteristics.

Nominal Traits

Nominal traits are described using simple statements of fact such as “+2.6 V” for the trait “Maximum high level,” rather than in terms of limits that are performance requirements.

Table 1-1: Nominal Traits — HFS 9PG1 Output Performance

Each channel and complement driving a 50 Ω load to ground, except as noted.

Name	Description
Maximum high level	+2.6 V
Minimum low level	-2.00 V
Maximum amplitude	3.00 V
Minimum amplitude	0.50 V
Level resolution	0.01 V
Operation when terminated through 50 Ω to -2 V	Output levels will be approximately 1 V more negative than the values programmed, specified, and displayed. Actual output levels more negative than -2 V may cause malfunction. Level accuracy specifications do not apply when terminating to -2 V. Both true and complement outputs must be terminated to the same voltage.

Table 1-1: Nominal Traits — HFS 9PG1 Output Performance (Cont.)

Each channel and complement driving a 50 Ω load to ground, except as noted.

Name	Description
Operation when terminated to high impedance loads	Output level range will double until certain internal limits are achieved. Since the programmed, specified, and displayed output levels do not match the actual output levels, level accuracy specifications do not apply when terminating to a high impedance load. Because of the larger voltage swings associated with doubled level range, output transition time specifications do not apply when driving a high impedance load.
Output limits	One high limit and one low limit may be enabled or disabled together.

Table 1-2: Nominal Traits — HFS 9PG2 Output Performance

Each channel and complement driving a 50 Ω load to ground, except as noted.

Name	Description
Maximum high level	+5.50 V
Minimum low level	-2.00 V
Maximum amplitude	5.50 V
Minimum amplitude	0.50 V
Level resolution	0.01 V
Operation when terminated through 50 Ω to -2 V	Output levels will be approximately 1 V more negative than the values programmed, specified, and displayed. Actual output levels more negative than -2 V may cause malfunction. Level accuracy specifications do not apply when terminating to -2 V. Both true and complement outputs must be terminated to the same voltage.
Transition time 20% to 80%	Variable from 800 ps to 5 ns
Transition time resolution	10 ps
Output limits	One high limit and one low limit may be enabled or disabled together.

Table 1-3: Nominal Traits — HFS 9DG1 Output Performance

Each channel and complement driving a 50 Ω load to ground, except as noted.

Name	Description
Maximum high level	+5.0 V
Minimum low level	-2.5 V
Maximum amplitude	3.00 V
Minimum amplitude	0.01 V
Level resolution	0.01 V
Operation when terminated through 50 Ω to -2 V	Output levels will be approximately 1 V more negative than the values programmed, specified, and displayed. Actual output levels more negative than -2 V may cause malfunction. Level accuracy specifications do not apply when terminating to -2 V. Both true and complement outputs must be terminated to the same voltage.
Operation when terminated to high impedance loads	Output level range will double until certain internal limits are achieved. Since the programmed, specified, and displayed output levels do not match the actual output levels, level accuracy specifications do not apply when terminating to a high impedance load. Because of the larger voltage swings associated with doubled level range, output transition time specifications do not apply when driving a high impedance load.
Output limits	One high limit and one low limit may be enabled or disabled together.

Table 1-4: Nominal Traits — HFS 9DG2 Output Performance

Each channel and complement driving a 50 Ω load to ground, except as noted.

Name	Description
Maximum high level	+5.50 V
Minimum low level	-2.00 V
Maximum amplitude	5.50 V
Minimum amplitude	0.01 V
Level resolution	0.01 V
Operation when terminated through 50 Ω to -2 V	Output levels will be approximately 1 V more negative than the values programmed, specified, and displayed. Actual output levels more negative than -2 V may cause malfunction. Level accuracy specifications do not apply when terminating to -2 V. Both true and complement outputs must be terminated to the same voltage.
Transition time 20% to 80%	Variable from 800 ps to 6 ns

Table 1–4: Nominal Traits — HFS 9DG2 Output Performance (Cont.)

Each channel and complement driving a 50 Ω load to ground, except as noted.

Name	Description
Transition time resolution	10 ps
Output limits	One high limit and one low limit may be enabled or disabled together.

Table 1–5: Nominal Traits — Time Base

Name	Description
Frequency range	HFS 9PG1, HFS 9DG1: 50 kHz to 630 MHz HFS 9PG2, HFS 9DG2: 50 kHz to 300 MHz ¹
Frequency resolution	≤ 0.1% of frequency setting
Minimum frequency setting when using half, quarter, or eighth pulse rate modes ²	half pulse rate: 100 kHz quarter pulse rate: 200 kHz eighth pulse rate: 400 kHz
Number of pulse periods in burst or auto-burst modes	User selectable from 1 to 65,536

¹ If the HFS 9PG2 or HFS 9DG2 is operated in half pulse rate mode, frequency can be extended to 600 MHz for the HFS 9PG2 and 630 MHz for the HFS 9DG2.

² All pulse rate modes result in 50 kHz output frequency.

Table 1–6: Nominal Traits — Performance to External Frequency Reference

Name	Description
PHASE LOCK IN input characteristic	0.1 μF DC blocking capacitor followed by 50 Ω termination to ground
Phase lock output frequency range	Any 2 ⁿ multiple or sub-multiple of the phase lock frequency that is within the allowed frequency range for the card being used
FRAME SYNC IN	Initiates a burst when using phase lock mode
FRAME SYNC IN input characteristic	50 Ω terminated to –2 V

Table 1–7: Nominal Traits — Output Edge Placement Performance¹

Name	Description
Channel deskew (Chan Delay) range, channels relative to time zero reference	–60 ns to 2.0 μ s
Channel deskew (Chan Delay) resolution	HFS 9PG1, HFS 9PG2: 5 ps HFS 9DG1, HFS 9DG2: 1 ps
Delay (Lead Delay) adjustment range	Zero to 20 μ s
Delay (Lead Delay, Trail Delay) adjustment resolution	HFS 9PG1, HFS 9PG2: 5 ps HFS 9DG1, HFS 9DG2: 1 ps
Pulse width adjustment range	HFS 9PG1, HFS 9PG2: Zero to (one period – 790 ps) inclusive HFS 9DG1, HFS 9DG2: Zero to (one period \times 65,536) inclusive
Pulse width adjustment resolution	HFS 9PG1, HFS 9PG2: 5 ps HFS 9DG1, HFS 9DG2: 1 ps
Fine knob resolution of timing	5 ps

¹ Measured at 50% levels, each channel independent.

Table 1–8: Nominal Traits — Transducer In Performance

Name	Description
TRANSDUCER IN input characteristic	HFS 9PG1: 1000 pF DC blocking capacitor followed by 50 Ω termination to ground HFS 9PG2: 100 pF DC blocking capacitor followed by 50 Ω termination to ground

Table 1–9: Nominal Traits — Skew Cal In Performance

Name	Description
SKEW CAL IN usage	Calibration use only. No signal, except from a channel OUTPUT connector during the calibration process, should ever be applied to this input.

Table 1-10: Nominal Traits — Trigger In Performance

Name	Description
Input Voltage range	±5 V maximum
Trigger level range	±4.70 V
Trigger level resolution	100 mV

Table 1-11: Nominal Traits — Trigger Out Performance

Name	Description
Pretrigger range, TRIGGER OUT before time zero reference	Zero to 70 ns
TRIGGER OUT pulse width in auto mode	<p>The graph plots pulse width in nanoseconds (ns) on a logarithmic y-axis (0.1 to 100) against output frequency in MHz on a logarithmic x-axis (0.01 to 1000). The pulse width is constant at approximately 20 ns for frequencies from 0.01 MHz to 10 MHz. Above 10 MHz, the pulse width drops sharply to about 1 ns and exhibits a sawtooth-like oscillation between 1 ns and 2 ns up to 1000 MHz.</p>

Table 1-12: Nominal Traits — Power Requirements

Name	HFS 9003 Description	HFS 9009 Description
Fuse ratings	5 A, 250 V, type 3AG, (Tektronix part 159-0014-00), and 4 A, 250 V, type 3AG, fast blow, (Tektronix part 159-0017-00)	15 A, 250 V, type 3AG, fast blow, (Tektronix part 159-0256-00)

Table 1-13: Nominal Traits — System Memory Performance

Name	Description
Non-volatile memory retention time	Instrument settings and calibration constants are retained in non-volatile memory for 5 years or more. Card identification is retained for 10 years. Extended storage above 50° C may degrade the life of all non-volatile memory.

Table 1-14: Nominal Traits — HFS 9003 Mechanical

Name	Description
Weight, in 12-channel configuration. (Shipping weight includes all standard accessories.)	Cabinet
	Rackmount
Net weight:	45 lbs. (20.5 kg)
	51 lbs. (23.2 kg)
Shipping weight:	60 lbs. (27.3 kg)
	66 lbs. (30.0 kg)
Overall Dimensions	Cabinet
	Rackmount
	Width: 16.3 in. (414 mm)
	19.0 in. (483 mm)
	Height: 7.0 in. (178 mm)
7.0 in. (178 mm)	
Depth: 24.75 in. (629 mm)	
24.75 in. (629 mm)	
Depth behind rack flange:	—
22.0 in. (559 mm)	
Cooling Method	Forced-air circulation with no air filter, maximum 318 cfm
Construction Material	Chassis parts are constructed of aluminum alloy; bezel is glass-filled polycarbonate with Lexan plastic inserts; cabinet is aluminum with textured epoxy paint.

Table 1-15: Nominal Traits — HFS 9009 Mechanical

Name	Description
Weight, in 36-channel configuration. (Shipping weight includes all standard accessories.)	Rackmount
	Net weight: 81 lbs. (33.7 kg)
Shipping weight:	100 lbs. (45.3 kg)
Overall Dimensions	Rackmount
	Width: 16.75 in. (425.79 mm)
	Height: 14.00 in. (355.89 mm)
	Depth: 24.00 in. (610.11 mm)
Cooling Method, mainframe	Forced-air circulation with air filter, maximum 318 cfm
Cooling Method, power supply	Forced-air circulation, maximum 106 cfm
Construction Material	Chassis parts are constructed of aluminum alloy with Lexan plastic inserts; cabinet is aluminum with textured epoxy paint.

Warranted Characteristics

Warranted characteristics are described in terms of quantifiable performance limits which are warranted. Names of characteristics that appear in boldface type have checks for verifying the specifications in the *Check Procedures* section.

Table 1-16: Warranted Characteristics — HFS 9PG1 Output Performance

Name	Description
High level accuracy (amplitude ≥ 1 V or high level ≥ 0 V)¹	$\pm 2\%$ of level, ± 50 mV
Low level accuracy (amplitude ≥ 1 V or high level ≥ 0 V)¹	$\pm 2\%$ of high level, $\pm 2\%$ of amplitude, ± 50 mV
Transition time 20% to 80% (amplitude ≤ 1 V)	≤ 200 ps

¹ If amplitude < 1 V and high level < 0 V, accuracy typically meets the specification but is not guaranteed

Table 1-17: Warranted Characteristics — HFS 9PG2 Output Performance

Name	Description
High level accuracy	$\pm 2\%$ of level, ± 50 mV
Low level accuracy	$\pm 2\%$ of high level, $\pm 2\%$ of amplitude, ± 50 mV
Transition time accuracy 20% to 80% (amplitude ≤ 1 V)	$\pm 10\%$ of setting, ± 300 ps

Table 1-18: Warranted Characteristics — HFS 9DG1 Output Performance

Name	Description
High level accuracy (amplitude ≥ 0.5 V)¹	$\pm 2\%$ of level, ± 50 mV
Low level accuracy (amplitude ≥ 0.5 V)¹	$\pm 2\%$ of high level, $\pm 2\%$ of amplitude, ± 50 mV
Transition time 20% to 80% (amplitude ≤ 1 V)	≤ 250 ps

¹ If amplitude < 0.5 V, accuracy typically meets the specification but is not guaranteed

Table 1–19: Warranted Characteristics — HFS 9DG2 Output Performance

Name	Description
High level accuracy (amplitude ≥ 0.5 V) ¹	$\pm 2\%$ of level, ± 50 mV
Low level accuracy (amplitude ≥ 0.5 V) ¹	$\pm 2\%$ of high level, $\pm 2\%$ of amplitude, ± 50 mV
Transition time accuracy 20% to 80% (amplitude ≤ 1 V)	$\pm 10\%$ of setting, ± 300 ps

¹ If amplitude < 0.5 V, accuracy typically meets the specification but is not guaranteed.

Table 1–20: Warranted Characteristics — Time Base

Name	Description
Frequency accuracy	$\pm 1\%$

Table 1–21: Warranted Characteristic — Performance to External Frequency Reference

Name	Description
PHASE LOCK IN frequency range	6 MHz to 630 MHz

Table 1–22: Warranted Characteristics — Output Edge Placement Performance¹

Name	Description
Delay of pulses relative to time zero reference (Lead Delay) accuracy	HFS 9PG1, HFS 9PG2: 1% of (Lead Delay + Chan Delay) ± 300 ps HFS 9DG1, HFS 9DG2: 1% of (Lead Delay + Chan Delay) ± 50 ps
Pulse width accuracy	HFS 9PG1: 1% of width ± 300 ps HFS 9PG2: 1% of width ± 300 ps [for widths ≥ 20 ns]; 1% of width + 300 ps, -500 ps [for widths < 20 ns] HFS 9DG1: 1% of width + 50 -75 ps HFS 9DG2: 1% of width + 50 ps, -250 ps [for widths ≥ 20 ns]; 1% of width + 50 ps, -450 ps [for widths < 20 ns]

¹ Measured at 50% levels, each channel independent.

Table 1–23: Warranted Characteristics — Trigger Out Performance

Name	Description
TRIGGER OUT signal levels	Amplitude ≥ 300 mV (-0.5 V \geq offset ≥ -1.5 V, driving 50Ω to ground)

Table 1–24: Warranted Characteristics — Power Requirements

Name	Description
Primary circuit dielectric break-down voltage	1500 VAC _{RMS} , 60 Hz for 10 seconds without breakdown
Primary Grounding	0.1 Ω maximum from chassis ground and protective earth ground

Table 1–25: Warranted Characteristics — Environmental and Safety

Name	HFS 9003 Description	HFS 9009 Description
Temperature	Operating: 0° C to +50° C (32° F to 122° F) Non-operating (storage): -40° C to +75° C (-40° F to 167° F)	Operating: 0° C to +40° C (32° F to 104° F) Non-operating (storage): -40° C to +75° C (-40° F to 167° F)
Altitude	Operating: 4 hours at 3,048 m (10,000 feet). Derate maximum operating temperature by -1° C (-1.8° F) for each 304.8 m (1,000 feet) above 1,524 m (5,000 feet) Non-operating: 2 hours at 12,192 m (40,000 feet)	
Humidity	Operating: < 95% RH, non-condensing, from 0° C to 30° C (32° F to 86° F) < 75% RH, non-condensing, from 31° C to 40° C (88° F to 104° F) (MIL-T-28800E, para 4.5.5.1.2.2, Type III, Class 5)	
Shock (non-operating)	MIL-T-28800E, para 4.5.5.4.1, Type III, Class 5	
Resistance to mishandling during bench use (operating)	MIL-T-28800E, para 4.5.5.4.3, Type III, Class 5	
Resistance to packaged transportation vibration, sinusoidal, in shipping package	Drops of 36 inches on all edges, faces, and corners National Safe Transit Association, test procedure 1A-B-2	
Resistance to packaged transportation vibration, sinusoidal, in shipping package	Packaged sinusoidal vibration National Safe Transit Association, test procedure 1A-B-1	
Resistance to packaged transportation random vibration	MIL-STD-810D, method 514.3, category I, Figure 514.3-1	

Table 1–25: Warranted Characteristics — Environmental and Safety (Cont.)

Name	HFS 9003 Description	HFS 9009 Description
Safety	Listed to UL1244 Certified to CAN/CSA-C22.2 No. 231–M89	
IEC Specifications	Installation Category II Pollution Degree 2 Safety Class I	

Typical Characteristics

Typical characteristics are described in terms of typical or average performance. Typical characteristics are not warranted.

Table 1–26: Typical Characteristics — Time Base

Name	Description
RMS jitter	15 ps, $\pm 0.05\%$ of interval
Recovery time between bursts or auto-bursts	15 μ s

Table 1–27: Typical Characteristics — HFS 9PG1 Output Performance

Name	Description
Transition time 20% to 80%	Amplitude ≤ 1 V: 150 ps 1 V < Amplitude ≤ 2 V: 190 ps 2 V < Amplitude ≤ 3 V: 225 ps
Output aberrations (beginning 200 ps after 50% point of transition)	Overshoot: +15%, +20 mV Undershoot: –10%, –20 mV

Table 1–28: Typical Characteristics — HFS 9PG2 Output Performance

Name	Description
Operation when terminated to high impedance loads	Output level range will double until certain internal limits are achieved. Since the programmed, specified, and displayed output levels do not match the actual output levels, level accuracy specifications do not apply when terminating to a high impedance load. Because of the larger voltage swings associated with doubled level range, output transition time specifications do not apply when driving a high impedance load.
Transition time accuracy 20% to 80%	±10% of setting, ±300 ps
Output aberrations	Overshoot: +15%, +20 mV Undershoot: -10%, -20 mV

Table 1–29: Typical Characteristics — HFS 9DG1 Output Performance

Name	Description
Transition time 20% to 80%	Amplitude ≤ 1 V: ≤ 250 ps, 250 ps 1 V < Amplitude < 2 V: 250 ps 2 V ≤ Amplitude ≤ 3 V: 260 ps
Output aberrations	Overshoot: +15%, +20 mV Undershoot: -10%, -20 mV

Table 1–30: Typical Characteristics — HFS 9DG2 Output Performance

Name	Description
Operation when terminated to high impedance loads	Output level range will double until certain internal limits are achieved. Since the programmed, specified, and displayed output levels do not match the actual output levels, level accuracy specifications do not apply when terminating to a high impedance load. Because of the larger voltage swings associated with doubled level range, output transition time specifications do not apply when driving a high impedance load.
Transition time accuracy 20% to 80%	±10% of setting, ±300 ps
Output aberrations	Overshoot: +15%, +20 mV Undershoot: -10%, -20 mV

Table 1–31: Typical Characteristics — Performance to External Frequency Reference

Name	Description
PHASE LOCK IN amplitude range	0.8 V to 1.0 V peak-to-peak
PHASE LOCK IN transition time requirement	20% to 80% in ≤ 10 ns
FRAME SYNC IN signal level	$-1.810\text{ V} \leq V_{\text{low}} \leq -1.475\text{ V}$ $-1.165\text{ V} \leq V_{\text{high}} \leq -0.810\text{ V}$ (standard 100 K ECL levels)
Setup time, rising edge of FRAME SYNC IN signal to rising edge of PHASE LOCK IN	650 ps minimum
Hold time, high level of FRAME SYNC IN after rising edge of PHASE LOCK IN	650 ps minimum
Time from frame sync qualified phase lock clock cycle to time-zero reference	70 ns minimum, 130 ns

Table 1–32: Typical Characteristics — Transducer In Performance

Name	Description
TRANSDUCER IN useful frequency range	HFS 9PG1: 25 MHz to > 1 GHz HFS 9PG2: 5 MHz to 300 MHz
TRANSDUCER IN amplitude requirement	1.0 V to 1.5 V peak-to-peak

Table 1–33: Typical Characteristics — Trigger In Performance

Name	Description
Input resistance	50 Ω
Trigger level accuracy	± 100 mV $\pm 5\%$ of trigger level
Trigger input rise/fall time requirement	≤ 10 ns
Minimum trigger input pulse width	1 ns
Trigger sensitivity	≤ 500 mV
Time from trigger in to time-zero reference	70 ns minimum, 130 ns typical

Table 1-34: Typical Characteristics — Trigger Out Performance

Name	Description
Pretrigger resolution	250 ps

Table 1-35: Typical Characteristics — Power Requirements

Name	HFS 9003 Description	HFS 9009 Description
Line Voltage	90 VAC _{RMS} to 130 VAC _{RMS} or 180 VAC _{RMS} to 250 VAC _{RMS} , range switched automatically	90 VAC _{RMS} to 104 VAC _{RMS} with maximum 7 cards installed, 104 VAC _{RMS} to 132 VAC _{RMS} with maximum 9 cards installed, or 180 VAC _{RMS} to 250 VAC _{RMS} , range switched automatically
Line frequency	48 Hz to 63 Hz	
Power consumption	540 W maximum	1190 W with maximum of 9 cards installed
Inrush surge current	50 A maximum up to 40 ms at 110 VAC 100 A maximum up to 40 ms at 220 VAC	

Operating Information

The HFS 9009 is built in a C-size VXI card-modular mainframe. It has a CPU card, a time base card, and up to nine pulse and data generator cards. A front panel module provides a keyboard and a flat-panel display (see Figure 2–1).

NOTE. Even though the HFS 9009 is built in a VXI mainframe, the instrument does not follow all VXI standards and therefore is not a true VXI instrument.

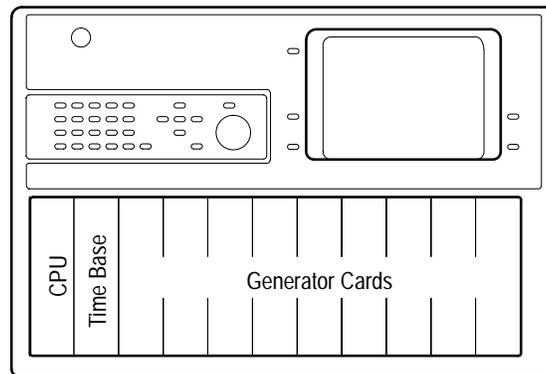


Figure 2–1: HFS 9009 Mainframe, Cards, and Front Panel

This section shows how to input simple settings for basic operation. For a more thorough explanation of how to set up the instrument, refer to the *HFS 9000 Series User Manual*.

Menu Selections

The front panel **MAIN MENU** button, shown in Figure 2–2, displays the top-level menu. Each item in this menu leads to a second-level menu. You can move through all menus using the arrow keys surrounding the **SELECT** button. Each arrow button moves the selection to the next menu item in the direction indicated. When the desired menu item is highlighted, press the **SELECT** button to activate that selection.

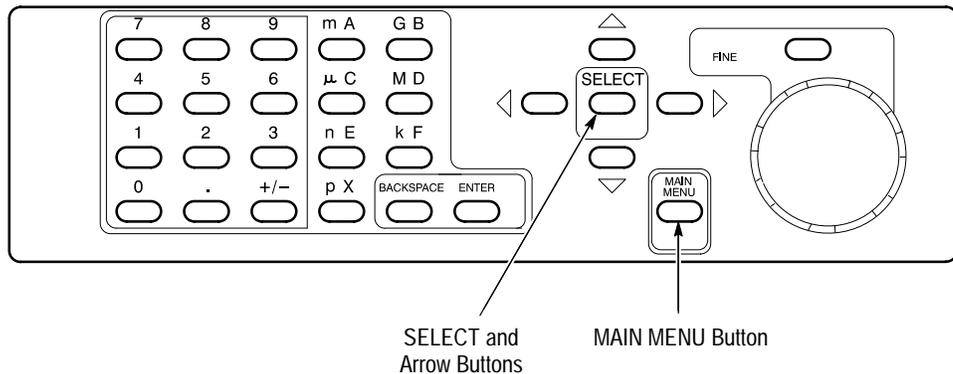


Figure 2-2: MAIN MENU, SELECT, and Arrow Button Locations

Resetting the HFS 9009

To reset all user-selected parameters to known default settings:

1. Press the **MAIN MENU** button (see Figure 2-2).
2. Use the arrow buttons to highlight the **Save/Recall Menu** item in the main menu (see Figures 2-2 and 2-3). Press the **SELECT** button.

```

Main Menu
press SELECT to show the Pulse Menu.

```

Pulse Menu	Time Base Menu	Levels Menu	—
Save/Recall Menu	GPIB Menu	RS-232 Menu	Cal/Deskew Menu

Figure 2-3: Main Menu Display

3. Highlight the **Reset** item and press **SELECT** again.
4. Verify the reset selection by highlighting **Yes** in the subsequent dialog box, then press **SELECT**. (To select options in the dialog box, use the up and down arrow keys, or turn the knob.)

Setting the Time Base

All pulse and data generator channels are governed by a single time base. Follow these steps to set up the time base to self-trigger repeatedly and to specify the number of pulses to be output from the pulse or data generators.

1. Press the **MAIN MENU** button.
2. Highlight the **Time Base Menu** item in the main menu. Press the **SELECT** button.

The time base normally waits for a trigger event, then specifies the number of pulses (**Count**) to be generated (see Figure 2–4). After that, the time base pauses for a rearm time, then waits for the next trigger event. The display screen above the Time Base menu graphically depicts this sequence.

Time Base Menu			
press SELECT: ▶ Auto Burst Auto-Burst			
Mode	Period	Count	Out Period
Auto	5ns	64	1
Trigger In	Trig Slope	Trig Level	PhaseLockIn
On	Positive	-1.3V	Off

Figure 2–4: The Time Base Menu

3. Use the arrow keys to highlight the **Mode** item. Press the **SELECT** button twice to select **Auto-Burst** in the menu item (see Figure 2–5).

Time Base Menu			
press SELECT: Auto Burst ▶ Auto-Burst			
Mode			
Auto-Burst			

Figure 2–5: Mode set to Auto-Burst

The **Period** and **Count** settings control the generated pulses. When either of these items are highlighted, the waveform display above the menu is updated to illustrate the parameter being adjusted.

4. Select the **Period** item. Use the knob to adjust the period. To get finer resolution, press the **FINE** button. The **FINE** light illuminates to indicate that fine mode is selected.

You may also enter numeric values with the keypad. Type in the number and, if necessary, press a key to specify units. Then finish by pressing the **ENTER** key.

5. Select the **Count** item. Set a value using the knob or type a value using the keypad. Press **ENTER** to terminate keypad entry.

The **Period** item can also be used to specify **Frequency**. When **Period** is highlighted, the **SELECT** button alternates between **Period** and **Frequency**. Use the knob or keypad to set values.

6. Highlight the **Period** item and press the **SELECT** button. Observe that the period setting changes to a reciprocal frequency setting.

The HFS 9009 is now set up to enable the output of pulses. Since the HFS 9009 is in auto-burst mode, no trigger input is required to generate pulses.

The UNDO Button

Whenever a setting is changed, the HFS 9009 remembers the old setting as well. Pressing the **UNDO** button at the right of the display panel restores the last setting. Pressing it twice undoes the undo.

Pulse Output

The following procedure demonstrates how to turn the pulse generator channels on. Any channel can be turned on from the Pulse menu **Output** item, but it is more convenient to turn on a channel from the front panel. Depending on the configuration of the HFS 9009, up to nine pulse and data generator cards can be installed, each with at least two channels. The controls for each type of card are shown in Figure 2–6. (Figure 2–1 shows the placement of the generator cards in the mainframe.)

1. Select a channel to use for the output by pressing the **OUTPUT** button for that channel. Observe that the associated light illuminates. If you want to use **OUTPUT** for any generator channel, you must turn on the **OUTPUT** separately.

The HFS 9009 is now creating pulse bursts. It generates the number of pulses entered for the count value at the frequency entered for the corresponding period value (or frequency value). When the pulse train is completed, it automatically starts over again after the rearm time.

2. Connect a cable to the output to access the generated pulses.
3. To select normal burst mode operation, highlight the **Mode** item of the Time Base menu. Use the **SELECT** button to select **Burst** mode. If burst is selected, the output is no longer triggered unless a suitable trigger signal is applied to the time base card **TRIGGER IN** connector. Press the **MANUAL TRIGGER** button at the right of the display panel to initiate a single burst from the HFS 9009.

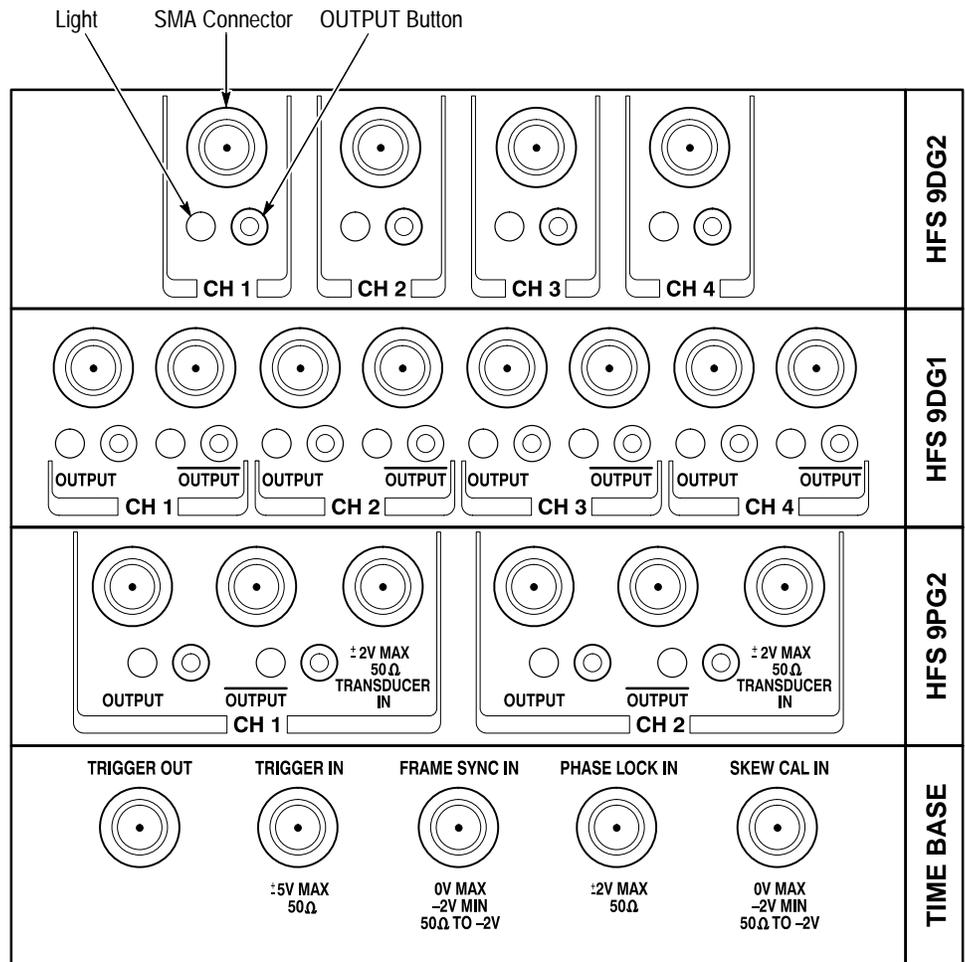


Figure 2-6: Controls and Connectors for the Pulse Generator, Data Generator, and Time Base Cards

Module Descriptions

This section describes the operation of each of the replaceable modules in the HFS 9009 Precision Pulse Generator. Refer to the *Diagrams* section of this manual for a block diagram of the HFS 9009.

Mainframe

The mainframe consists of a backplane, a power supply, and four fans.

Backplane The backplane complies with the *VXIbus System Specification Rev. 1.2*, dated June 21, 1989. The backplane is VXI standard C size and has 13 slots; a maximum of 11 slots may be used for the HFS 9000 configuration. The backplane is not a replaceable part.

Power Supply The HFS 9009 power supply is a single modular assembly located at the back of the mainframe. The power supply is a replaceable part.

Fans Four fans provide cooling for the power supply modules and the VXI modules installed in the card cage. Each fan can be replaced. All fans draw their power from the +12 V fan control of the power supply and draw a total of approximately 3 Amps.

The factory setting for the fan is variable speed. If the HFS 9009 is in a rackmount with reduced airflow, set the fan speed to high.

Front Panel

The front panel contains several modules. One module consists of the numeric keypad and encoder. This module is used to interact with the menus that appear on the electro-luminescent display. A second module contains a scan pushbutton matrix and LEDs, and mechanically supports the electro-luminescent display. The third module is the electro-luminescent display itself.

Cards

Six types of cards plug into the mainframe: the CPU card, time base card, high speed pulse generator card (HFS 9PG1), variable rate pulse generator card (HFS 9PG2), high speed data generator card (HFS 9DG1), and variable rate data

generator card (HFS 9DG2). Each HFS 9009 has one CPU card, one time base card, and up to nine generator cards.

CPU Card

The CPU receives commands for pulse output parameters from the front panel, the GPIB, or RS-232 interfaces. The CPU creates a series of time base and generator card commands which are then transmitted via the VXI Bus to set up the generator outputs.

The CPU card contains all product code in read-only memory (ROM). The CPU card also has volatile and nonvolatile random-access memory (RAM), as well as video display and bus timing circuitry.

Time Base Card

The time base contains a voltage-controlled oscillator (VCO) which is tunable from 325 MHz to 650 MHz. The time base also contains the trigger in, trigger out, and phase lock circuits.

The VCO output is connected to the generator cards through clock distribution cables. Clock distribution cables are located at the front of the cards. The time base card provides several connections for clock distribution cables, one of which is connected to each pulse and data generator card. The clock distribution cables provide a high-speed signal path for the clock because the VXI backplane cannot carry signals of sufficiently high frequency.

Pulse Generator Cards

Each pulse generator card provides two independent output channels. Each channel provides standard and logically-complemented outputs.

The pulse generator card channels divide the master clock signal into the requested frequency, and format the output signals. The pulse generator card controls the channel output levels, the channel delay, and the channel rising and falling edge time.

The pulse generator card transducer input can be used to bypass the VCO and timing generation circuits in the HFS 9009. When transducer in is enabled, a sine wave can be applied to the transducer input. You can use the channel output levels and rise and fall times to reshape the input signal.

High Speed Pulse Generator Cards (HFS 9PG1) run at a top speed of 630 MHz and have a fixed rise and fall time of 200 ps.

Variable Rate Pulse Generator Cards (HFS 9PG2) run at a top speed of 300 MHz. The rise time and fall times can be independently programmed from less than one nanosecond to five nanoseconds, which allows the user to adjust the speed of the pulse edges.

Data Time Generator Cards

Each data time generator card provides four independent output channels. The high speed data time generator card provides standard and logically-complemented outputs. The variable rate data time generator card provides only a single output for each channel. The data time generator card channels work in the same way as the pulse generator card channels. The master clock signal is divided into the requested frequency and format output signals by controlling the output levels, channel delay, and rising and falling edge time.

High Speed Data Time Generator Cards (HFS 9DG1) run at a top speed of 630 MHz and have a fixed rise and fall time of 200 ps.

Variable Rate Data Time Generator Cards (HFS9DG2) run at a top speed of 300 MHz. The rise and fall times can be independently programmed from less than one nanosecond to five nanoseconds, which allows the user to adjust the speed of the pulse edges.

Performance Verification

The following tests verify that the HFS 9000 Stimulus System achieves its specified performance.

Required Test Equipment

Refer to Table 4–1 for a list of the test equipment required to verify performance.

Table 4–1: Required Test Equipment

Item Number and Description	Minimum Requirements	Example	Purpose
1 Digital Volt Meter	DC volt accuracy: $\pm 0.1\%$ from 0.40 V to 5.5 V	Tektronix DM 511	Output level and amplitude checks
2 BNC female to dual banana plug	—	Tektronix part number 103-0090-00	Output level and amplitude checks
3 Cable, Precision Coaxial, BNC	36-inch, 50 Ω	Tektronix part number 012-0482-00	Output level and amplitude checks
4 Precision Feed-through Terminator	50 Ω , 0.1% at DC	Tektronix part number 011-0129-00	Output level and amplitude checks
5 Digital Sampling Oscilloscope	Δ time accuracy: $\pm (0.25\% + 10 \text{ ps})$ from 100 ps to 1 μs Freq. Measurement accuracy: $\pm 0.10\%$ from 50 kHz to 630 MHz	Tektronix 11801B Digital Sampling Oscilloscope or CSA803A Communication Signal Analyzer	Trigger Output Check, Rise and fall time checks, Edge placement checks, Frequency accuracy check
6 Sampling Head	Rise time: $\leq 60 \text{ ps}$ (10% to 90%)	Tektronix SD-22, SD-24, or SD-26	Used with Tektronix Digital Sampling Oscilloscope (item 5)
7 Attenuator, 5X, SMA	50 Ω , $\geq 12 \text{ GHz}$ bandwidth	Tektronix part number 015-1002-00	Rise and fall time checks
8 Cable, Coaxial, SMA (two required)	20-inch, 50 Ω	Tektronix part number 174-1427-00	Trigger Output Check, Rise and fall time checks, Edge placement check, Frequency accuracy check
9 Generator, Leveled Sine Wave	Capable of producing 0.8 V _{p-p} amplitude up to 600 MHz into 50 Ω	Tektronix SG 504	Phase lock check

Table 4-1: Required Test Equipment (Cont.)

Item Number and Description	Minimum Requirements	Example	Purpose
10 BNC female to SMA male adapter	—	Tektronix part number 015-1018-00	Output level and amplitude checks, Phase lock check
11 Threaded SMA female to SMA male slip-on connector	—	Tektronix part number 015-0553-00	SMA quick disconnect

Test Record

Identify the type of cards you will be testing and photocopy the appropriate tables from pages 4-3 to 4-9. Use these tables to record the performance test results for the instrument.

Table 4-2: Trigger Output Level and Phase Lock Test

Instrument Serial Number: _____		Page _____ of _____		Certificate Number: _____		
Temperature: _____		RH %: _____		Technician: _____		
Date of Calibration: _____						
Performance Test		Minimum	Incoming	Outgoing	Maximum	
Trigger Output Level Amplitude ≥ 300 mV (-0.5 V \geq offset ≥ -1.5 V, driving 50Ω to ground)						
Output	Maximum High Level	N/A	_____	_____	≤ -0.5 V	
	Minimum Low Level	≥ -1.5 V	_____	_____	N/A	
	Minimum Amplitude	≥ 300 mV _{p-p}	_____	_____	N/A	
Phase Lock Test 1% (frequency set accuracy of generator)						
Output	0.8 V, 250 MHz	250 MHz	247.5	_____	_____	252.5
Channel	0.8 V, 594 MHz	594 MHz	588.1	_____	_____	599.9

Table 4-3: Test Record for HFS 9DG1 Card

Channel: _____	Page _____ of _____
Instrument Serial Number: _____	Certificate Number: _____
Temperature: _____	RH %: _____
Date of Calibration: _____	Technician: _____

Performance Test		Nominal	Minimum	Incoming	Outgoing	Maximum
Output High Level: $\pm 2\%$ of level, ± 50 mV Low Level: $\pm 2\%$ of High Level, $\pm 2\%$ of amplitude (p-p), ± 50 mV						
Output Channel	Complement	+5.0 V	+4.850	_____	_____	+5.150
	Normal	+2.0 V	1.790	_____	_____	+2.210
	Normal	-2.5 V	-2.680	_____	_____	-2.320
	Complement	-1.5 V	-1.580	_____	_____	-1.420
Not Output Channel	Normal	+5.0 V	+4.850	_____	_____	+5.150
	Complement	+2.0 V	1.790	_____	_____	+2.210
	Complement	-2.5 V	-2.680	_____	_____	-2.320
	Normal	-1.5 V	-1.580	_____	_____	-1.420
Rise Time / Fall Time ≤ 250 ps for Amplitude ≤ 1 V						
Output Channel	Normal, 1V, Tr	250 ps	N/A	_____	_____	250 ps
	Complement, 1 V, Tf	250 ps	N/A	_____	_____	250 ps
Not Output Channel	Normal, 1V, Tf	250 ps	N/A	_____	_____	250 ps
	Complement, 1 V, Tr	250 ps	N/A	_____	_____	250 ps
Edge Placement Pulse Delay Time 1% of (Lead Delay + Chan Delay) ± 50 ps						
Output Channel	Normal	100 ps	49	_____	_____	151
		500 ps	445	_____	_____	555
		1 ns	0.940	_____	_____	1.060
		5 ns	4.900	_____	_____	5.100
		10 ns	9.850	_____	_____	10.150
		50 ns	49.45	_____	_____	50.55
		100 ns	98.95	_____	_____	101.05
Not Output Channel	Normal	100 ps	49	_____	_____	151
		500 ps	445	_____	_____	555
		1 ns	0.940	_____	_____	1.060
		5 ns	4.900	_____	_____	5.100
		10 ns	9.850	_____	_____	10.150
		50 ns	49.45	_____	_____	50.55
		100 ns	98.95	_____	_____	101.05
Edge Placement Pulse Width Variance 1% of width ± 50 ps						
Output Channel	Normal	500 ps	445	_____	_____	555
		750 ps	693	_____	_____	808
		1 ns	0.940	_____	_____	1.060
Not Output Channel	Normal	500 ps	445	_____	_____	555
		750 ps	693	_____	_____	808
		1 ns	0.940	_____	_____	1.060

Table 4-3: Test Record for HFS 9DG1 Card (Cont.)

Channel: _____ Page _____ of _____
Instrument Serial Number: _____ Certificate Number: _____
Temperature: _____ RH %: _____
Date of Calibration: _____ Technician: _____

Performance Test	Nominal	Minimum	Incoming	Outgoing	Maximum
Pulse Width Limits 1% of width +50 -75ps					
Output Channel Normal	5 ns	4.875	_____	_____	5.100
	10 ns	9.825	_____	_____	10.150
	50 ns	49.425	_____	_____	50.55
	100 ns	98.925	_____	_____	101.05
	500 ns	494.925	_____	_____	505.05
	1 μ s	0.990	_____	_____	1.010
Not Output Channel Normal	5 ns	4.875	_____	_____	5.100
	10 ns	9.825	_____	_____	10.150
	50 ns	49.425	_____	_____	50.55
	100 ns	98.925	_____	_____	101.05
	500 ns	494.925	_____	_____	505.05
	1 μ s	0.990	_____	_____	1.010
Frequency Accuracy \pm 1%					
Output Channel	50 kHz	49.50	_____	_____	50.50
	324 MHz	320.8	_____	_____	327.2
	326 MHz	322.7	_____	_____	329.3
	400 MHz	396.0	_____	_____	404.0
	433 MHz	428.7	_____	_____	437.3
	466 MHz	461.3	_____	_____	470.7
	500 MHz	495.0	_____	_____	505.0
	533 MHz	527.7	_____	_____	538.3
	566 MHz	560.3	_____	_____	571.7
	600 MHz	594.0	_____	_____	606.0
630 MHz	623.7	_____	_____	636.3	

Table 4-4: Test Record for HFS 9DG2 Card

Channel: _____	Page _____ of _____
Instrument Serial Number: _____	Certificate Number: _____
Temperature: _____	RH %: _____
Date of Calibration: _____	Technician: _____

Performance Test	Nominal	Minimum	Incoming	Outgoing	Maximum	
Output High Level: $\pm 2\%$ of level, ± 50 mV Low Level: $\pm 2\%$ of High Level, $\pm 2\%$ of amplitude (p-p), ± 50 mV						
Output Channel	Complement	+5.5 V	+5.340	_____	_____	+5.660
	Normal	0.0 V	-0.270	_____	_____	+0.270
	Normal	-2.0 V	-2.090	_____	_____	-1.910
	Complement	-1.0 V	-1.070	_____	_____	-0.930
Rise Time / Fall Time $\pm 10\%$ of setting ± 300 ps for Amplitude ≤ 1 V						
Output Channel	Normal, 1V, Tr	0.8 ns	0.420	_____	_____	1.180
	Complement, 1 V, Tf	0.8 ns	0.420	_____	_____	1.180
	Normal, 1 V, Tr	5 ns	4.200	_____	_____	5.800
	Complement, 1 V, Tf	5 ns	4.200	_____	_____	5.800
Edge Placement Pulse Delay Time 1% of (Lead Delay + Chan Delay) ± 50 ps						
Output Channel	Normal	100 ps	49	_____	_____	151
		500 ps	445	_____	_____	555
		1 ns	0.940	_____	_____	1.060
		5 ns	4.900	_____	_____	5.100
		10 ns	9.850	_____	_____	10.150
		50 ns	49.45	_____	_____	50.55
		100 ns	98.95	_____	_____	101.05
Edge Placement Pulse Width Limits (1% + 50 ps, -450 ps) for widths < 20 ns (1% + 50 ps, -250 ps) for widths ≥ 20 ns						
Output Channel		5 ns	4.500	_____	_____	5.100
		10 ns	9.450	_____	_____	10.150
		50 ns	49.25	_____	_____	50.55
		100 ns	98.75	_____	_____	101.05
		500 ns	494.8	_____	_____	505.1
		1 μ s	0.990	_____	_____	1.010
Frequency Accuracy $\pm 1\%$						
Output Channel		50 kHz	49.50	_____	_____	50.50
		162 MHz	160.4	_____	_____	163.6
		163 MHz	161.4	_____	_____	164.6
		200 MHz	198.0	_____	_____	202.0
		216.5 MHz	214.3	_____	_____	218.7
		233 MHz	230.7	_____	_____	235.3
		250 MHz	247.5	_____	_____	252.5
		266.5 MHz	263.8	_____	_____	269.2
		283 MHz	280.2	_____	_____	285.8
		300 MHz	297.0	_____	_____	303.0

Table 4-5: Test Record for HFS 9PG1 Card

Channel: _____		Page _____ of _____				
Instrument Serial Number: _____		Certificate Number: _____				
Temperature: _____		RH %: _____				
Date of Calibration: _____		Technician: _____				
Performance Test		Nominal	Minimum	Incoming	Outgoing	Maximum
Output High Level: $\pm 2\%$ of level, ± 50 mV		Low Level: $\pm 2\%$ of High Level, $\pm 2\%$ of amplitude (p-p), ± 50 mV				
Output Channel	Complement	+2.6 V	+2.498	_____	_____	+2.702
	Normal	-0.4 V	-0.562	_____	_____	-0.238
	Normal	-2 V	-2.090	_____	_____	-1.910
	Complement	-1 V	-1.070	_____	_____	-0.930
Not Output Channel	Normal	+2.6 V	+2.498	_____	_____	+2.702
	Complement	-0.4 V	-0.562	_____	_____	-0.238
	Complement	-2 V	-2.090	_____	_____	-1.910
	Normal	-1 V	-1.070	_____	_____	-0.930
Rise Time / Fall Time ≤ 200 ps for Amplitude ≤ 1 V						
Output Channel	Normal, 1V, Tr	200 ps	N/A	_____	_____	200 ps
	Complement, 1 V, Tf	200 ps	N/A	_____	_____	200 ps
Not Output Channel	Normal, 1V, Tf	200 ps	N/A	_____	_____	200 ps
	Complement, 1 V, Tr	200 ps	N/A	_____	_____	200 ps
Edge Placement Pulse Delay Time 1% of (Lead Delay + Chan Delay) ± 300 ps						
Output Channel	Normal	100 ps	-201	_____	_____	401
		500 ps	195	_____	_____	805
		1 ns	0.690	_____	_____	1.310
		5 ns	4.650	_____	_____	5.350
		10 ns	9.600	_____	_____	10.400
		50 ns	49.20	_____	_____	50.80
		100 ns	98.70	_____	_____	101.30
Not Output Channel	Normal	100 ps	-201	_____	_____	401
		500 ps	195	_____	_____	805
		1 ns	0.690	_____	_____	1.310
		5 ns	4.650	_____	_____	5.350
		10 ns	9.600	_____	_____	10.400
		50 ns	49.20	_____	_____	50.80
		100 ns	98.70	_____	_____	101.30
Edge Placement Pulse Width Variance 1% of width ± 300 ps						
Output Channel	Normal	500 ps	195	_____	_____	805
		750 ps	443	_____	_____	1060
		1 ns	0.690	_____	_____	1.310
Not Output Channel	Normal	500 ps	195	_____	_____	805
		750 ps	443	_____	_____	1058
		1 ns	0.690	_____	_____	1.310

Table 4-5: Test Record for HFS 9PG1 Card (Cont.)

Channel: _____	Page _____ of _____
Instrument Serial Number: _____	Certificate Number: _____
Temperature: _____	RH %: _____
Date of Calibration: _____	Technician: _____

Performance Test	Nominal	Minimum	Incoming	Outgoing	Maximum
Pulse Width Limits 1% of width ± 300 ps					
Output Channel Normal	5 ns	4.650	_____	_____	5.350
	10 ns	9.600	_____	_____	10.400
	50 ns	49.20	_____	_____	50.80
	100 ns	98.70	_____	_____	101.30
	500 ns	494.70	_____	_____	505.30
	1 µs	0.990	_____	_____	1.010
Not Output Channel Normal	5 ns	4.650	_____	_____	5.350
	10 ns	9.600	_____	_____	10.400
	50 ns	49.20	_____	_____	50.80
	100 ns	98.70	_____	_____	101.30
	500 ns	494.70	_____	_____	505.30
	1 µs	0.990	_____	_____	1.010
Frequency Accuracy ± 1%					
Output Channel	50 kHz	49.50	_____	_____	50.50
	324 MHz	320.8	_____	_____	327.2
	326 MHz	322.7	_____	_____	329.3
	400 MHz	396.0	_____	_____	404.0
	433 MHz	428.7	_____	_____	437.3
	466 MHz	461.3	_____	_____	470.7
	500 MHz	495.0	_____	_____	505.0
	533 MHz	527.7	_____	_____	538.3
	566 MHz	560.3	_____	_____	571.7
	600 MHz	594.0	_____	_____	606.0
630 MHz	623.7	_____	_____	636.3	

Table 4-6: Test Record for HFS 9PG2 Card

Channel: _____		Page _____ of _____				
Instrument Serial Number: _____		Certificate Number: _____				
Temperature: _____		RH %: _____				
Date of Calibration: _____		Technician: _____				
Performance Test		Nominal	Minimum	Incoming	Outgoing	Maximum
Output High Level: $\pm 2\%$ of level, ± 50 mV		Low Level: $\pm 2\%$ of High Level, $\pm 2\%$ of amplitude (p-p), ± 50 mV				
Output Channel	Complement	+5.5 V	+5.340	_____	_____	+5.660
	Normal	0 V	-0.270	_____	_____	+0.270
	Normal	-2 V	-2.090	_____	_____	-1.910
	Complement	-1 V	-1.070	_____	_____	-0.930
Not Output Channel	Normal	+5.5 V	+5.340	_____	_____	+5.660
	Complement	0 V	-0.270	_____	_____	+0.270
	Complement	-2 V	-2.090	_____	_____	-1.910
	Normal	-1 V	-1.070	_____	_____	-0.930
Rise Time / Fall Time $\pm 10\%$ of setting ± 300 ps for Amplitude ≤ 1 V						
Output Channel	Normal, 1V, Tr	0.8 ns	0.420	_____	_____	1.180
	Complement, 1 V, Tf	0.8 ns	0.420	_____	_____	1.180
	Normal, 1 V, Tr	5 ns	4.200	_____	_____	5.800
	Complement, 1 V, Tf	5 ns	4.200	_____	_____	5.800
Not Output Channel	Normal, 1V, Tf	0.8 ns	0.420	_____	_____	1.180
	Complement, 1 V, Tr	0.8 ns	0.420	_____	_____	1.180
	Normal, 1 V, Tf	5 ns	4.200	_____	_____	5.800
	Complement, 1 V, Tr	5 ns	4.200	_____	_____	5.800
Edge Placement Pulse Delay Time 1% of (Lead Delay + Chan Delay) ± 300 ps						
Output Channel	Normal	100 ps	-201	_____	_____	401
		500 ps	195	_____	_____	805
		1 ns	0.690	_____	_____	1.310
		5 ns	4.650	_____	_____	5.350
		10 ns	9.600	_____	_____	10.400
		50 ns	49.20	_____	_____	50.80
		100 ns	98.70	_____	_____	101.30
Not Output Channel	Normal	100 ps	-201	_____	_____	401
		500 ps	195	_____	_____	805
		1 ns	0.690	_____	_____	1.310
		5 ns	4.650	_____	_____	5.350
		10 ns	9.600	_____	_____	10.400
		50 ns	49.20	_____	_____	50.80
		100 ns	98.70	_____	_____	101.30

Table 4–6: Test Record for HFS 9PG2 Card (Cont.)

Channel: _____	Page _____ of _____
Instrument Serial Number: _____	Certificate Number: _____
Temperature: _____	RH %: _____
Date of Calibration: _____	Technician: _____

Performance Test	Nominal	Minimum	Incoming	Outgoing	Maximum		
Edge Placement Pulse Width Limits (1% of width + 300 ps, -500 ps) for widths < 20 ns (1% of width, ± 300 ps) for widths > 20 ns							
Output Channel	Normal	5 ns	4.450	_____	_____	5.350	
		10 ns	9.400	_____	_____	10.400	
		50 ns	49.20	_____	_____	50.80	
		100 ns	98.70	_____	_____	101.30	
		500 ns	494.7	_____	_____	505.3	
		1 μs	0.990	_____	_____	1.010	
Not Output Channel	Normal	5 ns	4.450	_____	_____	5.350	
		10 ns	9.400	_____	_____	10.400	
		50 ns	49.20	_____	_____	50.80	
		100 ns	98.70	_____	_____	101.30	
		500 ns	494.7	_____	_____	505.3	
		1 μs	0.990	_____	_____	1.010	
Frequency Accuracy ± 1%							
Output Channel	Nominal = HFS Setting	100 kHz	49.50	_____	_____	50.50	
	Output = Nominal/2		324 MHz	160.4	_____	_____	163.6
			326 MHz	161.4	_____	_____	164.6
			400 MHz	198.0	_____	_____	202.0
			433 MHz	214.3	_____	_____	218.7
			466 MHz	230.7	_____	_____	235.3
			500 MHz	247.5	_____	_____	252.5
			533 MHz	263.8	_____	_____	269.2
			566 MHz	280.2	_____	_____	285.8
	600 MHz	297.0	_____	_____	303.0		

Verification Sequence

The performance verification procedure consists of the following steps, performed in the following order:

1. Perform the HFS 9000 internal self test that follows this list of steps. If the self test indicates problems, refer to the *Maintenance* section in the Service Manual to repair the instrument.
2. Perform the internal calibration on page 4–12 if the HFS 9000 has not been recalibrated within the last six months, or if the HFS 9000 has been reconfigured with different cards or has been adjusted or repaired.
3. Follow the procedures in the Check Procedures section beginning on page 4–13 to verify that the HFS 9000 performs to every specification.

Self Test

The HFS 9000 is equipped with self-test diagnostic routines that execute automatically when you switch the power on. You may also manually select the diagnostic routines.

Use the following procedure to manually select the diagnostic routines:

1. Press **MAIN MENU** and select **Cal/Deskew Menu**.
2. Select **Self Test**.

The HFS 9000 display indicates the circuits under test as it proceeds through the diagnostics. The HFS 9000 returns to normal operating mode after successfully completing the diagnostics.

If the HFS 9000 detects a failure, it suspends normal operation and displays an error code (see the *Maintenance* section in the Service Manual for further information). The display presents two choices:

- Press any button other than the **SELECT** button to show a terse description of the failure. This additional information may assist you in isolating a failure to a module, or to determine if users can continue to operate the HFS 9000. The next diagnostic test will not begin until you press the **SELECT** button.
- Press the **SELECT** button to continue with the next diagnostic test.

A self-test failure does not necessarily indicate that the HFS 9000 is inoperable. However, it does indicate that the instrument is out of specification and that it might not be fully operational.

Calibration The calibration procedure adjusts the instrument to its internal voltage and timing references and saves the settings in non-volatile memory.

Calibrate the HFS 9000 at least every six months. The instrument does not need more frequent calibration unless it is reconfigured or used in an ambient temperature that differs by more than 5° C from the temperature it was last calibrated in.

***NOTE.** Run the calibration procedure only when the HFS 9000 has been powered on for 20 minutes in the temperature environment you expect it to be used in.*

To calibrate the HFS 9000, select the **Calibrate** item in the Cal/Deskew menu.

After you select the Calibrate item, verify this choice in the subsequent dialog box. After verification, the HFS 9000 starts the Timebase calibration and prompts you to attach an SMA cable from the front panel SKEW CAL IN connector to the TRIGGER OUT connector. The HFS 9000 then prompts you to connect each channel OUTPUT connector in turn. The HFS 9000 performs the calibration automatically during the time that each channel is connected. The time for the calibration procedure varies by configuration.

A 20 inch, 50 Ω coaxial SMA cable (Tektronix part number 174-1427-00) is supplied with the HFS 9000 as a standard accessory. This cable is suitable for use during calibration.

Check Procedures

Once you have run the self-test procedure, and, if necessary, calibrated the HFS 9000, these check procedures will verify that the instrument performs as specified.

Instrument Setup

Select **MAIN MENU** and reset the HFS 9000 using the **Reset** item in the Save/Recall menu. After this reset, the parameters listed below are properly set for all tests and need not be modified again. However, each check specifies a reset as a first step to ensure the following settings:

- Cal/Deskew menu, **Pretrigger** item: 70 ns
- Cal/Deskew menu, **Channel Delay** item: 0 s (all channels)
- Time Base menu, **Mode** item: Auto
- Levels menu, **Limit** item: Off
- Pulse menu, **Signal Type** item: Pulse

***NOTE.** Allow the HFS 9000 to warm up for a minimum of 20 minutes. The instrument must warm up in an ambient temperature within 5° C of the ambient temperature when last calibrated.*

After you have set up the first channel for a particular check, use the **Copy Channel** and **Paste Channel** menu items to transfer the setup to the other channels.

Output Level Checks (HFS 9DG1 Card Only)

These tests check the output level in volts DC of each data generator channel. You will need to repeat these checks for each output channel; the number of times you repeat a check depends on the configuration of your HFS 9000. A reference to “the channel” is a reference to the particular channel being checked.

Equipment Required	One DVM (digital voltmeter, item 1) One BNC female to dual banana connector (item 2) One precision coaxial cable (item 3) One feedthrough termination (item 4) One threaded SMA female to SMA male slip-on connector (item 11).
---------------------------	---

1. Reset the HFS 9000.
2. Set the Digital Voltmeter to measure DC volts on Auto Range.

3. Construct the termination assembly by connecting the following items in the order listed:
 - a. one BNC female to dual banana connector (item 2)
 - b. one precision coaxial cable (item 3)
 - c. one feedthrough termination (item 4)
 - d. one BNC female to SMA male adapter (item 10)
 - e. one threaded SMA female to SMA male slip-on connector (item 11).
4. Connect the banana plug end of the termination assembly to the input of the DVM and connect the other end to the channel normal **OUTPUT** connector.
5. Set the HFS 9000 according to Table 4–7.

Table 4–7: HFS 9DG1 Output Level Checks, First Settings

Control	Setting
Pulse menu, Channel	The channel under test
Pulse menu, Output	On
Pulse menu, ~Output	Off
Pulse menu, Pulse Rate	Off
Pulse menu, Polarity	Complement
Pulse menu, High Level	5.0 V
Pulse menu, Low Level	2.0 V

The output voltage reading on the DVM should be between 4.850 V and 5.150 V.

6. Change the Pulse menu **Polarity** item setting to **Normal**.

The output voltage reading on the DVM should be between 1.790 V and 2.210 V.

7. Set the HFS 9000 according to Table 4–8.

Table 4–8: HFS 9DG1 Output Level Checks, Second Settings

Control	Setting
Pulse menu, High Level	-1.5 V
Pulse menu, Low Level	-2.5 V

The output voltage reading on the DVM should be between -2.680 V and -2.320 V .

8. Change the Pulse menu **Polarity** item setting to **Complement**.

The output voltage reading on the DVM should be between -1.580 V and -1.420 V .

9. Move the feedthrough termination assembly to the channel complemented OUTPUT. The DVM is now set to monitor the complement output.
10. Set the HFS 9000 according to Table 4–9.

Table 4–9: HFS 9DG1 Output Level Checks, Third Settings

Control	Setting
Pulse menu, Output	Off
Pulse menu, ~Output	On
Pulse menu, Polarity	Normal
Pulse menu, High Level	5.0 V
Pulse menu, Low Level	2.0 V

The output voltage reading on the DVM should be between 4.850 V and 5.150 V .

11. Change the Pulse menu **Polarity** item setting to **Complement**.

The output voltage reading on the DVM should be between 1.790 V and 2.210 V .

12. Set the HFS 9000 according to Table 4–10.

Table 4–10: HFS 9DG1 Output Level Checks, Fourth Settings

Control	Setting
Pulse menu, High Level	-1.5 V
Pulse menu, Low Level	-2.5 V

The output voltage reading on the DVM should be between -2.680 V and -2.320 V .

13. Change the Pulse menu **Polarity** item setting to **Normal**.

The output voltage reading on the DVM should be between -1.580 V and -1.420 V .

14. Repeat steps 1 through 13 for each of the HFS 9DG1 channels in the system.
15. Disconnect test setup.

**Output Level Checks
(HFS 9DG2 and HFS 9PG2
Cards Only)**

These tests check the output level in volts DC of each pulse or data generator channel. You will need to repeat these checks for each output channel; the number of times you repeat a check depends on the configuration of your HFS 9000. A reference to “the channel” is a reference to the particular channel being checked.

Equipment Required	One DVM (digital voltmeter, item 1) One BNC female to dual banana connector (item 2) One precision coaxial cable (item 3) One feedthrough termination (item 4) One threaded SMA female to SMA male slip-on connector (item 11).
---------------------------	---

1. Reset the HFS 9000.
2. Set the Digital Voltmeter to measure DC volts on Auto Range.
3. Construct the termination assembly by connecting the following items in the order listed:
 - a. one BNC female to dual banana connector (item 2)
 - b. one precision coaxial cable (item 3)
 - c. one feedthrough termination (item 4)
 - d. one BNC female to SMA male adapter (item 10)
 - e. one threaded SMA female to SMA male slip-on connector (item 11).
4. Connect the banana plug end of the termination assembly to the input of the DVM and connect the other end to the channel normal **OUTPUT** connector.
5. Set the HFS 9000 according to Table 4–11.

Table 4–11: HFS 9DG2 and HFS 9PG2 Output Level Checks, First Settings

Control	Setting
Pulse menu, Channel	The channel under test
Pulse menu, Output	On
Pulse menu, ~Output	Off
Pulse menu, Pulse Rate	Off
Pulse menu, Polarity	Complement
Pulse menu, High Level	5.5 V
Pulse menu, Low Level	0 V

The output voltage reading on the DVM should be between 5.340 V and 5.660 V.

6. Change the Pulse menu **Polarity** item setting to **Normal**.

The output voltage reading on the DVM should be between –0.270 V and +0.270 V.

7. Set the HFS 9000 according to Table 4–12.

Table 4–12: HFS 9DG2 and HFS 9PG2 Output Level Checks, Second Settings

Control	Setting
Pulse menu, High Level	–1.0 V
Pulse menu, Low Level	–2.0 V

The output voltage reading on the DVM should be between –2.090 V and –1.910 V.

8. Change the Pulse menu **Polarity** item setting to **Complement**.

The output voltage reading on the DVM should be between –1.070 V and –0.930 V.

9. Move the feedthrough termination assembly to the channel complemented $\overline{\text{OUTPUT}}$ if available (HFS 9PG2). The DVM is now set to monitor the complement output.

10. Set the HFS 9000 according to Table 4–13.

Table 4–13: HFS 9PG2 Output Level Checks, Third Settings

Control	Setting
Pulse menu, Output	Off
Pulse menu, ~Output	On
Pulse menu, Polarity	Normal
Pulse menu, High Level	5.5 V
Pulse menu, Low Level	0 V

The output voltage reading on the DVM should be between 5.340 V and 5.660 V.

11. Change the Pulse menu **Polarity** item setting to **Complement**.

The output voltage reading on the DVM should be between –0.270 V and +0.270 V.

12. Set the HFS 9000 according to Table 4–14.

Table 4–14: HFS 9PG2 Output Level Checks, Fourth Settings

Control	Setting
Pulse menu, High Level	–1.0 V
Pulse menu, Low Level	–2.0 V

The output voltage reading on the DVM should be between –2.090 V and –1.910 V.

13. Change the Pulse menu **Polarity** item setting to **Normal**.

The output voltage reading on the DVM should be between –1.07 V and –0.93 V.

14. Repeat steps 1 through 13 for each of the HFS 9PG2 and HFS 9DG2 channels in the system.
15. Disconnect test setup.

Output Level Checks (HFS 9PG1 Card Only)

These tests check the output level in volts DC of each pulse generator channel. You will need to repeat these checks for each output channel; the number of times you repeat a check depends on the configuration of your HFS 9000. A reference to “the channel” is a reference to the particular channel being checked.

Equipment Required	One DVM (digital voltmeter, item 1) One BNC female to dual banana connector (item 2) One precision coaxial cable (item 3) One feedthrough termination (item 4) One threaded SMA female to SMA male slip-on connector (item 11).
---------------------------	---

1. Reset the HFS 9000.
2. Set the Digital Voltmeter to measure DC volts on Auto Range.
3. Construct the termination assembly by connecting the following items in the order listed:
 - a. one BNC female to dual banana connector (item 2)
 - b. one precision coaxial cable (item 3)
 - c. one feedthrough termination (item 4)
 - d. one BNC female to SMA male adapter (item 10)
 - e. one threaded SMA female to SMA male slip-on connector (item 11).
4. Connect the banana plug end of the termination assembly to the input of the DVM and connect the other end to the channel normal **OUTPUT** connector.
5. Set the HFS 9000 according to Table 4–15.

Table 4–15: HFS 9PG1 Output Level Checks, First Settings

Control	Setting
Pulse menu, Channel	The channel under test
Pulse menu, Output	On
Pulse menu, -Output	Off
Pulse menu, Pulse Rate	Off
Pulse menu, Polarity	Complement
Pulse menu, High Level	2.6 V
Pulse menu, Low Level	-0.4 V

The output voltage reading on the DVM should be between 2.498 V and 2.702 V.

6. Change the Pulse menu **Polarity** item setting to **Normal**.

The output voltage reading on the DVM should be between –0.562 V and –0.238 V.

7. Set the HFS 9000 according to Table 4–16.

Table 4–16: HFS 9PG1 Output Level Checks, Second Settings

Control	Setting
Pulse menu, High Level	–1.0 V
Pulse menu, Low Level	–2.0 V

The output voltage reading on the DVM should be between –2.090 V and –1.910 V.

8. Change the Pulse menu **Polarity** item setting to **Complement**.

The output voltage reading on the DVM should be between –1.07 V and –0.93 V.

9. Move the feedthrough termination assembly to the channel complemented OUTPUT. The DVM is now set to monitor the complement output.
10. Set the HFS 9000 according to Table 4–17.

Table 4–17: HFS 9PG1 Output Level Checks, Third Settings

Control	Setting
Pulse menu, Output	Off
Pulse menu, ~Output	On
Pulse menu, Polarity	Normal
Pulse menu, High Level	2.6 V
Pulse menu, Low Level	–0.4 V

The output voltage reading on the DVM should be between 2.498 V and 2.702 V.

11. Change the Pulse menu **Polarity** item setting to **Complement**.

The output voltage reading on the DVM should be between –0.562 V and –0.238 V.

12. Set the HFS 9000 according to Table 4–18.

Table 4–18: HFS 9PG1 Output Level Checks, Fourth Settings

Control	Setting
Pulse menu, High Level	–1.0 V
Pulse menu, Low Level	–2.0 V

The output voltage reading on the DVM should be between –2.090 V and –1.910 V.

13. Change the Pulse menu **Polarity** item setting to **Normal**.

The output voltage reading on the DVM should be between –1.07 V and –0.93 V.

14. Repeat steps 1 through 13 for each of the HFS 9PG1 channels in the system.
15. Disconnect test setup.

Trigger Output Level

This check verifies the level of the HFS 9000 trigger output.

Equipment Required	One Tektronix 11801B Digital Sampling Oscilloscope or CSA803A Communication Signal Analyzer (item 5) with sampling head (item 6) Two SMA coaxial cables (item 8)
---------------------------	---

1. Connect an SMA cable from the HFS 9000 **TRIGGER OUTPUT** to the Channel 1 input of the DSO sampling head.
2. Connect an SMA cable from the DSO trigger input to the HFS 9000 Channel 1 output.
3. Reset the HFS 9000.
4. Initialize the DSO and select the Channel 1 sampling head input.

- Press **AUTOSET** and set the HFS 9000 and DSO according to Table 4–19.

Table 4–19: Settings for Trigger Output Check

Control	Setting
HFS 9000:	
Pulse menu, Period	Press SELECT to change the Period item to a Frequency item
Pulse menu, Frequency	100 MHz
Pulse menu, Output	On
DSO:	
Main Size	2 ns
Vertical Size	200 mV
Vertical Offset	0
Main Position	Minimum
Measure	Min, Max, Amplitude

- Measure maximum value is less than or equal to -0.5 V, the minimum value is greater than or equal to -1.5 V and the amplitude is greater than or equal to 300 mV_{p-p}.

Rise Time and Fall Time Checks (HFS 9PG1 and HFS 9DG1 Cards Only)

These checks verify the rise time and fall times of HFS 9PG1 pulse card and HFS 9DG1 data time generator channels. You will check each HFS 9000 high speed channel in turn. A reference to “the channel” is a reference to the particular channel under test.

Equipment Required	One Tektronix 11801B Digital Sampling Oscilloscope or CSA803A Communication Signal Analyzer (item 5) with sampling head (item 6) Two SMA coaxial cables (item 8) One SMA 5X attenuator (item 7) One threaded SMA female to SMA male slip-on connector (item 11).
---------------------------	---

- Reset the HFS 9000, then make the settings according to Table 4–20.

Table 4-20: Settings for Rise Time and Fall Time Checks

Control	Setting
Pulse menu, Channel	The channel under test
Pulse menu, High Level	Press SELECT to change the High Level item to an Amplitude item, and the Low Level item to an Offset item
Pulse menu, Amplitude	1.0 V
Pulse menu, Offset	0 V
Pulse menu, Polarity	Normal
Pulse menu, Period	Press SELECT to change the Period item to a Frequency item
Pulse menu, Frequency	100 kHz
Pulse menu, Pulse Rate	Normal
Pulse menu, Output	On
Pulse menu, -Output	Off

2. Initialize the DSO.
3. Connect an SMA cable from the HFS 9000 **TRIGGER OUT** connector to the **DIRECT** connector located in the **TRIGGER INPUTS** section of the DSO. Set the DSO to trigger on that signal. Turn on averaging on the DSO.



CAUTION. To avoid accidentally damaging the sampling head of the DSO, place a 5X SMA attenuator on the sampling head input. Voltages in excess of 3 volts may damage the input circuit.

4. After placing a 5X SMA attenuator on the sampling head input, connect an SMA cable from the 5X SMA attenuator to the HFS 9000 normal **OUTPUT** connector of the channel under test. To save time connecting the cable to other channels, use the SMA slip-on connector on the end of the cable that connects to the HFS.
5. Set the DSO to display the signal with 50 mV/div (4 divisions) vertically at zero offset. Set the DSO time base to 1 μ s/div horizontally. Set the DSO **MAIN POSITION** to minimum.

6. Display the DSO measurement menu and turn on **RISE** and **FALL** measurements. Touch the **RISE** selector at the bottom of the DSO screen to display the **RISE** measurement parameters. Set these parameters according to Table 4–21.

Table 4–21: DSO Settings for Rise/Fall Time Checks

DSO Control	Setting
Left Limit	0%
Right Limit	100%
Proximal	20%
Distal	80%
Tracking	On
Level Mode	Relative

7. Once the DSO captures high and low levels, turn off tracking.
8. Set the DSO sweep speed to 500 ps/div and position the first rising edge at center screen. The measured rise time should be less than 200 ps for HFS 9PG1 cards, and less than 250 ps for a HFS 9DG1 cards. (Use waveform averaging to stabilize the measurement.)
9. Change the Pulse menu **Polarity** item setting to Complement. The measured fall time should be less than 200 ps for HFS 9PG1 cards, and less than 250 ps for HFS 9DG1 cards.
10. Repeat steps 1 through 9 for each of the HFS 9PG1 or HFS 9DG1 card channels in the system. (For Not Output channels, set **Output** off and **~Output** on.)
11. Disconnect test setup.

Rise Time and Fall Time Checks (HFS 9PG2 and HFS 9DG2 Cards Only)

These checks verify the rise time and fall times of HFS 9PG2 pulse card and HFS 9DG2 data time generator channels. You will check each HFS 9000 high speed channel in turn. A reference to “the channel” is a reference to the particular channel under test.

Equipment Required	One Tektronix 11801B Digital Sampling Oscilloscope or CSA803A Communication Signal Analyzer (item 5) with sampling head (item 6) Two SMA coaxial cables (item 8) One SMA 5X attenuator (item 7) One threaded SMA female to SMA male slip-on connector (item 11).
---------------------------	---

1. Reset the HFS 9000, then make the settings listed in Table 4–22.

Table 4–22: Settings for Rise Time and Fall Time Checks

Control	Setting
Pulse menu, Channel	The channel under test
Pulse menu, High Level	Press SELECT to change the High Level item to an Amplitude item, and the Low Level item to a Offset item
Pulse menu, Amplitude	1.0 V
Pulse menu, Offset	0 V
Pulse menu, Polarity	Normal
Pulse menu, Transition	800 ps
Pulse menu, Period	Press SELECT to change the Period item to a Frequency item
Pulse menu, Frequency	100 kHz
Pulse menu, Pulse Rate	Normal
Pulse menu, Output	On
Pulse menu, -Output	Off

2. Connect an SMA cable from the HFS 9000 **TRIGGER OUT** connector to the **DIRECT** connector located in the **TRIGGER INPUTS** section of the DSO. Set the DSO to trigger on that signal.



CAUTION. To avoid accidentally damaging the sampling head of the DSO, place a 5X SMA attenuator on the sampling head input. Voltages in excess of 3 volts may damage the input circuit.

3. After placing a 5X SMA attenuator on the sampling head input, connect an SMA cable from the 5X SMA attenuator to the HFS 9000 normal **OUTPUT** connector of the channel under test. To save time connecting the cable to other channels, use the SMA slip-on connector on the end of the cable that connects to the HFS.
4. Set the DSO to display the signal with 50 mV/div (4 divisions) vertically at zero offset. Set the DSO time base to 1 μ s/div horizontally. Set the DSO **MAIN POSITION** to minimum.
5. Display the DSO measurement menu and turn on **RISE** and **FALL** measurements. Touch the **RISE** selector at the bottom of the DSO screen to display the **RISE** measurement parameters. Set these parameters according to Table 4–23.

Table 4–23: DSO Settings for Rise/Fall Time Checks

DSO Control	Setting
Left Limit	0%
Right Limit	100%
Proximal	20%
Distal	80%
Tracking	On
Level Mode	Relative

6. Once the DSO captures high and low levels, turn off tracking.
7. Set the DSO sweep speed to 500 ps/div and position the first rising edge at center screen. The measured rise time should be between 420 ps and 1.18 ns (HFS 9PG2 & HFS 9DG2 cards). (Use waveform averaging to stabilize the measurement.)
8. Change the Pulse menu **Polarity** item setting to Complement. The measured fall time should be between 420 ps and 1.18 ns (HFS 9PG2 & HFS 9DG2 cards).
9. Change the Pulse menu **Polarity** item setting to Normal. Set the Pulse menu **Transition** item to 5 ns.
10. Set the DSO time base to 5 ns/div. Use the RISE measurement to verify that the rise time is between 4.2 ns and 5.8 ns (HFS 9PG2 & HFS 9DG2 cards).
11. Change the Pulse menu **Polarity** item setting to Complement. The measured fall time on the DSO should be between 4.2 ns and 5.8 ns (HFS 9PG2 & HFS 9DG2 cards).

12. Repeat steps 1 through 11 for each of the HFS 9PG2 or HFS 9DG2 card channels in the system. (For Not Output channels, set **Output** off and **~Output** on.)
13. Disconnect test setup.

Edge Placement Checks

These checks verify the accuracy of the pulse delays and pulse widths. You will check each HFS 9000 channel in turn. A reference to “the channel” is a reference to the particular channel being checked in this repetition.

Equipment Required	One Tektronix 11801B Digital Sampling Oscilloscope or CSA803A Communication Signal Analyzer (item 5) with sampling head (item 6) Two SMA coaxial cables (item 8) One threaded SMA female to SMA male slip-on connector (item 11).
---------------------------	---

1. Reset the HFS 9000, then make the settings according to Table 4–24.

Table 4–24: Settings for Edge Placement Checks

Control	Setting
Pulse menu, Channel	The channel under test
Pulse menu, High Level	Press SELECT to change the High Level item to an Amplitude item, and the Low Level item to an Offset item
Pulse menu, Amplitude	1.0 V
Pulse menu, Offset	0 V
Pulse menu, Period	Press SELECT to change the Period item to a Frequency item
Pulse menu, Frequency	100 kHz
Pulse menu, Output	On

2. If the channel is a Variable Rate (HFS 9PG2 or HFS 9DG2) channel, set transition to the lowest (fastest) rise time possible. (A quick way to do this is to enter “0” on the numeric keypad.)
3. Connect an SMA cable from the HFS 9000 **TRIGGER OUT** connector to the **DIRECT** connector located in the **TRIGGER INPUTS** section of the DSO.
4. Connect an SMA cable from the normal **OUTPUT** connector of the HFS 9000 channel under test to the sampling head input of the DSO. To save

time connecting the cable to other channels, use the SMA slip-on connector on the end of the cable that connects to the HFS.

5. Initialize the DSO, then set the DSO to display a triggered signal with 200 mV/div (5 divisions) vertically at zero offset. Set the DSO time base to 1 μ s/div horizontally. Set the DSO **MAIN POSITION** to minimum.
6. Display the DSO measurement menu and turn on **WIDTH** and **CROSS** measurements. On the DSO, touch the **WIDTH** selector at the bottom of the DSO screen to display the width measurement parameters. Set the DSO width **LEVEL MODE** parameter to **RELATIVE**. Turn the DSO tracking on.
7. On the DSO, turn tracking off when the high and low levels have been acquired.
8. Set the DSO sweep speed to 500 ps/div. Position the rising edge of the displayed waveform at the center of the DSO screen. On the DSO, save the cross measurement as the reference (in the Compare & References pop-up menu).
9. On the DSO, turn **COMPARE** on.
10. Refer to Table 4–25 or 4–26, as appropriate, and adjust for each of the specified Pulse menu **Lead Delay** settings listed in the left column. For each **Lead Delay** value, verify that the DSO **CROSS** measurement falls within the limits specified in the middle and right columns. You may need to adjust the DSO horizontal position to keep the rising edge on the screen.

Table 4–25: Lead Delay Limits for HFS 9PG1 and HFS 9PG2

HFS 9000 Pulse Menu Lead Delay Setting	DSO CROSS Measurement Minimum	DSO CROSS Measurement Maximum
100 ps	–201 ps	401 ps
500 ps	195 ps	805 ps
1 ns	690 ps	1.31 ns
5 ns	4.65 ns	5.35 ns
10 ns	9.60 ns	10.4 ns
50 ns	49.2 ns	50.8 ns
100 ns	98.7 ns	101.3 ns

Table 4-26: Lead Delay Limits for HFS 9DG1 and HFS 9DG2

HFS 9000 Pulse Menu Lead Delay Setting	DSO CROSS Measurement Minimum	DSO CROSS Measurement Maximum
100 ps	49 ps	151 ps
500 ps	445 ps	555 ps
1 ns	940 ps	1.060 ns
5 ns	4.9 ns	5.1 ns
10 ns	9.85 ns	10.15 ns
50 ns	49.45 ns	50.55 ns
100 ns	98.95 ns	101.05 ns

11. Set the DSO horizontal position to minimum. Turn the DSO COMPARE off.
12. On the HFS 9000, use the **SELECT** button to change the Pulse menu **Duty Cycle** item to a **Width** item. Set the **Lead Delay** item to zero.
13. Skip this step if the channel is a Variable Rate (HFS 9PG2 or HFS 9DG2) channel. Refer to Table 4-27 or Table 4-28. Adjust the DSO horizontal position to display the first rising edge at screen. While observing the width measurement readout on the DSO, adjust the HFS 9000 **Pulse Width** item with the knob in **Fine** mode until each reading in the left column is achieved on the DSO. Then, observe the **Width** item setting on the HFS 9000 that achieved this result. Verify that the HFS 9000 value is within the limits specified in the middle and right columns. You may need to adjust the DSO horizontal position to keep the pulse on the screen.

Table 4-27: Width Variance Limits for HFS 9PG1

DSO WIDTH Measurement Readout	HFS 9000 Width Setting Minimum	HFS 9000 Width Setting Maximum
500 ps	195 ps	805 ps
750 ps	443 ps	1.06 ns
1 ns	690 ps	1.31 ns

Table 4–28: Width Variance Limits for HFS 9DG1

DSO WIDTH Measurement Readout	HFS 9000 Width Setting Minimum	HFS 9000 Width Setting Maximum
650 ps	594 ps	732 ps
750 ps	693 ps	833 ps
1 ns	940 ps	1.085 ns

14. Refer to Tables 4–29, 4–30 and 4–31, as appropriate, and set each of the specified Pulse menu **Width** settings listed in the left column. For each **Width** setting, verify that the DSO WIDTH measurement falls within the limits specified in the middle and right columns. Adjust the horizontal time/division as necessary to keep a full pulse displayed on screen.

Table 4–29: Width Limits for HFS 9PG1 and HFS 9PG2

HFS 9000 Pulse Menu Width Setting	DSO WIDTH Measurement Minimum		DSO WIDTH Measurement Maximum
	HFS 9PG1	HFS 9PG2	
5 ns	4.65 ns	4.45 ns	5.35 ns
10 ns	9.60 ns	9.40 ns	10.4 ns
50 ns	49.2 ns	49.2 ns	50.8 ns
100 ns	98.7 ns	98.7 ns	101.3 ns
500 ns	494.7 ns	494.7 ns	505.3 ns
1 μ s	990 ns	990 ns	1.01 μ s

Table 4–30: Width Limits for HFS 9DG1

HFS 9000 Pulse Menu Width Setting	DSO WIDTH Measurement Minimum	DSO WIDTH Measurement Maximum
5 ns	4.875 ns	5.1 ns
10 ns	9.825 ns	10.15 ns
50 ns	49.45 ns	50.55 ns
100 ns	98.95 ns	101.05 ns
500 ns	494.95 ns	505.05 ns
1 μ s	990 ns	1.01 μ s

Table 4-31: Width Limits for HFS 9DG2 1

HFS 9000 Pulse Menu Width Setting	DSO WIDTH Measurement Minimum	DSO WIDTH Measurement Maximum
5 ns	4.500 ns	5.1 ns
10 ns	9.450 ns	10.15 ns
50 ns	49.25 ns	50.55 ns
100 ns	98.75 ns	101.05 ns
500 ns	494.8 ns	505.1 ns
1 μ s	990 ns	1.01 μ s

15. Repeat steps 1 through 14 for each of the channels in the system. (For Not Output channels, set **Output** off and **~Output** on).

16. Disconnect test setup.

Frequency Accuracy Check

Equipment Required	
	One Tektronix 11801B Digital Sampling Oscilloscope or CSA803A Communication Signal Analyzer (item 5) with sampling head (item 6)
	One SMA coaxial cable (item 8)
	One threaded SMA female to SMA male slip-on connector (item 11).

1. Reset the HFS 9000, then use the SELECT button to change the Pulse menu **Period** item to a **Frequency** item.
2. Connect an SMA cable from the HFS 9000 TRIGGER OUT connector to the DIRECT connector located in the TRIGGER INPUTS section of the DSO. Set the DSO to trigger on that signal.
3. Connect an SMA cable from the normal OUTPUT connector of any High Speed HFS 9000 channel to the sampling head input of the DSO. To save time connecting the cable to other channels, use the SMA slip-on connector on the end of the cable that connects to the HFS.

NOTE. If you have any HFS 9PG2 channels, set the Pulse menu **Pulse Rate** item to Half for those channels. If you have Variable Rate or HFS 9DG2 channels, use one of them for this test.

4. Turn on the output of the HFS 9000 channel you are using.

5. Set the DSO to display the signal with 200 mV/div vertically and a vertical offset of -1.3 V. Set the DSO time base to 500 ps/div horizontally. Set the DSO MAIN POSITION to minimum.
6. Display the DSO measurement menu and turn on the FREQUENCY measurement. On the DSO, turn TRACKING on and turn on AVERAGING with AVGN set to 32.
7. Refer to Tables 4–32, 4–33, or 4–34 as appropriate, and adjust for each of the specified Pulse menu **Frequency** settings listed in the left column. For each **Frequency** value, verify that the DSO FREQUENCY measurement falls within the limits specified in the middle and right columns. Adjust the horizontal size and position to make the display of a single cycle fill the DSO screen.

Table 4–32: Frequency Limits (HFS 9PG1 & HFS 9DG1)

HFS 9000 Pulse Menu Frequency Setting	DSO FREQUENCY Minimum	DSO FREQUENCY Maximum
50 kHz	49.5 kHz	50.5 kHz
324 MHz	320.8 MHz	327.2 MHz
326 MHz	322.7 MHz	329.3 MHz
400 MHz	396.0 MHz	404.0 MHz
433 MHz	428.7 MHz	437.3 MHz
466 MHz	461.3 MHz	470.7 MHz
500 MHz	495.0 MHz	505.0 MHz
533 MHz	527.7 MHz	538.3 MHz
566 MHz	560.3 MHz	571.7 MHz
600 MHz	594.0 MHz	606.0 MHz
630 MHz	623.7 MHz	636.3 MHz

Table 4–33: Frequency Limits (HFS 9PG2)

HFS 9000 Pulse Menu Frequency Setting	DSO FREQUENCY ($\div 2$) Minimum	DSO FREQUENCY ($\div 2$) Maximum
100 kHz	49.5 kHz	50.5 kHz
324 MHz	160.4 MHz	163.6 MHz
326 MHz	161.4 MHz	164.6 MHz
400 MHz	198 MHz	202 MHz
433 MHz	214.3 MHz	218.7 MHz

Table 4-33: Frequency Limits (HFS 9PG2) (Cont.)

HFS 9000 Pulse Menu Frequency Setting	DSO FREQUENCY (\div 2) Minimum	DSO FREQUENCY (\div 2) Maximum
466 MHz	230.7 MHz	235.3 MHz
500 MHz	247.5 MHz	252.5 MHz
533 MHz	263.8 MHz	269.2 MHz
566 MHz	280.2 MHz	285.8 MHz
600 MHz	297.0 MHz	303.0 MHz

Table 4-34: Frequency Limits (HFS 9DG2)

HFS 9000 Pulse Menu Frequency Setting	DSO FREQUENCY Minimum	DSO FREQUENCY Maximum
50 kHz	49.5 kHz	50.5 kHz
162 MHz	160.4 MHz	163.6 MHz
163 MHz	161.4 MHz	164.6 MHz
200 MHz	198.0 MHz	202.0 MHz
216.5 MHz	214.3 MHz	218.7 MHz
233 MHz	230.7 MHz	235.3 MHz
250 MHz	247.5 MHz	252.5 MHz
266.5 MHz	263.8 MHz	269.2 MHz
283 MHz	280.2 MHz	285.8 MHz
300 MHz	297.0 MHz	303.0 MHz

Phase Lock Check

Equipment Required	Generator, Leveled Sine Wave (item 9) BNC female to SMA male adapter (item 10).
---------------------------	--

This check verifies that the phase lock system is capable of detecting, accurately measuring, and holding an input signal.

NOTE. *If the HFS 9009 cannot determine the phase lock frequency, an error message is displayed. This will happen if the phase lock signal is not stable and continuous, or if the phase lock signal is outside the allowed frequency range, or if the HFS 9009 needs calibrating.*

1. Reset the HFS 9000.
2. Set the signal generator for an amplitude of $0.8 V_{p-p}$ and a frequency of 250 MHz. Connect the signal to the HFS 9000 **PHASE LOCK IN** connector. If your generator does not have better than 1% frequency accuracy, use the FREQUENCY measurement capability of the DSO to set the generator frequency to within 1%.
3. Set the Time Base menu **PhaseLockIn** item to On.
4. Check that the input frequency is correctly displayed on the HFS 9000 screen immediately above the menu area.
5. Wait at least five seconds and make sure that the HFS 9000 retains phase lock. (If phase lock is lost, you will see an error message.)
6. Set the Time Base menu **PhaseLockIn** item to Off.
7. Repeat steps 3 through 6 with the signal generator set to 594 MHz. If your generator does not have better than 1% frequency accuracy, use the FREQUENCY measurement capability of the DSO to set the generator frequency to within 1%.
8. You may optionally check other frequencies as well. Low frequency checks will require a different generator (such as a square wave generator) which meets to 20% to 80% risetime requirement of 10 ns or less for the **PHASE LOCK IN** input.
9. Disconnect test setup.



Adjustments

The input line power voltage range for the HFS 9009 is 90 VAC to 250 VAC and is range switched automatically. The DC outputs from the power supply are not adjustable.

Preventive Maintenance

Accumulations of dirt impair the efficiency of the cooling fans and reduce heat transfer from components. Dirt may also cause faulty operation of the fan speed control temperature sensor. Periodically vacuum dirt and dust from the inside of the mainframe, paying particular attention to the fans. Heavy accumulations of dirt should be removed with a soft brush.



CAUTION. Do not use water or alcohol to clean the backplane card connectors.

Removal and Replacement

The removal and replacement procedures describe the disassembly of the HFS 9009 to service the instrument. Observe all cautions and warnings. Refer to the *Diagrams* section of this manual for a block diagram of the HFS 9009.

Front Panel

The Front Panel must be removed to gain access to the keypad, display module, and bezel. Turn off instrument power when removing or replacing the front panel.

Removal ■ Remove the four screws holding on the front panel.

■ Disconnect the ribbon cable connecting the front panel module to the CPU card. Mark it for proper reconnection.

Replacement ■ Connect the ribbon cable between the front panel module and the CPU card.

■ Set the front panel into the instrument frame and replace the four screws.

Front Panel Keypad and Encoder Switch

The encoder switch and the keypad on the left of the front panel can be replaced if they are defective. Turn off instrument power when removing or replacing the modules.

Removal 1. Remove the front panel (see Front Panel Removal). Lay the front panel face down on the work bench.

2. Disconnect the ribbon cable located at the bottom of the keypad circuit board. Mark it for proper reconnection.

3. To remove the keypad circuit board assembly:

■ Unsolder the wires from the encoder switch where they attach to the circuit board. Note their orientation for replacement.

■ Remove the six screws which secure the circuit board and lift it off the circuit board.

4. To remove the encoder switch:

■ Unsolder the wires from the encoder switch.

- Using a hex wrench, loosen the two set screws in the knob and remove the knob from the encoder shaft.
- Remove the hex nut that secures the encoder switch and remove the encoder switch from the keypad assembly.

Replacement

1. To replace the encoder switch:
 - Insert the encoder switch through the front panel. Replace the hex nut that secures the encoder switch. Orient the switch so that the switch soldering lugs are closest to the circuit board assembly.
 - Resolder the wires to the encoder switch.
 - Using a hex wrench, place the knob on the encoder shaft and tighten the two set screws in the knob.
2. To replace the keypad circuit board assembly:
 - Resolder the wires from the encoder switch.
 - Align the holes in the circuit board with the spacers on the front panel. Replace the six screws which secure the circuit board.
 - Reconnect the flat ribbon cable to the keypad circuit board assembly.
3. Replace the front panel (see Front Panel Replacement).

Display Module

The Front Panel must be removed to gain access to the display module. Turn off instrument power when removing or replacing the front panel.

Removal

1. Remove the front panel (see Front Panel Removal).
2. Lay the front panel face down and remove the four nuts which attach the display module to the front panel.
3. Disconnect the ribbon cable located at the bottom of the display module, note its alignment for replacement, and lift off the display module.

Replacement

1. Set the display module on the front panel. Align the module so that the ribbon cable connector is closest to the ribbon cables on the top panel circuit board assembly.
2. Reconnect the ribbon cable.
3. Replace the four nuts which attach the display module to the front panel.
4. Replace the front panel (see Front Panel Replacement).

Top Panel Circuit Board and Trim Bezel

The Front Panel must be removed to gain access to the Top Panel circuit board assembly and front panel trim bezel. Turn off instrument power when removing or replacing the front panel.

Removal

1. Remove the front panel (see Front Panel Removal).
2. Lay the front panel face down. Remove the four nuts and washers which attach the display module to the front panel.
3. Disconnect the ribbon cable located at the bottom of the display module, note its alignment for replacement, and lift off the display module.
4. To remove the Top Panel circuit board assembly or Trim Bezel:
 - Disconnect the three flat panel ribbon connectors. Note their orientation for replacement.
 - Remove the four nuts which secure the Top Panel circuit board assembly and lift off the circuit board assembly.
 - Lift off the Trim Bezel.

Replacement

1. If the Trim Bezel was removed, replace it.
2. Place the top panel circuit board assembly back on the front panel and replace the four nuts which attach the circuit board assembly to the front panel. *Do not overtighten the nuts.* When you press the push buttons from the front panel you should feel a distinct “click.” If the nuts are overtightened, you will not feel a click when you depress the push buttons.
3. Set the display module on the front panel. Align the module so that the ribbon cable connector is closest to the ribbon cables on the top panel circuit board assembly.
4. Reconnect the ribbon cable located at the bottom of the display module.
5. Replace the four nuts which attach the display module to the front panel.
6. Replace the front panel (see Front Panel Replacement).

ON/STANDBY Switch

The **ON/STANDBY** push button is made up of two subassemblies. One is the power switch actuator assembly that fits through the front panel. The second subassembly is a power switch mounted on the internal chassis. The internally mounted switch is *not* a replaceable part. The power switch actuator on the front panel can be replaced. The Front Panel must be removed to gain access to the

power switch actuator. Turn off instrument power when removing or replacing the front panel.

- Removal**
1. Remove the front panel (see Front Panel Removal).
 2. To remove the power switch actuator:
 - Lay the front panel face down.
 - Remove the two nuts which secure the actuator. Lift off the actuator.

- Replacement**
1. Place the power switch actuator onto the front panel and reattach the two nuts.
 2. Replace the front panel (see Front Panel Replacement).

Cards

Pulse and data generator cards are located behind the small panels in the open area of the front panel. Turn off instrument power when removing or replacing cards.

- Removal**
1. Remove the front panel module (see Front Panel Removal).
 2. If the card you are removing is the time base card or any pulse or data generator card, remove the clock distribution cable (see Figure 6–1).

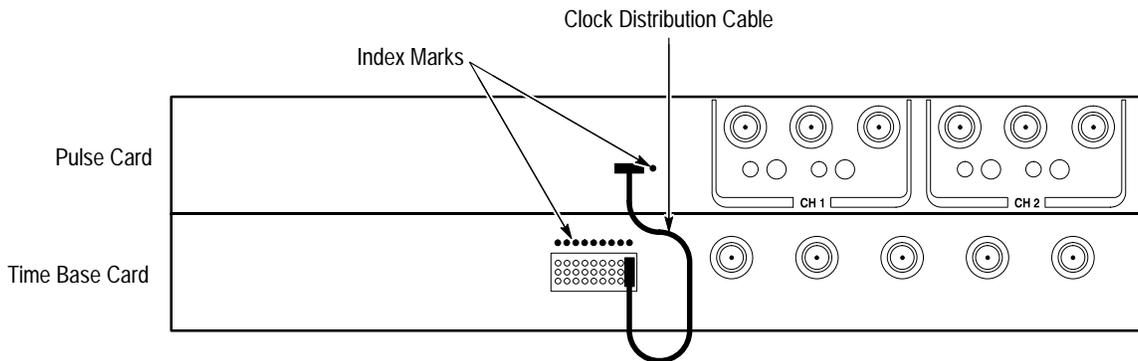


Figure 6–1: Clock Distribution Cable Location

3. Each card is fastened with two screws, one on either end of the card front panel. Remove these screws and pull the card straight forward.

- Replacement**
1. Push the card into the appropriate slot through in the mainframe. Refer to the *Diagrams* section of this manual to identify the proper card position in the

rack. Reattach the card with two screws, one on either end of the card front panel.

2. If the card is a pulse or data generator card, or a time base card, reattach the clock distribution cables. Align the index mark on the cable connectors with the index marks on the card. When all cards are installed, a clock distribution cable must connect the time base card to each pulse or data generator card (see Figure 6–1). The time base card has several connectors for clock distribution cables; it does not matter which of these connectors is used for each pulse or data generator card.

Mainframe Top Cover

For mainframe service operations, only the top cover needs to be removed.

Removal



WARNING. To avoid electric shock, disconnect the power source when removing or replacing the covers. Hazardous voltages are exposed when the covers are removed, even when the power switch is in the standby position. Use extreme caution when the instrument is connected to the power source while the covers are removed.

1. Remove the six screws located along the bottom of the top cover above the rack mount slides and toward the rear of the instrument (there are three screws on each side).
2. Remove the four screws that attach the front panel to the mainframe.
3. Disconnect the ribbon cable connecting the front panel module to the CPU card. Mark it for proper reconnection. Set the front panel aside.
4. Remove the four screws, their retaining nuts, and the vertical brackets from the front outside edge (two on each side).
5. Remove the six screws on the top of the cover and lift off the cover.

Replacement

1. Place the cover on the frame. Replace the six screws on the top of the cover.
2. Replace the six screws located along the bottom of the top cover and above the rack mount slides.
3. Replace the four screws, their retaining nuts, and vertical brackets along the front outside edge (two along each side).
4. Connect the ribbon cable between the front panel module and the CPU card.

5. Set the front panel into the instrument frame and replace the four screws.

Power Supply (lower back panel)



WARNING. To avoid electric shock, disconnect the power source when removing or replacing the power supply. Hazardous voltages are exposed when the power supply and covers are removed, even when the power switch is in the standby position.

Removal

1. Remove the five mounting screws and washers in the lower back panel (see Figure 6–2).
2. Carefully slide out the power supply (lower back panel) by pulling on the center handle.

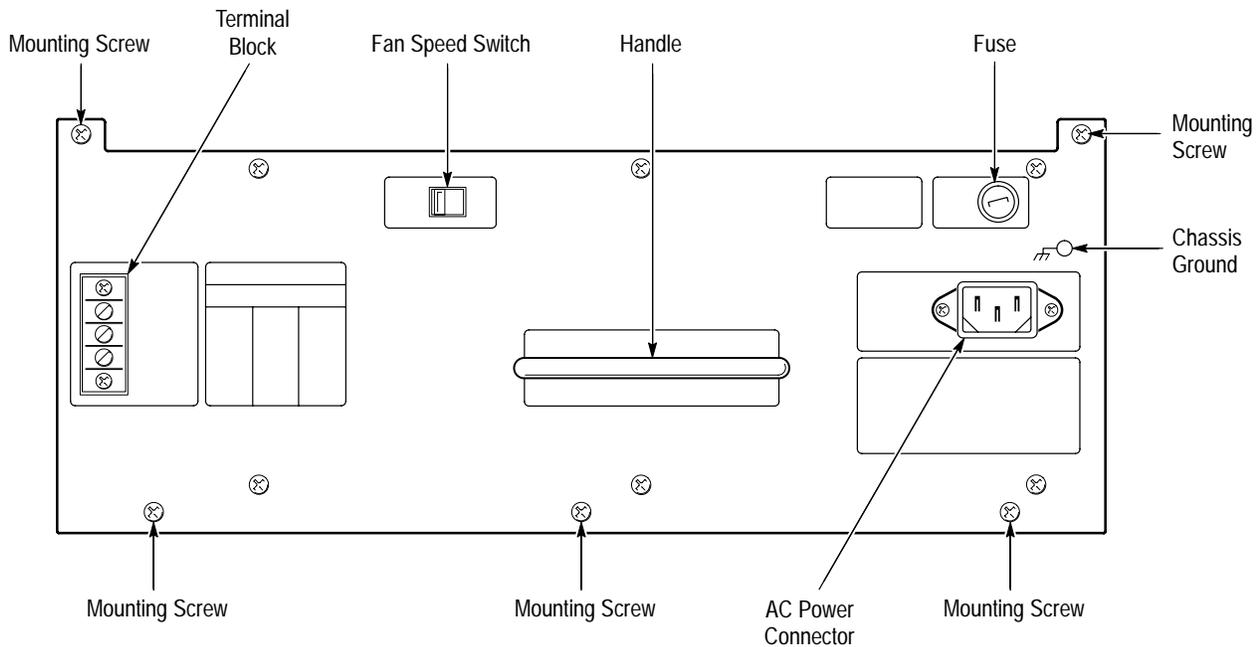


Figure 6–2: HFS 9009 Power Supply (rear view)

Replacement

1. Carefully slide the power supply (lower back panel) into the mainframe.
2. Replace the five mounting screws and washers in the lower back panel.

Fans (upper back panel)



WARNING. To avoid electric shock or personal injury, disconnect the power source when removing or replacing the fans. Hazardous voltages and dangerous fan blades are exposed when the fans and covers are removed, even when the power switch is in the standby position.

Removal

1. Remove the two handles of the upper back panel by removing the two screws in each handle.
2. Remove the two screws in the top cover of the mainframe that attach the upper back panel to the mainframe.
3. Slide out the upper back panel.
4. Remove the four screws and nuts that attach the fan unit to the upper back panel.
5. Disconnect the power supply cable from the fan.

Replacement

1. Position the fan unit so that the label in the center of the fan faces away from the outside of the upper back panel. The power connector should be at the top of the upper back panel.
2. Reconnect the power supply cable to the fan power connector.
3. Replace the four screws and nuts that attach the fan unit to the upper back panel.
4. Slide the upper back panel into the mainframe and replace the two screws in the top cover of the mainframe.
5. Replace the two handles.

Fan (side panel)



WARNING. To avoid electric shock or personal injury, disconnect the power source when removing or replacing the fans. Hazardous voltages and dangerous fan blades are exposed when the fans and covers are removed, even when the power switch is in the standby position.

- Removal**
1. Remove the power supply (see Power Supply Removal).
 2. Loosen the four thumbscrews that attach the fan unit to the side of the mainframe.
 3. Disconnect the power supply cable from the fan.
 4. Remove the four screws and four nuts that hold the two brackets to the fan.

- Replacement**
1. Install the two brackets on the new fan.
 2. Position the fan unit so that the label in the center of the fan faces to the outside of the mainframe. The power connector should be at the top.
 3. Reconnect the power supply cable to the fan.
 4. Tighten the four thumbscrews that attach the fan unit to the mainframe.
 5. Replace the power supply (see Power Supply Replacement).

Troubleshooting

This section provides information necessary to troubleshoot the HFS 9009 at the circuit board level. The primary troubleshooting method is to use the power-on and self-test diagnostics to identify faulty Field Replaceable Units (FRUs). The FRUs include the plug-in cards, front panel modules, fans, knobs, switches, and any individual component that is listed in the *Mechanical Parts List* section of this manual.

Power-On Diagnostics

Power-on diagnostics execute automatically whenever the mainframe power is switched on. The HFS 9009 uses three stages of diagnostics which run consecutively: the kernel test, controller test, and self test. Diagnostics advance to the next stage only if the preceding stage does not detect an error. In self-test diagnostics, once an error message is displayed on the screen, you can request that the diagnostics continue. When all tests successfully complete, the instrument goes into normal operating mode. Test failures result in error-code outputs which can be cross-referenced to suspect FRUs.

Kernel-Test Diagnostics

The kernel test is the first stage of diagnostics. It verifies the functionality of the hardware needed to run the internal operating system.

Controller-Test Diagnostics

The controller test is the second stage of diagnostics. It is run by the internal operating system. It verifies the CPU support circuitry on the controller (CPU) card, the backplane bus, and the front-panel module.

Self-Test Diagnostics

The self test is the last stage of diagnostics and verifies the functionality of the time base card and the pulse and data generator cards. This test differs from the kernel- and controller-test diagnostics in two ways. First, the self-test diagnostics display messages on the screen. Once a self-test failure has occurred, you can display more information or continue running the remaining diagnostics.

Second, the self-test diagnostics can be run at any time. Use the Cal/Deskew menu **Self Test** item on the front panel or execute the `*TST?` command from the GPIB or RS-232-C programmable ASCII interface. Refer to the Self-Test Diagnostics Section on page 6–12 of this manual or the *HFS 9000 User Manual* for more information.

Self-Test Diagnostics

You can run the self-test diagnostics using the **Self Test** item in the Cal/Deskew menu. In addition, the same function can be initiated from either ASCII interface (RS-232-C or GPIB) under the control of a remote computer or controller. Refer to the *HFS 9000 User Manual* for detailed information about using the programming interfaces. The *TST? query runs the self test and reports the results. The self test does not require operator interaction and does not create bus conditions that violate IEEE 488.1/488.2 standards. When the test is complete, the HFS 9009 returns to the state it was in prior to the self test.

The test response is a value as described in Table 6–1.

Table 6–1: Results from *TST?

Test Response Value	Meaning
0	test completed with no errors detected
SSCC	<p>system in which a slot and card produced the first detected error:</p> <p>SS = slot number: 01 = CPU slot 02 = time base slot 03 = slot A 04 = slot B ... 11 = slot I</p> <p>CC = card type: 10 = CPU card 20 = time base card 31 = high speed pulse generator card (HFS 9PG1) 32 = variable rate pulse generator card (HGS 9PG2) 33 = high speed data time generator card (HFS 9DG1) 34 = variable rate data time generator card (HFS 9DG2)</p>
9900	system configuration is not valid

The self test query can take 30 seconds or more to complete. If an error is detected, the self test stops, returns an error code, and does not finish the remaining tests.

Calibration

Calibration measures the performance of the HFS 9009 against specifications and performs automatic internal adjustments to bring the HFS 9009 into specification. Calibration differs from diagnostic tests in that diagnostic tests only verify that the circuits are operational.

Calibration is normally a function initiated by the user. However, calibration can be automatically initiated by the power-on diagnostics if they determine that the HFS 9009 is out of specification or has been reconfigured.

It is possible to generate error codes by running a calibration procedure at a time other than power on.

Error Indications

There are two mechanisms for reporting errors: diagnostic LED error indexes and extended mode menus.

Kernel-test and controller-test failures are identified by a LED error index, and, if they are not display related, by a displayed error message. These messages are in the following format:

```
CONTROLLER DIAGNOSTICS FAILED <test name>
```

When any kernel test or controller test fails, the CPU hangs in a loop and the instrument appears dead. For corrective action, see Table 6–2 and Figure 6–5.

Kernel and controller testing occurs quickly, so the LEDs will only turn on briefly as they switch between on and off states. If the LEDs never turn on during power on, or if any LEDs remain lit, then an error is indicated.

Self-test errors are identified by LED error indexes that indicate the faulty card, and by extended mode menus on the front panel. In all cases, a faulty FRU is identified by the LED error indications.

Bit Assignments For Diagnostic LEDs

The bank of diagnostic LEDs is located on the CPU card inside the LED cover. Figure 6–3 shows the location of the LED cover and LEDs. Keep in mind that the CPU card is positioned vertically in the HFS 9009 mainframe with the front panel connector at the top and the GPIB port at the bottom. The following instructions assume this vertical positioning of the CPU card.

To see the LEDs, remove the screw attaching the cover to the CPU card. A firmware update stick might be installed in the slot behind the cover. You can see the bank of eight LEDs on the side nearest to the serial port connector. You may need to use a small flashlight to see all of the unlit LEDs.

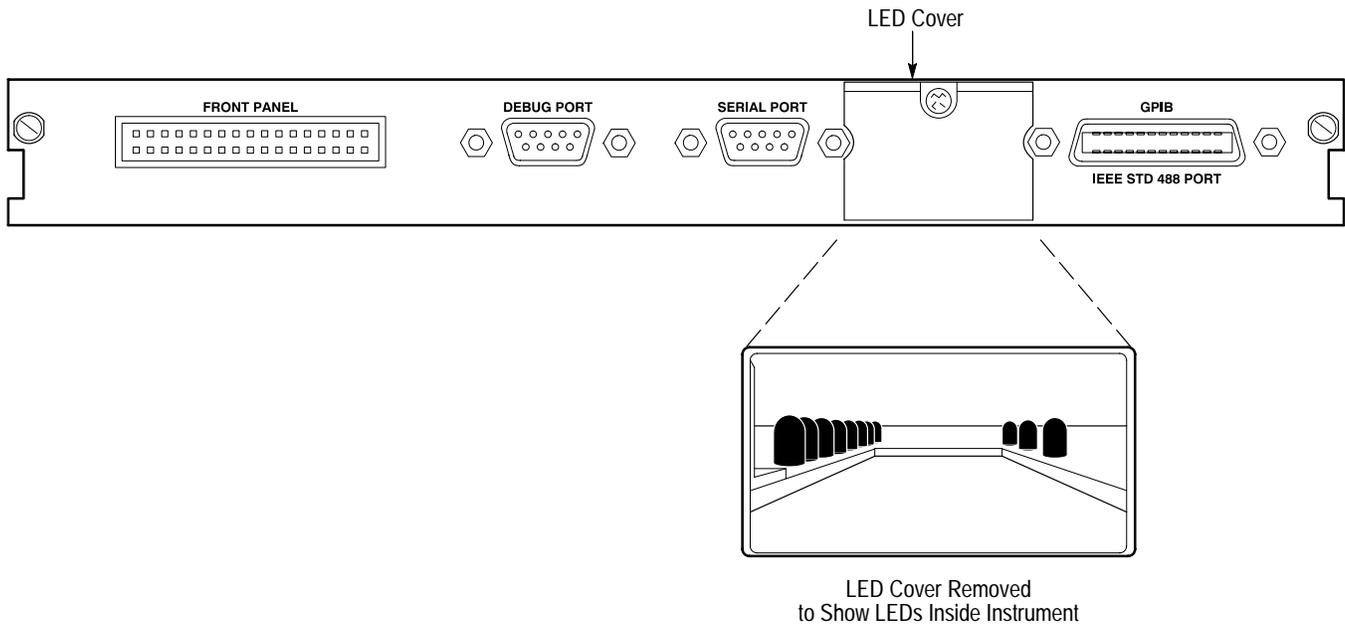


Figure 6-3: The Location of LEDs on the CPU Card

The eight LEDs are numbered D6 (farthest from the front panel) through D13 (nearest the front panel) as shown in Figure 6-4.

The onset, completion, or failure of testing is indicated by LED D13. LEDs D6 through D10 combine to display the error index code. These five LEDs are combined to make a hexadecimal value in the range of 00 through 1F. LED D6 is the low order bit; LED D10 is the high order bit.

At power on, status LEDs are turned off. At the start of the tests, status LEDs are turned on. If a kernel test fails but completes execution, the D13 LED turns off and the processor stops. If a kernel test is unable to finish, the D13 LED remains lit. To identify a failed test, read the error index code.

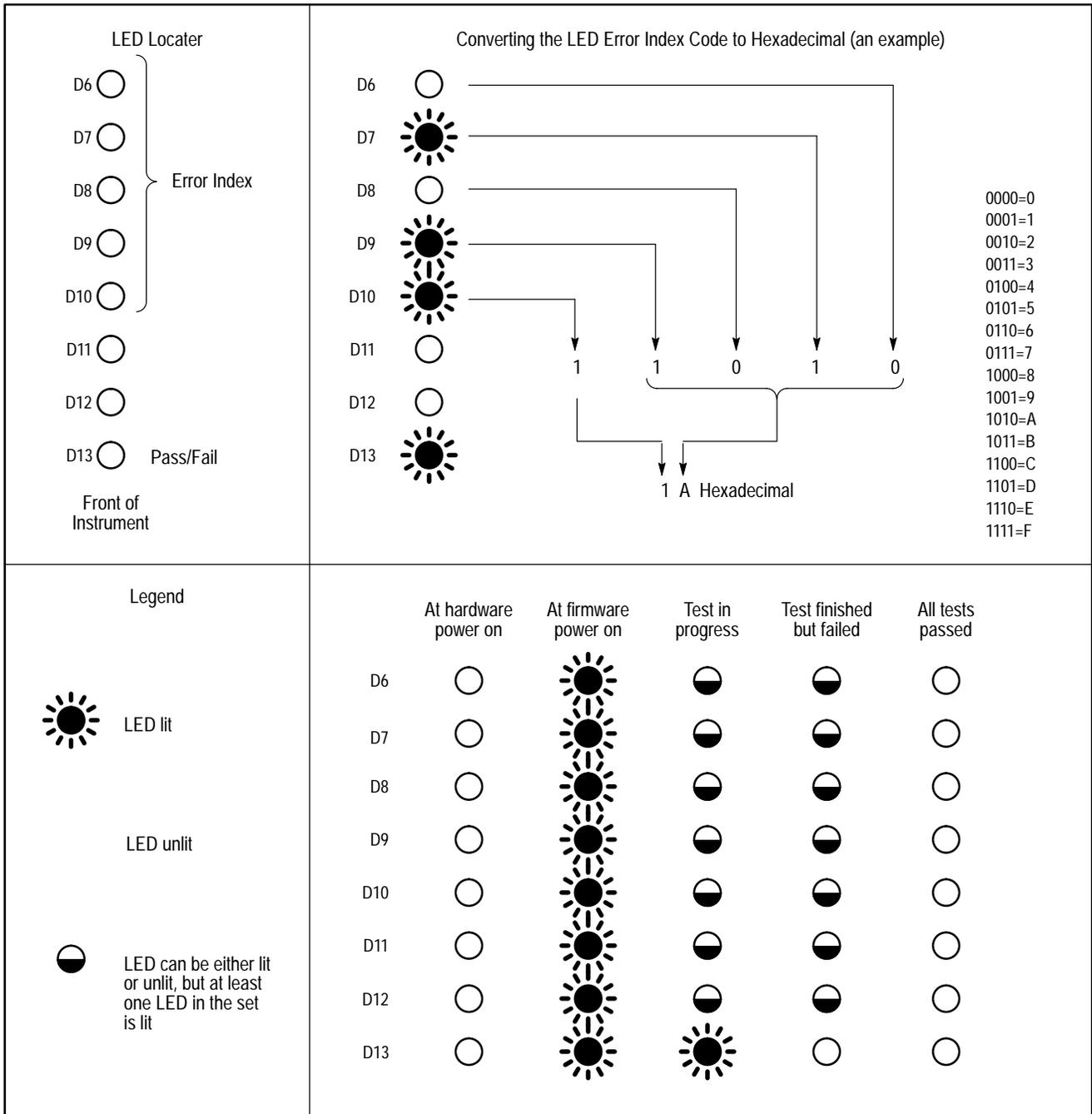


Figure 6-4: Bit Assignments for Diagnostic LEDs

Diagnostic Procedure

Table 6–2 and Figure 6–5 indicate how to proceed from each of the error index codes. Codes 1B and higher provide a message on the screen. You can press any button other than **SELECT** to see additional error information. This can be easier than decoding the error index code.

Table 6–2: Troubleshooting From the Error Index Code

If you see this Error Index Code ¹	Do This
01 through 09, 0B through 0F, 11	Replace the CPU card.
0A	Replace the front panel module and cable.
10	Follow the diagnostic procedure flowchart (Figure 6–5) starting at step A.
1A	Remove the cards one by one and retest. Always remove cards starting at the right and moving to the left. Stop before removing the CPU card. When you remove the last generator card, you will observe a configuration error (1B); ignore it and press SELECT to continue. If the test passes, the last card removed is faulty. If the 1A failure persists when only the CPU card is installed, then the possible sources of trouble are the CPU card or the backplane.
1B	Make sure the CPU card is installed in the left-most card slot, the Time Base card is installed in the next card slot, and the pulse and data generator cards are installed immediately to the right (starting with slot A). Any unused card slots must be to the right. If these conditions are met and the error persists, follow the procedure for Error Index Code 1A.
1E	Check the clock distribution cables (see Figure 6–1 on page 6–6). If they are installed correctly, follow the diagnostic procedure flowchart (Figure 6–5) starting at step B.
1F	Replace the time base card.

¹ These values are hexadecimal.

NOTE. If you observe multiple error messages, the power supply may be defective. Marginal power supply voltages can cause other apparently unrelated failures. If you believe the power supply is faulty, please contact your local Tektronix service representative.

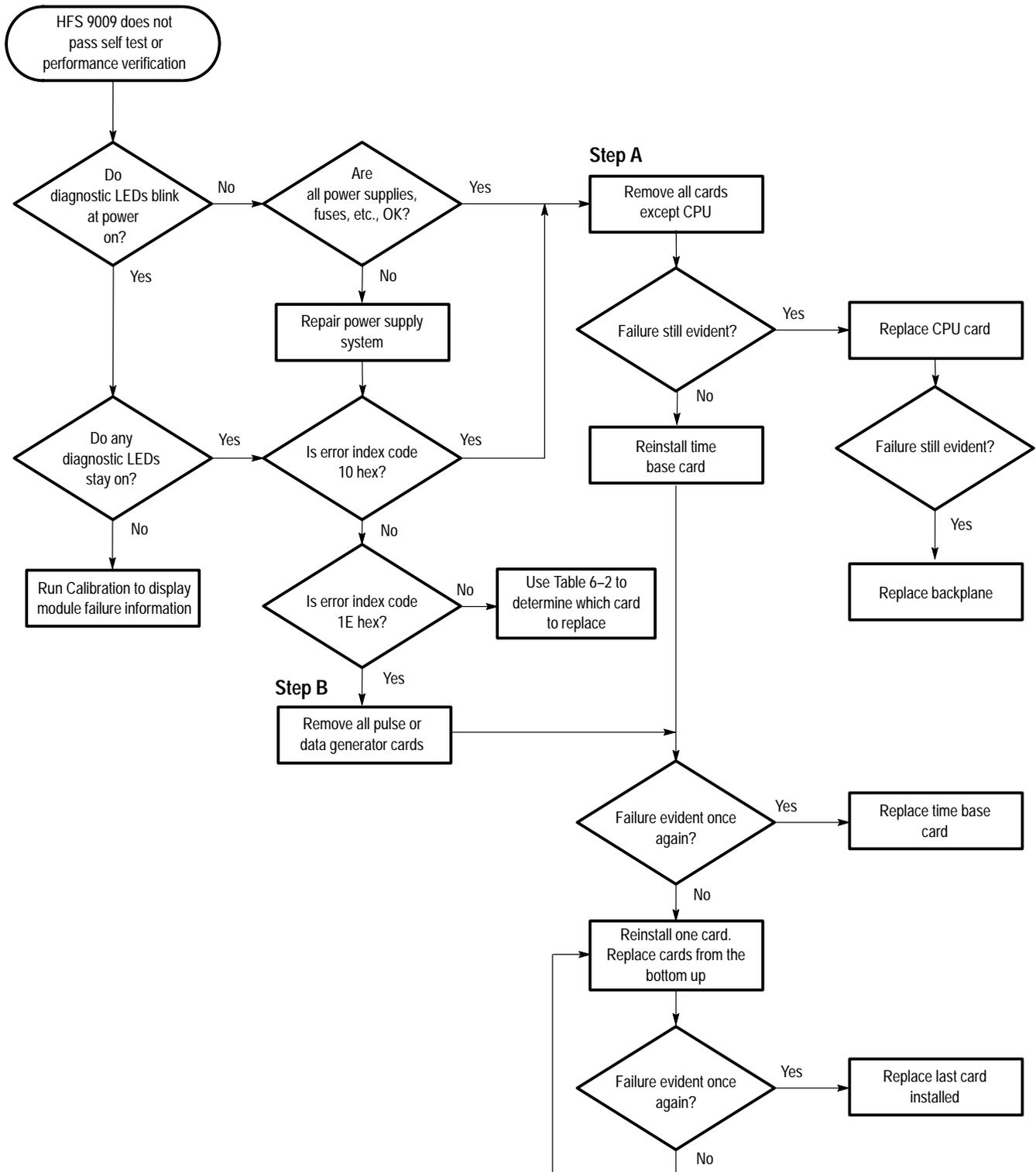


Figure 6-5: Diagnostic Procedure Flowchart

Options

The HFS 9009 is configured at the factory with the number and types of pulse and data generator cards specified at the time of ordering. Additional pulse and data generator cards can be installed if your HFS 9009 has available slots. Refer to the *Mechanical Parts List* section of this manual for part numbers and ordering information.

Installation should be performed by qualified service personnel. After installation, you should calibrate the HFS 9009 (refer to the *HFS 9000 User Manual* for calibration procedures). You should also run the Performance Verification procedures as described in this manual to ensure proper operation.

Additional options available from the factory are the rackmount kit and power cord options A1 through A5.



Electrical Parts List

Refer to the *Mechanical Parts List* section in this manual for a list of all parts.

Block Diagram

The HFS 9009 consists of three major electrical sections: the mainframe, front panel, and cards. Six types of cards may be installed in the HFS 9009:

- CPU card
- Time base card
- High speed pulse generator card (HFS 9PG1)
- Variable rate pulse generator card (HFS 9PG2)
- High speed data generator card (HFS 9DG1)
- Variable rate data generator card (HFS 9DG2)

Each HFS 9009 must have one CPU card, one time base card, and at least one pulse or data generator card. Figure 9-1 shows how these modules are interconnected.

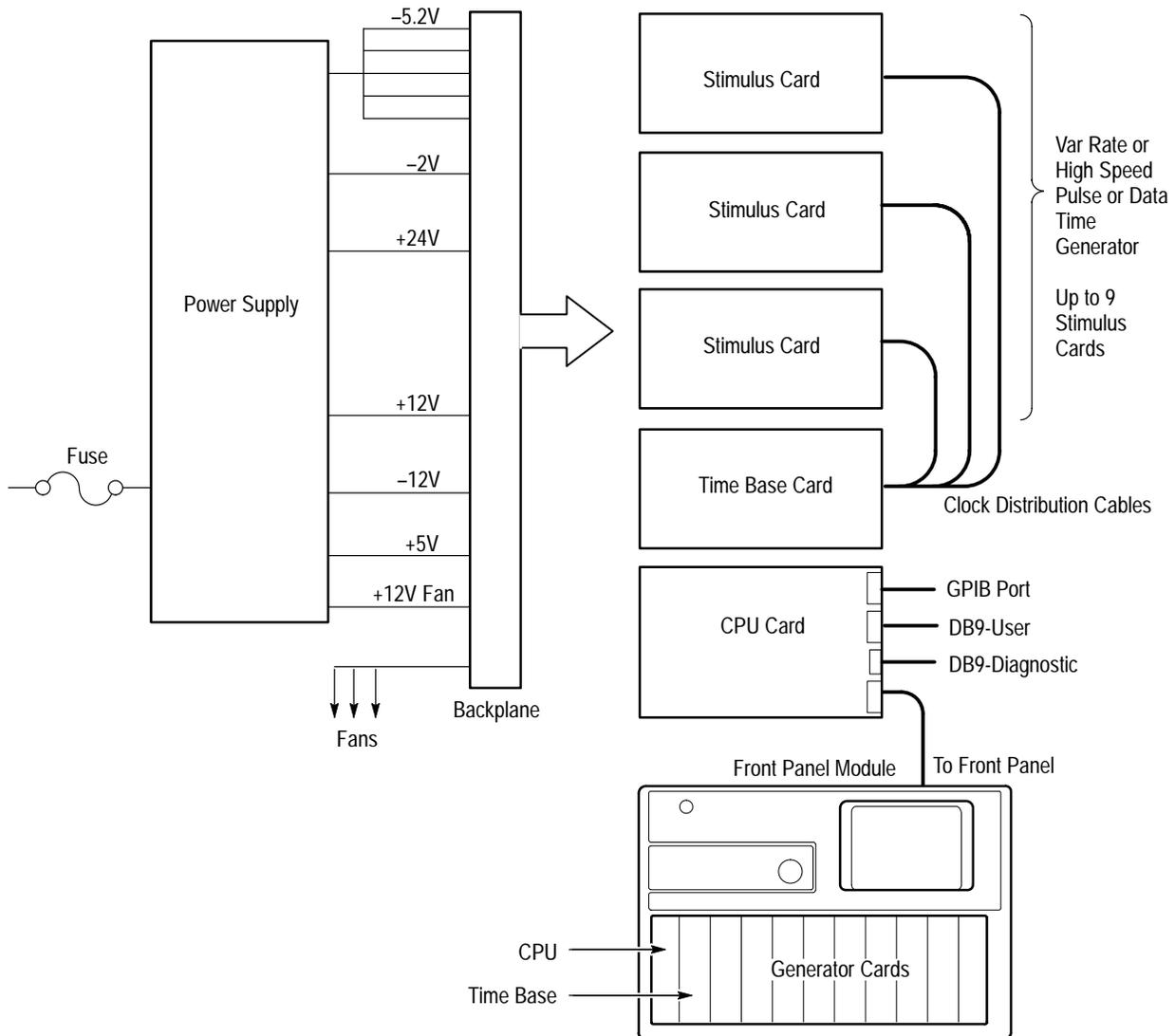


Figure 9-1: Module Block and Interconnection Diagram

Replaceable Parts List

This section contains a list of the replaceable modules for the HFS 9009. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Module Servicing

Modules can be serviced by selecting one of the following three options. Contact your local Tektronix service center or representative for repair assistance.

Module Exchange. In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1-800-TEK-WIDE, extension 6630.

Module Repair and Return. You may ship your module to us for repair, after which we will return it to you.

New Modules. You may purchase replacement modules in the same way as other replacement parts.

Using the Replaceable Parts List

This section contains a list of the mechanical and/or electrical components that are replaceable for the HFS 9009. Use this list to identify and order replacement parts. The following table describes each column in the parts list.

Parts List Column Descriptions

Column	Column Name	Description
1	Figure & Index Number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix Part Number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial Number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & Description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. Code	This indicates the code of the actual manufacturer of the part.
8	Mfr. Part Number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1-1972.

Mfr. Code to Manufacturer Cross Index The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

CROSS INDEX – MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
TK0191	SONY/TEKTRONIX	PO BOX 5209 TOKYO INTERNATIONAL	TOKYO JAPAN 100-31
TK0435	LEWIS SCREW CO	4300 S RACINE AVE	CHICAGO IL 60609-3320
TK1031	L AND M COMPONENTS DIV OF LAMB INDUSTRIES	PO BOX 25110	PORTLAND OR 97225
TK1148	ACACIA SALES INC (DIST)	7763 SW CIRRUS DR BLDG 26	BEAVERTON OR 97005-6452
TK1163	POLYCAST INC	9898 SW TIGARD ST	TIGARD OR 97223
TK1416	SHARP CORP	22-22 NAGAIKE-CHO ABENO-KU	OSAKA JAPAN
TK1543	CAMCAR/TEXTRON	600 18TH AVE	ROCKFORD IL 61108-5181
TK2469	UNITREK CORPORATION	3000 LEWIS & CLARK WAY SUITE 2	VANCOUVER WA 98601
OKB01	STAUFFER SUPPLY	810 SE SHERMAN	PORTLAND OR 97214
OKB05	NORTH STAR NAMEPLATE	5750 NE MOORE COURT	HILLSBORO OR 97124-6474
01536	TEXTRON INC CAMCAR DIV	1818 CHRISTINA ST	ROCKFORD IL 61108
2W944	PAPST MECHATRONIC CORP	AQUIDNECK INDUSTRIAL PK	NEWPORT RI 02840
72228	AMCA INTERNATIONAL CORP CONTINENTAL SCREW CO DIV	459 MT PLEASANT	NEW BEDFORD MA 02742
75915	LITTLEFUSE TRACOR INC SUB OF TRACOR INC	800 E NORTHWEST HWY	DES PLAINES IL 60016-3049
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001

Replaceable Parts List

Fig. & Index No.	Tektronix Part No.	Serial No.		Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
		Effective	Dscont				
10-1-1	950-1571-00			1	HOUSING TOP:	80009	950157100
-2	950-1314-00			10	SCREW:PHIL CNTR SINK 8-32 X .375	80009	950131400
-3	950-4332-00			10	SCREW:PHIL C SINK 8-32	80009	950433200
-4	378-0423-00			1	FILTER ASSY:	80009	378042300
-5	950-1229-00			1	HOUSING BOTTOM:	80009	950122900
-6	361-1683-00			2	CHASSIS SLIDE:	80009	361168300
-7	950-0895-55			8	SCREW:PHIL PNHD 8-32	80009	950089555
-8	950-2124-00			4	SCREW:PHIL PNHD 8-32X.50	80009	950212400
-9	950-1798-00			4	WASHER:NO. 8 INSIDE STAR	80009	950179800
-10	950-2722-00			4	PLASTIC FOOT:	80009	950272200
-11	950-1213-00			1	FILTER SUPPORT:	80009	950121300
-12	210-0115-00			1	SCREW:CAPTIVEPANEL 8-32	80009	210011500
-13	211-0848-00			2	SCREW:SHOULDERSLOTTED 4-40	80009	211084800

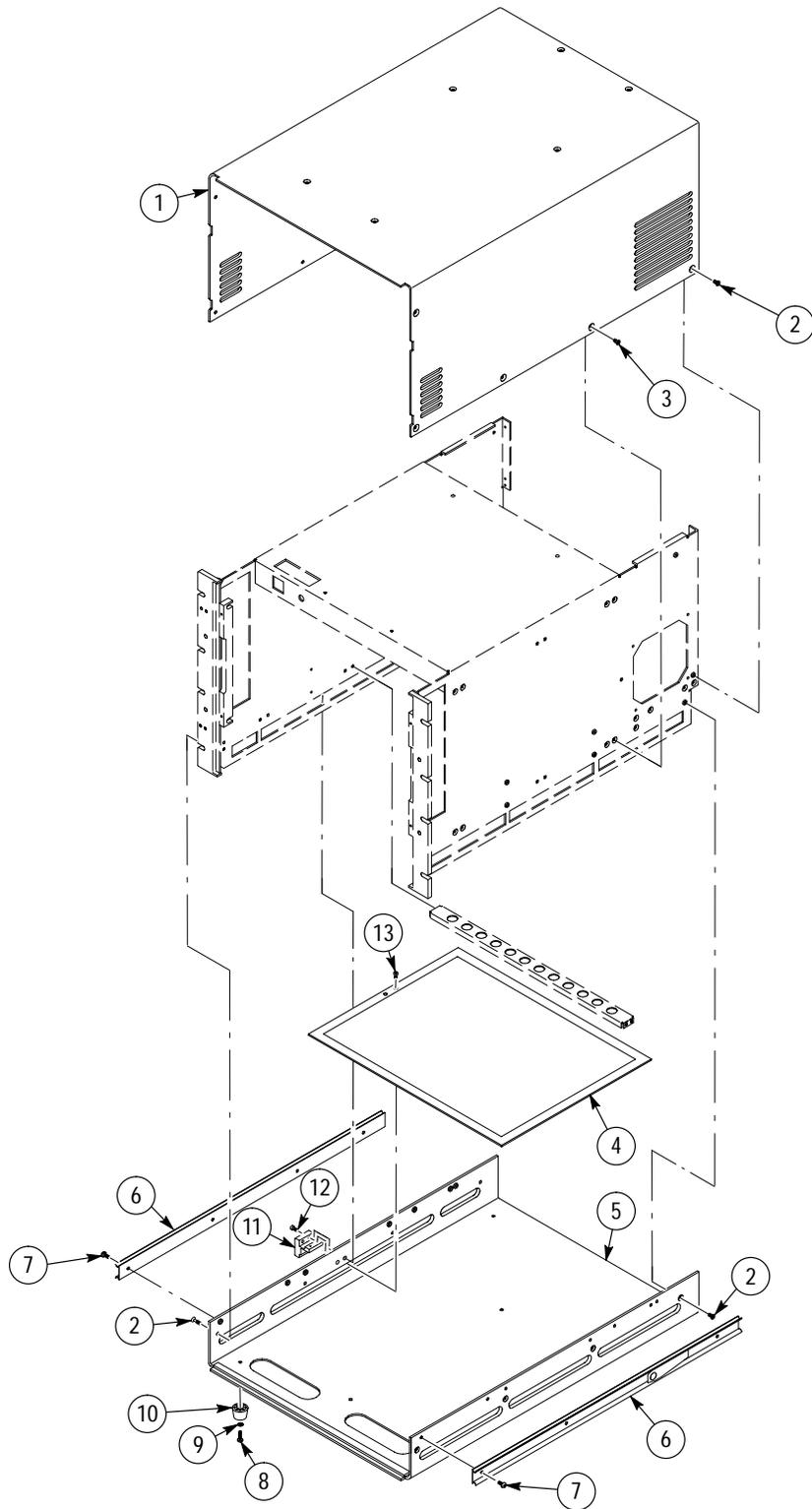


Figure 10-1: Cabinet

Replaceable Parts List

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
10-2-1	672-0317-02	B030222		1	CIRCUIT BD ASSY:HUMAN INTERFACE,BEZEL/LOW PANEL/TOP PANEL ASSY	80009	672-0317-02
-2	263-0101-00			1	SWITCH ASSEMBLY:ACTUATOR,PB,MOMENTARY	80009	263-0101-00
-3	210-0457-00			17	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	0KB01	ORDER BY DESCRIPTION
-4	175-2429-00			1	CA ASSY,SP,ELEC:34,28 AWG,15.0 L	1Y013	ORDER BY DESCRIPTION
-5	174-2142-01			1	CA ASSY,SP,ELEC:20,28 AWG,13.0 L	TK2469	174-2142-01
-6	174-2457-00			1	CA ASSY,SP,ELEC:16,26 AWG,3.0L,RIBBON,POLARIZED	TK2469	174-2457-00
-7	366-0582-01			1	KNOB:ENCODER	TK1163	ORDER BY DESCRIPTION
-8	950-3361-00			4	SCREW:PHIL C SINK 10-32, ZINC, 82 DEG	0KB01	950-3361-00

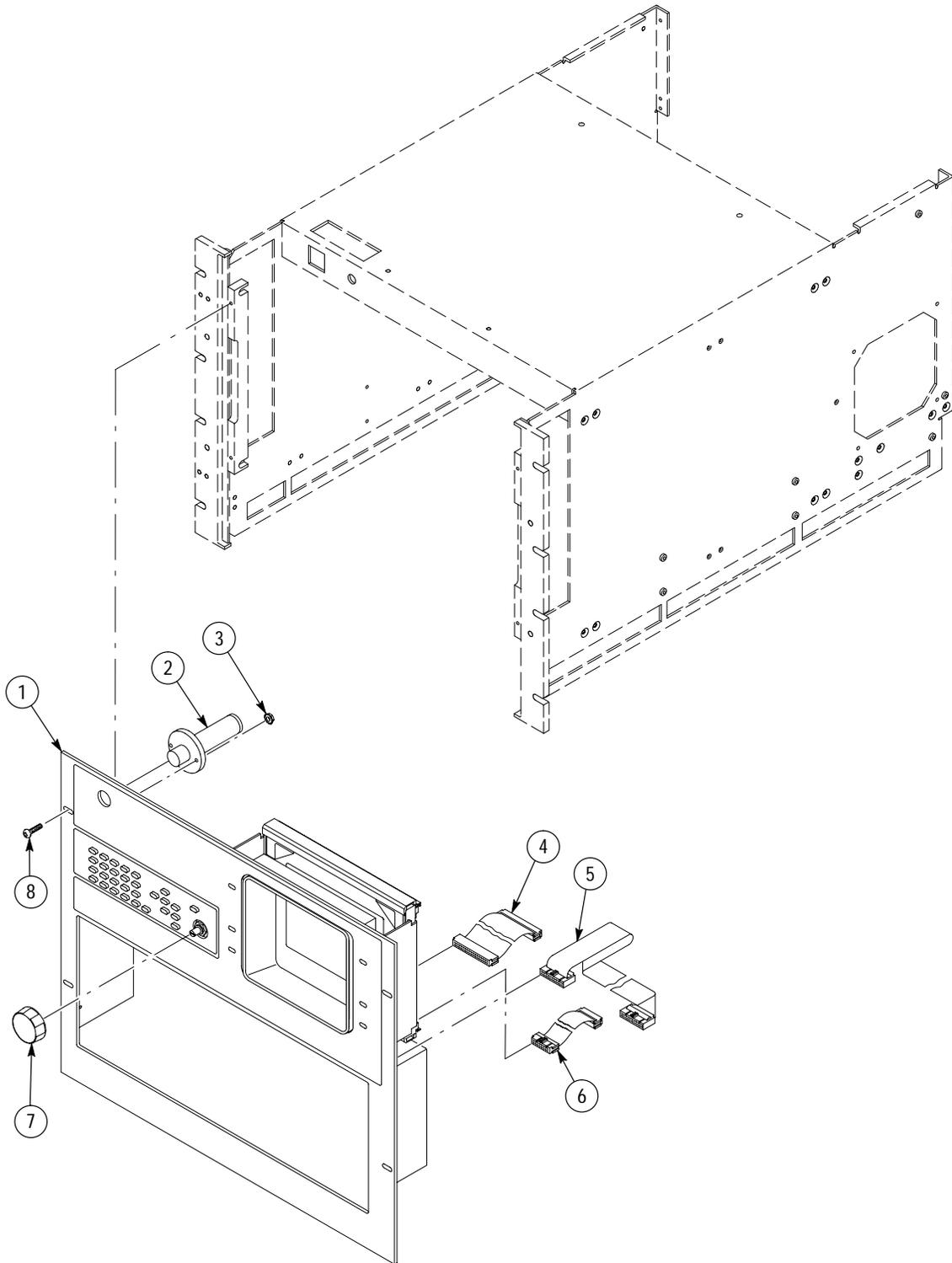


Figure 10-2: Front Panel

Replaceable Parts List

Fig. & Index No.	Tektronix Part No.	Serial No.		Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
		Effective	Dscont				
10-3-1	950-4332-00			4	SCREW:PHIL C SINK 8-32	80009	950433200
-2	950-1195-00			1	SWITCH,PWR:AC PWR DP PUSHBUTTON	TK1031	SPL6302.7.XX
-3	950-8711-00			1	LENS:FLAT GRN FOR 46	80009	950871100
	150-0217-00			1	DIODE,OPTO:LED,GRN,567MN,75MCD AT 14V/40MA	80009	150021700
-4	211-0866-00			13	SCREW:PHIL M2.5 X 10 BRZN	80009	211086600
-5	950-1237-00			1	CARD CAGE:TOP AND SIDES	80009	950123700
-6	211-0303-00			1	SCREW,MACHINE:4-40 X 0.25,FLH 100 DEG,STL	TK1543	ORDER BY DESC
-7	210-0586-00			1	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	TK0435	ORDER BY DESC
-8	950-1314-00			3	SCREW:PHIL CNTR SINK 8-32 X .375 BRIGHT ZINC	80009	950131400
-9	950-3792-00			1	INSULATING STRIP:	80009	950379200
-10	118-9121-00			1	BACKPLANE:AUTO CONFIGURE	80009	118912100
-11	950-1201-00			1	BRACKET:BACKPLANE	80009	950120100
-12	212-0202-00			1	SCREW: 8-32 X 5/16	80009	212020200
-13	950-1226-00			1	BOTTOM PLATE:PWR SPLY	80009	950122600
-14	950-1231-00			1	SUPPORT BAR:BOTTOM PLATE	80009	950123100
-15	950-1208-00			1	SPACER:BOTTOM	80009	950120800
-16	129-1455-00			1	STANDOFF:BOTTOM FRONT	80009	129145500
-17	950-3795-00			2	SCREW:M2.5 X 12 CHEESEHEAD	80009	950379500
-18	950-1202-00			2	CARD GUIDE:SUPPORT BRACKET	80009	950120200
-19	950-1271-00			1	FRONT PROFILE:BOTTOM	80009	950127100
-20	950-4337-00			2	SCREW:M2.5X8 CHEESEHEAD STL	80009	950433700
-21	950-1273-00			1	REAR PROFILE:BOTTOM	80009	950127300
-22	950-3776-00			1	CARD GUIDE:	80009	950377600
-23	950-3791-00			1	THREADED STRI:	80009	950379100
-24	950-3795-00			26	SCREW:M2.5 X 12 CHEESEHEAD	80009	950379500
-25	950-4337-00			1	SCREW:M2.5X8 CHEESEHEAD STL	80009	950433700
-26	950-1278-00			1	BRACKET:FRONT	80009	950127800
-27	950-4343-00			12	SCREW:PHIL CSNK 8-32 X 3-16 82 DEG BRT ZINC	80009	950434300
-28	211-0870-00			1	SCREW:M2.5X16 CHEESEHEAD	80009	211087000
-29	950-4151-00			1	BEZEL SPACER:PANEL DRW	80009	950415100
-30	950-1270-00			1	FRONT PROFILE:TOP	80009	950127000
-31	950-1272-00			1	BRACKET:TOP	80009	950-1272-00
-32	950-3361-00			4	SCREW:PHIL C SINK 10-32 X .5	80009	950336100
-33	950-0991-00			2	HANDLE:ALUMINUM BLK	80009	950099100
-34	950-8676-00			1	RACK EAR:LEFT	80009	950867600
-35	211-0875-00			16	SCREW:TORX DRIVE, PHIL, M4 X 8 FT HD BRZN	80009	211087500
-36	407-4136-00			2	BRACKET HANGER:ALUMINUM	80009	407413600
-37	212-0194-00			4	SCREW,MACHINE:8-32 X 0.636.FLH	80009	212019400
-38	012-1390-00			1	CABLE ASSEMBLY:COMPOSITE,2 SHLD,TWPR,13.0L	80009	012139000
-39	950-6023-00			1	RACK EAR:POLYCARB VX	80009	950602300

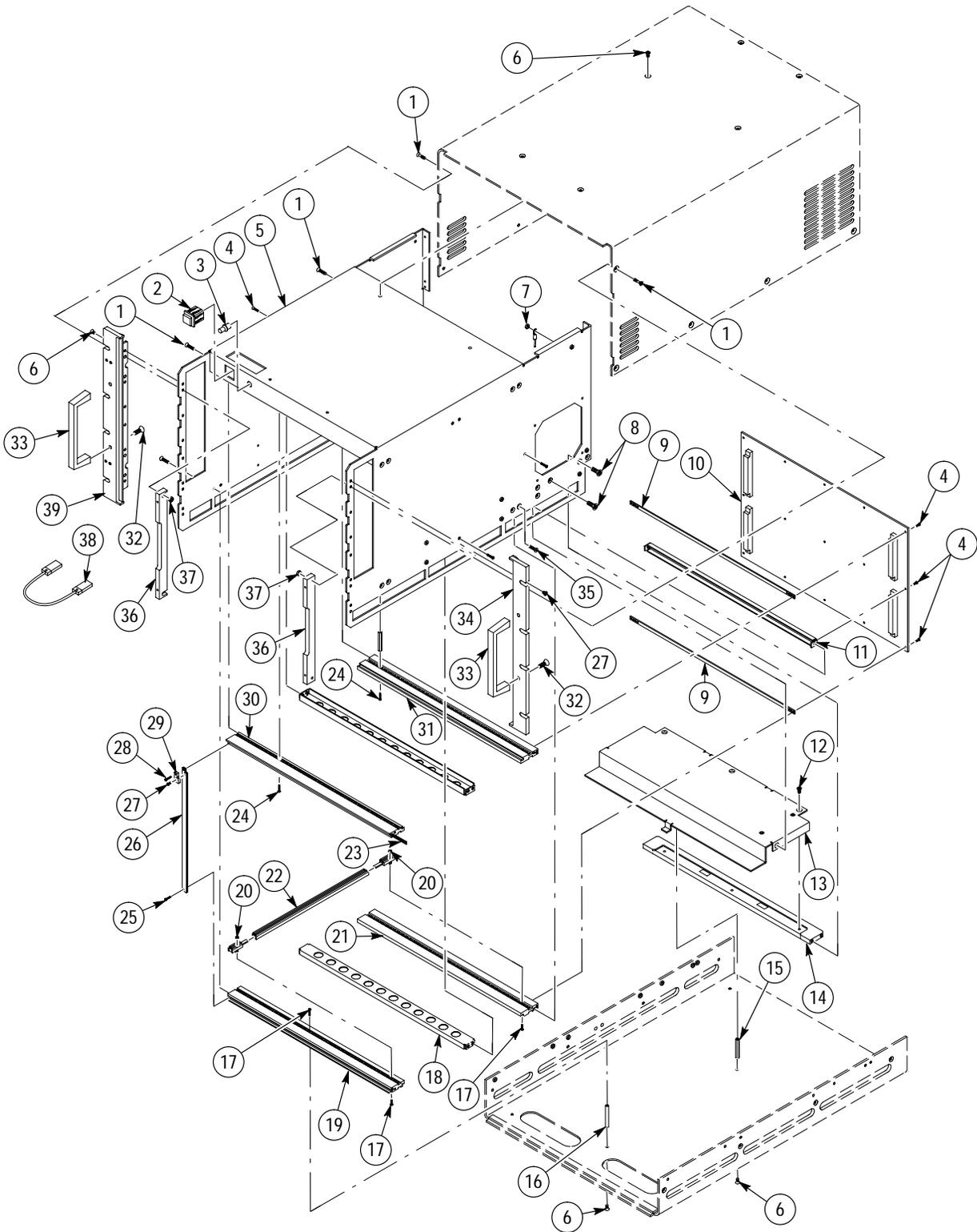


Figure 10-3: Mainframe and Chassis Parts

Replaceable Parts List

Fig. & Index No.	Tektronix Part No.	Serial No.		Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
		Effective	Dscont				
10-4-1	211-0303-00			2	SCREW,MACHINE:4-40 X 0.25,FLH 100 DEG,STL	TK1543	ORDER BY DESC
-2	950-1239-00			1	FAN PLATE:	80009	950123900
-3	950-1228-00			1	HANDLE BUSHING:	80009	950122800
-4	212-0203-00			1	SCREW:8-32 X 8/32 X 1	80009	212020300
-5	950-1227-00			1	HANDLE CAP:	80009	950122700
-6	950-2125-00			1	SCREW:PHIL PNHD 6-32X.75	80009	950212500
-7	950-1761-00			12	NUT:MACHINE,6-32 ZINC	80009	950176100
-8	119-1725-01			3	FAN,TUBEAXIAL:8 14.5VDC,6W,3200RPM,106CFM	2W944	4112 KX
-9	950-0895-00			4	SCREW:PHIL PNHD 8-32	80009	950089500
-10	950-1798-00			4	WASHER:NO. 8 INSIDE STAR	80009	950179800
-11	119-4885-00			1	POWER SUPPLY:	80009	119488500
-12	211-0522-00			4	SCREW,MACHINE:6-32 X 0.625,FLH,100 DEG,ST	TK0435	ORDER BY DESC
-13	950-1236-00			6	FAN BRACKET:	80009	950123600

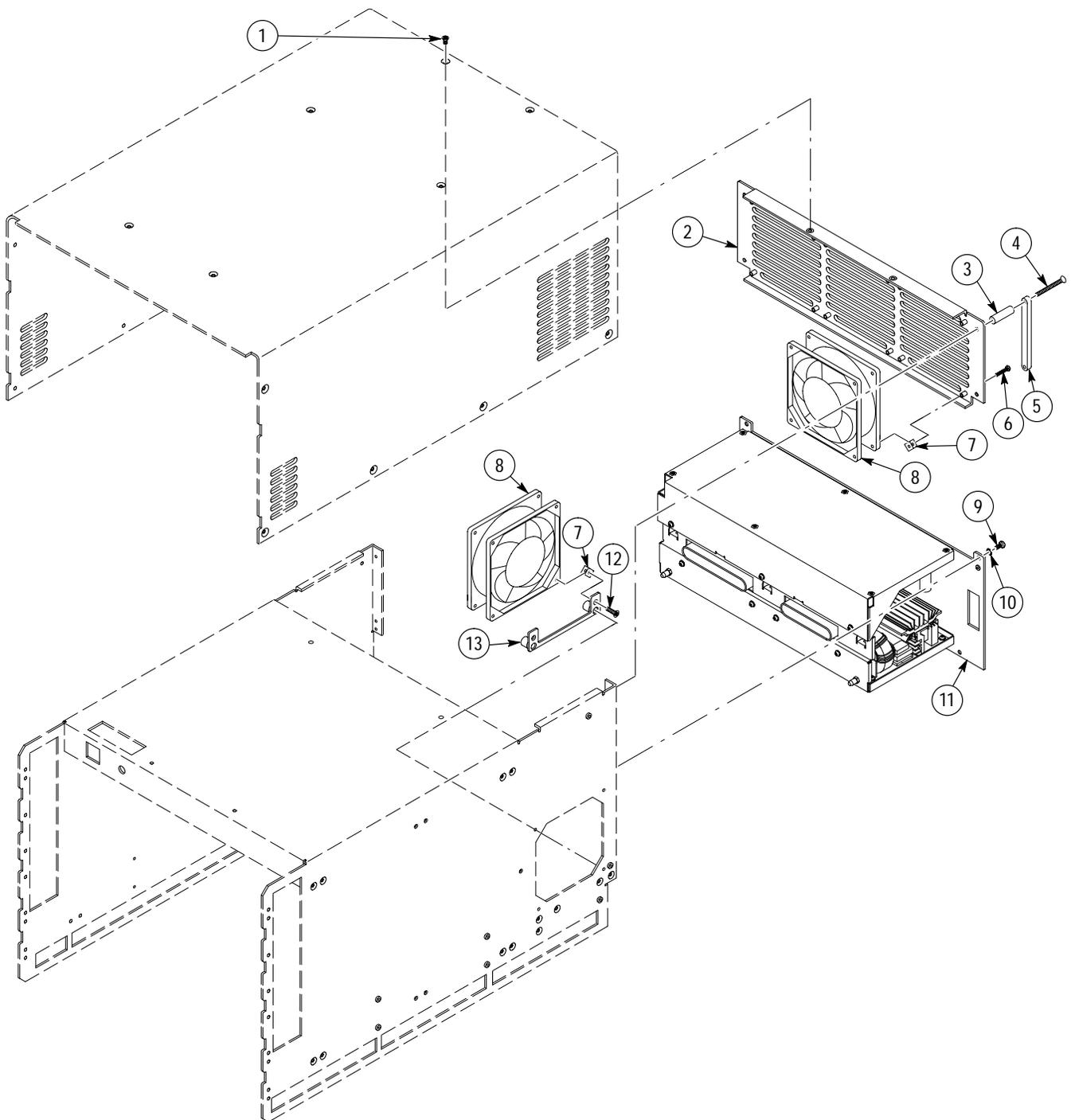


Figure 10-4: Power Supply and Fan Assembly

Replaceable Parts List

Fig. & Index No.	Tektronix Part No.	Serial No.		Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
		Effective	Dscont				
10-5-1	671-2581-05	B010100	B030206	1	CIRCUIT BD ASSY:CPU WITH FRONT PANEL	80009	671258105
10-5-1	671-2581-06	B030207	B030221	1	CIRCUIT BD ASSY:CPU WITH FRONT PANEL	80009	671258105
10-5-1	671-2581-07	B030222		1	CIRCUIT BD ASSY:CPU WITH FRONT PANEL	80009	671258105
-2	672-0316-01			1	CIRCUIT BD ASSY:TIMEBASE W/FRONT PANEL	80009	672031601
-3	672-1355-00			1	CIRCUIT BD ASSY:HI-SPEED PULSE W/FP	80009	672135500
-4	672-1356-02			1	CIRCUIT BD ASSY:VARIABLE RATE PULSE W/FP	80009	672135602

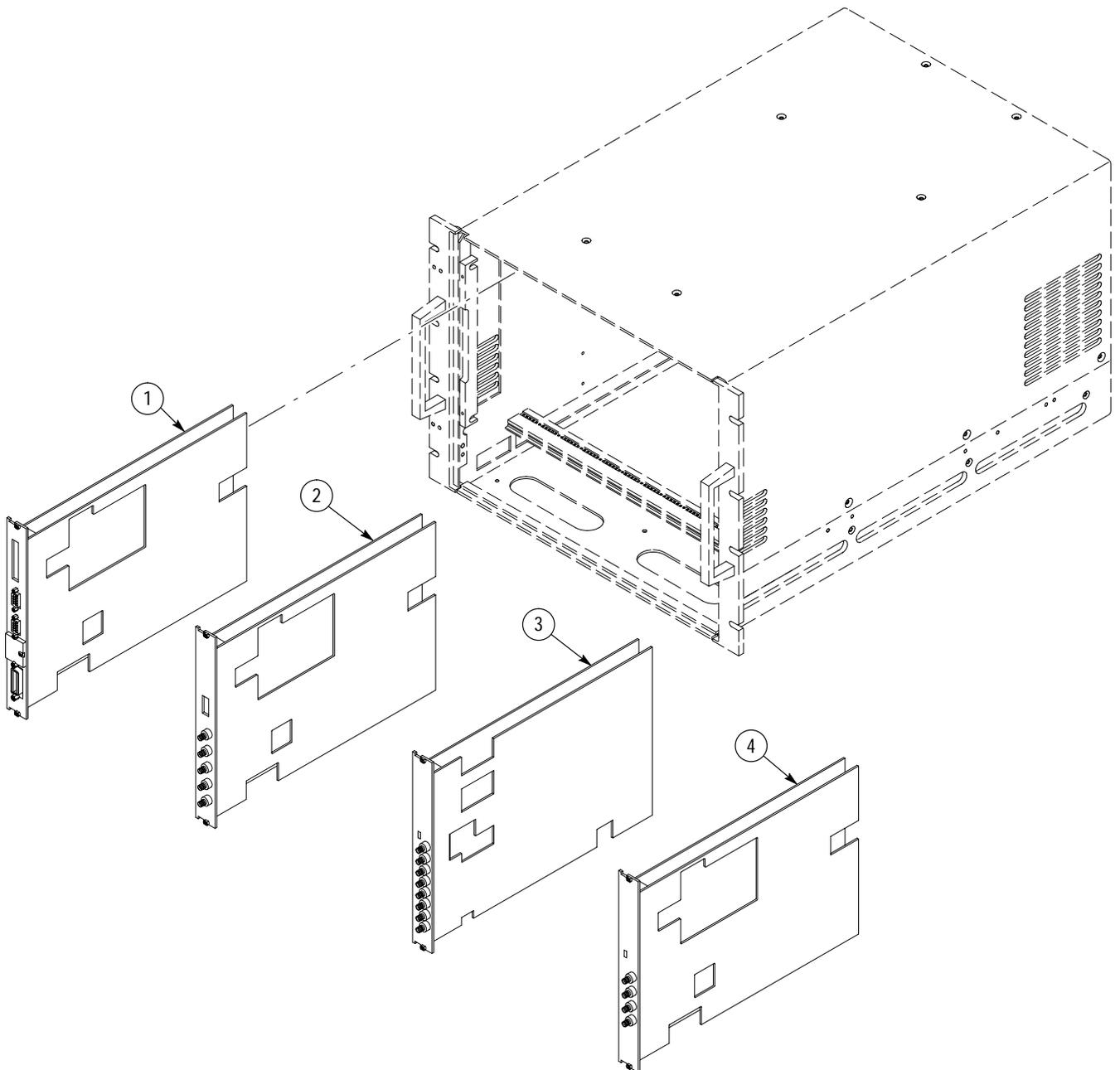


Figure 10-5: Circuit Cards

Replaceable Parts List

Fig. & Index No.	Tektronix Part No.	Serial No. Effective Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
STANDARD ACCESSORIES						
	012-1241-00		1	CABLE,INTCON:SHLD CMPST,RS-232	80009	012124100
	015-0572-00		1	ADAPTER,CONN:SMA FEMALE TO BNC MALE	91836	879-4-15-MA9
	015-1001-00		1	ATTENUATOR,FXD:2X ATTEN,50 OHM,SERIES	16179	2082-4573-06
	016-0537-00		1	POUCH,ACCESSORY:6 IN X 9 IN W/ZIPPER	80009	016053700
	070-8365-XX		1	MANUAL,TECH:USER REFERENCE	80009	070836501
	070-8366-XX		1	MANUAL,TECH:SERVICE REF	80009	070836601
	159-0256-00		1	FUSE,CARTRIDGE:15A,250V,FAST	75915	314-015
	161-0213-00		1	CABLE ASSY,PWR:3,16 AWG,2.5 M,GREY (STANDARD)	80009	161021300
	161-0209-00		1	CABLE ASSY,PWR:3,1.0MM SQ,220V,2.5 METERS (OPTION A1 ONLY-EUROPEAN)	80009	161020900
	161-0210-00		1	CABLE ASSY,PWR:3,1.0MM SQ,240V,2.5 METERS (OPTION A2 ONLY-UNITED KINGDOM)	80009	161021000
	161-0211-00		1	CABLE ASSY,PWR:3,1.0MM SQ,240V,2.5 METERS (OPTION A3 ONLY-AUSTRALIA)	80009	161021100
	161-0208-00		1	CABLE ASSY,PWR:3,16AWG,2.5M,13A/250V (OPTION A4 ONLY-NORTH AMERICAN)	80009	161020800
	161-0212-00		1	CABLE ASSY,PWR:3,1.0MM SQ,220V,2.5 METERS (OPTION A5 ONLY-SWITZERLAND)	80009	161021200
	174-1427-00		1	CABLE ASSY:COAX,RFD,50 OHM,20.0L,STR	TK2469	ORDER BY DESC

