Instruction Manual

Tektronix

DAS 92DM13A
Pentium Microprocessor Support

070–8707–00

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

Please check for change information at the rear of this manual.

First Printing: April 1993

Instrument Serial Numbers

Each instrument manufactured by Tektronix has a serial number on a panel insert or tag, or stamped on the chassis. The first letter in the serial number designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B010000	Tektronix, Inc., Beaverton, Oregon, USA
E200000	Tektronix United Kingdom, Ltd., London
J300000	Sony/Tektronix, Japan
H700000	Tektronix Holland, NV, Heerenveen, The Netherlands

Instruments manufactured for Tektronix by external vendors outside the United States are assigned a two digit alpha code to identify the country of manufacture (e.g., JP for Japan, HK for Hong Kong, IL for Israel, etc.).

Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077

Printed in U.S.A.

WARRANTY

Tektronix warrants that this product will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If any such product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Tektronix will provide such service at Customer's site without charge during the warranty period, if the service is performed within the normal on-site service area. Tektronix will provide on-site service outside the normal on-site service area only upon prior agreement and subject to payment of all travel expenses by Customer. When or where on-site service is not available, Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; or c) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

THIS WARRANTY IS GIVEN BY TEKTRONIX WITH RESPECT TO THIS PRODUCT IN LIEU OF ANY OTHER WARRANTIES, EXPRESSED OR IMPLIED. TEKTRONIX AND ITS VENDORS DISCLAIM ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. TEKTRONIX' RESPONSIBILITY TO REPAIR OR REPLACE DEFECTIVE PRODUCTS IS THE SOLE AND EXCLUSIVE REMEDY PROVIDED TO THE CUSTOMER FOR BREACH OF THIS WARRANTY. TEKTRONIX AND ITS VENDORS WILL NOT BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES IRRESPECTIVE OF WHETHER TEKTRONIX OR THE VENDOR HAS ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

SOFTWARE WARRANTY

Tektronix warrants that this software product will conform to the specifications in the documentation provided with the product, when used properly in the specified operating environment, for a period of three (3) months. The warranty period begins on the date of shipment, except that if the program is installed by Tektronix, the warranty period begins on the date of installation or one month after the date of shipment, whichever is earlier. If this software product does not conform as warranted, Tektronix will provide remedial services as described in the documentation provided with the product. Tektronix does not warrant that the functions contained in this software product will meet Customer's requirements or that operation of the programs will be uninterrupted or error-free or that all errors will be corrected.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for such service in accordance with the instructions received from Tektronix. If Tektronix is unable, within a reasonable time after receipt of such notice, to provide remedial services, Customer may terminate the license for this software product and return this software product and any associated materials to Tektronix for credit or refund.

This warranty shall not apply to any software product that has been modified or altered by Customer. Tektronix shall not be obligated to furnish service under this warranty with respect to any software product a) that is used in an operating environment other than that specified or in a manner inconsistent with the User Manual and documentation or b) when the software product has been integrated with other software if the result of such integration increases the time or difficulty of analyzing or servicing the software product or the problems ascribed to the software product.

THIS WARRANTY IS GIVEN BY TEKTRONIX WITH RESPECT TO THE LISTED PRODUCT IN LIEU OF ANY OTHER WARRANTIES, EXPRESSED OR IMPLIED. TEKTRONIX AND ITS VENDORS DISCLAIM ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. TEKTRONIX' RESPONSIBILITY TO PROVIDE REMEDIAL SERVICE WHEN SPECIFIED, REPLACE DEFECTIVE MEDIA, OR REFUND CUSTOMER'S PAYMENT IS THE SOLE AND EXCLUSIVE REMEDY PROVIDED TO THE CUSTOMER FOR BREACH OF THIS WARRANTY. TEKTRONIX AND ITS VENDORS WILL NOT BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES IRRESPECTIVE OF WHETHER TEKTRONIX OR THE VENDOR HAS ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Table of Contents

List of Figures

List of Tables

Preface: GUIDE TO DAS 9200 DOCUMENTATION

The Digital Analysis System (DAS) 9200 documentation package provides the information necessary to install, operate, maintain, and service the DAS 9200. The DAS 9200 documentation consists of the following:

- a series of microprocessor-specific **microprocessor support instructions** that describe the various microprocessor support packages.
- a **system user manual** that includes a beginning user's orientation, a discussion of DAS 9200 system-level operation, and reference information such as installation procedures, specifications, error messages, and a complete system glossary.
- a series of **module user manuals** that describe each of the DAS 9200 acquisition, pattern generation, and optional I/O modules.
- an **on-line documentation** package that includes context-sensitive technical notes.
- a **programmatic command language user manual** that describes the set of programmatic commands available for remotely controlling the DAS 9200.
- a series of **application software user manuals** that describe the various application software packages.
- a **technician's reference manual** that helps a qualified technician isolate DAS 9200 problems to the individual module level and determine corrective action (including on-site removal and replacement of modules).
- a **verification and adjustment procedures manual** that allows a qualified technician to make necessary adjustments and verify specifications of the mainframe and modules.
- a series of **workbooks** that teach concepts about the DAS 9200 acquisition modules and pattern generation modules.

GENERAL SAFETY SUMMARY/ MICROPROCESSOR SUPPORT

The general safety information in this summary is for operating and servicing personnel. Specific warnings and cautions can be found throughout the manual where they apply and may not appear in this summary. While using this product you may need to access parts of the mainframe system; if so, read the General Safety Summary in your system user manual for warnings and cautions related to operating the mainframe system.

TERMS IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION

CAUTION indicates a hazard to property, including the equipment itself, and could cause minor personal injury.

WARNING

WARNING indicates solely a personal injury hazard not immediately accessible as you read the marking.

DANGER indicates a personal injury hazard immediately accessible as you read the marking.

SYMBOLS AS MARKED ON EQUIPMENT

DANGER High Voltage	Protective ground (earth) terminal	ATTENTION Refer to manual

USE CARE WITH COVERS REMOVED

To avoid personal injury, remove jewelry such as rings, watches, and other metallic objects before removing the cover. Do not touch exposed connections and components within the product while the power cord is connected.

REMOVE FROM OPERATION

If you have reason to believe that the instrument has suffered a component failure, do not operate the instrument until the cause of the failure has been determined and corrected.

USE THE PROPER FUSE

To avoid fire hazard, use only a fuse of the correct type, voltage rating, and current rating.

REMOVE LOOSE OBJECTS

During disassembly or installation procedures, screws or other small objects may fall to the bottom of the mainframe. To avoid shorting out the power supply, do not power on the instrument until such objects have been removed.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Section 1: OVERVIEW

This section provides basic information on the following:

- the 92DM13A Microprocessor Support product
- software compatibility
- DAS 9200 configuration
- your Pentium microprocessor system requirements
- 92DM13A restrictions
- this manual

The 92DM13A Microprocessor Support product disassembles data from systems that are based on the Intel Pentium™ microprocessor. The 92DM13A product runs on a DAS 9200 logic analyzer equipped with two 92A96 Data Acquisition Modules combined to form one variable-width module.

The 92DM13A supports the Pentium microprocessor in a 273-pin PGA package.

This product consists of software on a floppy disk, a probe adapter, and this manual. The software includes setup files, a demonstration reference memory, symbol tables, and a disassembler program. A complete list of accessories and options is provided at the end of the mechanical parts list in *Appendix D: Parts Lists and Schematics*.

A demonstration reference memory is provided so you can see an example of disassembled instruction mnemonics. You can view the reference memory without connecting the DAS 9200 to your system under test. The reference memory is automatically installed on the DAS 9200 when you install the disassembler software. Directions for viewing this file are in *Section 4: Acquiring and Viewing Disassembled Data*.

To use this product efficiently, you need to have the following:

- knowledge of your DAS 9200 configuration and its operation
- knowledge of your Pentium microprocessor system
- this manual
- the *DAS 9200 System User Manual*
- the *92A96 Module User Manual,* Tektronix, Inc. 1992
- a user manual for your Pentium microprocessor
- LA-LINK (if you want to download symbols from your high-level development system)

DAS 9200 SYSTEM SOFTWARE COMPATIBILITY

The 92DM13A Microprocessor Support Product is compatible with DAS 9200 System Software Release 3, Version 1.3 or higher, DAS 92XTerm System Software Release 3, Version 1.3 or higher, and DAS 9202XT System Software Release 3, Version 1.3 or higher.

DAS 9200 CONFIGURATION

To use the microprocessor support product, your DAS 9200 must be equipped with two 92A96 Data Acquisition Modules combined to form one variable-width module with probe cables and standard probes.

The standard probe assemblies consist of four sets of one clock probe and three 8-channel data probes each. The clock probe (a single channel), and each channel of the 8-channel probe, has one signal connection and one ground connection. Leadsets and KlipChips are not required.

Figure 1-1 shows an overview of a DAS 9200 connected to a typical probe adapter.

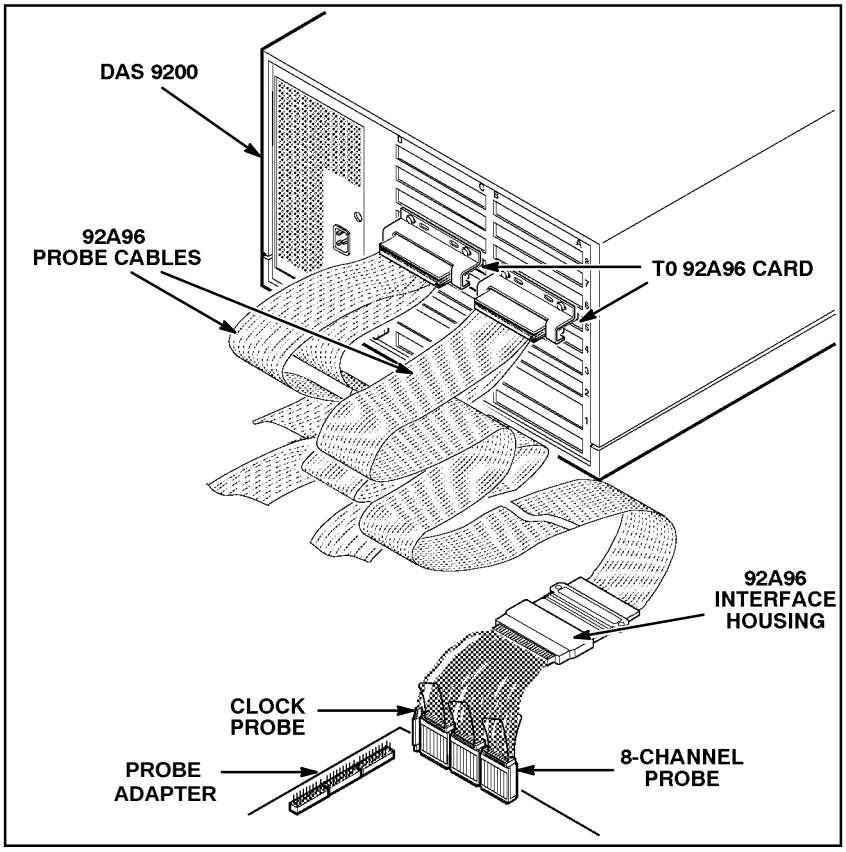

Figure 1-1. DAS 9200 connected to a typical probe adapter.

REQUIREMENTS AND RESTRICTIONS

You should review all electrical, environmental, and mechanical specifications in Appendix C as they pertain to your system under test. The remainder of this section describes other requirements and restrictions of the microprocessor support product.

System Clock Rate. The microprocessor support product supports the Pentium microprocessor at speeds of up to 66.66 MHz[1].

Pentium Cache. The cache on the Pentium microprocessor must be turned off for acquired data to be properly disassembled.

Probe Adapter Clearance. Your Pentium microprocessor system must have a minimum amount of clear space surrounding the Pentium microprocessor to accommodate the probe adapter. Figure C–2 in *Appendix C: Service Information* gives these dimensions.

[1] Specification at time of printing. Contact your DAS 9200 sales representative for current information on the fastest devices supported.

Probe Adapter Loading. Any electrical connection to your system adds an additional ac and dc load. The probe adapter was carefully designed to add a minimum load to your system. However, this additional load may affect the operation of the Pentium microprocessor in systems with extremely tight timing margins. Appendix C contains complete specifications on how the probe adapter affects your system.

Pentium System and Probe Adapter Cooling. You must be sure to retain the original level of cooling for your Pentium microprocessor system after you install the probe adapter. To maintain the required operating temperature, you may need to provide additional cooling for the probe adapter.

ABOUT THIS MANUAL

This manual is based on the assumption that you are familiar with the operation of the DAS 9200 mainframe and the 92A96 Acquisition Module. Therefore, details about system software and how to move through the menu structure are not provided. An overview of those functions is provided so that you do not need to consult another manual.

This manual provides detailed information on how to do the following:

- connect to your system under test
- setup disassembler software and use it
- view acquired data
- maintain disassembler hardware

Read *Section 5: General Purpose Analysis* if you are going to acquire and view timing or state data for purposes other than disassembly.

Manual Conventions

The following conventions are used in this manual:

- the terms disassembler and disassembler software are used interchangeably in reference to the 92DM13A software that disassembles bus cycles into instruction mnemonics and cycle types.
- due to the size of DAS 9200 fields, selection names and file names for the Pentium microprocessor support have been truncated to P5.
- the term system under test (SUT) is used to refer to the Pentium microprocessor system from which data is being acquired.
- references to 92A96 Modules include all versions of those modules unless otherwise noted.
- a signal that is active low has a pound sign (#) following its name.

Section 2: INSTALLATION AND CONNECTIONS

This section describes how to do the following:

- install the support software
- configure the DAS 9200
- position the modules in the DAS 9200
- configure the probe adapter
- connect the DAS 9200 to the system under test (SUT)

INSTALLING SOFTWARE

Before installing the microprocessor application software, you should be aware that there are three different versions of DAS 9200 system software: the 9201T version, the 92XTerm, and the 9202XT version. The 9201T version allows you to operate the DAS 9200 from a 9201T terminal. The 92XTerm version allows you to operate the DAS 9200 in an X window on a workstation. The 9202XT version allows you to operate the DAS 9200 in an X window on a 9202XT terminal.

NOTE

To use the microprocessor support package, you must install application software that is compatible with your DAS 9200 mainframe configuration and system software.

Two floppy disks are shipped with the 92DM13A support. To determine which floppy disk contains compatible application software, follow these steps:

1. Note the terminal type that will display the DAS 9200 user interface.
2. Power on the DAS 9200 mainframe or system, and press the Select Menu key.
3. Select the HW/SW Version menu in the Utilities menu column and press Return.
4. Look at the System Software line to find the version of system software loaded. Use Table 2-1 to choose the appropriate floppy disk to install.

Table 2-1
Choosing the Correct Floppy Disk

Terminal Type	System Software Line Information*	Install Floppy Disk Labelled
9200T/9201T	Release 3, Version 1.30†	DAS 9201T Application Software - 92DM13A
X window on a workstation or a 9202XT	Release 3, Version 1.30‡	DAS 92XTERM Application SW - 92DM13A

*The lowest versions supported are shown; higher version numbers within the same release are also supported.
†The 9201T version of this application should operate properly with DAS 9200 system software Release 2, Version 1.20. However, you should be aware that this application was actually tested using Release 3. Version 1.3, the currently supported version.

If you have any two types of DAS 9200 system software (9201T, 92XTerm, 9202XT), and you switch between the two, you must install compatible application software on each system.

If you try to install application software onto an incompatible system or terminal using DAS 9200 System Software Release 3, V1.1 or greater, an error message displays.

If you try to install application software onto an incompatible system or terminal using DAS 9200 System Software Release 3, V1.0 or lower, the system will install the software but it will not operate properly when you try to use it.

Install the disassembler software onto the DAS 9200 as follows:

1. Power on the DAS 9200 mainframe.
2. Insert the appropriate disk into the DAS 9200's floppy drive.
3. Press the Select Menu key and select the Disk Services menu.
4. Select Install Application in the Operation field of the menu.
5. Press F8: EXECUTE OPERATION and follow the on-screen prompts.

NOTE

After each install and load operation, a message appears on the screen informing you the operation succeeded or failed. If the message tells you the operation failed, you may need to remove applications or files from the hard disk and try installing or loading again. If the operation fails again, refer to Appendix A: Error Messages and Disassembly Problems.

If there is inadequate disk free space available on the hard disk, you must use the Remove Application or Delete File function of the Disk Services menu to free up enough disk space to install the support software. The approximate space required to install the software is listed on the label of the floppy disk.

CONFIGURING THE VARIABLE-WIDTH MODULE

To acquire data from a Pentium microprocessor, two 92A96 Modules are required. They must be configured into one variable-width module.

When using a variable-width module, both 92A96 Modules must be positioned in adjacent DAS 9200 slots in a single mainframe. You cannot use slots 1 or 8 when creating a variable-width module. The modules do not need to have the same memory depth.

Check the System Configuration menu to see if the module is defined correctly. Figure 2-1 shows how the Sys Config menu looks when two 92A96 Modules are combined into one variable-width module.

The 92A96 Module in the higher-numbered slot is referred to as the HI module; the module in the lower-numbered slot is referred to as the LO module. Probe connections on the probe adapter board are labeled to identify which module and which probe group connects to them. For example, HI_A0 indicates the A0 probe group from the HI module.

Clock pins on the probe adapter do not have the HI/LO designation; they are just labeled CK0, CK1, CK2, and CK3. Each pair of clock pins connect to the same signal on the probe adapter. The clock probes from both modules must connect to the appropriate clock pins for Custom clocking to function properly.

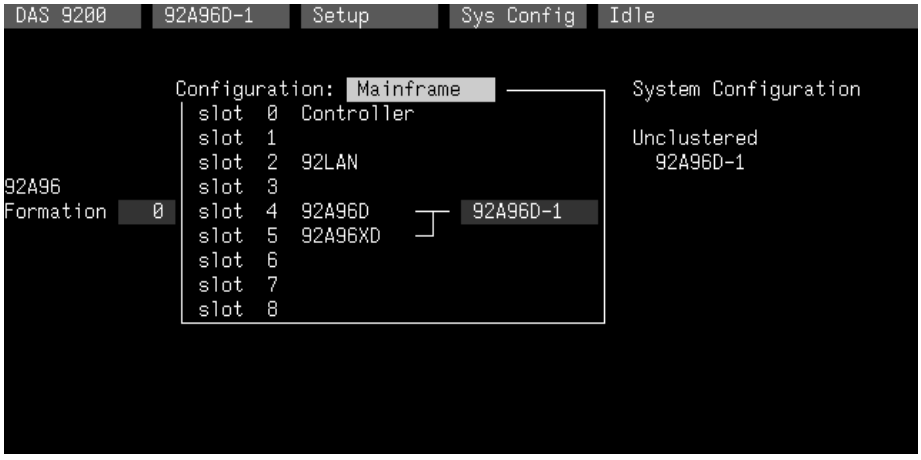

Figure 2-1. Sys Config menu with a variable-width module defined.

Refer to your module user manual for information about variable-width modules, and for additional information about connecting probe cables, and positioning and installing 92A96 Modules.

In a system with many modules, it is easier to identify which modules are connected to the probe adapter if slot number labels are applied to the 92A96 probe interface housings and DAS 9200 mainframe. Figure 2-2 shows where to apply slot number labels.

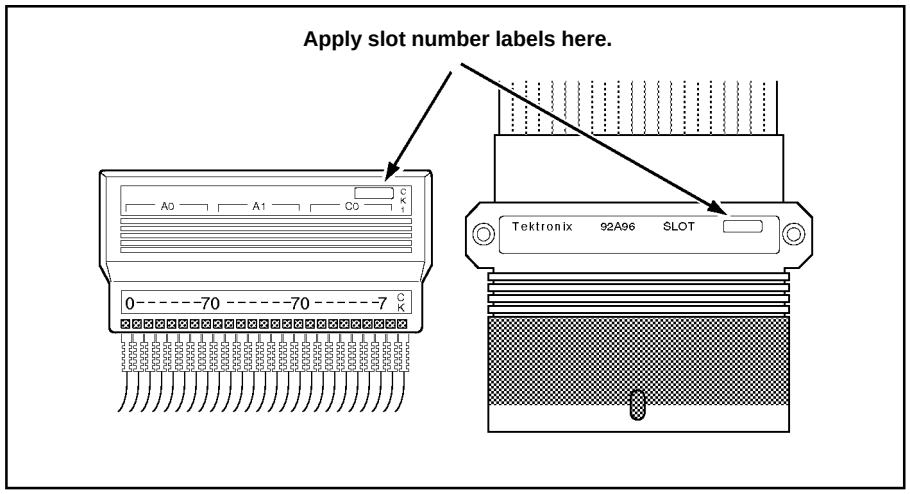

Figure 2-2. Applying slot number labels.

CONFIGURING THE PROBE ADAPTER

There are three jumpers on the probe adapter. One is set to match the input clock of the Pentium microprocessor. The second is used to configure the probe adapter for either disassembler operation or to acquire timing data. The third is used to help the circuitry track BOFF and HLDA cycles.

CLK Jumper

The CLK jumper (J1905) should be placed in the ≥33 position to acquire data from a system running at or faster than 33 MHz. The jumper should be placed in the <33 position to acquire data from a system running slower than 33 MHz.

Figure 2-3 shows the location of J1905 on the probe adapter.

Disassembly/Timing Jumper

The Disassembly/Timing jumper (J1902) should be placed in the D position to acquire disassembled data, and in the T position to acquire timing data. Table 2-2 shows how to position this jumper depending on the type of clocking you are using and the type of display you want to view.

Table 2-2
Disassembly/Timing Jumper Information

J1902 Position	Clocking	Display Menu
D (Disassembly)	Custom	Disassembly, State or Graph
T (Timing)	Internal	Timing
	External	Timing or State

Figure 2-3 shows the location of J1902 on the probe adapter.

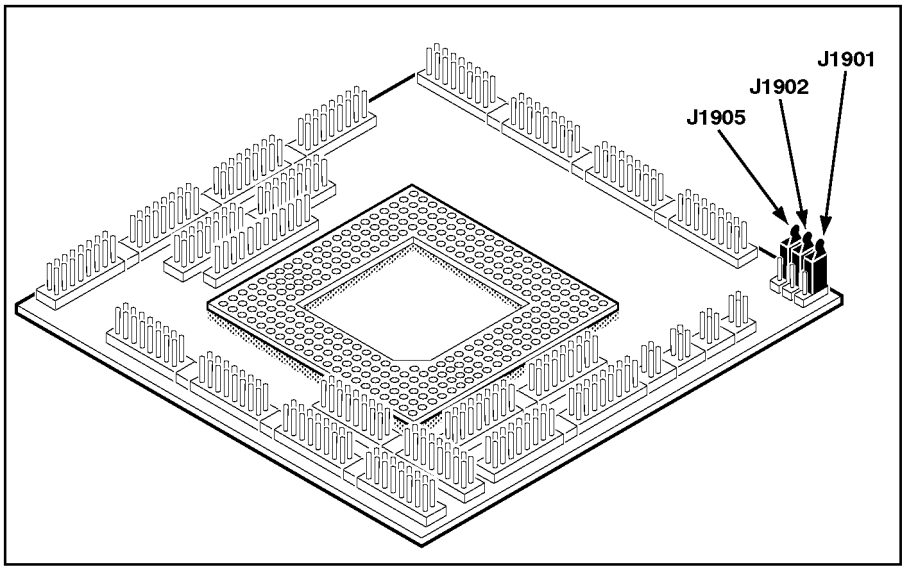

Figure 2-3. Jumper locations on the probe adapter.

Tracking Jumper

The Tracking jumper (J1901) should not need to be moved from the default position; pins 1 and 2 connected. The only time this jumper should be moved is when the tracking circuitry malfunctions. An indication of such a malfunction is when you see activity on the bus during a BOFF or HLDA cycle that is uncharacteristic of the Pentium microprocessor. When the jumper is in the 2, 3 position, the circuitry on the probe adapter does not track BOFF and HLDA cycles. A data

sample will show that such a cycle occurred but it will not contain meaningful information.

This jumper only affects the probe adapter when J1902 is in the D position.

Figure 2-3 shows the location of J1901 on the probe adapter.

CONNECTING TO THE SYSTEM UNDER TEST

Before you connect to the SUT, you must connect the standard probes to the 92A96 Module card. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to *Appendix C: Service Information* for the required clearances.

To connect the DAS 9200 to the SUT, do the following:

1. Turn off power to your SUT. It is not necessary to turn off power to the DAS 9200.

   CAUTION

   Static discharge can damage the microprocessor, the probe adapter, the podlets, or the 92A96 Module. To prevent static damage, handle the microprocessor only in a static-free environment.

   Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground jack located on the back of the DAS 9200. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown Figure 2-4. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the Pentium microprocessor from your SUT.
5. Line up the pin A1 indicator on the microprocessor with the pin A1 indicator on the probe adapter board.

CAUTION

Failure to correctly place the microprocessor into the probe adapter may permanently damage the microprocessor once power is applied.

6. Place the microprocessor into the probe adapter as shown in Figure 2-4.

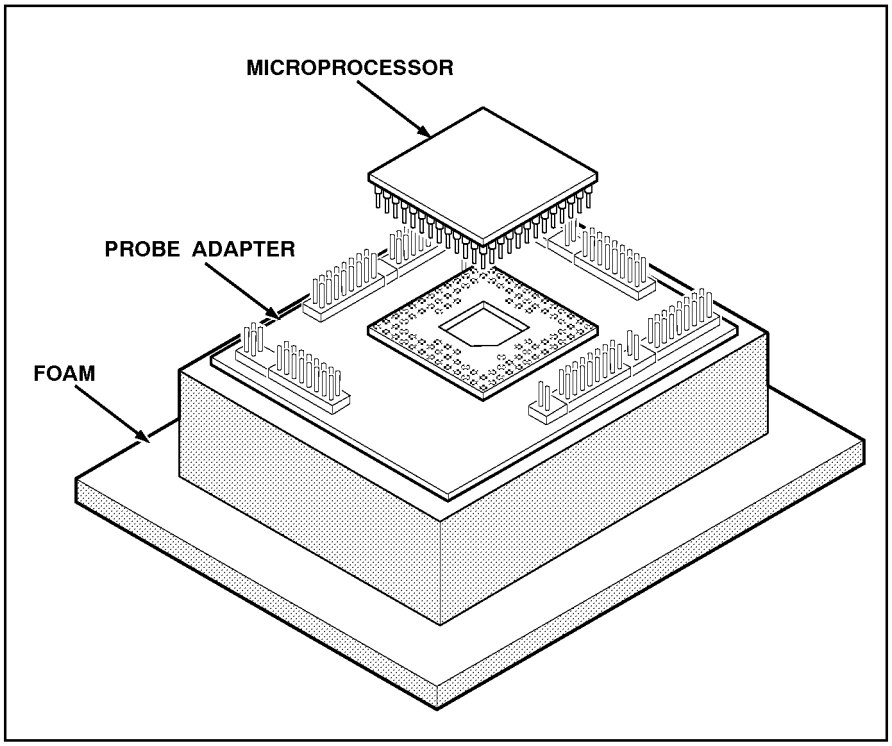

Figure 2-4. Placing the microprocessor into a typical PGA probe adapter.

7. Connect the clock and 8-channel probes to the probe adapter as shown in Figure 2-5. Match the channel groups and numbers on the interface housing to the corresponding pins on the probe adapter.

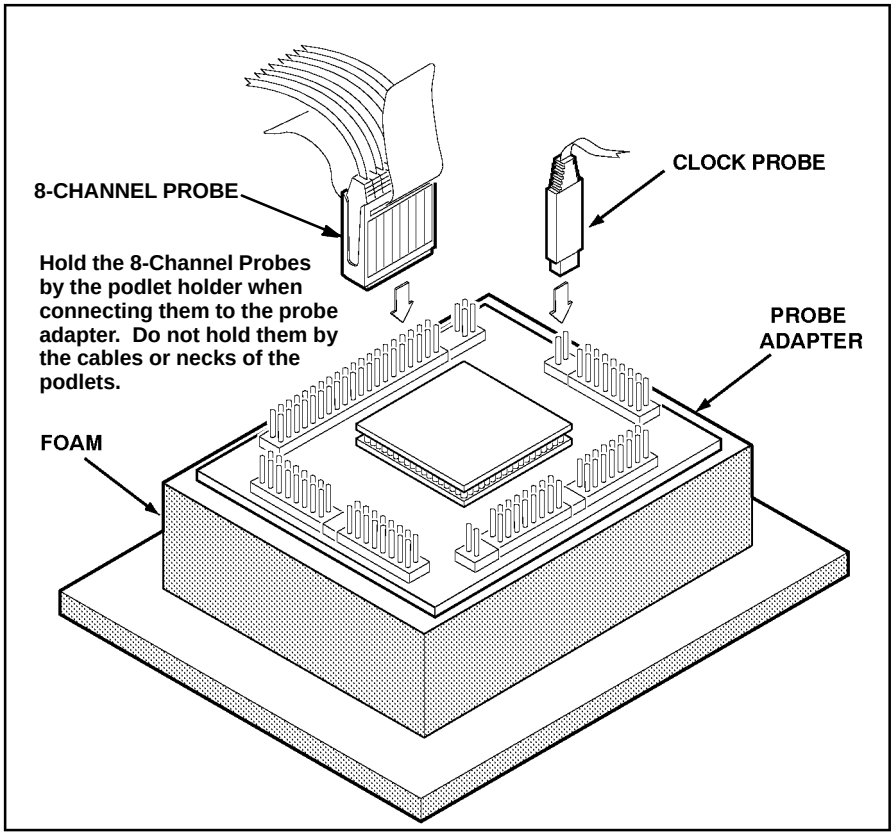

Figure 2-5. Connecting the podlets to a typical PGA probe adapter.

8. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on your SUT.
9. Place the probe adapter onto the SUT as shown in Figure 2-6.

NOTE

You may need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind this may increase loading, which can reduce the electrical performance of your probe adapter.

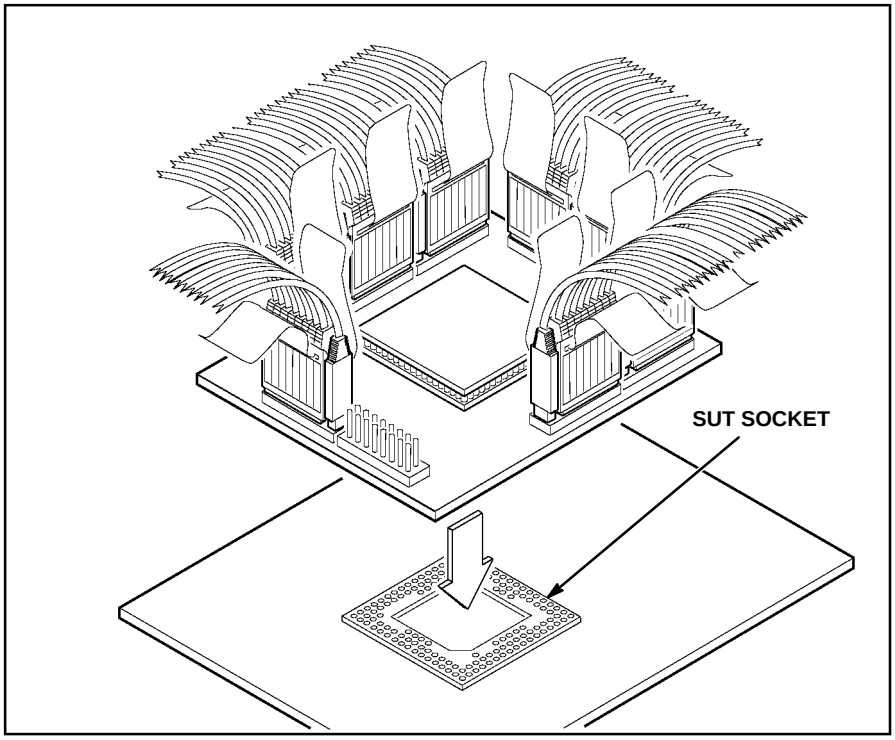

Figure 2-6. Placing a typical PGA probe adapter onto the SUT.

Section 3: SETTING UP DISASSEMBLER SOFTWARE

This section tells how to prepare the disassembler software to acquire data and discusses the following:

- loading support software
- channel groups and assignments
- changes that affect disassembly
- clocking options
- symbols
- triggering

Before you acquire and disassemble data, you need to load support software, and specify setups for clocking, triggering, and using symbols. The disassembly software provides default values for each of these setup controls, but you can change them as needed.

LOADING DISASSEMBLER SOFTWARE

To load the disassembler software, follow these steps:

1. Press the Menu Select key, select the appropriate 92A96 Module, select its Configuration menu, and press Return.
2. Select P5 in the Software Support field.
3. Press F8: EXECUTE OPERATION.

When you load the support software, the Channel, Clock, and Trigger menus are automatically set up to acquire data from your Pentium microprocessor system. You can change the setups in the Clock and Trigger menus as needed. Refer to *Channel Groups and Assignments* for information on what can be changed in the Channel menu.

CHANNEL GROUPS AND ASSIGNMENTS

The disassembler software automatically defines the channel groups for the microprocessor. The channel groups for the Pentium microprocessor are Address, Data, Data_Lo, DataSize, Control, Cache, Debug, Misc, Misc2, and BT. These groups cannot be changed; however, you can define and display additional groups. If you want to know which signal is in which group, refer to the channel assignment tables in *Appendix C: Service Information*. Channel assignments are also shown in the 92A96 Channel setup menu.

CHANGES THAT AFFECT DISASSEMBLY

You can change part of the default setups for the 92A96 Module. However, keep in mind that if you change any of the following items, the disassembled data will be affected:

- threshold voltage
- display polarity

CLOCKING

You can use the Clock menu to set clocking choices to control data sampling. The 92DM13A software offers a customized clocking selection for the Pentium microprocessor. This clocking choice (Custom) is the default selection whenever you select the P5 Support in the Configuration menu.

The 92DM13A software provides two modes for acquiring Pentium microprocessor data: Alternate Bus Master Cycles Included or Alternate Bus Master Cycles Excluded. The default is Alternate Bus Master Cycles Excluded. You can change the clocking mode by changing the Alternate Bus Master Cycles option field in the Clock menu.

Alternate Bus Master Cycles. An alternate bus master cycle is defined as the Pentium microprocessor giving up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Backoff cycles will always be acquired regardless of the Alternate Bus Master selection.

Figure 3-1 shows the Clock menu. A description of how cycles are sampled by the disassembler is found in Appendix B.

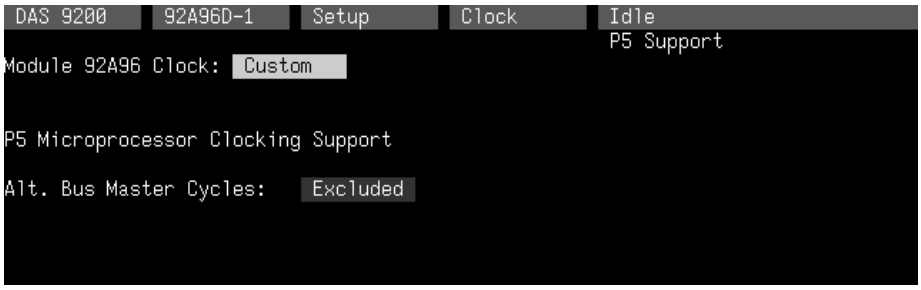

Figure 3-1. Clock menu.

Disassembly will not be correct with the Internal or External clocking modes. Refer to *Section 5: General Purpose Analysis* for a description of using these other clock selections with this microprocessor support package.

To select the clocking mode, do the following:

1. Press the Select Menu key.
2. Select the Clock menu for the module you want to use.
3. Move the cursor to the Alternate Bus Master Cycles field and select one of the following types of clocking:
   - Included
   - Excluded

SYMBOLS

Symbols can be used to represent a specific channel group value or a range of channel group values (defined by upper and lower bounds).

You can use symbol tables to display channel group information symbolically in the State and Disassembly menus, to control triggering, and to perform data searches. There is a symbol table file (named P5_Ctrl) supplied by the disassembler software that replaces specific Control channel group values.

Table 3-1 shows the name, bit pattern, and meaning for the symbols in the file P5_Ctrl, the Control group symbol table.

Table 3-1
P5_Ctrl Symbol Table Definitions

Symbol	Control Group Value PRDY BUSCHK# SCYC LAST_D BOFF# M/IO# INIT RESET_L SMIACT# LOCK# AHOLD HLDA D/C# W/R#	Meaning
RESET	X 1 X X X X X X X X X X X X	Microprocessor reset
FETCH	X 0 0 X X 1 X X X 0 1 1 0 0	Memory code read (Opcode fetch)
LOCKED_RD	X 0 0 X X 0 X X X 0 1 X 1 0	Locked memory read
LOCKED_WR	X 0 0 X X 0 X X X 0 1 X 1 1	Locked memory write
MEM_READ	X 0 0 X X X X X X 0 1 1 1 0	Nonopcode memory read cycle
MEM_WRITE	X 0 0 X X X X X X 0 1 1 1 1	Any memory write
I/O_READ	X 0 0 X X X X X X 0 1 0 1 0	Read from an I/O port
I/O_WRITE	X 0 0 X X X X X X 0 1 0 1 1	Write to an I/O port
MEM_RD/WR*	X 0 0 X X X X X X 0 1 1 1 X	Nonopcode memory read or write
I/O_RD/WR*	X 0 0 X X X X X X 0 1 0 1 X	Read from or write to an I/O port
READ*	X 0 0 X X X X X X 0 1 X 1 0	Any memory or I/O read except an Opcode Fetch or Int Ack cycle
WRITE*	X 0 0 X X X X X X 0 1 X 1 1	Any memory or I/O write
INT_ACK	X 0 0 X X X X X X 0 1 0 0 0	Interrupt Acknowledge cycle
SPECIAL	X 0 0 X X X X X X 0 1 0 0 1	Special cycle
RESERVED	X 0 0 X X X X X X 0 1 1 0 1	Reserved
ALT_B_MTR	X 0 0 X X X X X X 1 X X X X	Bus released to another bus master
BOFF	X 0 X X X X X X X X 0 X X X	Back Off bus cycle
PROBE_MD	X 0 1 X X X X X X X X X X X	The microprocessor is in probe mode
BUS_CHECK*	X 0 X 0 X X X X X 0 1 X X X	Unsuccessful completion of a bus cycle
LOCKED*	X 0 X 1 X 0 X X X X X X X X	Any locked cycle
SPLIT_CYC*	X 0 X 1 X 0 1 X X X X X X X	A split bus cycle
SYSMGT_MD*	X 0 X X 0 X X X X X X X X X	The microprocessor is in System Management Mode

*These symbols are for triggering purposes only; they are not displayed.

Refer to *Triggering* in this section and *Displaying the Address Group Symbolically* in Section 4 for more information on using and displaying symbolic values. Refer also to *Searching Through Data* in Section 4 for information on how to use symbol table values for data searches.

Copying and Editing the Predefined Symbol Tables. You cannot directly edit any symbol tables supplied by microprocessor support. But you can make a copy of a predefined symbol table and then edit the copy for your specific use.

To create a new symbol table, follow these steps:

1. Select the Symbol Editor menu from the Menu Selection overlay.
2. Press F2: FILE FUNCTIONS.
3. Select Open File in the Function field and press Return.
4. Select New File in the Edit Status field and press Return.
5. Enter a new symbol table file name in the New File Name field.
6. Select Pattern or Range in the Table Type field to match the symbol table you are copying and press Return.
7. Press F5: EXECUTE FUNCTION.
8. Select Merge Files in the Function field and press Return.
9. Select the file to base your new symbol table on, such as the P5_Ctrl file.
10. Press F5: EXECUTE FUNCTION.
11. Press F8: EXIT & SAVE.
12. Edit the file as desired keeping the following in mind:
    - If the new symbol has fewer don't cares than an existing symbol, it must be placed ahead of the existing symbol.
    - If the new symbol has more don't cares than an existing symbol, it must be placed after the existing symbol.
    - Do not duplicate symbol names.

    Also refer to your *DAS 9200 System User Manual* for more information on editing the symbol table.
13. Select the Channel menu from the Menu Selection overlay.
14. Change the file name of the symbol table for the Control group (or whichever group's symbol table you are replacing) to the one that you specified in step 5.

TRIGGERING

All the Trigger menu selections available for use with your 92A96 Module are still valid for disassembly. Refer to your module user manual for a list and description of these selections.

You can use the Home key to quickly clear the word recognizer field of any channel group with a symbolic radix. To clear a word recognizer, open the field, press the Home key, and close the field. The first entry on the list is blank.

The DAS 9200 makes it possible to cross-trigger with other modules or to an external instrument. You may want to consider sending or receiving a signal to or from another module, or to the Sync Out SMB connector on the module. You should refer to your *DAS 9200 System User Manual* for an in-depth description of defining and using signals, and to specific module user manuals for a description of using the Sync Out SMB connector.

Section 4: ACQUIRING AND VIEWING DISASSEMBLED DATA

This section describes how to acquire data and view it disassembled in the Disassembly display. This section explains:

- acquiring data
- viewing disassembled data in various formats
- functions of the Disassembly Format Definition overlay
- displaying groups symbolically
- restoring and viewing the demonstration reference memory
- searching through data
- printing data

ACQUIRING DATA

Once you load the disassembler software, choose a clocking mode, and specify the trigger, you are ready to acquire data. Press the F1: START acquisition key to begin the acquisition. You can press the F1: STOP key at any time to stop acquisition.

If you have any problems acquiring data, refer to *Appendix A: Error Messages and Disassembly Problems*.

VIEWING DISASSEMBLED DATA

Disassembled data is displayed in the Disassembly menu in four different formats: Hardware, Software, Control Flow, and Subroutine. To select a format, follow these steps:

1. Press the Select Menu key and select the Disasm menu.
2. Press F5: DEFINE FORMAT.
3. Select the desired format in the Display Mode field.
4. Press F8: EXIT & SAVE.

NOTE

Selections in the Disassembly Format Definition overlay must be set correctly in order for your acquired data to be disassembled correctly. Refer to Disassembly Format Definition Overlay *later in this section.*

DAS 9200 system software does not allow more than 32 channels in each channel group. Therefore, two channel groups are used to acquire 64-bit wide Pentium microprocessor data: Data (D63-D32) and Data_Lo (D31-D0).

To handle the display of disassembled data from both data groups, the disassembler may display more than one line for each data sample (sequence). For samples with two display lines, data displayed under the Data column of the first line is from the Data_Lo group (D31-0); data displayed under the Data column of the second line is from the Data group (D63-32). Figure 4-1 shows examples of multiple display lines used to display Data_Lo and Data group information.

When one of the two data groups does not contain valid bytes for a nonfetch cycle, the line for the group with the invalid bytes is not displayed. When neither data group contains valid bytes, both lines are displayed; this is an unexpected condition. Hyphens (—) in the Data column indicate invalid bytes as determined by the BE7#-BE0# signals.

The disassembler synthesizes the A2-A0 signals.

Out-of-order fetches will be correctly disassembled, but displayed in the order they were fetched. In Hardware mode, the cycles will be properly disassembled and identified by an asterisk (*) to the left of the instruction. To see the cycles in executed order, use Software mode. If the out-of-order fetch is a marked cycle, it will be marked with the letter m and an asterisk to the left of the instruction.

The display of a (16) or (32) in the Mnemonic column indicates the default code segment size is either 16 or 32 bits. If the mnemonic fills the entire column width, the (16) or (32) will not be displayed.

An SMM to the right of the Mnemonics column indicates a System Management Mode cycle. If the mnemonic fills the entire column width, the SMM will not be displayed.

Asterisks in the Mnemonics column indicate that there is insufficient data available for complete disassembly of the instruction. The number of asterisks shows the width of the data that is not available. Two asterisks (**) represent a byte.

A pound sign (#) in the display indicates an immediate value. A lowercase “t” indicates a decimal value except for register numbers. PC-relative branches will display the absolute address (as calculated by the disassembler).

Hardware Display Format

The Hardware display format shows the Address, Data, Data_Lo, Control, and DataSize channels for each sample of acquired data. The disassembler displays all valid data in the Hardware display format and always display at least one line of information. Because fetches should have valid data for the Data and Data_Lo groups, most fetches should use at least two display lines. For example, a fetch cycle can show both an instruction, and a READ EXTENSION or FLUSH (or both).

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 4-1 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled within the vector name.

Table 4-1
Cycle Type Definitions

(RESET)	A reset cycle
(MEM READ)	A nonlocked read from memory that is not an opcode fetch
(LOCKED MEM READ)	A locked read from memory
(MEM WRITE)	Any nonlocked write to memory
(LOCKED MEM WRITE)	Any locked write to memory
(IO READ)	A read from an I/O port
(IO WRITE)	A write to an I/O port
(INT ACK)	Responding to an interrupt
(SHUTDOWN)	A Shutdown cycle: the cycle type is SPECIAL; the address is 0
(CACHE FLUSH)	A Cache Flush cycle: the cycle type is SPECIAL; the address is 1
(HALT)	A Halt cycle: the cycle type is SPECIAL; the address is 2
(WRITEBACK)	A Writeback cycle: the cycle type is SPECIAL; the address is 3
(FLUSH ACK)	A Flush Acknowledge cycle: the cycle type is SPECIAL; the address is 4
(BRANCH TRACE)	A Branch Trace cycle: the cycle type is SPECIAL; the address is 5
(RESERVED)	A reserved cycle
(ALTERNATE BUS MASTER)	The bus is released to an Alternate Bus Master
(BACK OFF)	A Back Off Bus cycle
(PROBE MODE READ)	A Probe mode read cycle
(PROBE MODE WRITE)	A Probe mode write cycle
(UNKNOWN)	An invalid/unknown cycle
(BURST LINE FILL)*	Fetch cycle computed to be a Burst Fill. The data is fetched but will not be executed because it is part of a 32-byte fetch. The data will possibly be stored in the cache.
(BACKOFF/BURST FLUSH)*	Burst/Fetch cycle computed to be flushed due to a Back Off cycle
(EXTENSION)*	A Fetch cycle computed to be an opcode extension
(FLUSH)*	A Fetch cycle computed to be an opcode flush

*Cycle type is computed by the disassembler.

Figure 4-1 shows an example of the Hardware display.

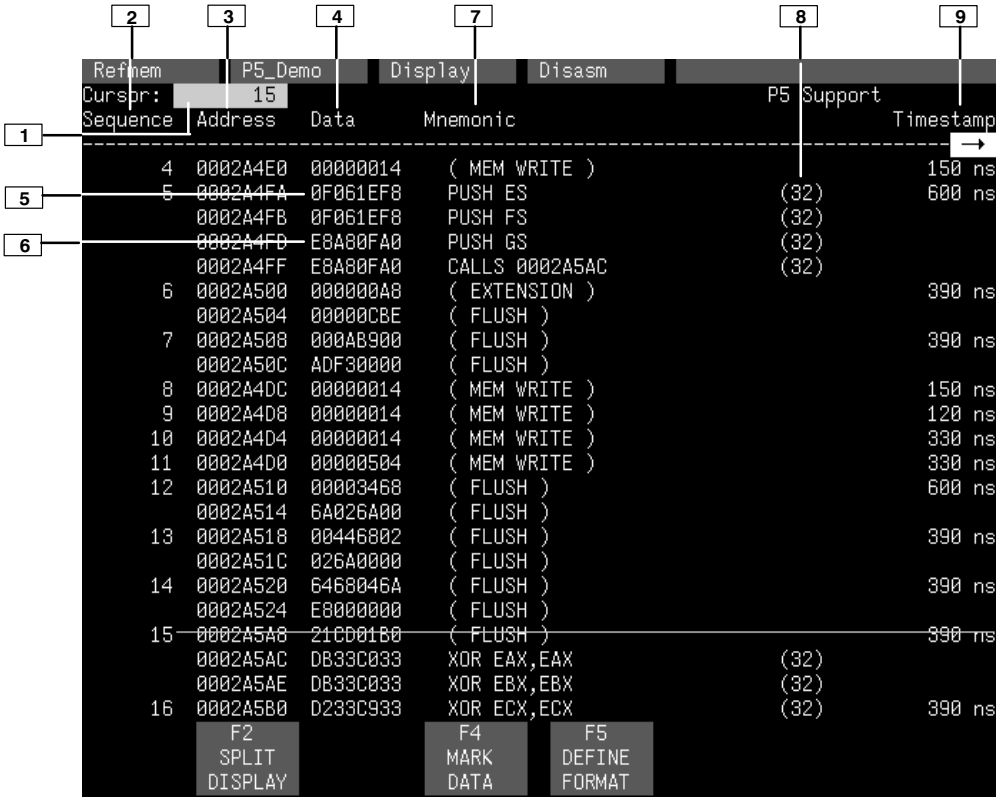

Figure 4-1. Hardware display.

1 **Cursor.** Shows the DAS 9200 sequence number on which the cursor is positioned.

2 **Sequence Column.** Lists DAS 9200 memory locations for the acquired data.

3 **Address Group.** Lists data from channels connected to A31-A3 of the Pentium microprocessor address bus. The disassembler synthesizes the A2-A0 signals.

4 **Data Column.** Lists data from channels connected to either D63-D32 or D31-D0 of the Pentium microprocessor data bus. Refer to the general description of viewing disassembled data for information on how the disassembler determines when to display information for the Data group.

5 This part of the sample is displaying data from channels connected to D31-D0 of the Pentium microprocessor data bus.

6 This part of the sample is displaying data from channels connected to D63-D32 of the Pentium microprocessor data bus.

7 **Mnemonic Column.** Lists the instructions that have been disassembled.

8 This part of the mnemonic, (16) or (32), indicates that the fetch is from a 16- or 32-bit code segment size and disassembled accordingly.

9 **Timestamp Column.** Lists the timestamp values when a timestamp selection is made in the Disassembly Format Definition overlay.

Gaps in the acquired data, caused by data qualification specified in the Trigger menu, are indicated by a gray background behind the Address, Data, and Data_Lo groups.

Software Display Format

The Software display format displays only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. The display is designed to resemble assembly language listings.

Out-of-order fetches are shown in the order the fetches are executed. An asterisk indicates an out-of-order fetch. The sequence number of the out-of-order fetch will not be displayed if the previous executed instruction has a higher sequence number. The sequence number of the out-of-order fetch will be displayed if the previous executed instruction has a smaller sequence number.

Since you cannot place the cursor on an instruction without a sequence number, you will not be able to scroll to some out-of-order fetch instructions. To scroll to these instructions, you will have to switch to the Hardware display format.

Control Flow Display Format

The Control Flow display format displays any instruction that changes the flow of control, such as the following:

- the first fetch of instructions that cause a branch in the address
- conditional jumps actually taken; therefore, the branches not taken are not displayed
- NMI and interrupt cycles; reset cycles and vectored reads are not displayed

Instructions that always generate a change in the flow of control in the Pentium microprocessor are as follows:

CALL	IRET	RET
INT	JMP	

Instructions that could (but do not always) generate a change in the flow of control in the Pentium microprocessor are as follows:

BOUND	JL/JNGE	JNP/JPO
DIV	JLE/JNG	JNS
IDIV	JNB/JAE/JNC	JO
INTO	JNBE/JA	JP/JPE
JB/JNAE/JC	JNE/JNZ	JS
JBE/JNA	JNL/JGE	LOOP
JCXZ/JECXZ	JNLE/JG	LOOPNZ/LOOPNE
JE/JZ	JNO	LOOPZ/LOOPE

If a conditional jump branches to an address that is reached sequentially (no address break in the fetch sequence), the disassembler cannot determine if the branch was taken. If there are two conditional jump instructions close together that branch to the same fetch line, then the disassembler may not be able to determine which conditional jump was actually taken. You can use the mark cycle function to correct the disassembly. Refer to *Marking Cycles* later in this section.

Subroutine Display Format

The Subroutine display format shows the first fetch of subroutine calls and return instructions (such as NMI and interrupt cycles); reset cycles and vectored reads are not displayed. Conditional subroutine calls will be displayed only when the disassembler determines that they have been taken. Instructions that always generate a subroutine call or a return in the Pentium microprocessor are as follows:

CALL	INT	IRET	RET

Instructions that could (but do not always) generate a subroutine call or a return in the Pentium microprocessor are as follows:

BOUND	DIV	IDIV	INT

Disassembly Format Definition Overlay

The Disassembly Format Definition overlay allows you to make optional display selections for the Disassembly menu and tailor it for your applications. To access this overlay, press F5: DEFINE FORMAT.

You can use this overlay to do the following:

- choose the format (mode) in which the Disassembly menu displays disassembled data
- set the interval in which the data cursor will scroll through disassembled data
- display and define the format of the timestamp
- highlight various types of disassembled cycles
- choose to disassemble across gaps
- select code segment size
- choose an interrupt table
- specify the starting address of the interrupt table
- specify the size of the interrupt table
- change the position of any channel group in the display
- change the radix for any channel group
- choose which symbol tables are to be used when channel groups are displayed symbolically

The Disassembly Format Definition overlay is shown in Figure 4-2.

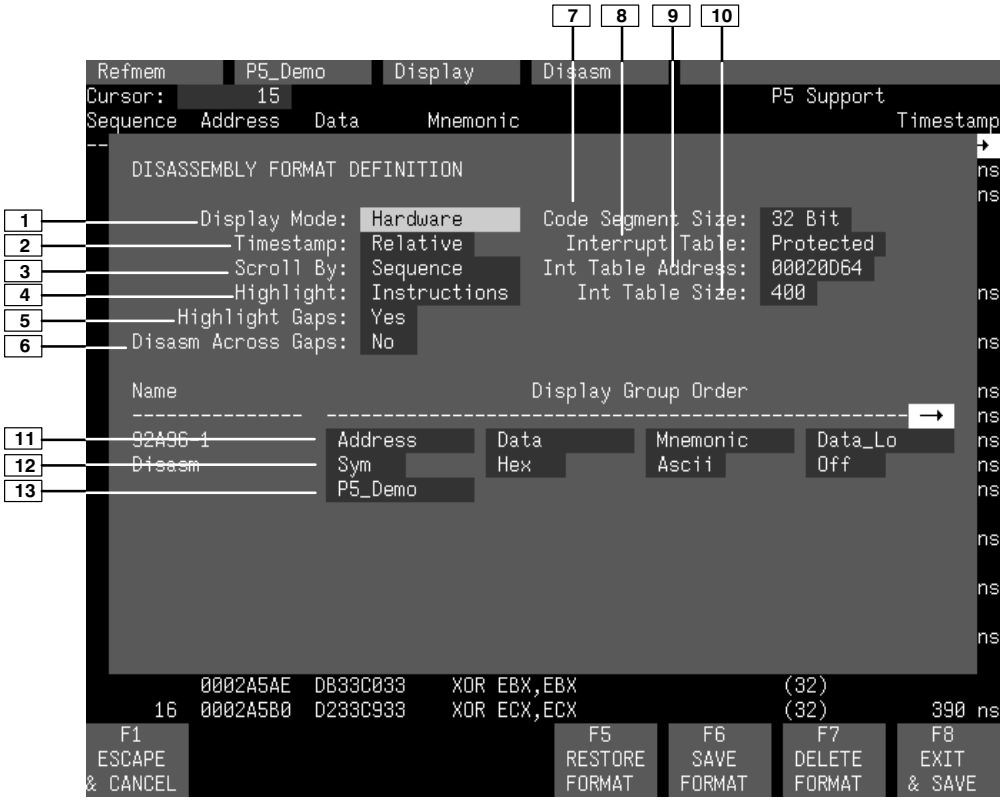

Figure 4-2. Disassembly Format Definition overlay.

1 **Display Mode.** You can select Hardware, Software, Control Flow, or Subroutine format.

2 **Timestamp.** You can display the timestamp as an Absolute, Relative, or Delta value. You can also set the timestamp display to Off.

Timestamp values show the amount of time that has elapsed between data samples. An Absolute timestamp shows the amount of time elapsed between when the acquisition was started (after pressing F1: START) and each subsequent data sample. A Relative timestamp shows the amount of time elapsed between successive samples. A Delta timestamp shows the amount of time between the sample with the delta user mark and each previous or subsequent data sample.

3 **Scroll By.** You can scroll by Sequence, Instruction, Control Flow, or Subroutine.

4 **Highlight.** You can highlight Instructions, Control Flow, or Subroutines. With highlighting on, only the selected type of samples are shown as white text with a black background; all other samples are shown as gray text with a black background. You can also set the highlighting to Off.

5 **Highlight Gaps.** You can choose to highlight or not to highlight gaps. Gaps are caused by qualifying data storage in the Trigger menu and are indicated by a gray background behind the address values.

6 **Disasm Across Gaps.** You can choose to continue or not to continue to disassemble data across gaps. Disassembling data across gaps causes the disassembler to disassemble data as if no gap existed. Disassembled data will be invalid if the last sample before the gap does not logically match the sample immediately following the gap.

7 **Code Segment Size.** You can select the default code segment size: 16 bit or 32 bit. The default code segment size is 16 bit.

8 **Interrupt Table.** You can specify if the interrupt table is Real or Protected. (Selecting Virtual is equivalent to selecting Protected.) The default interrupt table is Real.

9 **Interrupt Table Address.** If your SUT has had its vector table relocated, you must use this field to inform the disassembler of the new base address. If the value in the Interrupt Table Address field is incorrect, the disassembler will not interpret interrupts or exceptions correctly. You can specify the starting address of the interrupt table in hexadecimal. The default starting address is 0x00000000.

10 **Interrupt Table Size.** You can specify the size of the interrupt table in hexadecimal. The default size is 0x400.

11 **Group Name.** You can specify the name of the group that displays in the column in which the cursor is positioned. When you move a group, the group is inserted in the new column position and removed from its old position. Remaining groups will move one column position in either direction as appropriate.

12 **Group Radix.** You can select the radix in which each group displays. The radix selections for most groups are Binary, Octal, Hexadecimal, Symbol, and Off. The only selections for Mnemonics group are ASCII or Off. You should only select the symbolic radix when a symbol table is available for that group. The timestamp value always displays in decimal.

13 **Symbol Table.** You can specify a symbol table to use for each group where symbolic is the selected radix.

Function Keys

F1: ESCAPE & CANCEL. Closes the overlay and discards any changes you have made since entering it.

F5: RESTORE FORMAT. Displays a list of saved disassembly formats for the current module or cluster setup. Use the cursor keys to select the desired format to restore and press the Open/Close key.

F6: SAVE FORMAT. Saves the current selections for the Disassembly Format Definition overlay in a file on disk. You can enter a file name up to ten characters long.

F7: DELETE FORMAT. Displays a list of saved disassembly format files for the current module or cluster setup. Use the cursor keys to select the desired format to delete and press the Open/Close key. You cannot delete the Default format.

F8: EXIT & SAVE. Exits the overlay and executes or saves any changes made.

Displaying the Address Group Symbolically

The address group can be displayed as symbolic values in the Disassembly menu similar to the way the Control group can be displayed as symbol values in the State menu. You can use the Symbol Editor menu to create symbol tables in which symbols are assigned to various address ranges or patterns. You can then change the radix of the Address group in the Disassembly menu using the Disassembly Format Definition overlay. If an address appears in the operand field of a mnemonic, it will also be displayed symbolically.

Figure 4-3 shows the Address group displayed symbolically.

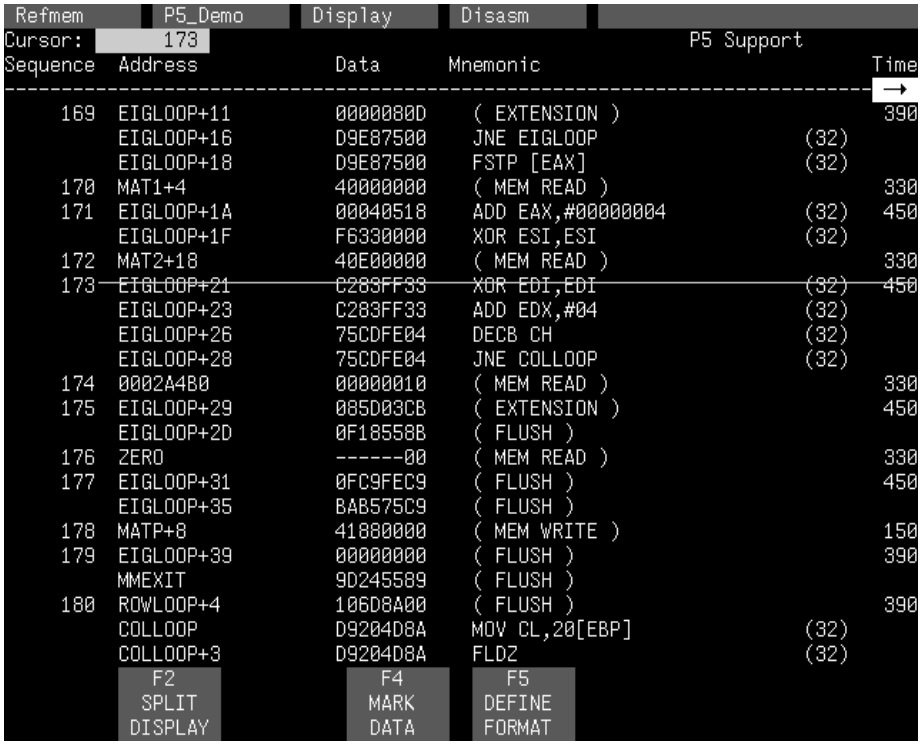

Figure 4-3. Address group displayed symbolically. The Symbol Table file used in this example is also called P5_Demo.

Marking Cycles

Marking cycles synchronizes disassembly software.

Occasionally you may want to change the disassembler's interpretation of a prefetch cycle type.

The Disassembly software occasionally loses track at the start of an acquisition if there is not enough history, when a flush occurs that the disassembler misinterprets as an instruction, or if Pentium the cache is on. The Mark Opcode function identifies an opcode and lets you synchronize the disassembly if the software has lost track.

Function key F4: MARK DATA provides the Mark Opcode function that allows you to change the interpretation of any prefetch cycle type. Using F4: MARK DATA, you can select a cycle and change it to a combination of the following types:

- Opcode (the first byte of an executed instruction)
- Extension (a subsequent byte of an executed instruction)
- Flush (an opcode or extension that is fetched but not executed)
- Any (any valid opcode, extension or flush)
- 16-bit or 32-bit default segment size

To mark a cycle, perform these steps:

1. Place the cursor on the cycle to be marked.
2. Press F4: MARK DATA, select the cycle type you want associated with the current cycle, and press Return.

The marked cycle is indicated in the disassembly column with a small m before the sequence number. Several cycles before and after the mark can be interpreted differently due to the mark.

If the Disassembly menu is set up for software format and an out-of-order fetch does not have a sequence number, you must change to the hardware format to mark that sequence number.

You can also use the F4: MARK DATA key to specify the default segment size mode (16 bit or 32 bit) for the cycle. The segment size selection changes the cycle the cursor is on and the remaining cycles to the end of memory or to the next mark.

The default segment size of the cycle is independent of any prefix override bytes in the particular fetch. For example, if you mark cycle 455 with a default size of 32 bits, but there are address/operand override prefixes in the instruction, the default size will be 32 bits but the size of the instruction will be 16 bits.

You can only make one selection at a time. If you decide to mark both the opcode and the default size of a cycle, you must do them in separate steps.

Figure 4-4 shows the mark opcode selections for a fetch cycle on the 32-bit bus of a Pentium microprocessor. The Lo: or Hi: indicates the lower or upper half of the Pentium microprocessor data bus. The lower half of the Pentium microprocessor data bus (D31-0) connects to the Data_Lo channel group; the upper half of the Pentium microprocessor data bus (D63-32) connects to the Data channel group.

You can scroll through the selection list to view the selections not shown in this figure. The selections not shown are: 16 Bit Default Segment Size, 32 Bit Default Segment Size, Undo marks on this cycle, and a range of user marks.

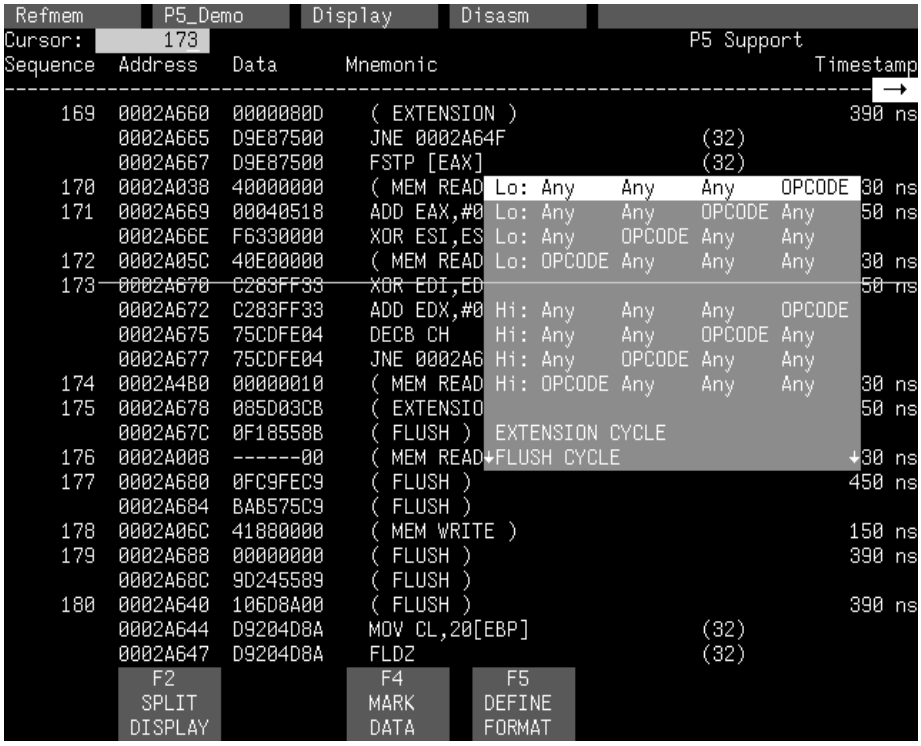

Figure 4-4. Mark opcode selections for a 32-bit wide segment.

You can also choose to undo a mark. This causes the cycle, and any other cycles that may have changed when you initially marked the cycle, to revert to its original state at the time of the acquisition.

To undo a mark, do the following:

1. Place the cursor on the marked cycle.
2. Press F4: MARK DATA, select “Undo marks on this cycle,” and press Return.

EXCEPTION VECTORS

The disassembler software also displays Pentium microprocessor exception vectors. You can select to display the interrupt vectors for either the Protected or Real Addressing Mode in the Interrupt Table field of the Processor Support submenu. (Selecting Protected is equivalent to selecting Virtual.)

The Pentium microprocessor initially places the exception vector table at address 00000000 (the default value). However, you can relocate the table using the Processor Support submenu by entering the address in the Interrupt Table Address field. The Interrupt Table Address field provides the disassembler with the offset address; enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception table. The Interrupt Table Size field lets you specify a three-digit hexadecimal size for the table.

Table 4-2 lists the Pentium microprocessor exception vectors (interrupt cycle types) for Protected Mode (also used for Virtual 8086 Mode); Table 4-3 lists the same information for Real Addressing Mode. Interrupt cycle types are computed cycle types and cannot be used to control triggering. When the Pentium microprocessor processes an interrupt, the disassembler software displays the type of interrupt, if known.

Table 4-2
Interrupt Vectors for Protected Mode

Exception Number	Location in IDT (in hexadecimal)	Interrupt Name
0	0000	Divide Errors
1	0008	Debug Exceptions
2	0010	NMI Interrupt
3	0018	Breakpoint Interrupt
4	0020	Into Detected Overflow
5	0028	Bound Range Exceeded
6	0030	Invalid Opcode
7	0038	Device Not Available
8	0040	Double Fault
9	0048	Reserved
10	0050	Invalid TSS
11	0058	Segment Not Present
12	0060	Stack Exception
13	0068	General Protection
14	0070	Page Fault
15	0078	Reserved
16	0080	Coprocessor Error
17	0088	Alignment Check
18	0090	Machine Check
19-31	0098-00F8	Reserved
32-255	0100-07F8	User Defined

Table 4-3
Interrupt Vectors for Real Addressing Mode

Exception Number	Location in IV Table (in hexadecimal)	Displayed Interrupt Name
0	0000	Divide Error
1	0004	Debug Exceptions
2	0008	NMI Interrupt
3	000C	Breakpoint Interrupt
4	0010	INTO Detected Interrupt
5	0014	Bound Range Exceeded
6	0018	Invalid Opcode
7	001C	Device Not Available
8	0020	Double Fault
9-11	0024- 002C	Reserved
12	0030	Stack Exception
13	0034	Segment Overrun
14-15	0038-003C	Reserved
16	0040	Coprocessor Error
17-31	0044-007C	Reserved
32-255	0080-03FC	User Defined

Figure 4-5 shows the display of an interrupt mnemonic. Sequence 681 shows an INT 33 instruction. Sequences 688 and 689 show the associated table read. All INT # instructions are displayed with decimal numbers as indicated by a “t” following the value.

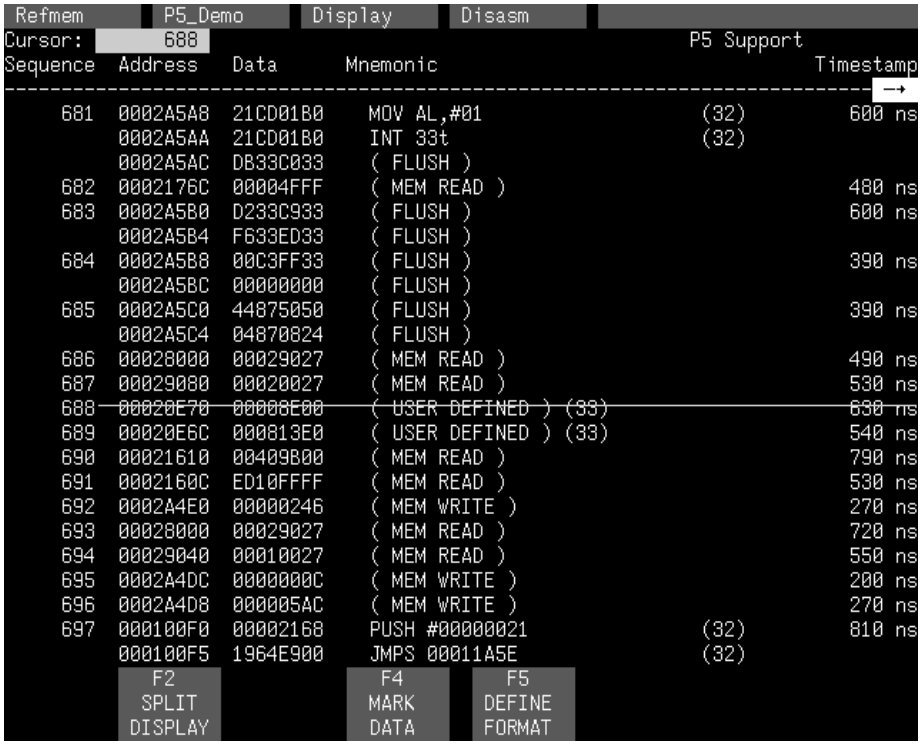

Figure 4-5. Display of an INT 33 instruction.

OUT-OF-ORDER FETCHES

The Pentium microprocessor can prefetch cycles out of ascending order. For example, a branch to address 1008 could cause the following sequence of addresses across the bus: 1008, 1000, 1018, and 1010. The data at address 1008 is executed, but the data at address 1000 is not. The data at addresses 1018 and 1010 are executed, but the data at address 1010 is executed before the data at 1018. An example of the fetched order versus the executed order is shown in the table below.

Fetched Order	Executed Order
1008	1008
1000	1010
1018	1018
1010	

In the Hardware display format, the out-of-order fetches are displayed in the order they are fetched. They will be properly disassembled and identified by an asterisk to the left of the instruction.

In the Hardware display format, you can determine the executed order of the out-of-order fetches by looking at the address of the out-of-order cycles and the subsequent cycles. Fetch cycles always have the sequence numbers displayed.

In the Software display format, out-of-order fetches are displayed in the order they were executed. If the previously executed instruction had a larger sequence number than the out-of-order fetch, the sequence number will not be displayed. If the previous sequence number is smaller than the out-of-order fetch, the sequence number will be displayed. To mark an instruction without a sequence number, you will have to switch to the Hardware display format.

In the Software display format, out-of-order fetches can cause up to sixteen lines of information to need to be displayed but only eight lines will actually be displayed. The disassembler displays <more> in the Mnemonic column to indicate that more than eight lines are available. To view more than eight lines of information, you must use the Hardware display format.

SPECULATIVE PREFETCH CYCLES

Speculative prefetch cycles can occur when the Pentium microprocessor executes an instruction that has been previously executed. To minimize prefetch delays, the Pentium microprocessor predicts the outcome of the branch instruction and starts prefetching at that address. When the branch instruction is executed, the target address is determined. If the Pentium microprocessor predicted the target address correctly, then the needed code has already been fetched. If it did not correctly predict the target address, then the speculative prefetch cycles that had been fetched will be flushed and fetching will begin at the target address.

Figure 4-6 shows an example of speculative prefetch cycles. The previous time (not shown) that the JNE instruction was executed, the branch was taken and the new target address was 0x2A63C. The microprocessor assumed that the address would be 0x2A63C and so started fetching at 0x2A638 (which contains 0x2A63C). Cycles at sequences 338, 339, and 340 are speculative prefetch cycles. When the instruction was executed, the microprocessor determined that the branch was not taken, flushed the speculative prefetch cycles, and started fetching at 0x2A680 (sequence 341), which contained the next instruction after the JNE.

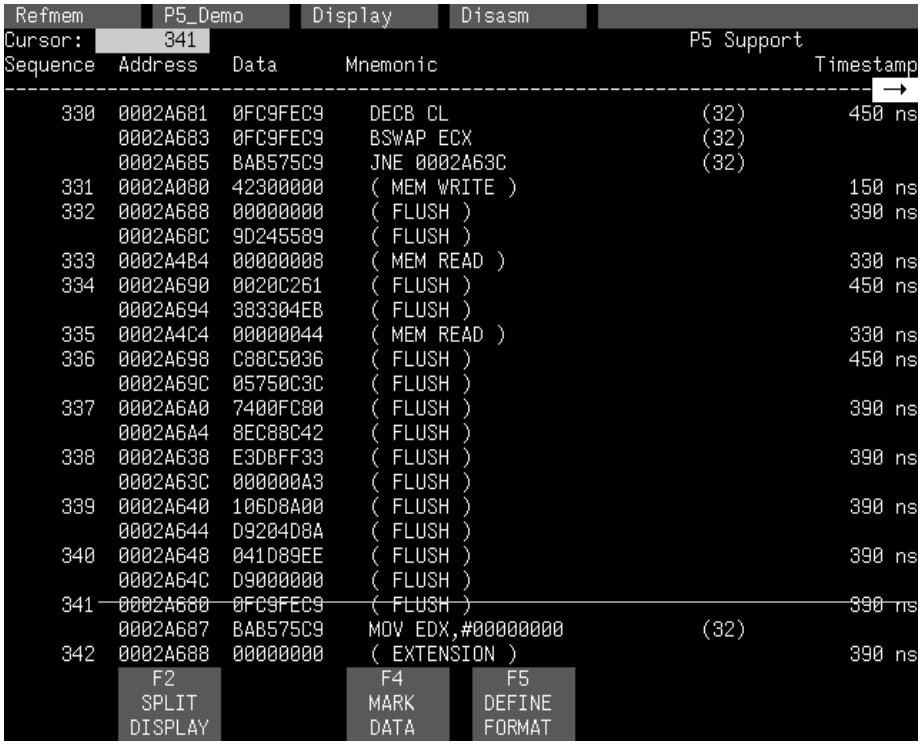

Figure 4-6. Speculative prefetch cycles. Sequences 338 through 340 show speculative prefetch cycles. These cycles were flushed and execution continued at sequence 341.

CACHE INVALIDATION CYCLES

Cache Invalidation cycles are needed to keep the microprocessor's cache contents consistent with external memory. On a non-burst cycle that is also a Cache Invalidation cycle, the data and address will be valid as probed. On a burst cycle that is also a Cache Invalidation cycle, the data will be valid, but the addresses will not be valid as probed and the software will try to calculate the address from the surrounding cycles. Fetch cycles are disassembled. A letter c to the left of the mnemonic indicates a Cache Invalidation cycle.

BURST CYCLES

On all burst cycles, only the first cycle contains a good address. (The Pentium microprocessor doesn't increment the address for a burst.) The disassembler calculates the remaining burst cycle addresses for display.

SYSTEM MANAGEMENT MODE (SMM)

The Pentium microprocessor provides a special mode called System Management Mode where the Pentium CPU executes code from a separate, alternate memory space called SMRAM. The disassembler uses information from the SMIACT# signal to determine when the Pentium microprocessor is operating in this mode. When the disassembler detects that the microprocessor is operating in this mode, it displays an SMM to the right of the mnemonic.

SEARCHING THROUGH DATA

The disassembler does not have a Disassembly Search Definition overlay. However, you can effectively search through disassembled data by following these steps:

1. Press F2: SPLIT DISPLAY to use the split-screen display.
2. Press F5: SPLIT HORIZ to split the screen into two horizontal displays.
3. Press F2: LOCK CURSOR. A list of selections appears.
4. Select **lock cursors at the same sequence** and press Return.
5. Press F8: EXIT & SAVE to display the menus in a split screen.
6. If the active window is the Disassembly menu, press F3: SWITCH WINDOWS to make the State menu active. The cursor and Cursor field are yellow in the active window.
7. Press F6: DEFINE SEARCH to use the search function of the State menu to search for the desired sequence.

To search on Control group values, change the radix to binary and refer to Table 3-1 to find the binary equivalent values for the cycles you want to locate.

When searching for data in a clustered module setup in the State menu, the searches are conducted only for the master module. You can, however, define either module to be the master module. Refer to the description of the State Search Definitiion overlay in your *92A96 Module User Manual* for a description of how to search through state data. Also refer to that manual for a description of how to return to a full screen display.

To abort a search, press the Esc (escape) key.

Figure 4-7 shows the screen split into Disassembly and State windows with the cursors locked on the same bus cycle.

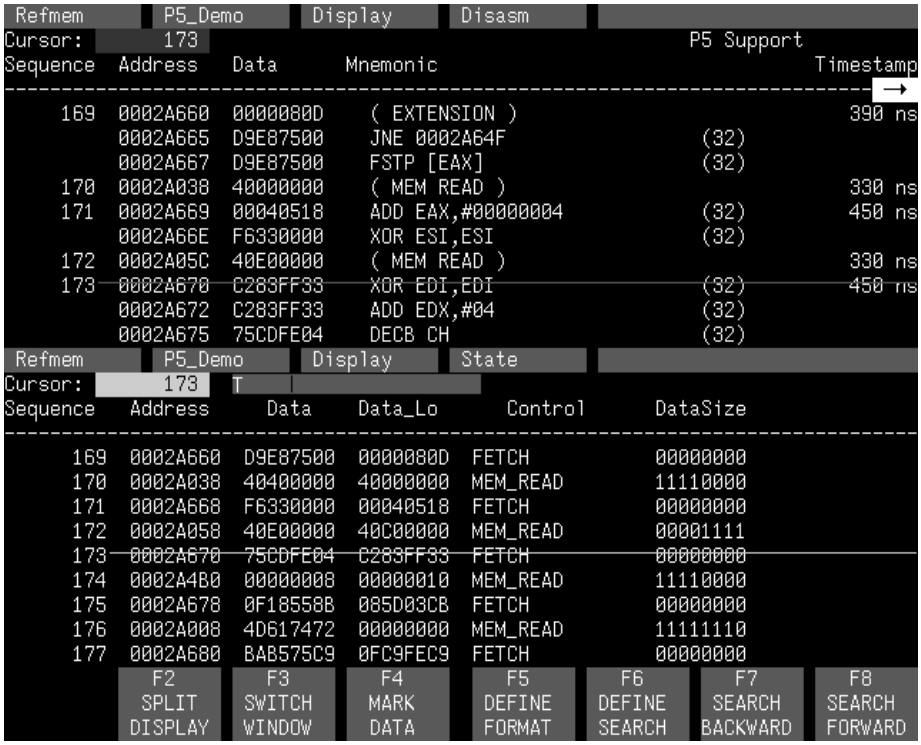

Figure 4-7. Disassembly and State split-screen display. You can use this method to perform searches.

PRINTING DATA

To print disassembled data, use the Disassembly Print overlay. To access this overlay, press the Shift and Print keys at the same time from the Disassembly menu. The Disassembly Print overlay is exactly the same as the State Table Print overlay. Refer to your *92A96 Module User Manual* for a description of this overlay.

REFERENCE MEMORY

A demonstration reference memory file is provided so you can see an example of how your Pentium microprocessor instruction mnemonics look when they are disassembled. A symbol table for the Address group of the demonstration reference memory (called P5_Demo) is also provided so you can see an example of range symbols. Viewing the reference memory is not a requirement for preparing the 92A96 Module for use. You can view the reference memory file without connecting the DAS 9200 to your SUT.

To view the P5_Demo Refmem, follow these steps:

1. Press the Select Menu key, and select the P5_Demo file from the Refmem column.
2. Select the Disasm menu, and press Return.
3. Press F5: DEFINE FORMAT to access the Disassembly Format Definition overlay, and enter the values shown in areas 7, 8, 9, and 10 in Figure 4-2.
4. Press F8: EXIT & SAVE.

You can affect the display of the disassembled data from the Disassembly Format Definition overlay, which you can access through the Disassembly menu.

If there is not enough free space on the hard disk, you can delete the P5_Demo files (reference memory and Address group symbol table). It is not necessary to the operation of the disassembler.

Section 5: GENERAL PURPOSE ANALYSIS

You may need to perform general purpose (timing) analysis on your Pentium microprocessor system prior to, during, and after attempting to integrate your software with the Pentium microprocessor system hardware. When performing hardware analysis, you should use the data acquisition module to acquire data with a finer resolution. When more data samples are taken in a given period of time, the resolution in the Timing display increases, letting you see signal activity that would otherwise go undetected.

This section provides information on the following:

- clocking
- triggering
- displaying data
- supplied Timing Format Definition file

To acquire and display timing data, you need to reconfigure the probe adapter, change the clocking selection and trigger program, acquire data, and view it in the Timing menu. A predefined Timing Format Definition overlay file called P5_96 can be used to view Pentium microprocessor timing data. A description of these files and how to use them can be found later in this section.

Keep in mind when you view data in the State display that it uses the default channel grouping setup with all groups visible and will look different than the Disassembly display.

CLOCKING

To change the data sampling rate, use the Clock menu.

The Disassembly/Timing jumper, J1902, on the probe adapter should be set in the Timing position to acquire timing data. For more information on the Disassembly/Timing jumper, refer to Section 2.

When using the 92A96 Module for timing analysis, you should use the Internal or External clocking modes. The Internal clock selection can sample data up to 100 MHz, which has a 10 ns resolution between samples. The External clock selection samples data on every active clock edge on the 92A96 clock inputs up to 100 MHz.

The Clock menu is shown in Figure 3-1. The default clocking mode is Custom when microprocessor support is used; you will need to change it to either Internal or External. Your *92A96 Module User Manual* contains an in-depth description of Internal and External clocking.

Custom Clocking

Custom clocking only stores one data sample for each bus transaction, which can take one or more clock cycles. Custom clocking also time-aligns certain signals that otherwise would be skewed relative to the current bus transaction. This clocking selection is generally unproductive for timing analysis. Refer to Appendix B for a more in-depth description of how Custom clocking is used with the probe adapter to acquire data.

Internal Clocking

When you select Internal as the clocking mode, the 92A96 Module stores one data sample as often as every 10 ns (100 MHz). This clocking selection is commonly referred to as asynchronous.

Two typical uses of Internal clocking might be to verify that all the Pentium microprocessor signals are transitioning as expected or to measure timing relationship between signal transitions.

It is possible to acquire asynchronous data at rates of 200 MHz and 400 MHz. The faster the 92A96 Module acquires data, the fewer channels it can acquire data on. A single 92A96 Module can acquire data on 24 channels at 400 MHz or 2.5 ns resolution. Refer to your *92A96 Module User Manual* for information on sampling data at speeds faster than 100 MHz.

External Clocking

When you select External as the clocking mode, the 92A96 Module acquires and stores data based on the clock channel up to 100 MHz (using only one clock edge). This clocking selection is commonly referred to as synchronous.

By selecting the rising edge of CLK: 3 on the acquisition module as the clock channel, and turning off the remaining three clocks, the module will sample data on every rising edge of the clock. No data is acquired on the falling clock edge unless you select both edges.

A clock probe from each module (HI and LO) must connect to the appropriate set of clock pins on the probe adapter. (The clock channels are double probed.)

You can also use the other three clock channels as qualifiers or clocks to further modify the clocking in of information from your Pentium microprocessor system.

TRIGGERING

All the Trigger menu selections available for use with the 92A96 Module are still valid for timing analysis. Refer to your module user manual for a list and description of the selections.

ACQUIRING DATA

You can acquire data as described in the *Acquiring Data* description in Section 4. The Disassembly/Timing jumper, J1902, on the probe adapter should be set in the Timing position to acquire timing data.

DISPLAYING DATA

General purpose analysis requires that you view data in either the State or Timing menus. The following discussion describes these menus.

Timing Menu

In the Timing menu, every channel is shown as a waveform, and groups of channels are shown as bus forms.

A predefined Timing Format Definition overlay file, part of the Pentium microprocessor support, is available for you to use when displaying data in the Timing format. The P5_96 file is installed on the DAS 9200 with the support software.

The P5_96 Timing Format file displays the Address, Data, Data_Lo, and DataSize groups as bus forms containing bus values instead of as individual timing waveforms. The remaining signals are displayed as individual traces. Figure 5-1 shows data displayed using the P5_96 file.

To select the supplied Timing Format Definition file, follow these steps:

1. Select the Timing menu and press F5: DEFINE FORMAT.
2. Press F5: RESTORE FORMAT.
3. Select P5_96 and press the Return key. A message tells you the format file is selected.
4. Press F8: EXIT & SAVE to return to the Timing menu.

Refer to the channel assignment tables in Appendix C for the lists of individual channels and their Pentium microprocessor signal names.

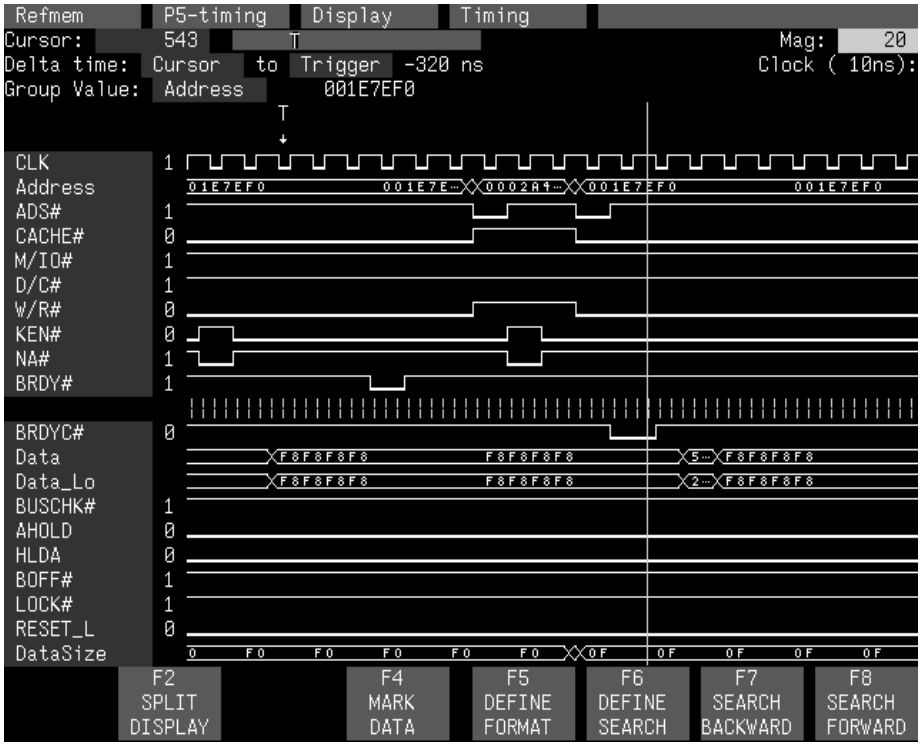

Figure 5-1. Timing data using the P5_96 Timing Format file.

State Menu

In the State menu, all channel group values are shown based on the selected radix in the Channel menu or the State Format Definition overlay. No disassembly occurs. Figure 5-2 shows State data.

If you want to display other channel groups, access the State Format Definition overlay and change the radix from Off to Hex, Bin, or Oct. This overlay also allows you to add the Timestamp group (and change the radix) to the data display.

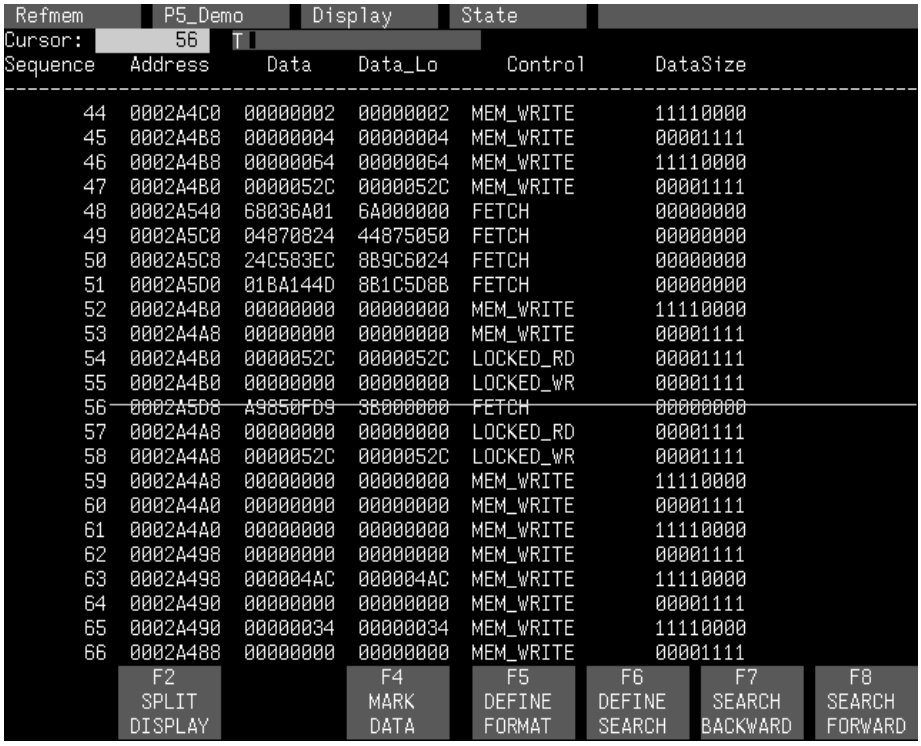

Figure 5-2. State data.

SEARCHING THROUGH DATA

To search through data, you can use either the Timing Search Definition overlay or the State Search Definition overlay. You can use these overlays and search through data as described in your *92A96 Module User Manual*.

Before performing a search in the Timing menu, be sure to check the State Format Definition overlay and make sure the channels on which you want to conduct a search are visible. Channels visible in the Timing menu cannot be searched on unless they are also visible in the State menu.

PRINTING DATA

To print state data, you can use the State Print overlay. To access this overlay, press the Shift and Print keys at the same time from the State menu.

To print timing data, you can use the Timing Print overlay. To access this overlay, press the Shift and Print keys at the same time from the Timing menu.

For detailed information on the State Print overlay or the Timing Print overlay, refer to your *92A96 Module User Manual*.

Appendix A: ERROR MESSAGES AND DISASSEMBLY PROBLEMS

This appendix describes error messages and disassembly problems that you may encounter while acquiring data.

MODULE ERROR MESSAGES

These error messages will appear in the Module Monitor menu when there are problems with acquiring data or satisfying the trigger program. The error messages are listed in alphabetical order; a description of the error message and the recommended solution follow the error message.

Slow Clock. This message appears when the active clock channel (or channels) is not changing, is typically changing at 1 ms or slower intervals, or one of the clock qualifiers is held in the wrong state. Check for the following:

1. The Pentium microprocessor system is powered on and running. Be sure the system is not halted.
2. P5 Support is selected in the appropriate 92A96 Configuration menu.
3. Custom is selected in the Clock menu.
4. The connections between the 92A96 Module and the probe adapter are correct.
   - The clock and 8-channel probe connections between the interface housings and probe adapter are correct (module name, clock, section names, and channel numbers match), are properly oriented (GND connects to ground), and fully engaged.
   - The connections between the interface housings and 92A96 probe cables have matched color labels, matched slot numbers, and are properly keyed.
   - The connections between the 92A96 probe cables and probe connectors have matched color labels, matched slot numbers, and are properly keyed.
5. The orientation of pin A1 on the microprocessor, the probe adapter, and SUT are correct.
6. There are no bent or missing pins on the Pentium microprocessor or on of the probe adapter socket.
7. The Disassembly/Timing jumper is in the D position.

Waiting for Stop. This message appears when the trigger condition is satisfied and memory is full but the Manual Stop mode is selected in the Cluster Setup menu. The solution is to manually stop the DAS 9200 by pressing F1: STOP.

This message can also appear when other modules in the cluster have not filled their memories. Wait for the other modules to fill their memories. If the message does not disappear in a short time, press F1: STOP.

Waiting for Stop-Store. This message appears when the trigger condition is satisfied but the amount of post-fill memory specified in the trigger position field is not yet filled. Press F1: STOP to view the acquired data, then check for the following:

1. The trigger program in the Trigger menu is correct.
2. The storage qualification in the Trigger menu is correct.
3. The system or the module does not have an exception or fault. The Pentium microprocessor system or acquisition module might have experienced a hardware or software exception or fault after the trigger condition was satisfied.

Waiting for Trigger. This message appears when the trigger condition does not occur. Check for the following:

1. The Pentium microprocessor system is powered on and running. Be sure the system is not halted.
2. The trigger conditions are not being satisfied. The Module Monitor menu shows which state events are not occurring. Press F1: STOP, access the Trigger menu, and redefine the conditions for that state. Also refer to the description on *Triggering* in Section 3.

OTHER DISASSEMBLY PROBLEMS

There may be problems with disassembly for which no error messages are displayed. Some of these problems and their recommended solutions follow.

Incorrect Data. If the data acquired is obviously incorrect, check the following:

1. P5 Support is selected in the 92A96 Configuration menu.
2. The internal instruction cache on the Pentium microprocessor is turned off. Disable the internal instruction cache.
3. Custom is selected in the Clock menu.

4. The Disassembly/Timing jumper is in the D position.
5. The connections between the 92A96 Module and the probe adapter are correct.
   - The clock and 8-channel probe connections between the interface housings and probe adapter are correct (module name, clock, section names, and channel numbers match), are properly oriented (GND connects to ground), and fully engaged.
   - The connections between the interface housings and 92A96 probe cables have matched color labels, matched slot numbers, and are properly keyed.
   - The connections between the 92A96 probe cables and probe connectors have matched color labels, matched slot numbers, and are properly keyed.
6. The orientation of pin A1 on the microprocessor, the probe adapter, and SUT are correct
7. No bent or missing pins on the Pentium microprocessor or on either of the probe adapter sockets.

Other Suggestions. If the previous suggestions do not fix the problem with acquiring disassembled bus cycles or instruction mnemonics, try the following:

1. Reload the module setup by selecting the P5 Support in the 92A96 Configuration menu to restore the DAS 9200 to a known state.
2. Possible ac and dc loading problems may be remedied by removing the protective socket from the probe adapter. The socket may add enough additional inductance to your Pentium microprocessor system to affect it. Refer to Appendix C for a description to remove sockets from the probe adapter.

If the DAS 9200 still is not acquiring data after trying these solutions, there may be a problem with your Pentium microprocessor system. Try performing hardware analysis with your DAS 9200 system to ensure that the Pentium microprocessor signals are valid at the time the probe adapter samples them.

Refer to *Section 5: General Purpose Analysis* for information on data sampling rates using either the Internal or External clocking selections in the Clock menu. Also refer to *Appendix B: How Data is Acquired* to see when the disassembler samples the various Pentium microprocessor system signals.

Appendix B: HOW DATA IS ACQUIRED

This appendix explains how the 92A96 Module acquires Pentium microprocessor signals using the 92DM13A probe adapter and software. This appendix also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra 92A96 channels available for you to use for additional connections.

92A96 CUSTOM CLOCKING

A special clocking program is loaded to the 92A96 Module every time P5 Software Support is selected in the Configuration menu. With Custom clocking, the module logs in signals from multiple groups of channels at different times when they are valid on the Pentium CPU bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking, the module's clocking state machine (CSM) generates one master sample for each Pentium microprocessor bus cycle, no matter how many clock cycles are contained in that cycle.

Figure B-1 shows the sample points and the master samples for a single cycle followed by a burst transfer. In this figure, SPA indicates the sample point for address, SPD indicates the sample point for data, and MAST SAMP indicates the master sample point. The ADS#, address, and data signals are delayed by two CLK cycles in this figure. This figure also shows the timing relationships of LAST_D and DVALID_D, signals synthesized by sequential logic on the probe adapter.

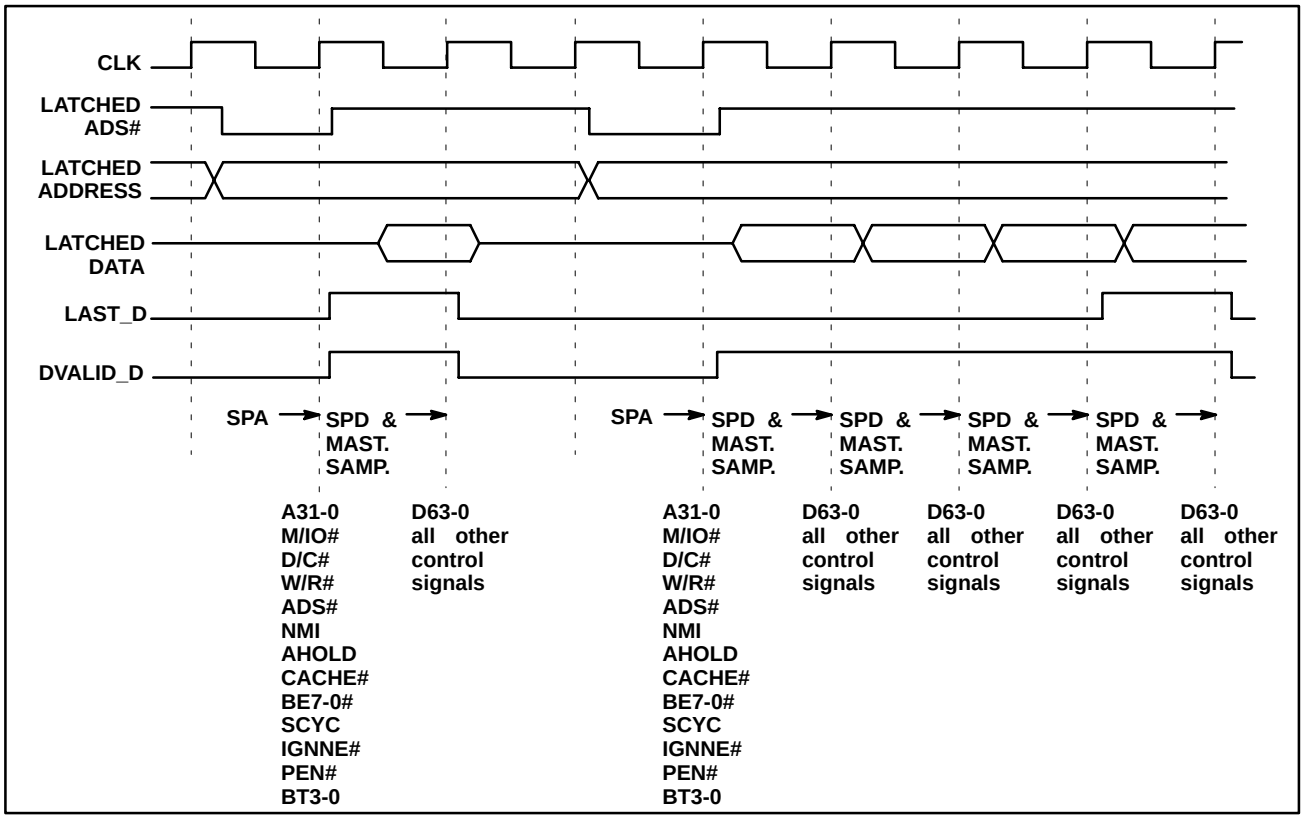

Figure B-1. Pentium microprocessor bus timing: single cycle followed by a burst transfer.

With relationship to actual real time, nondelayed Pentium signals, the first sample point in a cycle occurs two clocks after ADS# is asserted. The second (and subsequent, if the cycle is a burst) sample point occurs two clocks after BRDY# or BRDYC# are asserted.

Figure B-2 shows the sample points and the master samples for a single cycle transfer pipelined into another single cycle transfer. In this figure, SPA indicates the sample point for address, SPD indicates the sample point for data, and MAST SAMP indicates the master sample point. The ADS#, address, and data signals are delayed by two CLK cycles in this figure. This figure also shows the timing relationships of LAST_D, DVALID_D, and PIPE_D, the signals synthesized by sequential logic on the probe adapter.

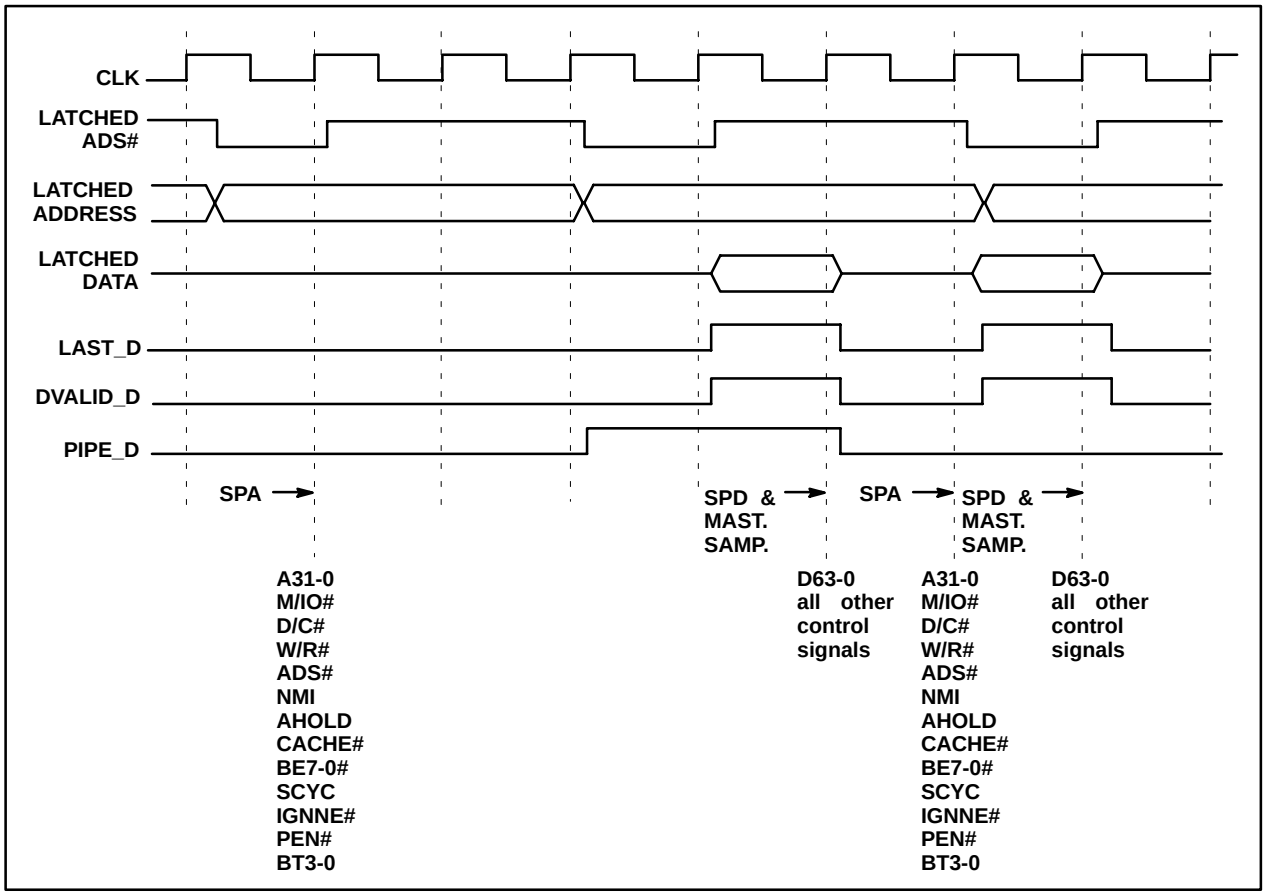

Figure B-2. Pentium microprocessor bus timing: single cycle transfer pipelined into another single cycle transfer.

With relationship to actual real time, nondelayed Pentium signals, the first sample point in a cycle occurs two clocks after ADS# is asserted. When ADS# is asserted again to pipeline a second cycle into the first, the first sample point for that second cycle comes three clocks after the last BRDY# or BRDYC# is returned from the first outstanding cycle.

The second (and subsequent, if the cycle is a burst) sample point occurs two clocks after BRDY# or BRDYC# is asserted whether the cycle is pipelined or not.

CLOCKING OPTIONS

The 92A96 Custom clocking algorithm for the Pentium microprocessor has two variations: Alternate Bus Master Cycles Excluded, and Alternate Bus Master Cycles Included.

Alternate Bus Master Cycles Included

All bus cycles, including alternate bus master cycles and backoff cycles, are logged in.

When the HLDA signal is high, the Pentium microprocessor has given up the bus to an alternate device. The Pentium system design affects what data will be logged in. The DAS 9200 only samples the data at the pins of the Pentium microprocessor. To properly log in bus activity, any buffers between the Pentium microprocessor and the alternate bus master must be enabled and pointing at the Pentium microprocessor.

There are three possible Pentium system designs and clocking interactions when an alternate bus master has control of the bus. The three different possibilities are listed below (in each case, the HLDA signal is logged in as a high level):

- If the alternate bus master drives the same control lines as the Pentium microprocessor, and the Pentium microprocessor “sees” these signals, the bus activity is logged in like normal bus cycles except that the HLDA signal is high.
- If none of the control lines are driven or if the Pentium microprocessor can not see them, the DAS 9200 will still clock in an alternate bus master cycle. The information on the bus, one clock prior to the HLDA signal going low, is logged in. If the ADS# signal goes low on the same clock when the HLDA signal goes low, the address that gets logged in will be the “next address,” not the address that occurred one clock before the HLDA signal went low.
- If some of the Pentium microprocessor control lines are visible (but not all), the DAS 9200 logs in what it determines is valid from the control signals and logs in the remaining bus signals one clock cycle prior to the HLDA signal going low. If the ADS# signal goes low on the same clock that the HLDA signal goes low, the “next address” will be logged in instead of the previously saved address.

When the BOFF# signal goes low (active), a backoff cycle has been requested and the Pentium microprocessor gives up the bus on the next clock cycle. The DAS 9200 aborts the bus cycle that it is currently logging in (the Pentium microprocessor will restart this cycle once the BOFF# signal goes high). A backoff cycle will be logged in using one of the three interactions described earlier for the HLDA signal (except that the BOFF# signal is stored as a low-level signal in each of the cases).

Alternate Bus Master Cycles Excluded

Whenever the HLDA signal is high, no bus cycles are logged in. Only bus cycles driven by the Pentium microprocessor (HLDA low) will be logged in. Backoff cycles (caused by the BOFF# signal) are stored.

ALTERNATE MICROPROCESSOR CONNECTIONS

You can connect to microprocessor signals that are not required for disassembly so you can do more advanced timing analysis. These signals may or may not be accessible on the probe adapter board. The following paragraphs and tables list signals that are accessible or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel connection tables in Appendix C.

Signals On the Probe Adapter

The probe adapter board contains pins for microprocessor signals that are not acquired by the support software. You can connect extra podlets to these pins because they can be useful for general purpose analysis. However, these signals are not defined in the Channel setup menu; you must enter the Channel setup menu and assign those signals to a new channel group.

Table B-1 shows the microprocessor signals available on J1371 of the probe adapter.

Table B-1
Signals on J1371

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	7	TDO
2	PRDY	8	TRST#
3	R/S#	9	TMS
4	TDI	10	NMI
5	TCK	11	RESET
6	GND	12	GND

Signals Not On the Probe Adapter

Table B-2 shows the microprocessor signals that are not accessible on the probe adapter.

Table B-2
Signals Not Available on the Probe Adapter

Pentium Microprocessor Signal Name			
A20M#	FRCMC#	NC-T18	DP3
AP	ADSC#	DP7	DP2
BREQ	NC-Q19	DP6	DP1
EWBE#	NC-R19	DP5	DP0
IERR#	NC-S19	DP4	

Extra 92A96 Channels

Table B-3 shows the extra 92A96 channels available for you to use to make alternate Pentium microprocessor system connections. You can also disconnect channels not required for disassembly to make alternate connections. The channel assignment tables in Appendix C indicate channels not required for disassembly.

Table B-3
Extra 92A96 Channels

92A96 Section: Channel			
HI_C1:7	HI_C0:7	LO_C1:7	LO_C0:7
HI_C1:6	HI_C0:6	LO_C1:6	LO_C0:6
HI_C1:5	HI_C0:5	LO_C1:5	LO_C0:5
HI_C1:4	HI_C0:4	LO_C1:4	LO_C0:4
HI_C1:3	HI_C0:3	LO_C1:3	LO_C0:3
HI_C1:2	HI_C0:2	LO_C1:2	LO_C0:2
HI_C1:1	HI_C0:1	LO_C1:1	LO_C0:1
HI_C1:0	HI_C0:0	LO_C1:0	LO_C0:0

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid personal injury, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so. Refer to the General Safety Summary and the Servicing Safety Summary prior to performing any service.

Appendix C: SERVICE INFORMATION

This appendix contains the following information:

- safety summary
- brief description of the probe adapter and how it works
- care and maintenance procedures
- specification tables
- channel assignment tables
- dimensions of the probe adapter
- removing and replacing individual signal leads
- removing and replacing sockets

SERVICING SAFETY INFORMATION

The following servicing safety information is for service technicians. Follow these safety precautions, along with the general precautions outlined in your *92A96 Module User Manual*, while installing or servicing this product.

Do Not Service Alone. Do not perform internal service or adjustment on this product unless another person is present and able to give first aid and resuscitation.

Use Care When Servicing With Power On. To avoid personal injury from dangerous voltages, remove jewelry such as rings, watches, and other metallic objects before servicing. Do not touch the product's exposed connections and components while power is on.

PROBE ADAPTER DESCRIPTION

The probe adapter is a nonintrusive piece of hardware that allows the 92A96 Module to acquire data from a Pentium microprocessor in its own operating environment with little affect, if any, on that system. Refer to Figure C-1 while reading the following discussion.

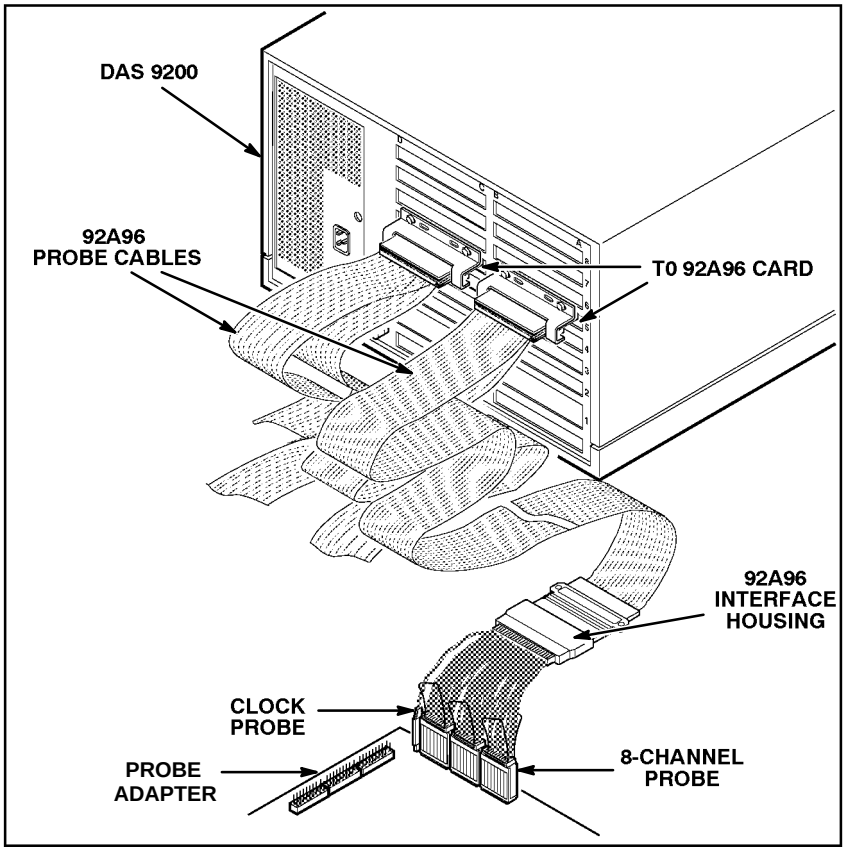

Figure C-1. Overview of the standard probe and probe adapter.

The probe adapter consists of a circuit board and a socket for the Pentium microprocessor. The probe adapter connects to the SUT. Signals from the Pentium microprocessor system flow from the probe adapter to the podlet groups and through the probe signal leads to the 92A96 Module.

All circuitry on the probe adapter is powered from the system under test.

The probe adapter accommodates the Intel Pentium microprocessor in a 273-pin PGA package.

Configuring the Probe Adapter

The probe adapter contains three jumpers that need to be in the correct position for proper data display. The CLK jumper (J1905) should be placed in the ≥33 position to acquire data from a system running at or faster than 33 MHz. The jumper should be placed in the <33 position to acquire data from a system running slower than 33 MHz.

The Disassembly/Timing jumper (J1902) should be placed in the D position to acquire disassembly data, and in the T position to acquire timing data.

The Tracking jumper (J1901) should not need to be moved from the default position; pins 1 and 2 connected. The only time this jumper should be moved is when the tracking circuitry malfunctions. An indication of such a malfunction is when you see activity on the bus during a BOFF or HLDA cycle that is uncharacteristic of the Pentium microprocessor. When the jumper is in the 2, 3 position, the circuitry on the probe adapter does not track BOFF and HLDA cycles. A data sample will show that such a cycle occurred, but will not contain any meaningful information.

Probe Adapter Circuit Description

There are 21 active components on the probe adapter: three 22V10-7 PALs, seven 18-bit clocked latches, five 10-bit CMOS clocked latches, five 10-bit CMOS bus switch packages, and one PLL (phase locked loop) low-skew clock generator for clock distribution.

The PALs implement three sequential state machines that monitor the Pentium microprocessor bus and generate three important signals:

- PIPE_D, indicates Pentium microprocessor bus pipelining is occurring
- LAST_D, indicates the end of a Pentium microprocessor bus cycle
- DVALID_D, indicates valid data is present on the Pentium microprocessor data bus

These signals are required for the Clocking State Machine (CSM) of the logic analyzer to accurately strobe addresses and data information from the Pentium microprocessor bus.

The Pentium microprocessor 32-bit address bus and those control signals valid with address (for example W/R# and M/IO#) are latched with 74FCT162501 transceivers and held with ADS# in 74FCT2823 latches until the next ADS#. This makes the signals available for a longer time than the minimum time on the Pentium microprocessor. Latching also provides low loading and the shortest possible setup and hold time windows.

The Pentium microprocessor 64-bit data bus and some of the control signals are latched to realign the signals with the PIPE_D, LAST_D, and DVALID_D outputs from the PAL.

A PLL clock generator is used to provide eight, 0-delay copies of the Pentium microprocessor CLK input that are distributed to the latches and PALs.

The probe adapter uses up to two CLK periods of delay to realign signals for acquisition. Table C-1 shows the relative signal delays when using the probe adapter. The Hardware CLK Delays column lists the number of clocks that signals are delayed on the probe adapter board when J1902 is in the D position. The Firmware CLK Delays column lists the number of clocks that signals are delayed by the CSM when P5 Custom clocking is selected. Hardware clock delays and firmware clock delays are additive.

Table C-1
Signal Delays When Using the Probe Adapter

Pentium Microprocessor Signal Name	Hardware CLK Delays	Firmware (CSM) CLK Delays*
BOFF#	2	1
A31-A0, BE7#-BE0#, ADS#, D/C#, W/R#, M/IO#, BT3-BT0, CACHE#, SCYC, AHOLD	2	0
HLDA, BRDY#, BRDYC#, D63-D0, NA#, KEN#, EADS#, LOCK#, SMIACT#, BUSCHK#, IU, IV, IBT, PRDY	1	1
RESET	1	0
INIT, PCD, APCHK#, HOLD, FLUSH#, PWT, PCHK#, WB/WT#, BP2, BP3, PM0/BP0, PM1/BP1, INV, FERR#, INTR, HITM#, HIT#	0	1
NMI, SMI#, R/S#, CLK, IGNNE#, PEN#	0	0

*When the clock selection is anything other than P5, all firmware clock delays are 0.

When J1902 is in the T position, all hardware clock delays are 0, which makes the probe adapter transparent for timing measurements. All circuitry on the probe adapter is bypassed changing all the latches to buffers and sending the Pentium microprocessor signals straight through to the podlets. Signal relationships are maintained with the addition of 6 ns maximum delay for those signals connected through buffers. Any signal that has a hardware clock delay identified in Table C-1 will have a 6 ns maximum delay through the probe adapter.

There is one pullup resistor on the BRDYC# line. When the Pentium microprocessor is operating in normal (or component) mode, the pullup resistor pulls this line high, which causes the acquisition module to see BRDYC# as inactive. When the Pentium microprocessor is operating in Chip-Set mode, the pullup is overdriven.

CARE AND MAINTENANCE

The probe adapter does not require scheduled or periodic maintenance. To maintain good electrical contact, keep the probe adapter free of dirt, dust, and contaminants. Also, ensure that any electrically conductive contaminants are removed.

Dirt and dust can usually be removed with a soft brush. For more extensive cleaning, use only a damp cloth. Abrasive cleaners and organic solvents should never be used.

CAUTION

The semiconductor devices contained on the probe adapter are susceptible to static-discharge damage. To prevent damage, service the probe adapter only in a static-free environment.

If the probe adapter is connected to your system, grasp the ground lug on the back of the DAS 9200 mainframe to discharge your stored static electricity. If the probe adapter is not connected, touch any of the ground pins (row of square pins closest to the edge of the probe adapter circuit board labeled GND) to discharge stored static electricity from the probe adapter.

Always wear a grounding wrist strap, or similar device, while servicing the instrument.

Exercise care when soldering on a multilayer circuit board. Excessive heat can damage the through-hole plating or lift a run or pad and damage the board beyond repair. Do not apply heat for longer than three seconds. Do not apply heat consecutively to adjacent leads. Allow a moment for the board to cool between each operation.

If you must replace an electrical component on a circuit board, exercise extreme caution while unsoldering or soldering the new component. Use a pencil-type soldering iron of less than 18 watts and an approved desoldering tool. Ensure that the replacement is an equivalent part by comparing the description as listed in the replaceable parts list.

SPECIFICATIONS

These specifications are for a probe adapter connected to a 92A96 Acquisition Module and the system under test (SUT). Table C-2 shows the electrical requirements the SUT must produce for the disassembler to acquire correct data. Table C-3 shows environmental specifications.

Table C-2
Electrical Specifications

Characteristics	Requirements	
SUT DC Power Requirement		
Voltage	+4.75 V to +5.25 V	
Current	850 mA (I typical, measured)	
SUT Clock Rate	66.66 MHz maximum	
Minimum Setup Time Required		
A31-A3, D63-D0, BE7#-BE0#, CACHE#, SCYC, M/IO#, D/C#, RESET, HLDA, ADS#, W/R#, BRDY#, BRDYC#, PRDY, BOFF#, NA#, KEN#, EADS#, LOCK#, AHOLD, SMIACT#, BUSCHK#, IU, IV, IBT, BT3-BT0	4 ns	
All Other Signals	6 ns	
Minimum Hold Time Required		
All Signals	1 ns	
	Specification	
Measured Typical SUT Signal Loading	**AC Load**	**DC Load**
Clk	8 pF	1 S4403 PLL
A31-A3, D63-D0	8-13 pF	1 74FCT162501AT
BE7#-BE0#	13 pF	1 74FCT162501AT
CACHE#, SCYC, M/IO#, RESET, D/C#	10-14 pF	1 74FCT162501AT
ADS#, W/R#, BRDY#,HLDA	7-9 pF	1 22V10 PAL
ADSC#, BRDYC#	10 pF	10 k + 1 22V10 PAL
KEN#	15 pF	10 k + 1 74FCT162501AT
PRDY	23 pF	1 74FCT162501AT
BOFF#, NA#, EADS#, LOCK#, IBT, AHOLD, SMIACT#, BUSCHK#, IU, IV	11-15 pF	1 74FCT162501AT
BT3-BT0	10-13 pF	1 74FCT162501AT
All Other Signals	5-9 pF + 1 podlet	1 podlet
Not Connected Signals	2 pF	none

One podlet load is 100k ohm in parallel (+) with 10 pF.

Figure C-2 shows the dimensions of the probe adapter with the podlet holders attached.

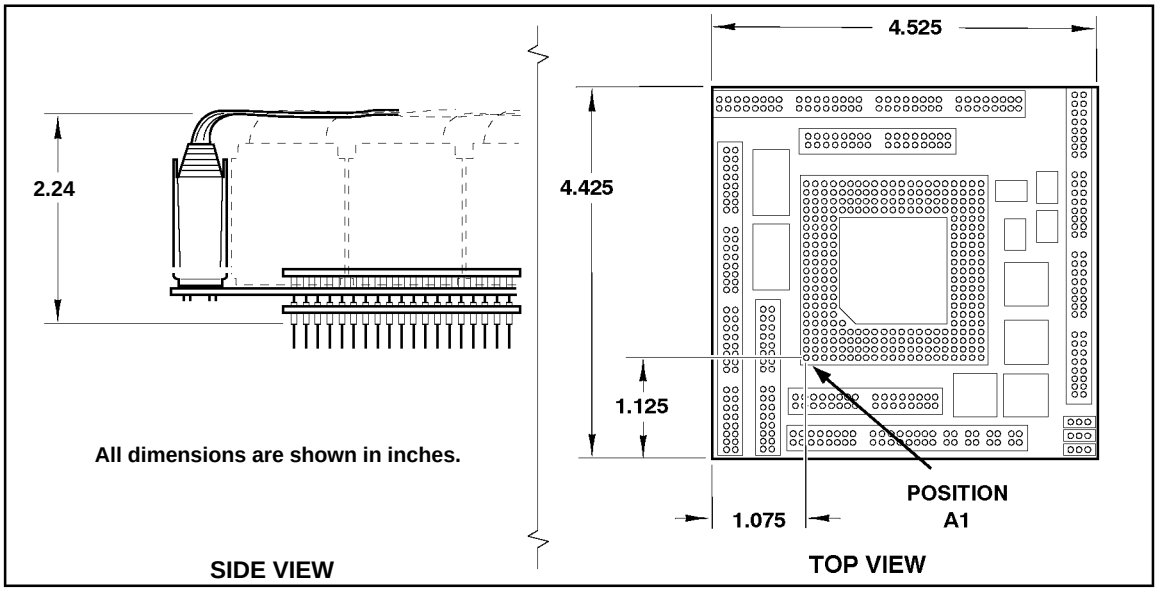

Figure C-2. Minimum clearance of the probe adapter.

Table C-3
Environmental Specifications

Characteristic	Description
Temperature	
Max. Operating	+50°C (122°F)*
Min. Operating	0°C (+32°F)
Nonoperating	–55°C to +75°C (–67° to +167°F)
Humidity	10 to 95% relative humidity†
Altitude	
Operating	4.5 km (15,000 ft) maximum
Nonoperating	15 km (50,000 ft) maximum
Electrostatic Immunity	The probe adapter is static sensitive

* Not to exceed Pentium microprocessor thermal considerations. Forced air cooling may be required across the CPU.
† Tested to Tektronix standard 062-2847-00 class 5.

Channel Assignments

All channel assignments listed in the following tables are required for disassembly unless noted otherwise. A pound sign (#) following a signal name indicates that the signal is active low.

The 92A96 Module in the higher-numbered slot is referred to as the HI module; the module in the lower-numbered slot is referred to as the LO module. Probe connections on the probe adapter board are labeled to identify which module and which probe group connects to them. For example, HI_A0 indicates the A0 probe group from the HI module.

Clock pins on the probe adapter board do not have the HI/LO designation; they are just labeled CK0, CK1, CK2, and CK3. Each pair of clock pins connect to the same signal on the probe adapter. The clock podlets from both modules must connect to the appropriate clock pins for 92A96 P5 Custom clocking to function properly.

Table C-4 shows the 92A96 section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. The channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).

Table C-4
92DM13A Control Group Channel Assignments

Bit Order	Variable-Width Module Section & Channel		Pentium Microprocessor Signal Name
	LO or HI Module	Section & Channel	
MSB	HI	C3:2	INIT
	LO/HI	C2:0	RESET‡
	HI	C3:6	PRDY
	LO	C3:5	BUSCHK#
	LO	C2:6	SMIACT#
	HI	C2:6	LOCK#
	HI	C2:5	SCYC
	LO	C2:4	LAST_D
	HI	C3:3	AHOLD
	LO/HI	C2:2	HLDA‡
	LO/HI	C2:1	BOFF#‡
	LO	C2:7	M/IO#
	LO	C3:7	D/C#
LSB	LO	C3:3	W/R#

All signals required for disassembly.
‡Signal is double probed for clocking purposes. Only data from the LO module is displayed.

Table C-5 shows the 92A96 section and channel assignments for the Address group, starting with the most significant bit (MSB).

Table C-5
92DM13A Address Group Channel Assignments

Bit Order	Variable-Width Module Section & Channel		Pentium Microprocessor Signal Name
	LO or HI Module	Section & Channel	
MSB	LO	A3:7	A31
	LO	A3:6	A30
	LO	A3:5	A29
	LO	A3:4	A28
	LO	A3:3	A27
	LO	A3:2	A26
	LO	A3:1	A25
	LO	A3:0	A24
	LO	A2:7	A23
	LO	A2:6	A22
	LO	A2:5	A21
	LO	A2:4	A20
	LO	A2:3	A19
	LO	A2:2	A18
	LO	A2:1	A17
	LO	A2:0	A16
	LO	A1:7	A15
	LO	A1:6	A14
	LO	A1:5	A13
	LO	A1:4	A12
	LO	A1:3	A11
	LO	A1:2	A10
	LO	A1:1	A9
	LO	A1:0	A8
	LO	A0:7	A7
	LO	A0:6	A6
	LO	A0:5	A5
	LO	A0:4	A4
	LO	A0:3	A3
	LO	A0:2	GND (A2)
	LO	A0:1	GND (A1)
LSB	LO	A0:0	GND (A0)

All signals required for disassembly.

Table C-6 shows the 92A96 section and channel assignments for the Data group, starting with the most significant bit (MSB).

Table C-6
92DM13A Data Group Channel Assignments

Bit Order	Variable-Width Module Section & Channel		Pentium Microprocessor Signal Name
	LO or HI Module	Section & Channel	
MSB	HI	D3:7	D63
	HI	D3:6	D62
	HI	D3:5	D61
	HI	D3:4	D60
	HI	D3:3	D59
	HI	D3:2	D58
	HI	D3:1	D57
	HI	D3:0	D56
	HI	D2:7	D55
	HI	D2:6	D54
	HI	D2:5	D53
	HI	D2:4	D52
	HI	D2:3	D51
	HI	D2:2	D50
	HI	D2:1	D49
	HI	D2:0	D48
	HI	D1:7	D47
	HI	D1:6	D46
	HI	D1:5	D45
	HI	D1:4	D44
	HI	D1:3	D43
	HI	D1:2	D42
	HI	D1:1	D41
	HI	D1:0	D40
	HI	D0:7	D39
	HI	D0:6	D38
	HI	D0:5	D37
	HI	D0:4	D36
	HI	D0:3	D35
	HI	D0:2	D34
	HI	D0:1	D33
LSB	HI	D0:0	D32

All signals required for disassembly.

Table C-7 shows the 92A96 section and channel assignments for the Data_Lo group, starting with the most significant bit (MSB).

Table C-7
92DM13A Data_Lo Group Channel Assignments

Bit Order	Variable-Width Module Section & Channel		Pentium Microprocessor Signal Name
	LO or HI Module	Section & Channel	
MSB	LO	D3:7	D31
	LO	D3:6	D30
	LO	D3:5	D29
	LO	D3:4	D28
	LO	D3:3	D27
	LO	D3:2	D26
	LO	D3:1	D25
	LO	D3:0	D24
	LO	D2:7	D23
	LO	D2:6	D22
	LO	D2:5	D21
	LO	D2:4	D20
	LO	D2:3	D19
	LO	D2:2	D18
	LO	D2:1	D17
	LO	D2:0	D16
	LO	D1:7	D15
	LO	D1:6	D14
	LO	D1:5	D13
	LO	D1:4	D12
	LO	D1:3	D11
	LO	D1:2	D10
	LO	D1:1	D9
	LO	D1:0	D8
	LO	D0:7	D7
	LO	D0:6	D6
	LO	D0:5	D5
	LO	D0:4	D4
	LO	D0:3	D3
	LO	D0:2	D2
	LO	D0:1	D1
LSB	LO	D0:0	D0

All signals required for disassembly.

Table C-8 shows the 92A96 section and channel assignments for the DataSize group, and the microprocessor signal to which each channel connects, starting with the most significant bit (MSB).

Table C-8
92DM13A DataSize Group Channel Assignments

Bit Order	Variable-Width Module Section & Channel		Pentium Microprocessor Signal Name
	LO or HI Module	Section & Channel	
MSB	HI	A1:3	BE7#
	HI	A1:2	BE6#
	HI	A1:1	BE5#
	HI	A1:0	BE4#
	HI	A0:7	BE3#
	HI	A0:6	BE2#
	HI	A0:5	BE1#
LSB	HI	A0:4	BE0#

All signals required for disassembly.

Table C-9 shows the 92A96 section and channel assignments for the Cache group, and the microprocessor signal to which each channel connects, starting with the most significant bit (MSB).

Table C-9
92DM13A Cache Group Channel Assignments

Bit Order	Variable-Width Module Section & Channel		Pentium Microprocessor Signal Name
	LO or HI Module	Section & Channel	
MSB	HI	C2:7	CACHE#†
	LO	C3:2	KEN#†
	HI	A3:0	EADS#†
	HI	A3:4	FLUSH#†
	HI	A3:7	PCD†
	HI	A3:3	PWT†
	HI	A1:4	HIT#†
	HI	A1:5	HITM#†
	HI	A2:7	INV†
LSB	HI	A3:1	WB/WT#†

† Signal not required for disassembly.

Table C-10 shows the 92A96 section and channel assignments for the Debug group, and the microprocessor signal to which each channel connects, starting with the most significant bit (MSB).

Table C-10
92DM13A Debug Group Channel Assignments

Bit Order	Variable-Width Module Section & Channel		Pentium Microprocessor Signal Name
	LO or HI Module	Section & Channel	
MSB	HI	A2:4	BP3†
	HI	A2:5	BP2†
	HI	A2:2	PM1/BP1†
	HI	A2:3	PM0/BP0†
	HI	A2:0	IU†
	HI	A2:6	IV†
	HI	A1:7	IBT†
LSB	HI	C2:4	R/S#†

† Signal not required for disassembly.

Table C-11 shows the 92A96 section and channel assignments for the Misc group, and the microprocessor signal to which each channel connects, starting with the most significant bit (MSB).

Table C-11
92DM13A Misc Group Channel Assignments

Bit Order	Variable-Width Module Section & Channel		Pentium Microprocessor Signal Name
	LO or HI Module	Section & Channel	
MSB	HI	C3:4	CLK†
	LO	C2:3	ADS#‡
	LO	C3:6	NA#†
	LO	C3:1	BRDY#†
	LO	C2:5	BRDYC#†
	LO	C3:0	PIPE_D†
	LO	C3:4	DVALID_D†
	HI	C3:5	PEN#†
	HI	A3:6	APCHK#†
LSB	HI	A3:2	PCHK#†

† Signal not required for disassembly.
‡Signal is double probed for clocking purposes. Only data from the LO module is displayed.

Table C-12 shows the 92A96 section and channel assignments for the Misc2 group, and the microprocessor signal to which each channel connects, starting with the most significant bit (MSB).

Table C-12
92DM13A Misc2 Group Channel Assignments

Bit Order	Variable-Width Module Section & Channel		Pentium Microprocessor Signal Name
	LO or HI Module	Section & Channel	
MSB	HI	C3:7	NMI†
	HI	A1:6	INTR†
	HI	C3:0	SMI#†
	HI	C3:1	IGNNE#†
	HI	A2:1	FERR#†
LSB	HI	A3:5	HOLD†

† Signal not required for disassembly.

Table C-13 shows the 92A96 section and channel assignments for the BT group, and the microprocessor signal to which each channel connects, starting with the most significant bit (MSB).

Table C-13
92DM13A BT Group Channel Assignments

Bit Order	Variable-Width Module Section & Channel		Pentium Microprocessor Signal Name
	LO or HI Module	Section & Channel	
MSB	HI	A0:3	BT3†
	HI	A0:2	BT2†
	HI	A0:1	BT1†
LSB	HI	A0:0	BT0†

† Signal not required for disassembly.

Table C-14 shows the 92A96 section and channel assignments for the clock channels (not part of any group), and the signal to which each channel connects. Assignments are the same for HI and LO modules.

Table C-14
92DM13A Clock Channel Assignments

Clock Channel	Signal Name	Clk or Qual
CLK3	CLK=	CLK, rising
CLK2	LAST_D=*	QUAL
CLK1	PIPE_D=*	QUAL
CLK0	DVALID_D=*	QUAL

* Signal is derived on the probe adapter, and is triple-probed.
All signals required for disassembly.

DISCONNECTING PROBES

You may need to disconnect the clock and 8-channel probes from the probe adapter to use them on another application, to connect individual podlets to other signals in your Pentium microprocessor system, or to replace defective clock or probe channels (podlets). Refer to Figure C-3 and the following procedure to disconnect the clock and 8-channel probes from the probe adapter. Use the antistatic shipping material to support the probe adapter while disconnecting the clock and 8-channel probes.

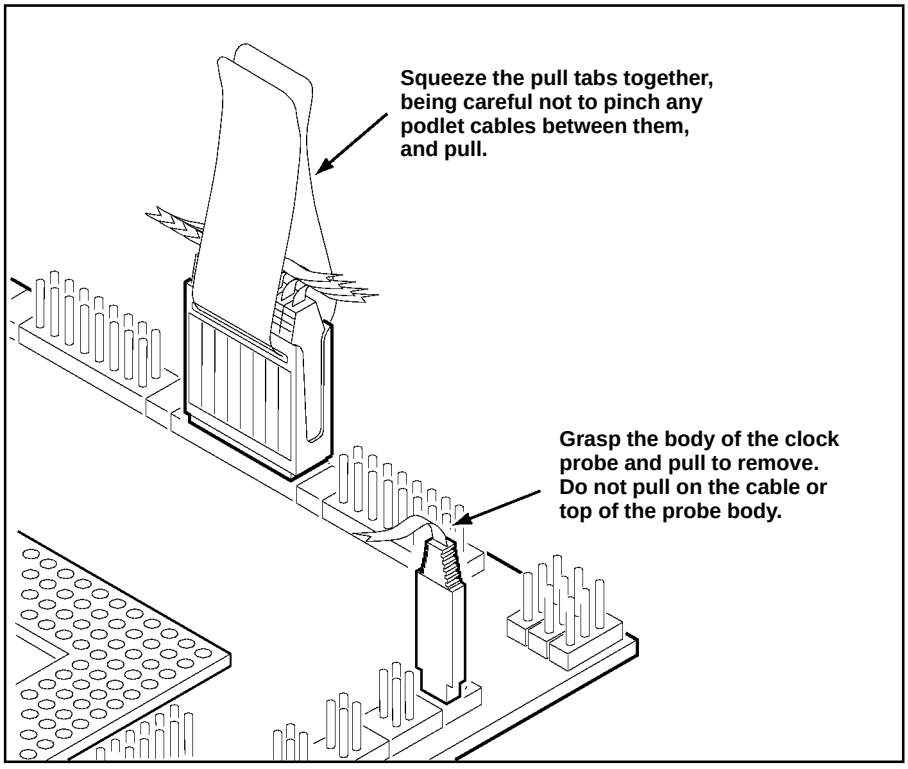

Figure C-3. Disconnecting clock and 8-channel probes.

1. Power off the SUT. It is not necessary to power off the DAS 9200.

CAUTION

Pulling on the cables, on the neck of the clock probe, or pinching the cables between the pull tabs can damage the probes. Always handle the probes by their bodies.

2. Firmly grasp the body of a clock probe and gently pull it off of the square pins.

3. Squeeze the pull tabs on the podlet holder together, be careful not to pinch any podlet cables between them.
4. Gently pull the 8-channel probe off of the square pins.

REMOVING AND REPLACING PROBE PODLETS

Each 8-channel probe consists of 8 single-channel podlets ganged together in a podlet holder. You may need to remove these podlets from the 8-channel probe to use for alternate connections to Pentium microprocessor system signals.

Refer to the discussions on *Alternate Microprocessor Connections* in Appendix B and *Channel Assignments* in Appendix C for information about which channels you can use to make alternate connections between the DAS 9200 and system under test without disturbing the channel connections required for disassembly.

You can also use these procedures to replace a defective clock probe or a defective podlet from an 8-channel probe.

Removing Probe Podlets from the Interface Housing

Refer to Figure C-4 and the following procedure to remove a clock probe or an 8-channel probe podlet from the interface housing.

1. Power off the SUT. It is not necessary to power off the DAS 9200.
2. Use a small pointed tool such as a ballpoint pen, pencil, or straightened paper clip to press down on the latch detent of the podlet through an opening on the interface housing.
3. Gently pull the podlet connector out of the housing with one hand while pressing down on the latch detent with the pointed tool.

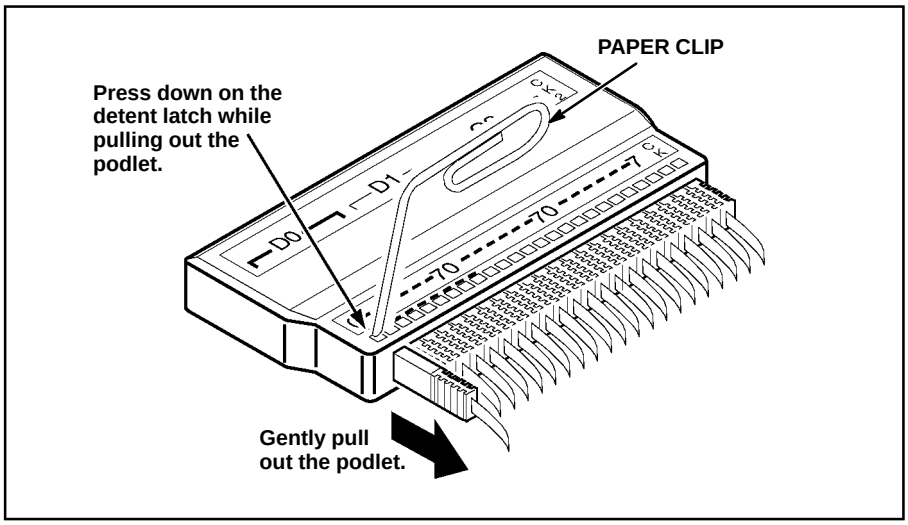

Figure C-4. Removing a clock or probe podlet from the interface housing.

Replacing a Clock Probe

To replace a clock probe, insert a new clock probe into the same clock channel position on the interface housing. Insert the clock probe into the interface housing with the detent latch oriented to the label side of the housing. Refer to Figure C-4.

Removing Probe Podlets from the Podlet Holder

Refer to Figure C-5 and the following procedure to remove the 8-channel probe podlets from the podlet holder.

CAUTION

Excessive pulling on the sides of the holder can damage the podlet holder. Spread the holder open wide enough to clear and remove the podlets.

1. To remove podlets from the podlet holder, grasp the plastic pull tab on each side of the podlet holder and gently spread the sides of the holder open just enough to clear a podlet.
2. Remove the middle two podlets from the podlet holder by pushing up on the metal pin receptacles.
3. Release the tabs on the podlet holder.
4. Remove the remaining podlets by turning and extracting each one at a time.

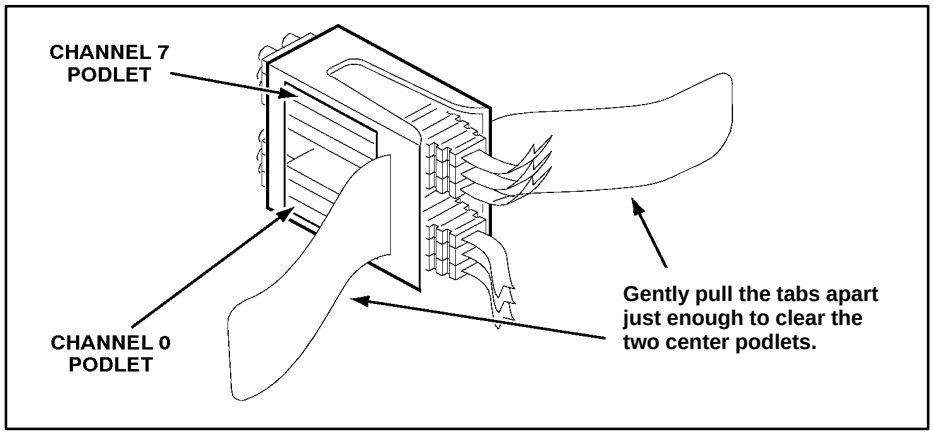

Figure C-5. Ganging together the 8-channel probe podlets.

Replacing 8-Channel Probe Podlets

The channel podlets must retain the same channel order on both the interface housing and in the podlet holder. Be sure to replace the old podlet with a podlet of the same color. Table C-15 shows the color code and channel number of each podlet for an 8-channel probe.

Table C-15
Podlet-to-Channel Color Code

Podlet Color	Channel
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7

Refer to Figure C-5 and the following procedure to replace an 8-channel probe podlet.

1. Insert the appropriately colored podlet into the interface housing with the detent latch oriented to the label side of the housing.
2. If you are replacing a single podlet, orient the podlet connector marked GND towards the side of the podlet holder labeled GROUND.
3. Grasp the plastic pull tab on each side of the holder and gently spread the sides of the holder open just enough to clear the podlet.

4. Hold the podlet body with the other hand and place it in the holder in the correct channel order. Do not grasp and turn the podlet cable.
5. If you are reganging all the podlets of an 8-channel probe, begin ganging the podlets together starting with either channel 0 or channel 7. Orient the podlet channel marked GND towards the side of the podlet holder labeled GROUND.

CAUTION

Avoid twisting the podlet cables between the interface housing and the podlet holder. To prevent damage to the podlets, keep the podlet cables parallel to each other when ganging them into the holder.

6. Hold the podlet body, turn the podlet body parallel to the sides of the holder, move it into the holder, and use your fingers to press it into place perpendicular to the sides of the holder. Be sure to gang the podlets in the correct channel order according to the channel label on the podlet holder and podlet color code, with all ground channels toward the Ground side of the holder. Do not place the podlet into the holder by grasping the podlet cable.
7. Continue placing the next two podlets, one at a time, in channel order, in the podlet holder. Orient all ground channels toward the Ground side of the holder.
8. The fourth podlet should be either channel 0 or 7, whichever one is not already placed in the holder. Place this podlet in the other end of the podlet holder and orient the ground channel correctly.
9. Continue placing the next two podlets, one at a time, in channel order, in the podlet holder. Continue orienting the ground channels correctly.

CAUTION

Excessive pulling on the sides can break the podlet holder. Spread the holder open only wide enough to clear the podlet.

10. Grasp the plastic pull tab on each side of the holder and gently spread the sides of the holder open just enough to clear a podlet.
11. Place the last pair of podlets (channels 3 and 4) in the podlet holder in proper channel order, orienting the ground channels to the Ground side of the holder.

REMOVING AND REPLACING SOCKETS

The probe adapter board contains sockets designed to protect the probe adapter, and to make it easy to insert and remove the microprocessor. The socket on top of the probe adapter board is soldered and cannot be removed. The protective socket on the bottom of the probe adapter board can be removed.

You should not have to remove the replaceable protective socket on the probe adapter unless the pins on the socket are damaged. To remove the protective socket, refer to Figure C-6 and follow these steps:

1. Place a proper (nonmetallic) socket removal tool between the socket and the probe adapter board. Figure C-6 shows an AMP PGA removal tool.

CAUTION

Do not use a screwdriver to remove the protective socket from the probe adapter board. You can easily damage the etched runs on the board.

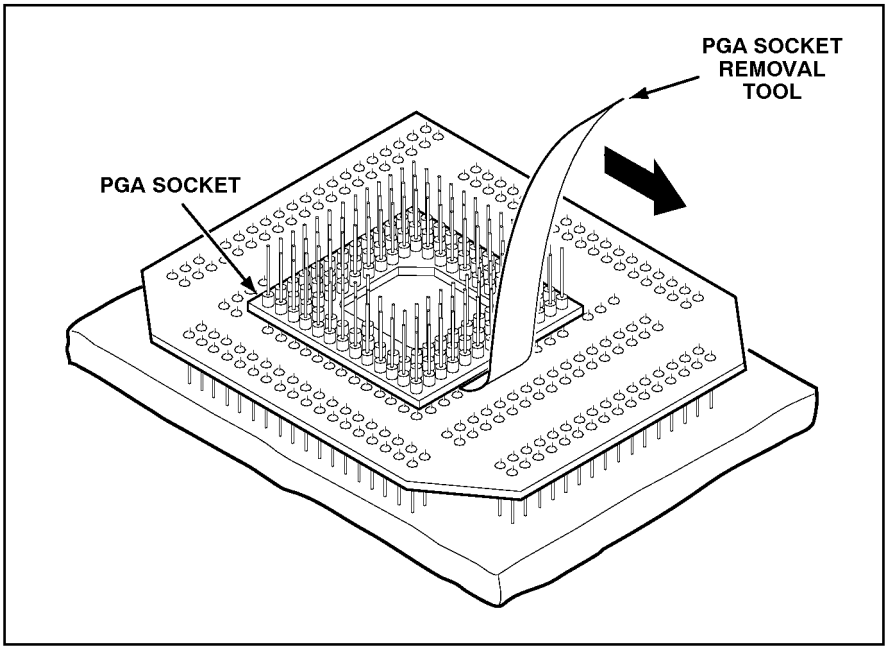

Figure C-6. Removing a protective socket from a typical PGA probe adapter board.

2. Push down on the handle of the tool until the socket begins to separate from the probe adapter board pins.

CAUTION

Do not completely pry off one side of the protective socket and then the other. Applying uneven pressure can damage the socket's pins. Do not use board components as leverage to remove the socket.

3. Perform step 2 on all sides of the socket. Use even pressure alternately on all sides until the socket is loose.
4. Remove the socket from the board.

To replace the protective socket, follow these steps:

1. Spray an electrical contact lubricant on the probe adapter socket so the replacement socket can be easily inserted.
2. Check that the new socket's pins are straight.
3. Place the socket on the pins of the probe adapter board aligning pin A1 with pin A1; make sure that all pins line up correctly.
4. Press the socket onto the board by applying equal pressure on two opposed sides of the socket.

F

G

H

I

J

L

M

O

P

R

S

T

U

V