Instruction Manual

Tektronix

TMS 165
i960RP Microprocessor Support

070-9681-01

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 165 i960RP microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 165 i960RP support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- The term “XXX” or “P54C” used in field selections and file names must be replaced with i960RP. This is the name of the microprocessor in field selections and file names you must use to operate the i960RP support.
- The term “SUT” (system under test) refers to the microprocessor-based system from which data will be acquired.

- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.
- The term “module” refers to a 102/136-channel or a 96-channel module.
- A tilde (~) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics and tasks:

- A description of the TMS 165 microprocessor support package
- Logic analyzer software compatibility
- Your SUT (system under test) requirements
- Support restrictions
- How to connect to your SUT

Support Description

The TMS 165 microprocessor support package disassembles data from systems that are based on the i960RP microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 165 microprocessor support.

The TMS 165 supports the i960RP microprocessor in a 352-pin BGA package.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *i960RP Microprocessor User's Manual*, Intel, February 1996, Intel order number: 272736-001

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the i960RP support, the Tektronix logic analyzer must be equipped with either a 102/136-channel module, or a 96-channel module at a minimum. The module must be equipped with enough probes to acquire channel and clock data from signals in your i960RP-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other i960RP support requirements and restrictions.

System Clock Rate. The TMS 165 support can acquire data from the i960RP microprocessor at speeds of up to 33 MHz[1].

Hardware Reset. If a hardware reset occurs in your i960RP system during an acquisition, the disassembler might acquire an invalid sample.

Cache Invalidation. Correct disassembly is not guaranteed for microprocessor systems that run cache invalidations concurrent with burst cycles. Data for these cycles will not be disassembled and will be labeled as Cache Invalidation cycles.

Disabling the Instruction Cache. To disassemble acquired data, you must disable the internal instruction cache. Disabling the instruction cache makes all instruction prefetches visible on the bus so that they can be acquired and disassembled.

Disabling the Data Cache. To disassemble acquired data, you must disable the internal data cache. Disabling the data cache makes all data prefetches visible on the bus so that they can be acquired and disassembled.

1 **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

Dynamic Bus Sizing. When the Bus Size Control signals (BS16# or BS8#) are asserted, the i960RP microprocessor allows the bus width to be changed to handle extra cycles (when more than one cycle is required for a transaction). The disassembler does not support changing the bus size for extra cycles. To keep the disassembler synchronized, you can use the mark cycles function as described in the *Operating Basics* chapter.

Automatic dequeueing. Automatic dequeueing may not be performed in all circumstances. When a branch takes place the automatic dequeueing may or may not take place depending on word alignment of the target of the branch. For more information on automatic dequeueing and word alignment refer to section 4.3.2 in the *i960RP Microprocessor User's Manual*, Intel, February 1996.

PCI Functionality. PCI functionality is not supported on the i960RP support.

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. The probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

With a Probe Adapter and Elastomer

To connect the logic analyzer to a SUT using the elastomer and the probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer.

3. Place the elastomer over the pad array on your SUT. The elastomer is keyed by one of the three holes being larger then the other two.

4. Place the probe adapter over the elastomer being careful to orient the larger hole in the probe adapter over the larger flange of the elastomer.

CAUTION. *Failure to correctly place the elastomer may result in damage to the probe adapter, the elastomer, and your SUT.*

One of the holes on the Probe Adapter is larger then the other two. The larger hole is a key for the large flange on the elastomer.

5. Fasten the probe adapter to the SUT using three screws, six flat washers, and three hex nuts. Refer to Figure 1–1.

6. Tighten the screws. The elastomer needs to be compressed at the rate of 3 lb. per linear inch. Tighten the screws at a torque rating of 3 in. lbs, minimum, and 8 in. lbs., maximum torque.

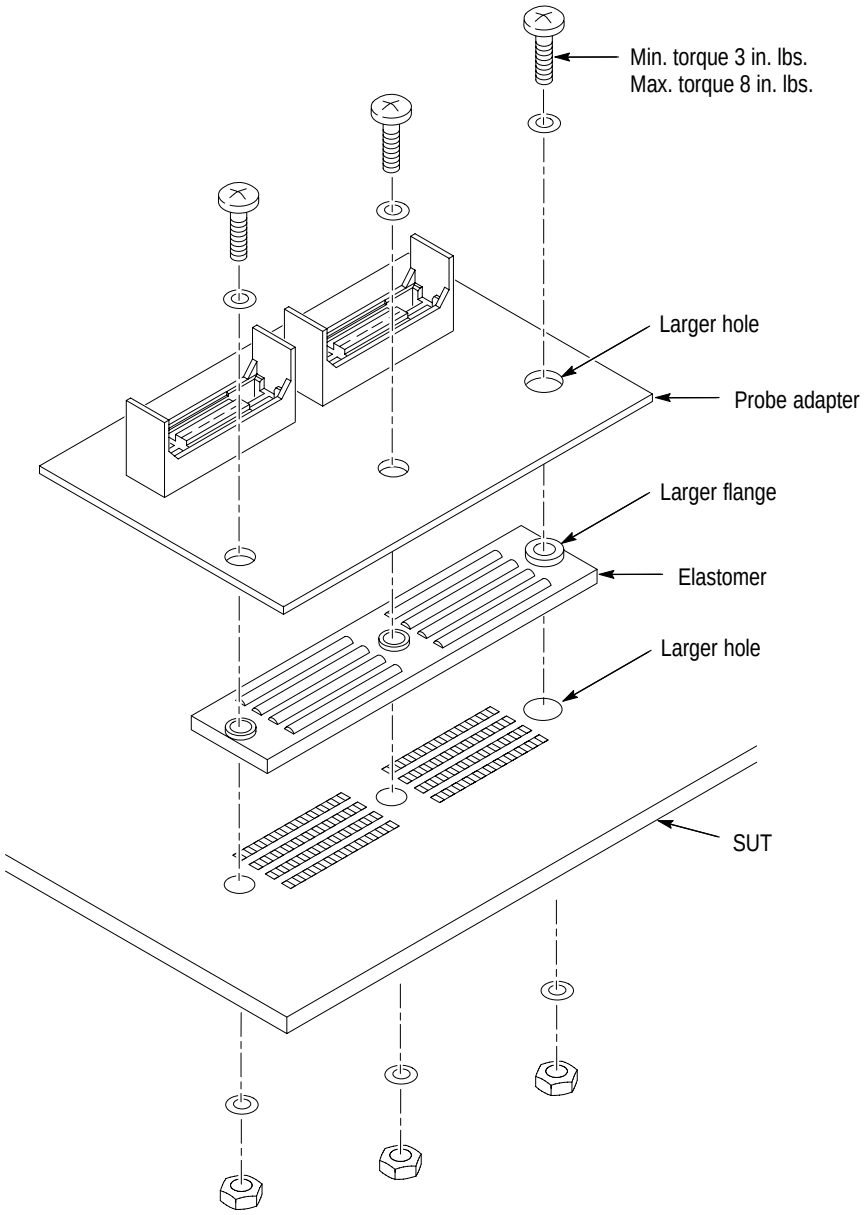


Figure 1–1: Attaching the probe adapter to your SUT

CAUTION. *Incorrect handling of the P6434 probe or Mass Termination Interface (MTIF) probe while connecting it to the probe adapter board connector can result in damage to the P6434 probe, the MTIF probe, or to the mating connector.*

To avoid damaging the P6434 probe or MTIF probe always position the P6434 probe or MTIF probe perpendicular to the mating connector and gently connect.

7. Line up the pin 1 indicator on the P6434 probe or the MTIF probe with the pin-1 indicator on the Mictor connector on the probe adapter board. The Mictor connector on the probe adapter board is keyed to prevent incorrect insertion of the P6434 probe or the MTIF probe.

8. Position the P6434 probe or the MTIF probe perpendicular to the mating connector and gently connect the probe to the mating connector on the probe adapter as shown in Figure 1–2.

9. When connected, push down the latch releases on the P6434 probe or the MTIF probe to set the latch. To remove, pull up on the latch release to disengage the latch.

10. Connect the module end of the P6434 probe or the MTIF probe to the corresponding connector (match label colors) on the logic analyzer module. The module end of the P6434 probe or the MTIF probe is also keyed.

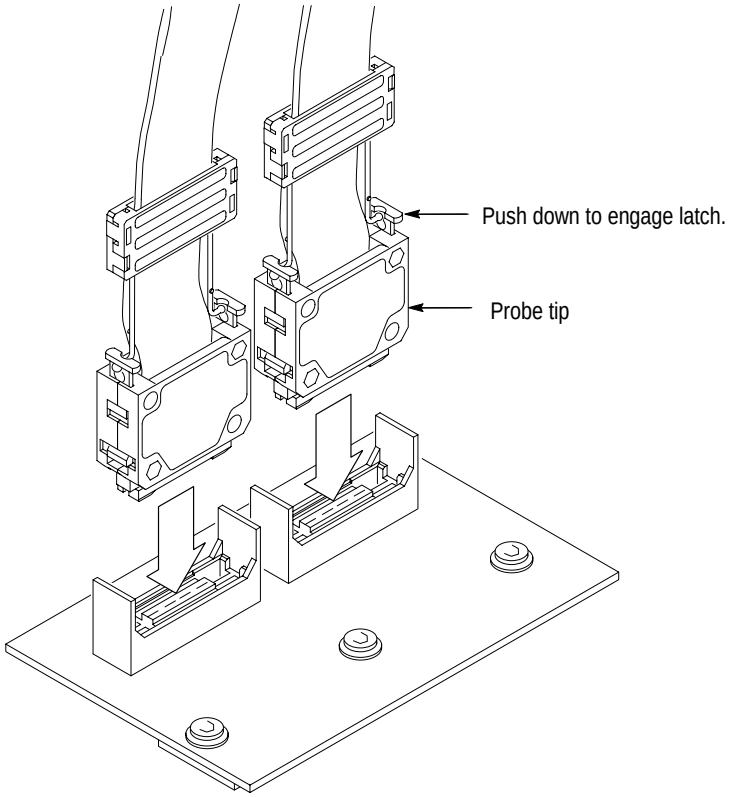


Figure 1–2: Connecting probes to the probe adapter

***NOTE**. If you are using a Mass Termination Interface (MTIF), refer to those instructions to complete the connection.*

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to i960RP signals in the SUT using a test clip (or adapter), follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.
3. Use Table 1–1 and Table 1–2 to connect the channel probes, clock probes, and leadsets between the logic analyzer and the i960RP signal pins on your test clip (or adapter).

   Connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip (or adapter).

Table 1–1: i960RP signal connections for channel probes

Section:channel	i960RP signal	Section:channel	i960RP signal
A3:7	AD31	D3:7	D31 †
A3:6	AD30	D3:6	D30 †
A3:5	AD29	D3:5	D29 †
A3:4	AD28	D3:4	D28 †
A3:3	AD27	D3:3	D27 †
A3:2	AD26	D3:2	D26 †
A3:1	AD25	D3:1	D25 †
A3:0	AD24	D3:0	D24 †
A2:7	AD23	D2:7	D23 †
A2:6	AD22	D2:6	D22 †
A2:5	AD21	D2:5	D21 †
A2:4	AD20	D2:4	D20 †
A2:3	AD19	D2:3	D19 †
A2:2	AD18	D2:2	D18 †

Table 1–1: i960RP signal connections for channel probes (cont.)

Section:channel	i960RP signal	Section:channel	i960RP signal
A2:1	AD17	D2:1	D17 †
A2:0	AD16	D2:0	D16 †
A1:7	AD15	D1:7	D15 †
A1:6	AD14	D1:6	D14 †
A1:5	AD13	D1:5	D13 †
A1:4	AD12	D1:4	D12 †
A1:3	AD11	D1:3	D11 †
A1:2	AD10	D1:2	D10 †
A1:1	AD9	D1:1	D9 †
A1:0	AD8	D1:0	D8 †
A0:7	AD7	D0:7	D7 †
A0:6	AD6	D0:6	D6 †
A0:5	AD5	D0:5	D5 †
A0:4	AD4	D0:4	D4 †
A0:3	AD3	D0:3	D3 †
A0:2	AD2	D0:2	D2 †
A0:1	AD1	D0:1	D1 †
A0:0	AD0	D0:0	D0 †
C3:7	S_CLK	C2:7	LOCK~
C3:6	BE3~	C2:6	D/C~
C3:5	BE1~	C2:5	BLAST~
C3:4	W/R~	C2:4	WIDTH0
C3:3	L_RST~	C2:3	HOLDA
C3:2	BE2~	C2:2	RDYRCV~
C3:1	BE0~	C2:1	LRDYRCV~
C3:0	WIDTH1	C2:0	ADS~

Table 1–1: i960RP signal connections for channel probes (cont.)

Section:channel	i960RP signal	Section:channel	i960RP signal
C1:7	XINT7~ *	C0:7	XINT5~ *
C1:6	XINT3~ *	C0:6	XINT1~ *
C1:5	P_RST~ *	C0:5	NMI~ *
C1:4	DEN~ *	C0:4	WAIT~ *
C1:3	XINT6~ *	C0:3	XINT4~ *
C1:2	XINT2~ *	C0:2	XINT0~ *
C1:1	FAIL~ *	C0:1	HOLD *
C1:0	DT/R~ *	C0:0	ALE *

***** **Signal not required for disassembly.**

† **The Data bus is multiplexed, acquisition channels D3:7-0, D2:7-0, D1:7-0, and D0:7-0 do not need to be physically connected. But these are not extra channels and can not be connected to podlets as these channels are already assigned to Data channels and will get their inputs from the Address channels.**

Table 1–2 shows the clock probes and the i960RP signal to which they must connect for disassembly to be correct.

Table 1–2: i960RP signal connections for clock probes

Section:channel	i960RP signal
CK:1	BLAST~ =
CK:0	S_CLK =

= **Indicates the channel is double probed.**

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 165 i960RP support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the i960RP support are: Address, Data, Control, ByteEnbl, Aux, Interrupt and Misc.

If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–4.

Clocking Options

The TMS 165 support offers a microprocessor-specific clocking mode for the i960RP microprocessor. This clocking mode is the default selection whenever you load the i960RP support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The TMS 165 support has two modes of clocking:

- Ext. Bus Master Cycles Excluded, where DMA cycles are not acquired. This is the default acquisition clocking selection.
- Ext. Bus Master Cycles Included, where DMA cycles are acquired.

Symbols

The TMS 165 support supplies one symbol table file. The i960RP_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file i960RP_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value HOLDA WIDTH1 WIDTH0 LOCK~ BLAST~ W/R~ D/C~ RDYRCV~ LRDYRCV~	Meaning
HALT	X X 1 1 X X X X X	Processor halted
FETCH_8	1 0 0 0 X 0 0 0 X	Code read – 8 bit
FETCH_8	1 0 0 0 X 0 0 X 0	Code read – 8 bit
FETCH_16	1 0 0 1 X 0 0 0 X	Code read – 16 bit
FETCH_16	1 0 0 1 X 0 0 X 0	Code read – 16 bit
FETCH_32	1 0 1 0 X 0 0 X 0	Code read – 32 bit
FETCH_32	1 0 1 0 X 0 0 X 0	Code read – 32 bit
READ_8	1 0 0 0 X 0 1 0 X	Non burst 8 bit memory read cycle
READ_8	1 0 0 0 X 0 1 X 0	Non burst 8 bit memory read cycle
READ_16	1 0 0 1 X 0 1 0 X	Non burst 16 bit memory read cycle
READ_16	1 0 0 1 X 0 1 X 0	Non burst 16 bit memory read cycle
READ_32	1 0 1 0 X 0 1 0 X	Non burst 32 bit memory read cycle
READ_32	1 0 1 0 X 0 1 X 0	Non burst 32 bit memory read cycle

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value LOCK~ HOLDA WIDTH1 WIDTH0 BLAST~ W/R~ D/C~ RDYRCV~ LRDYRCV~	Meaning
WRITE_8	1 0 0 0 X 1 1 0 X	Non burst 8 bit memory write cycle
WRITE_8	1 0 0 0 X 1 1 X 0	Non burst 8 bit memory write cycle
WRITE_16	1 0 0 1 X 1 1 0 X	Non burst 16 bit memory write cycle
WRITE_16	1 0 0 1 X 1 1 X 0	Non burst 16 bit memory write cycle
WRITE_32	1 0 1 0 X 1 1 0 X	Non burst 32 bit memory write cycle
WRITE_32	1 0 1 0 X 1 1 X 0	Non burst 32 bit memory write cycle
L_READ_8	0 0 0 0 0 0 1 0 X	8 bit read cycle of the atomic memory
L_READ_8	0 0 0 0 0 0 1 0 X	8 bit read cycle of the atomic memory
L_READ_16	0 0 0 1 0 0 1 X 0	16 bit read cycle of the atomic memory
L_READ_16	0 0 0 1 0 0 1 X 0	16 bit read cycle of the atomic memory
L_READ_32	0 0 1 0 0 0 1 0 X	32 bit read cycle of the atomic memory
L_READ_32	0 0 1 0 0 0 1 X 0	32 bit read cycle of the atomic memory
L_WRITE_8	0 0 0 0 0 1 1 X 0	8 bit write cycle of the atomic memory
L_WRITE_8	0 0 0 0 0 1 1 0 X	8 bit write cycle of the atomic memory
L_WRITE_16	0 0 0 1 0 1 1 X 0	16 bit write cycle of the atomic memory
L_WRITE_16	0 0 0 1 0 1 1 0 X	16 bit write cycle of the atomic memory
L_WRITE_32	0 0 1 0 0 1 1 X 0	32 bit write cycle of the atomic memory
L_WRITE_32	0 0 1 0 0 1 1 0 X	32 bit write cycle of the atomic memory
DMA_READ	X 1 X X X 0 X 0 X	DMA read from memory
DMA_READ	X 1 X X X 0 X X 0	DMA read from memory
DMA_WRITE	X 1 X X X 1 X 0 X	DMA write to memory
DMA_WRITE	X 1 X X X 1 X X 0	DMA write to memory

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value HOLDA WIDTH1 WIDTH0 LOCK~ BLAST~ W/R~ D/C~ RDYRCV~ LRDYRCV~	Meaning
BACK_OFF	1 0 X X 1 X 1 1 1	Processor in back off state
UNDEFINED	X X X X X X X X X	None of the above

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- Changing the way data is displayed
- Changing disassembled cycles with the mark cycles function

Acquiring Data

Once you load the i960RP support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE*. Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–9.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows these special characters and strings, and gives a definition of what they represent.

Table 2–2: Meaning of special characters in the display

Character or string displayed	Meaning
#	Indicates an immediate value
>	There is insufficient room on the screen to show all available data
m or >>	The instruction was manually marked by the user
t	Indicates the number shown is in decimal, such as #12t
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–3: Cycle type definitions

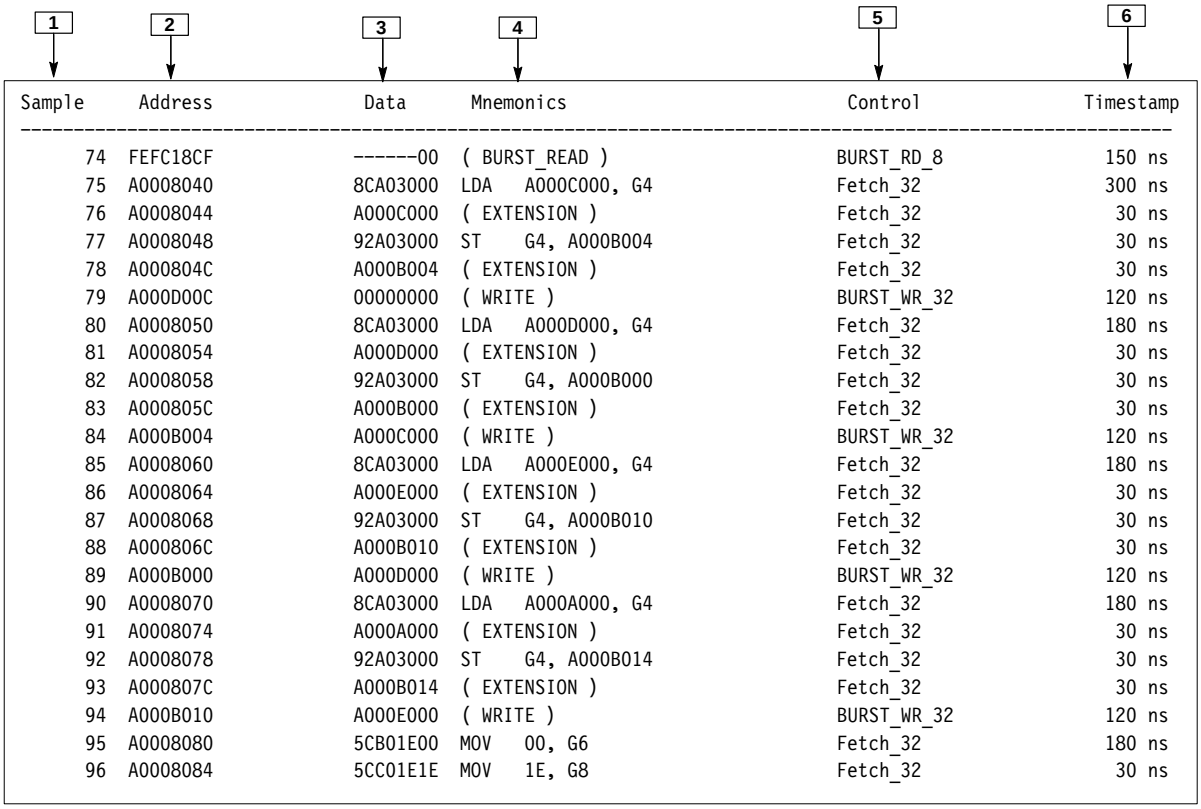
Cycle type	Definition
(READ)	Basic read from memory
(WRITE)	Basic write to memory
(BURST_READ)	Burst read from memory
(BURST_WRITE)	Burst write to memory
(LOCKED_READ)	Read cycle of the atomic memory access
(LOCKED_WRITE)	Write cycle to the atomic memory access
(DMA_READ)	DMA read from memory
(DMA_WRITE)	DMA write to memory
(HALT)	Processor halt
(BACK_OFF)	Processor in back off state
(STEST FAIL)	Processor has failed in self test
(RESET LOCATION)	Processor has reset and started fetching at address FEFF FF38
(FLUSH) †	Instruction fetch not executed by the processor
(EXTENSION) †	The second word of an extended opcode is fetched from memory
(PREFETCH BYTE) †	8-bit instruction fetch
(PREFETCH HALF-WORD) †	16-bit instruction fetch

Table 2–3: Cycle type definitions (cont.)

Cycle type	Definition
* ILLEGAL INSTRUCTION * †	Not a valid instruction
(UNKNOWN)	Unrecognized cycle type

† **This cycle type is deduced by the disassembler. This means that this cycle type is determined by other factors in addition to the control group value.**

Figure 2–1 shows an example of the Hardware display.




```
Sample     Address            Data      Mnemonics                          Control          Timestamp
-------------------------------------------------------------------------------------------------------
     74  FEFC18CF           ------00  ( BURST_READ )                     BURST_RD_8          150 ns
     75  A0008040           8CA03000  LDA   A000C000, G4                 Fetch_32            300 ns
     76  A0008044           A000C000  ( EXTENSION )                      Fetch_32             30 ns
     77  A0008048           92A03000  ST    G4, A000B004                 Fetch_32             30 ns
     78  A000804C           A000B004  ( EXTENSION )                      Fetch_32             30 ns
     79  A000D00C           00000000  ( WRITE )                          BURST_WR_32         120 ns
     80  A0008050           8CA03000  LDA   A000D000, G4                 Fetch_32            180 ns
     81  A0008054           A000D000  ( EXTENSION )                      Fetch_32             30 ns
     82  A0008058           92A03000  ST    G4, A000B000                 Fetch_32             30 ns
     83  A000805C           A000B000  ( EXTENSION )                      Fetch_32             30 ns
     84  A000B004           A000C000  ( WRITE )                          BURST_WR_32         120 ns
     85  A0008060           8CA03000  LDA   A000E000, G4                 Fetch_32            180 ns
     86  A0008064           A000E000  ( EXTENSION )                      Fetch_32             30 ns
     87  A0008068           92A03000  ST    G4, A000B010                 Fetch_32             30 ns
     88  A000806C           A000B010  ( EXTENSION )                      Fetch_32             30 ns
     89  A000B000           A000D000  ( WRITE )                          BURST_WR_32         120 ns
     90  A0008070           8CA03000  LDA   A000A000, G4                 Fetch_32            180 ns
     91  A0008074           A000A000  ( EXTENSION )                      Fetch_32             30 ns
     92  A0008078           92A03000  ST    G4, A000B014                 Fetch_32             30 ns
     93  A000807C           A000B014  ( EXTENSION )                      Fetch_32             30 ns
     94  A000B010           A000E000  ( WRITE )                          BURST_WR_32         120 ns
     95  A0008080           5CB01E00  MOV   00, G6                       Fetch_32            180 ns
     96  A0008084           5CC01E1E  MOV   1E, G8                       Fetch_32             30 ns
```

Figure 2–1: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the i960RP address bus.

3 **Data Group.** Lists data from channels connected to the i960RP data bus.

4 **Mnemonics Column.** Lists the disassembled instructions and cycle types.

5 **Control Group.** Lists data from channels connected to i960RP microprocessor control signals (shown symbolically).

6 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

The Control Flow display format also shows the following cycles:

- Illegal instructions
- UNKNOWN cycle types, the disassembler does not recognize the Control group value

Instructions that unconditionally change the flow of control, and will always be displayed, are as follows:

CALL	CALLX	CALLS	
B	BX	BAL	BALX
RET	FMARK		

Instructions that conditionally generate a change in the flow of control, and will be displayed if they are determined to be taken, are as follows:

BBC	BBS	BNO	BG	BE
BGE	BL	BNE	BLE	BO
CMPOBG	CMPOBE	CMPOBGE	CMPOBL	CMPOBNE
CMPOBLE	CMPIBNO	CMPIBG	CMPIBE	CMPIBGE
CMPIBL	CMPIBNE	COMPIBLE	CMPIBO	
FAULTE	FAULTNE	FAULTL	FAULTLE	
FAULTG	FAULTGE	FAULTO	FAULTNO	
MARK				

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

The Subroutine display format also shows the following cycles:

- Illegal instructions
- UNKNOWN cycle types; the disassembler does not recognize the Control group value

Instructions that unconditionally affect the subroutine display are as follows:

CALL CALLX CALLS RET

There are no instructions that conditionally affect the subroutine display.

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the i960RP support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

There are no optional fields for this support package. Refer to the information on basic operations for descriptions of common fields.

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

- Specify the starting address of the exception vector table
- Specify the starting address of the fault vector table

The i960RP microprocessor support product has two additional fields: Interrupt Table Base, and Fault Table Base. These fields appear in the area indicated in the basic operations user manual.

NOTE. *Do not enter an address that resides in the internal RAM in these fields. Do not enter the same value in both fields. If you enter an address value that resides in the internal RAM, is outside the range, or is the same, the default value is used. With the default value, interrupts and faults will not be identified.*

Interrupt Table Base. You can specify the starting address of the interrupt table in hexadecimal. The address range is 00000400-FEFFFFFF and the default starting address is 0x00000500.

Fault Table Base. You can specify the starting address of the fault table in hexadecimal. The address range is 00000400-FEFFFFFF and the default starting address is 0x00000600.

NOTE. *The default values are arbitrary, but should be greater than 3FF.*

Marking Cycles

The disassembler will only allow marking of instruction fetch cycles. Instruction fetch cycle include read extensions and flush cycles. If the cursor is placed on any other cycle type, no cycle marks will be available.

Cycle marking is only allowed for word aligned address sequences. This is done to disable marking on second, third, and forth bytes in the case of an 8-bit region, and on the second byte in the case of a 16-bite region whose address will not be word aligned.

If you mark a word aligned sequence in a 8-bit region, the same mark is used for the successive three samples. If you mark a word aligned sequences in a 16-bit region, the same mark is used for the next successive sample. In case of any branch, including interrupts and faults, in which the target is unknown, flushing of the samples must be done using the marking option. This is because of the instruction buffering used by the i960RP.

Therefore, if the target of the branch is not double aligned, the word previous to the target will also be fetched but not executed. You must identify this condition and execute a flush. Refer to section 4.3.2 in the *i960RP Microprocessor User's Manual*, Intel, February 1996, for more information on marking word aligned sequences.

Using the marking cycles function, you can select a cycle and change it to one of the following cycle types:

- Opcode – Mark the sequence as an opcode fetch
- Extension – Mark the sequence as an extension cycle
- Flush – Mark the sequence as a flush cycle
- Undo mark – Remove all marks from the current sequence

Information on basic operations contains more details on marking cycles.

Displaying Exception Vectors

The disassembler can display exception vectors (interrupts and faults). The interrupt and fault tables must reside in external memory for the accesses to be visible on the bus and to the disassembler.

You can relocate the interrupt table by entering the starting address in the interrupt table base field. The interrupt table base field provides the disassembler with the base address; enter an eight-digit hexadecimal value corresponding to the base of the base address of the interrupt table.

You can relocate the fault table by entering the starting address in the fault table base field. The fault table base field provides the disassembler with the base address; enter an eight-digit hexadecimal value corresponding to the base address of the fault table.

You can make these selections in the disassembly property page (the disassembly format definition overlay).

Table 2–4 lists i960RP exception vectors.

Table 2–4: Exception vectors

Exception number	Location in IV* table (in hexadecimal)	Displayed exception name
8	024	(INT 8 VECTOR)
9	028	(INT 9 VECTOR)
10	02C	(INT 10 VECTOR)
...	...	...
243	3D0	(INT 243 VECTOR)
244-247	3D4-3E0	(RESERVED)
248	3E4	(NMI PROCEDURE)
249-251	3E8-3F0	(RESERVED)
252	3F4	(INT 252 VECTOR)
253	3F8	(INT 253 VECTOR)

Table 2–4: Exception vectors (cont.)

Exception number	Location in IV* table (in hexadecimal)	Displayed exception name
254	3FC	(INT 254 VECTOR)
255	400	(INT 255 VECTOR)

* IV means interrupt vector.

Table 2–5 lists i960RP fault vectors.

Table 2–5: Fault vectors

Fault number	Location in Fault table (in hexadecimal)	Displayed fault name
0	00	(OVERRIDE/P'LL FAULT)
1	08	(TRACE FAULT)
2	10	(OPERATION FAULT)
3	18	(ARITHMETIC FAULT)
4	20	(RESERVED)
5	28	(CONSTRAINT FAULT)
6	30	(RESERVED)
7	38	(PROTECTION FAULT)
8-9	40	(RESERVED)
Ah	50	(TYPE FAULT)
Bh-Fh	58	(RESERVED)

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your i960RP microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires i960RP signals
- List of other accessible microprocessor signals and extra probe channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a elastomer interconnect. The probe adapter connects to the connection pads on the SUT. Signals from the microprocessor-based system flow from the SUT through the elastomer to the probe adapter, then to the channel groups and through the probe signal leads to the module.

Configuration

The probe adapter does not require any configuration.

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–1, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements	
SUT clock		
Clock rate	Max. 33 MHz	
Minimum setup time required	5 ns	
Minimum hold time required	0 ns	
	Specification	
Measured typical SUT signal loading	**AC load**	**DC load**
SIGNAL	7 pF + 1 podlet	1 podlet
S_CLK	22 pF + 1 podlet	1 podlet

Table 3–2 shows the environmental specifications.

Table 3–2: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed i960RP microprocessor thermal considerations. Forced air cooling may be required across the CPU.**

Table 3–3 shows the certifications and compliances that apply to the probe adapter.

Table 3–3: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.

Figure 3–1 shows the dimensions of the probe adapter.

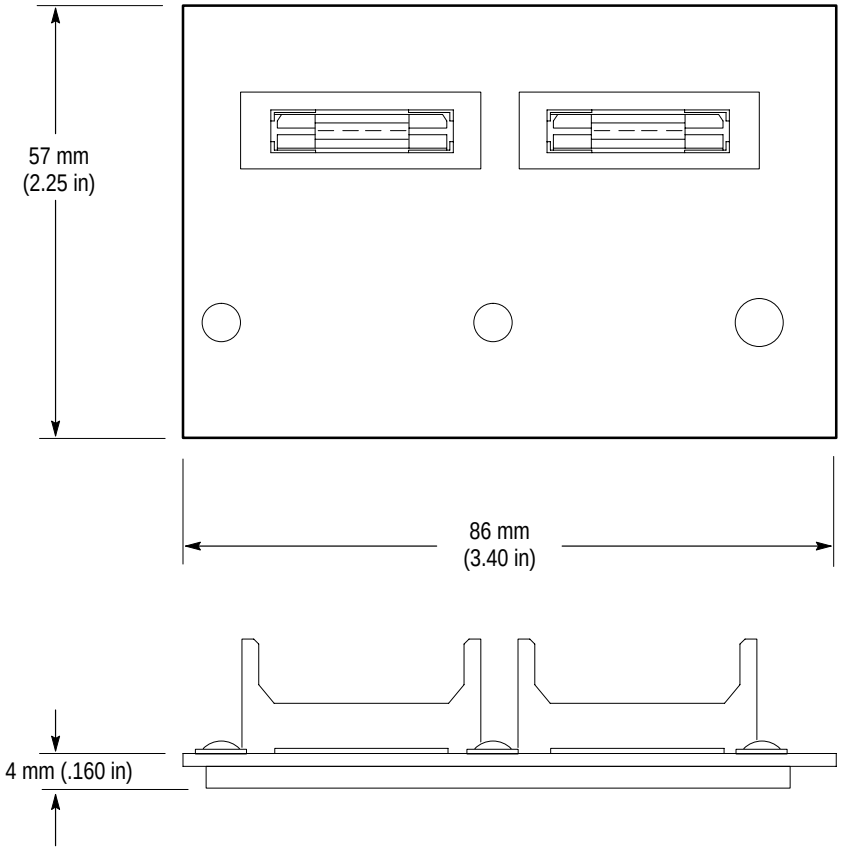


Figure 3–1: Dimensions of the probe adapter

Channel Assignments

Channel assignments shown in Table 3–4 through Table 3–10 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.
- An equals sign (=) following a signal name indicates that it is double probed.

Table 3–4 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–4: Address group channel assignments

Bit order	Section:channel	i960RP signal name
31	AD3:7	A31
30	AD3:6	A30
29	AD3:5	A29
28	AD3:4	A28
27	AD3:3	A27
26	AD3:2	A26
25	AD3:1	A25
24	AD3:0	A24
23	AD2:7	A23
22	AD2:6	A22
21	AD2:5	A21
20	AD2:4	A20
19	AD2:3	A19
18	AD2:2	A18
17	AD2:1	A17
16	AD2:0	A16
15	AD1:7	A15
14	AD1:6	A14
13	AD1:5	A13
12	AD1:4	A12
11	AD1:3	A11
10	AD1:2	A10
9	AD1:1	A9

Table 3–4: Address group channel assignments (cont.)

Bit order	Section:channel	i960RP signal name
8	AD1:0	A8
7	AD0:7	A7
6	AD0:6	A6
5	AD0:5	A5
4	AD0:4	A4
3	AD0:3	A3
2	AD0:2	A2
1	AD0:1	A1
0	AD0:0	A0

The Data bus is multiplexed. Channels D3:7-0, D2:7-0, D1:7-0, and D0:7-0 do not need to be physically connected. The data channels are not extra channels and you can not connect podlets to these channels as they are already assigned to data channels and will get their inputs from the address channels. By default, the Data channel group is displayed in hexadecimal.

Table 3–5 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–5: Control group channel assignments

Bit order	Section:channel	i960RP signal name
8	C2:7	LOCK~
7	C2:3	HOLDA
6	C3:0	WIDTH1
5	C2:4	WIDTH0
4	C2:5	BLAST~
3	C3:4	W/R~
2	C2:6	D/C~
1	C2:2	RDYRCV~
0	C2:1	LRDYRCV~

Table 3–6 shows the probe section and channel assignments for the ByteEnbl group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3–6: ByteEnbl group channel assignments

Bit order	Section:channel	i960RP signal name
3	C3:6	BE3~
2	C3:2	BE2~
1	C3:5	BE1~
0	C3:1	BE0~

Table 3–7 shows the probe section and channel assignments for the Aux group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–7: Aux group channel assignments

Bit order	Section:channel	i960RP signal name
2	C3:7	S_CLK
1	C3:3	L_RST~
0	C2:0	ADS~

Table 3–8 shows the probe section and channel assignments for the Intr group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–8: Intr group channel assignments

Bit order	Section:channel	i960RP signal name
8	C0:5	NMI~ *
7	C1:7	XINT7~ *
6	C1:3	XINT6~ *
5	C0:7	XINT5~ *
4	C0:3	XINT4~ *
3	C1:6	XINT3~ *
2	C1:2	XINT2~ *
1	C0:6	XINT1~ *
0	C0:2	XINT0~ *

*** Signal not required for disassembly.**

Table 3–9 shows the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–9: Misc group channel assignments

Bit order	Section:channel	i960RP signal name
6	C1:5	P_RST~ *
5	C1:0	DT/R~ *
4	C1:1	FAIL~ *
3	C0:1	HOLD *
2	C1:4	DEN~ *
1	C0:4	WAIT~ *
0	C0:0	ALE *

***** **Signal not required for disassembly.**

Table 3–10 shows the probe section and channel assignments for the clock probes (not part of any group) and the i960RP signal to which each channel connects.

Table 3–10: Clock channel assignments

Section:channel	i960RP signal name
CK:1	BLAST~ =
CK:0	S_CLK =

= **Indicates that the signal is double probed.**

How Data is Acquired

This part of this chapter explains how the module acquires i960RP signals using the TMS 165 software and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra probe channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the i960RP support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the i960RP bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module Clocking State Machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

The CSM has two states: Address_Ta and Data_Td. These two states handle all of the states of the microprocessor, which are address (Ta), wait/data (Tw/Td), recovery (Tr), and hold (Th).

The sampling is done at the rising edge of the CLKIN signal. The CSM enters the Data_Td state from the Address_Ta state only if ADS~ is asserted. To do this the CSM also requires the HOLDA signal to be deasserted if DMA is excluded, or asserted if DMA is included. The address and control signals, Addr[31:0], W/R~, ADS~, S_CLK, L_RST~, LOCK~, HOLDA, WIDTH[1:0], NMI~, XINT[7:0]~, HOLD, and FAIL~ are sampled before entering the data state.

When the CSM is in the Data_Td state, the data and control lines, Data[31:0], DEN~, BE[3:0]~, D/C~, BLAST~, RDYRCV~, LRDYRCV~, DT/R~, and WAIT~ are sampled and master strobed if either RDYRCV~ or LRDYRCV~ are asserted with BLAST~ deasserted.

If it is the last data transfer of the burst and non-burst accesses, BLAST~ is asserted which takes the CSM to the address state. If BLAST~ is not asserted the CSM keeps waiting in the data state only, which indicates the burst access. In all of these cases HOLDA is deasserted. If the RDYRCV~ is not asserted in this state then the CSM keeps waiting in the data state without strobing any of the address, data, or control lines. This means the processor is in a wait state (Tw). When DMA is included and HOLDA is asserted in this state, it is a DMA access, and the CSM goes back to the Address_Ta state. Data and control lines are sampled and master is strobed. If BLAST~ and ADS~ are all deasserted in this state, the CSM just comes back to the Address_Ta state.

The processor always has a Tr state following the Tw/Td state. This allows the system components adequate time to remove their outputs from the bus before the processor drives the next address on the address/data lines. The CSM goes to the Address_Ta state after the last transfer of the bus access. The processor remains in the same state until the bus is recovered, during which time the control signals BLAST~ and other signals will be inactive.

When the recovery state is complete, and if their are no new accesses required, the bus enters the Ta state. The CSM keeps waiting in the Address_Ta state without strobing.

Figure 3–2 shows the sample points and the master sample point.

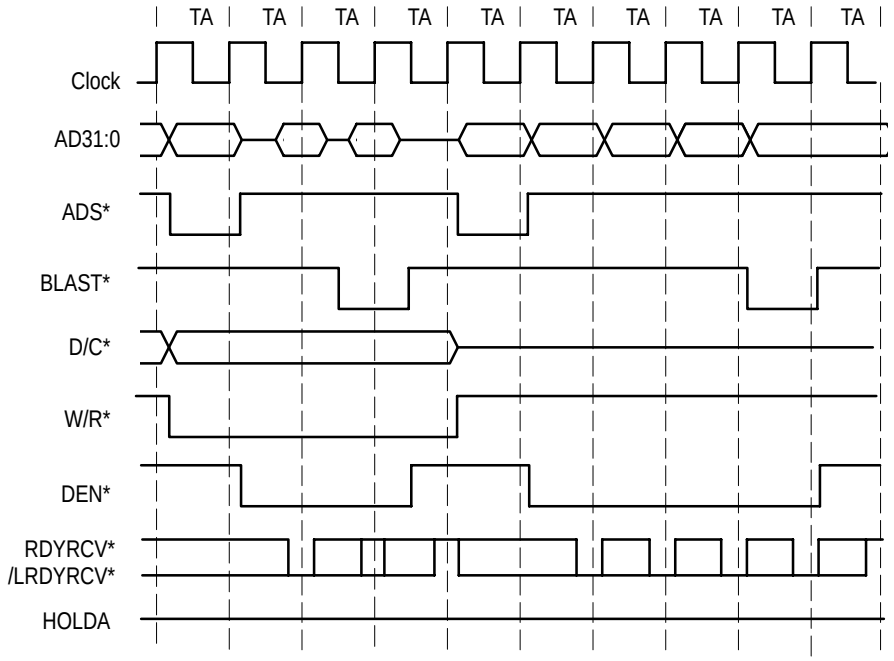


Figure 3–2: i960RP bus timing diagram

Clocking Options

The clocking algorithm for the i960RP support has two variations: Alternate Bus Master Cycles Excluded and Alternate Bus Master Cycles Included.

Alternate Bus Master Cycles Excluded. Whenever the HLDA signal is high, no bus cycles are logged in. Only bus cycles initiated by the i960RP microprocessor (HLDA low) will be logged in. Backoff cycles (caused by the BOFF# signal) are stored.

Alternate Bus Master Cycles Included. All bus cycles, including Alternate Bus Master cycles and Backoff cycles, are logged in.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so that you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–4. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals Not On the Probe Adapter

Table 3–11 shows the i960RP signals that are not brought out on the probe adapter. If you need access to any of these signals, you must use an alternate method of connection.

Table 3–11: Signals not on the i960RP probe adapter

i960RP signal name	i960RP pin number
STEST	AE3
TCK	B24
TDI	D26
TDO	D25
TMS	C24
TRST~	C25
P_AD31:0	AD9
P_C/BE3:0~	AE11 AE15 AF18 AF21
P_DEVSEL~	AF16
P_FRAME~	AF15
P_GNT~	AF8
P_IDSEL	AD12
P_INT[A:D]~	AF7 AD7 AE6 AF6
P_IRDY	AE15
P_LOCK~	AD17
P_PAR	AD18
P_PERR~	AF17
P_REQ~	AE8
P_SERR~	AE17
P_STOP~	AE16
P_TRDY~	AD16

Table 3–11: Signals not on the i960RP probe adapter (cont.)

i960RP signal name	i960RP pin number						
S_AD31:0	J26 L24 P25 Y25 AC25	J24 M24 P26 Y26 AC26	K25 M25 P24 Y24 AC24	K26 M26 R25 AA25 AD25	K24 N25 W25 AA26 AE24	L25 N26 W26 AB25	L26 N24 W24 AB24
S_C/BE3:0~	M25	R26	V24	AA24			
S_DEVSEL~	T24						
S_FRAME~	R24						
S_GNT0~/S_REQ~	H26						
S_GNT5:1~	D24	E26	F26	G25	G24		
S_IDSEL	M26						
S_IRDY~	T25						
S_LOCK~	U26						
S_PAR	V26						
S_PERR~	U24						
S_REQ0~/S_GNT~	H24						
S_RST~	J25						
S_SERR~	V25						
S_STOP~	U25						
S_TRDY~	T26						
S_REQ4:1~	E24	F24	G26	H25			
S_REQ5~/S_ARB_EN	E25						
CAS7:0~	H2 F2	H1 F1	H3	G2	G1	G3	
CE1:0~	L1	L3					
DALE1	M2	M1					
DP3:0	D2	D1	D3	C2			
DWE1:0~	K2	K1					
LEAF1:0~	M3	L2					
MA11:0	B3 B6	C3 C6	B4 B7	C4 A7	B5 C7	A5	C5
MWE3:0~	K3	J2	J1	J3			
RAS3:0~	F3	E2	E1	E3			
DACK~	AD3						
DREQ~	AD2						
PICCLK	U3						
PICD1:0	T2	T1					
SCL	U1						

Table 3–11: Signals not on the i960RP probe adapter (cont.)

i960RP signal name	i960RP pin number
SDA	U2
P_CLK	AD8
ICEADS~	AC1
ICEBRK~	AA1
ICEBUS7:0	AA3 Y2 Y1 Y3 W2 W1 W3 V2
ICECLK	AB2
ICELOCK~	AB3
ICEMSG~	AA2
ICESEL~	AC2
ICEVLD~	AB1
MSGFRM~	AC3

Extra Channels

Table 3–12 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Channels not defined in a channel group by the TMS 165 software are logged in with the Master sample point.

Table 3–12: Extra module sections and channels

Module	Section: channels
102-channels	Qual:1 Qual:0
136-channels	E3:7-0 E2:7-0 E1:7-0 E0:7-0 Qual:3-0
96-channels	None

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This chapter contains information on the probe adapter circuit description.

Probe Adapter Circuit Description

The TMS 165 i960RP support uses a passive probe adapter. The probe adapter does not contain any active circuitry.

There are no user serviceable or replaceable parts on the TMS 165 i960RP probe adapter board.

Replaceable Parts

Replaceable Parts

This section contains a list of the replaceable parts for the TMS 165 i960RP microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved parts as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Parts List

The tabular information in the Replaceable Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

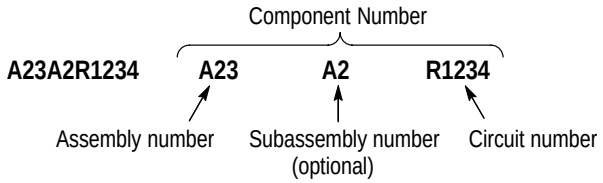
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
0KB01	STAUFFER SUPPLY CO	810 SE SHERMAN	PORTLAND, OR 97214–4657
73743	FISCHER SPECIAL MFG CO	111 INDUSTRIAL RD PO BOX 76500	COLD SPRINGS, KY 41076
93907	CAMCAR DIV OF TEXTRON INC	ATTN: ALICIA SANFORD 516 18TH AVE	ROCKFORD, IL 611045181
TK2548	XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON, OR 97005
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0608–00			1	ADAPTER, PROBE: i960RP, 160–PIN AMPLIFEX, PROBE ADAPTER, TMS165 OPT 01	80009	010–0608–00
–1	211–0578–00			3	SCREW, MACHINE: 6–32 X 0.438, PNH, STL CD PL, POZ	93907	ORDER BY DESCRIPTION
–2	210–3057–00			6	WASHER, FLAT: 0.17 ID X 0.375 OD X 0.03 THK, NYLON	0KB01	LWNY–012NA–M
–3	671–3467–00			1	CIRCUIT BD ASSY: i960RP, 160–PIN AMPLIFEX, 389–2306–00 WIRED, TMS165 OPT 01	80009	671–3467–00
–4	131–6233–00			1	CONN, ELASTOMER: COMPRESSION/SMD, P2P CONNECTOR, STR, 160 POS, 0.05 X 0.15CTR, 0.098 H X 3.0 L, 4 ROW,	00779	95–1444–70–1
–5	210–0408–00			3	NUT, PLAIN, HEX: 6–32 X 0.312, BRS CD PL	73743	3040–402
					STANDARD ACCESSORIES		
	070–9681–00			1	MANUAL,TECH: INSTRUCTION, i960RP, DISSASEMBLER, TMS 165	80009	070–9681–00
	070–9803–00			1	MANUAL, TECH: TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH: BASIC OPERATIONS OF MICROPROCESSOR SUPPORT ON DAS/TLA, LOGIC ANALYZER, DP, SHRINK WRAP	TK2548	070980200

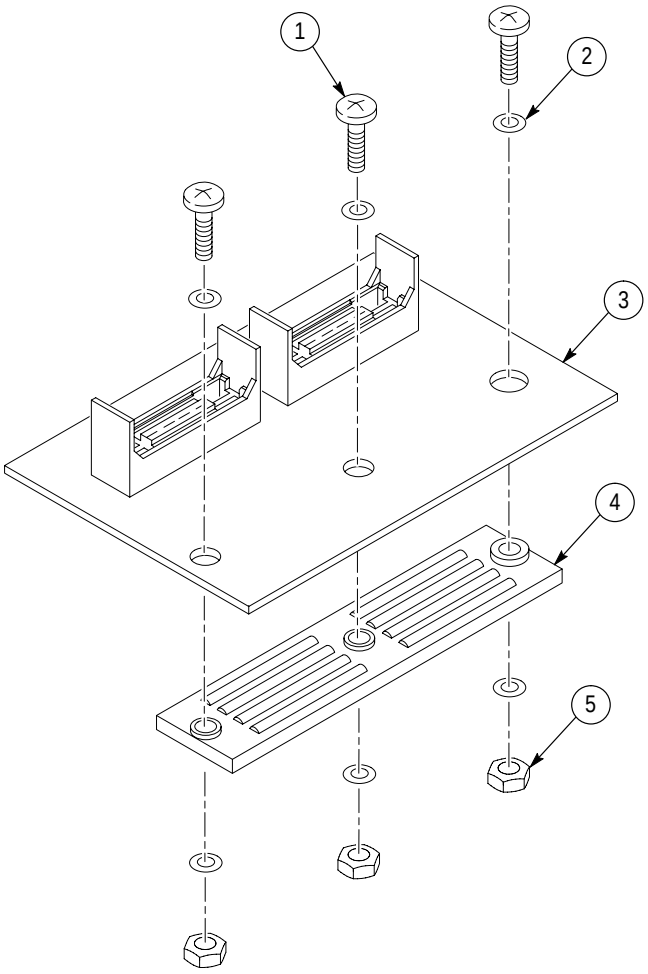


Figure 1: i960RP probe adapter exploded view

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