Instruction Manual

Tektronix

TMS 164
i960 Hx Microprocessor Support

070-9818-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

SOFTWARE WARRANTY

Tektronix warrants that the media on which this software product is furnished and the encoding of the programs on the media will be free from defects in materials and workmanship for a period of three (3) months from the date of shipment. If a medium or encoding proves defective during the warranty period, Tektronix will provide a replacement in exchange for the defective medium. Except as to the media on which this software product is furnished, this software product is provided “as is” without warranty of any kind, either express or implied. Tektronix does not warrant that the functions contained in this software product will meet Customer’s requirements or that the operation of the programs will be uninterrupted or error-free.

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In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 164 i960 Hx microprocessor support and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor supports on the logic analyzer for which the TMS 164 i960 Hx support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor supports, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor supports is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names must be replaced with i960 Hx. This is the name of the microprocessor in field selections and file names you must use to operate the i960 Hx support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 102/136-channel or a 96-channel module.
- i960 Hx refers to all supported variations of the i960 Hx microprocessor unless otherwise noted.
- A pound sign (#) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics:

- The TMS 164 i960 Hx microprocessor support product
- Logic analyzer system software compatibility
- Your i960 Hx system requirements
- i960 Hx support product restrictions
- How to configure the probe adapter
- How to connect to the system under test (SUT)
- How to apply power to and remove power from the probe adapter

Product Description

The TMS 164 microprocessor support product disassembles data from systems that are based on the Intel, Inc. i960 Hx microprocessor. The TMS 164 runs on a compatible Tektronix logic analyzer equipped with a a 102/136-channel module or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to the meet the minimum channel requirements for the TMS 164 microprocessor support.

Table 1–1 shows which microprocessors, packages, and speeds the TMS 164 supports.

Table 1–1: Product support

Microprocessor	Package	Maximum speed
i960 HA	PGA	40 MHz
i960 HD	PGA	33 MHz
i960 HT	PGA	25 MHz

A complete list of accessories and options is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this product efficiently, you need to have the items listed in the basic operations user manual as well as the *i960 Hx Microprocessor User's Manual*, Intel, August, 1995.

The basic operations user manual also contains a general description of support products.

Logic Analyzer System Software Compatibility

The label on the application floppy disk states which version of logic analyzer system software the application is compatible with.

Logic Analyzer Configuration

To use the i960 Hx support product, the logic analyzer must be equipped with either a 102/136-channel module or a 96-channel module at a minimum. The module must be equipped with enough probes to acquire clock and channel data from signals in your i960HX-based system.

The basic operations user manual contains information on how to configure the logic analyzer under *Configuring the Logic Analyzer* in the *Getting Started* chapter.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor support products in the *Getting Started* chapter in the basic operations user manual as they pertain to your SUT:

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other i960 Hx support product requirements and restrictions.

System Clock Rate. The microprocessor support product supports the i960 Hx microprocessor at speeds of up to 40 MHz[1].

1 **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

SUT Power. Whenever the SUT is powered off, be sure to remove power from the probe adapter. Refer to *Applying and Removing Power* at the end of this chapter for information on how to remove power from the probe adapter.

Disabling the Data, Instruction, and Vector Caches. You must disable the internal Data, Instruction, and Vector caches. Disabling the caches make most instructions visible on the bus so the logic analyzer can acquire and disassemble them.

Configuring the Probe Adapter

The i960 Hx microprocessor uses the high-order four address lines to define 16 memory regions. The characteristics of each region is set up by software at power-up. You must set the DIP switches on the probe adapter to match the software settings of each memory region.

All the switches are open when the probe adapter is shipped; READY# and BTERM# are always monitored in all the memory regions until you change the settings. Figure 1–1 shows the location of the DIP switches on the probe adapter.

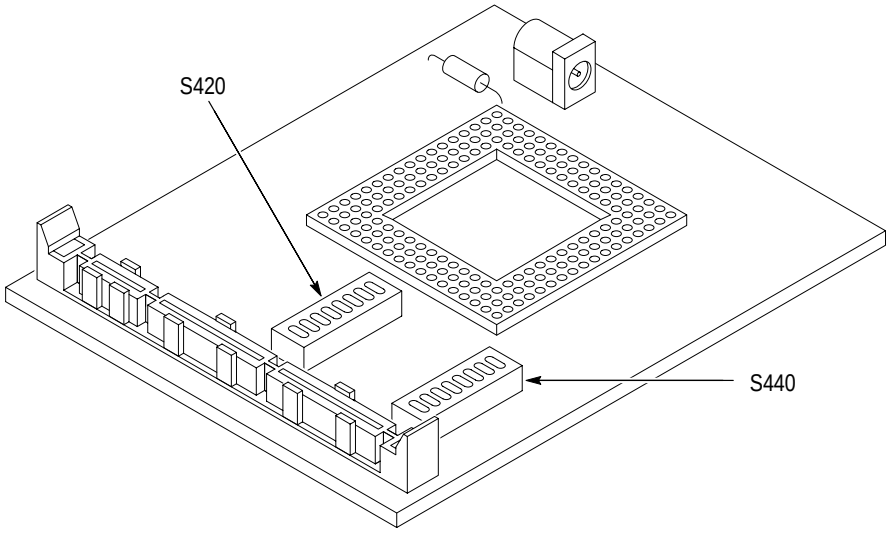


Figure 1–1: Location of the DIP switches on the probe adapter

To configure the probe adapter, follow these steps:

1. Determine how the i960 Hx system is configured in each of its regions. Compare bits 29, 28, and 24 in PMCON register to the bit values in Table 1–2 to determine how to set the DIP switch on the probe adapter.

Table 1–2: PMCON register entry and DIP switch settings

READY# and BTERM# Enable	Burst Enable	Pipeline Enable	DIP switch setting	Definition
0	0	0	Closed	Normal cycles; READY# and BTERM# disabled
0	0	1	Closed	Pipelined Read cycles enabled; normal write cycles. READY# and BTERM# disabled.
0	1	0	Closed	READY# and BTERM# disabled; burst cycles enabled.
0	1	1	Closed	READY# and BTERM# inputs disabled; pipelined burst read enabled, burst write cycles enabled.
1	0	0	Open	READY# and BTERM# inputs are enabled; burst and read pipelining mode disabled.
1	0	1	Open	READY# and BTERM# inputs ignored for pipelined read, valid for write; burst mode disabled.
1	1	0	Open	READY# and BTERM# inputs enabled; burst cycle enabled and pipeline mode disabled.
1	1	1	Open	READY# and BTERM# inputs ignored for pipelined burst read, but valid for burst write.

2. Use Table 1–3 to determine which DIP switch to set for each memory region.

Table 1–3: Address region and DIP switch assignments

Address region (A31-A28)	Switch	Address region (A31-A28)	Switch
0 (0000)	S420-S0	8 (1000)	S440-S8
1 (0001)	S420-S1	9 (1001)	S440-S9
2 (0010)	S420-S2	A (1010)	S440-S10
3 (0011)	S420-S3	B (1011)	S440-S11
4 (0100)	S420-S4	C (1100)	S440-S12
5 (0101)	S420-S5	D (1101)	S440-S13
6 (0110)	S420-S6	E (1110)	S440-S14
7 (0111)	S420-S7	F (1111)	S440-S15

Connecting to a System Under Test

Before you connect to the SUT, you must connect the standard probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The clock and channel probes shown in the connection figures are for the 92A96 module. If you are using a different module, your probes will look different than those shown.

The *Requirements and Restrictions* description in the basic operations user manual shows the vertical dimensions of an acquisition probe connected to square pins on a circuit board.

If a probe adapter has one or two high-density cables (probe adapter does not have pins to which the clock and channel probes connect), it requires an LAHDP2 probe to make connections between the logic analyzer and a SUT.

To connect the logic analyzer to a SUT using a PGA probe adapter and an LAHDP2 probe, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the low-profile probe adapter, the acquisition probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and low-profile probe adapter.

2. To discharge your stored static electricity, touch the ground jack located on the back of the logic analyzer. Then, touch the black foam on the underside of the probe adapter to discharge stored static electricity from the probe adapter.

3. Remove the microprocessor from the SUT.

4. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter may permanently damage the microprocessor once power is applied.*

5. Place the microprocessor into the probe adapter as shown in Figure 1–2.

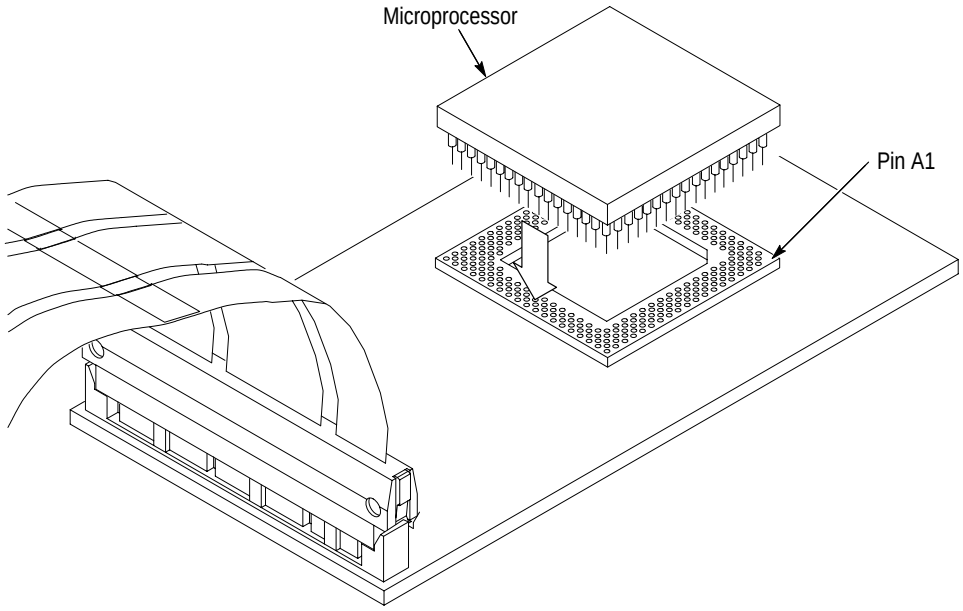


Figure 1–2: Placing a microprocessor into a PGA probe adapter

6. Remove the black foam from the underside of the probe adapter.

7. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the SUT.

8. Place the probe adapter onto the SUT as shown in Figure 1–3.

NOTE. *You may need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind this may increase loading, which can reduce the electrical performance of the probe adapter.*

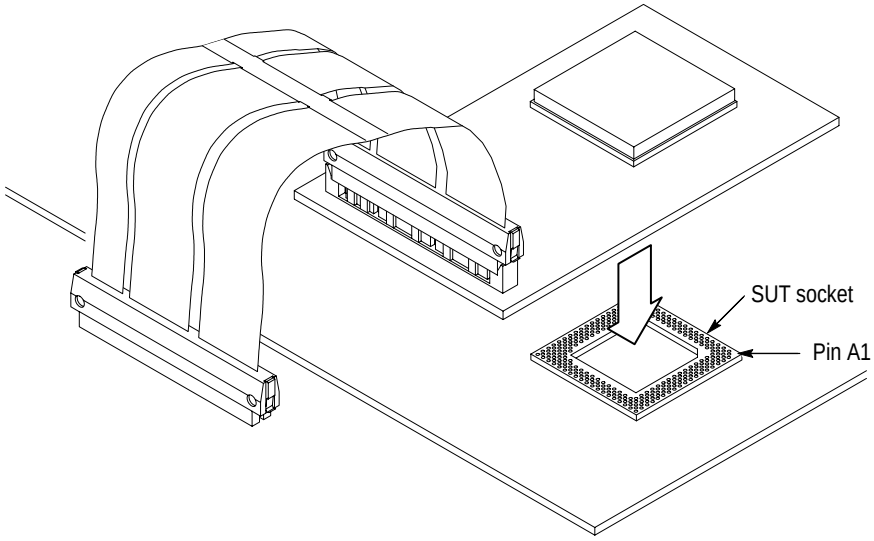


Figure 1–3: Placing a PGA probe adapter onto the SUT

9. Connect the clock and channel probes to the LAHDP2 probe as shown in the basic operations user manual.

10. Align pin 1 on the LO cable connector, the end on the narrowest cable strip of the cable, with pin 1 on the LO connector on the LAHDP2 probe. Connect the cable to the connector as shown in Figure 1–4.

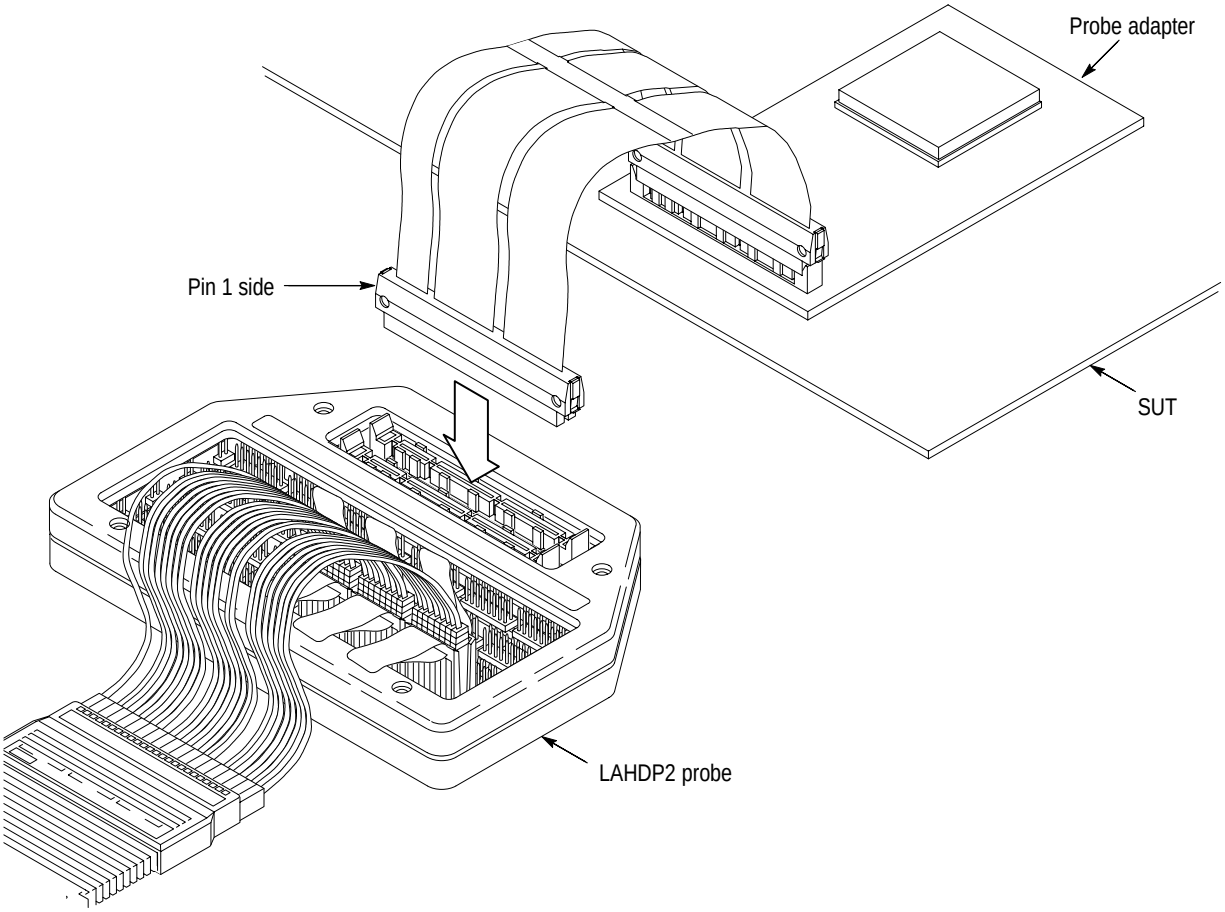


Figure 1–4: Connecting the LO cable to an LAHDP2 probe

Applying and Removing Power

A power supply for the TMS 164 i960 Hx probe adapter is included with the product. The power supply provides +5 V power to the probe adapter. When the power supply is on, the LED indicator is lit. The center connector of the power jack connects to Vcc.

***NOTE**. Whenever the SUT is powered off, be sure to remove power from the probe adapter.*

To apply power to the i960 Hx probe adapter and SUT, follow these steps:

CAUTION. *Failure to use the +5 V power supply provided by Tektronix may permanently damage the probe adapter and i960 Hx microprocessor. Do not mistake another power supply that looks similar for the +5 V power supply.*

1. Connect the +5 V power supply to the jack on the probe adapter. Figure 1–5 shows the location of the jack on the adapter board.

CAUTION. *Failure to apply power to the probe adapter before applying power to your SUT may permanently damage the i960 Hx microprocessor and SUT.*

2. Plug the power supply for the probe adapter into an electrical outlet. The power LED should light up.
3. Power on the SUT.

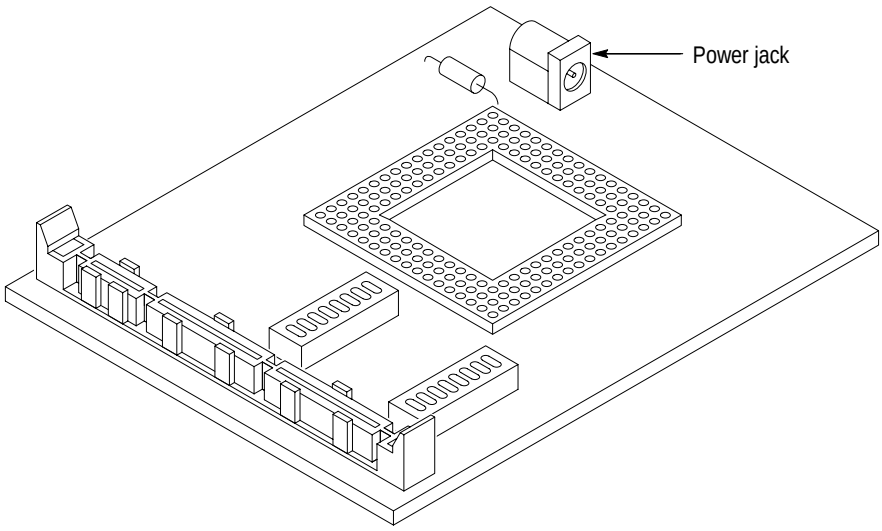


Figure 1–5: Location of the power jack

To remove power from the SUT and i960 Hx probe adapter, follow these steps:

CAUTION. *Failure to power down your SUT before removing the power from the probe adapter may permanently damage the i960 Hx microprocessor and SUT.*

1. Power down the SUT.
2. Unplug the power supply for the probe adapter from the electrical outlet.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 164 i960 Hx support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the i960 Hx support are Address, Data, Control, ByteEnable, Aux, and Misc. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–5.

Clocking Options

The TMS 164 support offers a microprocessor-specific clocking mode for the i960 Hx microprocessor. This clocking mode is the default selecton whenever you load the i960 Hx support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

The clocking for the TMS 164 support is DMA cycles.

DMA Cycles This option field in the Clock menu lets you choose whether to Include or Exclude DMA cycles.

A description of how cycles are sampled by the acquisition module using the application and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. The basic operations user manual contains information on how to use these other clock selections iwth any microprocessor support package in the *Reference* chapter under *General Purpose Analysis*.

Symbols

The TMS 164 application supplies one pattern symbol table file. The i960 Hx_Ctrl file replaces specific Control channel group values with symbolic values when SYM or PATTERN is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file i960 Hx_Ctrl, the Control channel group symbol table.

Table 2–1: Control Group symbol table definitions

Symbol	Control Group value LOCK# HOLD BLAST# W/R#	D/C# BOFF#	CT3 CT2 CT1 CT0	Meaning
FETCH	1 0 X 0	0 1	X X X X	An opcode fetch
READ	1 0 0 0	1 1	X X X X	A read from memory
WRITE	1 0 0 1	1 1	X X X X	A write to memory
L_READ	0 0 X 0	1 1	X X X X	The read portion of an atomic memory access
L_WRITE	0 0 X 1	1 1	X X X X	The write portion of an atomic memory access
DMA_READ	X 1 X 0	X 1	X X X X	A DMA read from memory
DMA_WRITE	X 1 X 1	X 1	X X X X	A DMA write to memory
BURST_RD	1 0 1 0	1 1	X X X X	A burst read from memory
BURST_WR	1 0 1 1	1 1	X X X X	A burst write to memory
BACK_OFF	X X X X	X 0	X X X X	The BOFF# signal is asserted
UNKNOWN	X X X X	X X	X X X X	Invalid group value

Information on basic operations describes how to use symbolic values for triggering and displaying other channel groups symbolically, such as the Address channel group.

Symbols Used for Symbolic Addressing

The i960 Hx architecture defines a set of system tables that are read by the microprocessor during initialization and software execution. The i960 Hx microprocessor support supplies data structure symbol tables to provide symbolic address representation for these i960 Hx system data structures.

If you are using only a single data structure symbol table during disassembly, you can directly specify that symbol table in either the Channel menu, or the State or Disassembly Format Definition overlays. You must first use the Symbol Editor to set the base address of the symbol table to the base address of the corresponding system data structure in your system. The Initialization Boot Record symbol table is always located at the same address so you do not have to set the base.

Only one symbol table can be used with each channel group. This means that if you want to use more than one of these data structure symbol tables, you must merge them together to make one symbol table.

Merging Symbol Tables. You do not have to recreate a new table each time you move the tables in your system as long as the relative difference in address locations doesn't change. If you move the tables in your system without changing the relative difference in address locations, you only need to redefine the base address for the symbol table.

Table 2–2 shows the name and address range for the symbols in the file 960HX_IBR, the Initialization Boot Record symbol table. This symbol table can only be merged with other symbol tables that have already had the base address added into their values.

Table 2–2: Initialization Boot record (IBR) symbol table

Symbol name	Lower address boundary	Upper address boundary
IBR_BCON0	FEFFFF30	FEFFFF33
IBR_BCON1	FEFFFF34	FEFFFF37
IBR_BCON2	FEFFFF38	FEFFFF3B
IBR_BCON3	FEFFFF3C	FEFFFF3F
IBR_FSTIP	FEFFFF40	FEFFFF43
IBR_PRCB	FEFFFF44	FEFFFF47
IBR_CHK_W	FEFFFF48	FEFFFF5F

Table 2–3 shows the name and address range for the symbols in the file 960HX_PRCB, the Process Control Block symbol table.

Table 2–3: Process Control Block (PRCB) symbol table

Symbol name	Lower address boundary	Upper address Boundary
PRCB_FTB	0	3
PRCB_CTB	4	7
PRCB_ACR	8	B
PRCB_FCW	C	F
PRCB_ITB	10	13
PRCB_SPB	14	17
PRCB_ISP	1C	1F
PRCB_ICC	20	23
PRCB_RCC	24	27

Table 2–4 shows the name and address range for the symbols in the file 960HX_CTBL, the Control Table symbol table.

Table 2–4: Control Table symbol table*

Symbol name	Lower address boundary	Upper address boundary
IMAP0	10	13
IMAP1	14	17
IMAP2	18	1B
ICON	1C	1F
PMCON0	20	23
PMCON1	24	27
PMCON2	28	2B
PMCON3	2C	2F
PMCON4	30	33
PMCON5	34	37

Table 2–4: Control Table symbol table* (cont.)

Symbol name	Lower address boundary	Upper address boundary
PMCON6	38	3B
PMCON7	3C	3F
PMCON8	40	43
PMCON9	44	47
PMCON10	48	4B
PMCON11	4C	4F
PMCON12	50	53
PMCON13	54	57
PMCON14	58	5B
PMCON15	5C	5F
BPCON	64	67
TC	68	6B
BCON	6C	6F

* **Do not confuse this table with the Control Group symbol table.**

Table 2–5 shows the name and address range for the symbols in the file 960HX_IBR, the Interrupt Table symbol table.

Table 2–5: Interrupt Table symbol table

Symbol name	Lower address boundary	Upper address boundary
PEND_PRI	0	3
PEND_INT	4	23
INT_VECT	24	403

Table 2–6 shows the name and address range for the symbols in the file 960HX_FAULT, the Fault Table symbol table.

Table 2–6: Fault Table symbol table

Symbol name	Lower address boundary	Upper address boundary
PAR_FAULT	0	7
TR_FAULT	8	F
OP_FAULT	10	17
AR_FAULT	18	1F
CON_FAULT	28	2F
PRO_FAULT	38	3F
MAC_FAULT	40	47
TYP_FAULT	50	5F
OVR_FAULT	80	8F

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- Changing the way data is displayed
- Changing disassembled cycles with the mark cycles function

Acquiring Data

Once you load the i960 Hx support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE*. Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–12.*

The default display format shows the Address, Data, Control, and Byte Enable channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–7 shows these special characters and strings, and gives a definition of what they represent.

Table 2–7: Meaning of special characters in the display

Character or string displayed	Meaning
********	Indicates there is insufficient data available for complete disassembly of the instruction. The number of asterisks displayed indicates the width of the data that is unavailable. Two asterisks represent one byte.
**	Indicates there is insufficient data available for complete disassembly of the instruction. "**" indicates one register number that is unavailable.
>> or m	The instruction was manually marked by the user

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–8 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–8: Cycle type definitions

Cycle type	Definition
(READ)	A basic read cycle
(WRITE)	A basic write cycle
(BURST_READ)	A burst mode read cycle
(BURST_WRITE)	A burst mode write cycle
(LOCKED_READ)	The read portion of atomic read/write cycle
(LOCKED_WRITE)	The write portion of atomic read/write cycle
(DMA_READ)	A DMA read from memory.
(DMA_WRITE)	A DMA write to memory.
(STEST FAIL)	Processor has failed in self test.
(RESET LOCATION)	Processor has RESET and started fetching at address FEFF FF30.

Table 2–8: Cycle type definitions (cont.)

Cycle type	Definition
(FLUSH)†	An instruction fetch that the processor did not use
(EXTENSION)†	The second word of the two-word instruction
(PREFETCH BYTE)†	The 2nd, 3rd and 4th byte of an instruction in an 8-bit memory region
(PREFETCH HALF-WORD)†	The 2nd 16-bit word of an instruction in a 16-bit memory region
* ILLEGAL INSTRUCTION *	Not a valid instruction
UNKNOWN	Not a valid cycle type

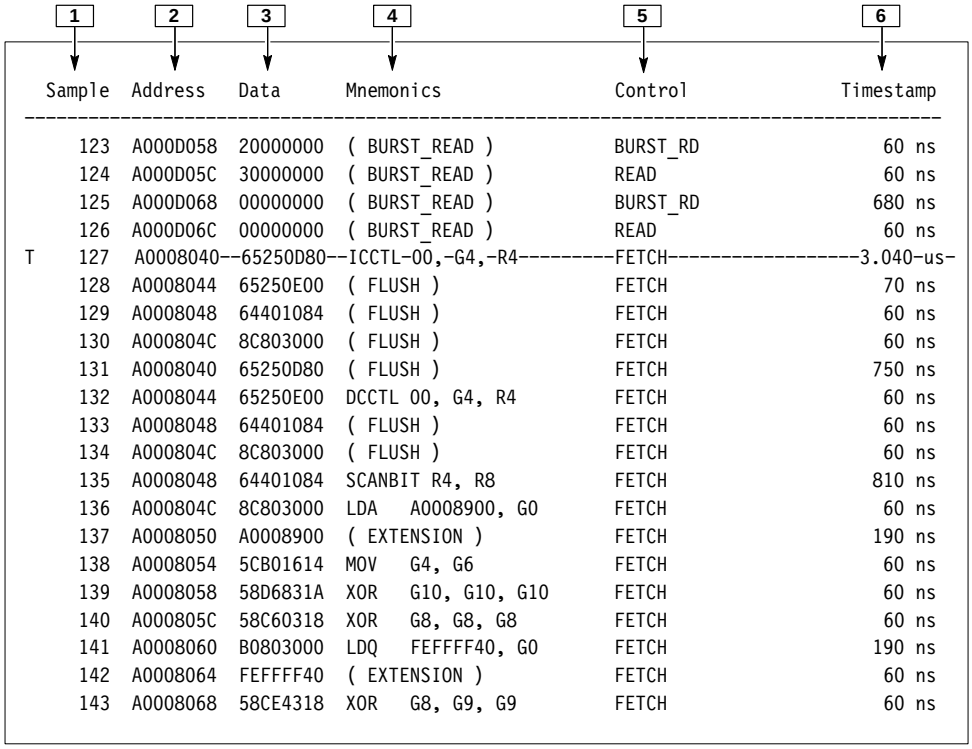
† **Calculated cycle type.**

Interrupts and fault tables will be displayed in parentheses in the disassembly as shown below in Table 2–9.

Table 2–9: Interrupt or Exception label definitions

Interrupt or Exception type	Definition
(INTR n VECTOR READ)	The vector entry read from the interrupt table; n indicates the number of the interrupt.
(INTR PROC ENTRY)	Entry to the interrupt handling procedure.
(FAULT TABLE READ)	READ from the fault table occurs to get the procedure address in case of local call, or proc entry in case of system call.
(OPERATION FAULT PROC: LOCAL) (ARITHMETIC FAULT PROC: LOCAL)	Entry to the fault handling procedure in Local call.
(OPERATION FAULT PROC: SYSTEM) (ARITHMETIC FAULT PROC: SYSTEM)	Entry to the fault handling procedure in System call.

Figure 2–1 shows an example of the Hardware display.




```
  Sample  Address   Data      Mnemonics                Control              Timestamp
-------------------------------------------------------------------------------------
     123  A000D058  20000000  ( BURST_READ )           BURST_RD               60 ns
     124  A000D05C  30000000  ( BURST_READ )           READ                   60 ns
     125  A000D068  00000000  ( BURST_READ )           BURST_RD              680 ns
     126  A000D06C  00000000  ( BURST_READ )           READ                   60 ns
T    127  A0008040--65250D80--ICCTL-00,-G4,-R4---------FETCH-----------------3.040-us-
     128  A0008044  65250E00  ( FLUSH )                FETCH                  70 ns
     129  A0008048  64401084  ( FLUSH )                FETCH                  60 ns
     130  A000804C  8C803000  ( FLUSH )                FETCH                  60 ns
     131  A0008040  65250D80  ( FLUSH )                FETCH                 750 ns
     132  A0008044  65250E00  DCCTL 00, G4, R4         FETCH                  60 ns
     133  A0008048  64401084  ( FLUSH )                FETCH                  60 ns
     134  A000804C  8C803000  ( FLUSH )                FETCH                  60 ns
     135  A0008048  64401084  SCANBIT R4, R8           FETCH                 810 ns
     136  A000804C  8C803000  LDA   A0008900, G0       FETCH                  60 ns
     137  A0008050  A0008900  ( EXTENSION )            FETCH                 190 ns
     138  A0008054  5CB01614  MOV   G4, G6             FETCH                  60 ns
     139  A0008058  58D6831A  XOR   G10, G10, G10      FETCH                  60 ns
     140  A000805C  58C60318  XOR   G8, G8, G8         FETCH                  60 ns
     141  A0008060  B0803000  LDQ   FEFFFF40, G0       FETCH                 190 ns
     142  A0008064  FEFFFF40  ( EXTENSION )            FETCH                  60 ns
     143  A0008068  58CE4318  XOR   G8, G9, G9         FETCH                  60 ns
```

Figure 2–1: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the i960 Hx address bus.

3 **Data Group.** Lists data from channels connected to the i960 Hx data bus.

4 **Mnemonics Column.** Lists the disassembled instructions and cycle types.

5 **Control Group.** Lists data from channels connected to i960 Hx microprocessor control signals (shown symbolically).

6 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

The Software display format also shows the following cycles:

- Reset vector, Interrupt vector
- Reads from the vector table that appear due to servicing exceptions
- Illegal instructions
- (UNKNOWN) cycle types; the disassembler does not recognize the Control group value

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control. Instructions that do not actually change the control flow are not displayed, such as a conditional branch that is not taken.

Instructions that generate a change in the flow of control in an i960 Hx microprocessor are as follows:

CALL	B	BX
CALLS	BAL	FMARK
CALLX	BALX	RET

Instructions that can generate a change in the flow of control based on a condition or setting in the control register in an i960 Hx microprocessor are as follows:

BBC	CMPIBGE	FAULTE
BBS	CMPIBL	FAULTG
BE	CMPIBLE	FAULTGE
BG	CMPIBNE	FAULTL
BGE	CMPIBNO	FAULTLE
BL	CMPIBO	FAULTNE
BLE	CMPOBE	FAULTNO
BNE	CMPOBG	FAULTO
BNO	CMPOBGE	MARK
BO	CMPOBL	
CMPIBE	CMPOBLE	
CMPIBG	CMPOBNE	

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or return in an i960 Hx microprocessor are as follows:

CALL	CALLX
CALLS	RET

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the i960 Hx support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

Optional Display Selections

You can make optional selections for disassembled data.

In addition to the common display options (described in the basic operations user manual), you can change the displayed data in the following ways:

- Specify the base address of the Interrupt table.
- Specify the base address of the Fault table.
- Specify the Byte order.

The i960 Hx microprocessor support product has three additional fields: Interrupt table base, Fault table base, and Byte order. These fields appear in the area indicated in the basic operations user manual. Table 2–10 below lists the three additional display options and their ranges and default settings.

Table 2–10: Optional display selections

Display selection	Description	Range	Default
Interrupt table base	This field is necessary to compute the interrupt vector number.	00000800–FEFFFFFF	00000800
Fault table base	This field is necessary to identify the fault and its occurrence.	00000900–FEFFFFFF	00000900
Byte Order	This field is used to select Byte ordering. Default setting is Little Endian, with option of Big Endian.	—	Little Endian

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)

You can mark word-aligned address sequences, but not the second, third, or fourth bytes in the 8-bit memory region, or the second byte in the 16-bit region. If you mark the word-aligned sequence in the 8- or 16-bit region, the same mark is applied to the next three or one bytes, respectively.

If the target of branch is not double word-aligned, then the word prior to the nonaligned double word target is also fetched but not executed. When the target is not explicitly known in the instruction, the disassembler can not identify the target. You will need to identify and flush such sequences.

Mark selections are as follows:

```
Opcode
Extension
Flush
Undo Mark
```

The basic operations user manual contains more information on marking cycles.

Microcoded Instructions

A microcoded instruction is an instruction that takes more than one cycle to execute. Execution of these instructions results in refetch behavior. Automatic dequeueing is provided for all microcoded instructions in REG format. Automatic dequeueing is not provided for microcoded instructions in COBR, CTRL, or MEM formats.

Table 2–11 below shows an example of refetch behavior and how the sequence is disassembled.

Table 2–11: Refetch behavior example

Sequence	Disassembled
A000B000 : FLUSHREG	A000B000 : FLUSHREG
A000B004 : MOV R4,G4	A000B004 : FLUSH
A000B008 : XOR R2,R6,R10	A000B008 : FLUSH
A000B00C : NAND G4,G6,G8	A000B00C : FLUSH
A000B000 : FLUSHREG /* refetched because FLUSHREG is a microcoded inst*/	A000B000 : FLUSH

Table 2–11: Refetch behavior example (cont.)

Sequence	Disassembled
A000B004 : MOV R4,G4	A000B004 :MOV R4,G4
A000B008 : XOR R2,R6,R10	A000B008 : XOR R2,R6,R10
A000B00C : NAND G4,G6,G8	A000B00C : NAND G4,G6,G8

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your i960 Hx microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires i960 Hx signals
- List of other accessible microprocessor signals and extra probe channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a i960 Hx microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the supplied power adapter.

The probe adapter accommodates the Intel, Inc. i960 Hx microprocessor in a 168-pin PGA package.

Configuring the Probe Adapter

You can set up each memory region in the i960 Hx system through software. The probe adapter DIP switches must be set up to match your system's memory region setup. To configure the probe adapter, follow these steps:

1. Determine how the i960 Hx system is configured in each of its regions. Compare bits 29, 28, and 24 in PMCON register of each region to the bit values in Table 1–2 to determine how to set the DIP switch on the probe adapter.
2. Use Table 1–3 to determine which DIP switch to set for each memory region.

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–1, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements	
Probe adapter power supply requirements		
Voltage	90-265 VAC	
Current	1.1 A maximum at 100 VAC	
Frequency	47-63 Hz	
Power	25 W maximum	
SUT clock*		
i960 HA clock rate	40 MHz	
i960 HD clock rate	33 MHz	
i960 HT clock rate	25 MHz	
Minimum setup time required†		
BTERM#, READY#	8.5 ns	
All other signals	5 ns	
Minimum hold time required†		
All signals	0 ns	
Measured typical SUT signal loading	**AC load**	**DC load**
CLKIN	12 pF	2 74FCT162244ET 1 PAL22V10
A31:A28, BTERM#, READY#	8.5 pF	1 74FCT162244ET 1 PAL22V10/PAL16L8
WAIT#	7.0 pF	2 74FCT162244ET
A27:A2, D31:D0, DP3:DP0, CT3:CT0, BE#3:BE#0, BOFF#, HOLD, W/R#, LOCK#, NMI#, SUP#, ADS#, DEN#, BLAST#, D/C#, BREQ, RESET#, HOLDA, PCHK#, DT/R#, BSTALL	3.5 pF	1 74FCT162244

*** Maximum measured Clock frequency is 33 MHz.**

† **Setup and hold times are with respect to the CLKIN signal from the probe adapter.**

Table 3–2 shows the environmental specifications.

Table 3–2: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° F to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed i960 Hx microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–3 shows the certifications and compliances that apply to the probe adapter.

Table 3–3: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.

Figure 3–1 shows the dimensions of the probe adapter.

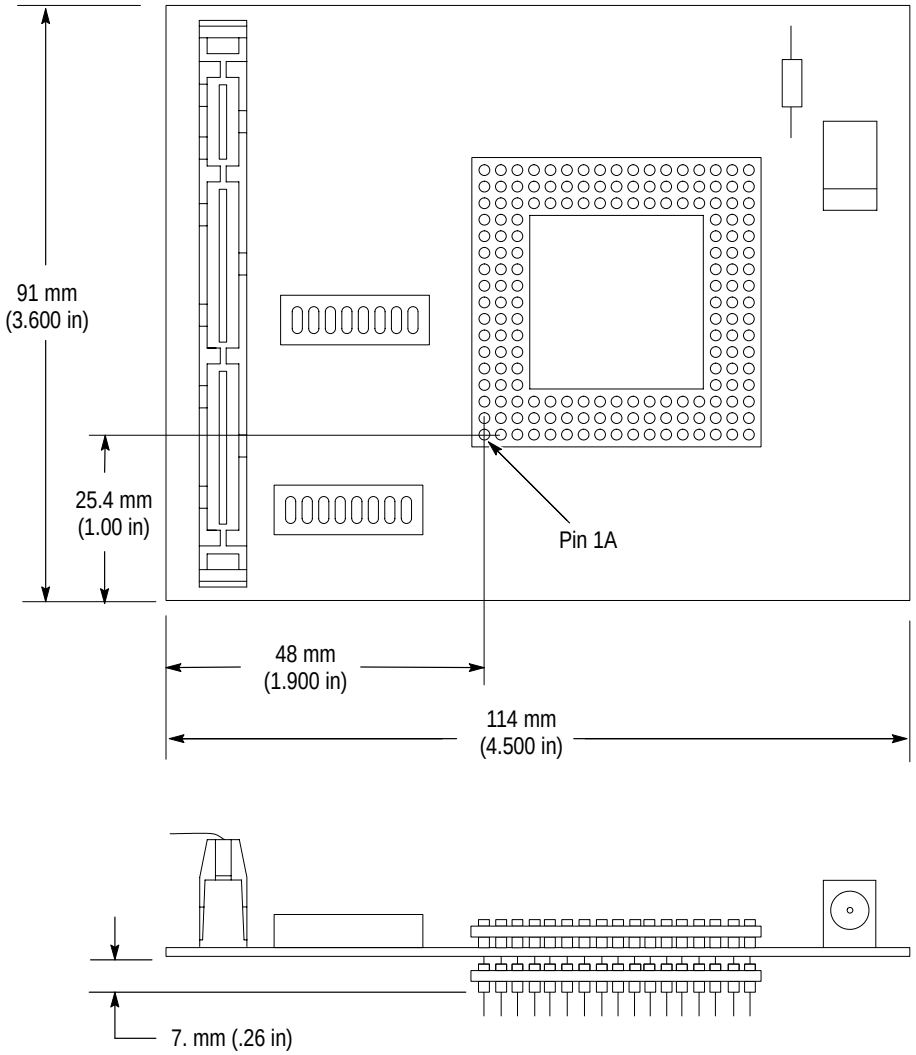


Figure 3–1: Minimum clearance of the standard probe adapter

Channel Assignments

Channel assignments shown in Table 3–4 through Table 3–10 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A pound sign (#) following a signal name indicates an active low signal
- An equals sign (=) following a signal name indicates that it is double probed.
- If there are two modules (such as used to form 96-channels), the module in the higher-numbered slot is referred to as the HI module and the module in the lower-numbered slot is referred to as the LO module.

Table 3–4 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–4: Address group channel assignments

Bit order	Section:channel	i960 Hx signal name
31	A3:7	A31
30	A3:6	A30
29	A3:5	A29
28	A3:4	A28
27	A3:3	A27
26	A3:2	A26
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14

Table 3–4: Address group channel assignments (cont.)

Bit order	Section:channel	i960 Hx signal name
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1*
0	A0:0	A0*

*** Signal grounded on the TMS 164 probe adapter; this is not an i960 Hx signal.**

Table 3–5 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: Data group channel assignments

Bit order	Section:channel	i960 Hx signal name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23

Table 3–5: Data group channel assignments (cont.)

Bit order	Section:channel	i960 Hx signal name
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–6 shows the probe section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. The default display radix is Symbolic for the 102/136-channel module and SYM for the 96-channel module.

Table 3–6: Control group channel assignments

Section: channel	i960 Hx signal name
C2:5	LOCK#
C2:1	HOLDA
C2:2	BLAST#
C3:2	W/R#
C2:4	D/C#
C2:6	BOFF#
C3:5	CT3
C3:1	CT2
C3:4	CT1
C3:0	CT0

Table 3–7 shows the probe section and channel assignments for the ByteEnbl group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3–7: ByteEnbl group channel assignments

Bit order	Section: channel	i960 Hx signal name
3	C3:7	BE3#
2	C3:3	BE2#
1	C2:3	BE1#
0	C2:7	BE0#

Table 3–8 shows the probe section and channel assignments for the Aux group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–8: Aux group channel assignments

Bit order	Section: channel	i960 Hx g signal name
1	C2:3	DEN#
0	C2:0	ADS#

Table 3–9 shows the section and channel assignments for the Misc group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–9: Misc group channel assignments

Section: channel	i960 Hx signal name
C0:0	NMI#
C1:7	DP3
C1:3	DP2
C1:6	DP1
C1:2	DP0
C1:4	WAIT#
C1:1	READY#
C1:0	BTERM#
C1:5	CLKIN
C0:1	DT/R#
C0:5	SUP#
C0:4	RESET#
C0:7	PCHK#
C0:6	BREQ
C0:3	BSTALL
C0:2	HOLD

Table 3–10 shows the section and channel assignments for the clock channels (not part of any group), and the microprocessor signal to which each channel connects. These channels are used only to clock in data; they are not acquired or displayed.

Table 3–10: Clock channel assignments

Section: channel	i960 Hx signal name
CLK0	CLKIN=
CLK1	P_BTERM#
CLK2	P_READY#
CLK3	WAIT#=

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–10, you must connect another channel probe to the signal, a technique called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

How Data is Acquired

This part of this chapter explains how the module acquires i960 Hx signals using the TMS 164 software and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra probe channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the i960 Hx support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the i960 Hx bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–2 shows the sample points and the master sample point.

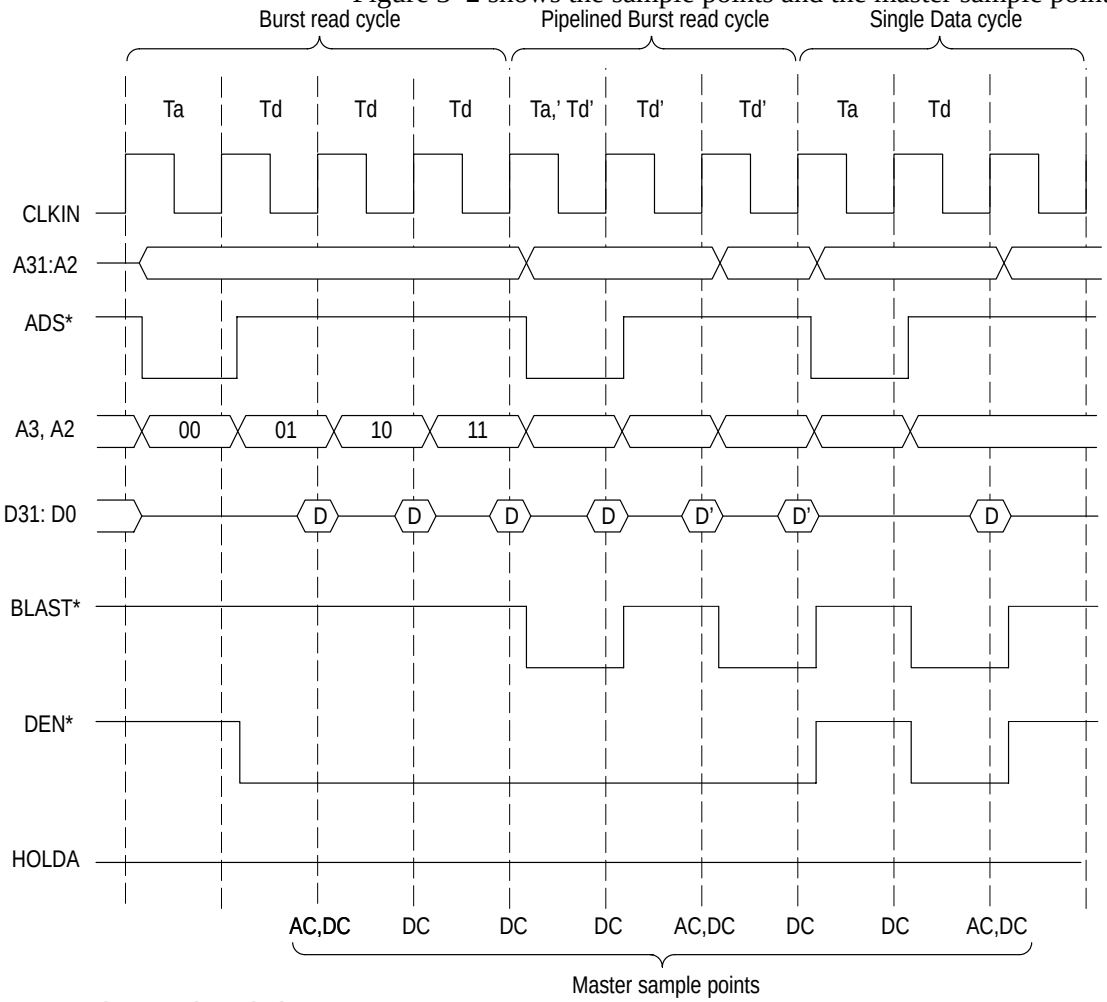


Figure 3–2: i960 Hx bus timing

The CSM has the states START, DMA, DATA, and BURST which handle all the states of processor address, data, wait, and hold.

The sampling is done at the rising edge of the CLKIN signal. The CSM enters the DATA state from the START state if ADS# is asserted, which is identified as the start of valid bus cycle. To do this, it also requires the HOLDA signal to be deasserted if DMA is excluded. If DMA is included, CSM goes to DMA state from START state if HOLDA is asserted.

If it is a single data transfer, CSM goes from the DATA state back to the START state and BLAST# is asserted low to indicate the end of the bus cycle. If the cycle is terminated which is indicated by assertion of P_BTERM#, the CSM also goes to the START state. If a burst cycle has occurred, BLAST# indicates deassertion. For this, the CSM goes to the BURST state. For all these the address, data, and control signals will be strobed and a master strobe will also be given. The ADS# will be deasserted for all of these.

If P_BTERM# is asserted the cycle is terminated and the CSM goes back to START state after logging the address, data, and control signals. A pipelined non-burst access may also occur when in DATA cycle which is identified by the assertion of both ADS# and BLAST#. The CSM keeps logging in address, data, and control signals and keeps waiting in DATA state.

When the CSM is in BURST state it remains in that state until the end of the bus cycle, which is indicated by the assertion of BLAST#. A3:2 data and control signals are logged until it remains in the BURST state. When BLAST# is asserted, CSM goes to START state. If P_BTERM# is asserted, the cycle is terminated and CSM goes back to START state after logging the address, data, and control signals. A pipelined burst occurs when BLAST# and ADS# are asserted at the same time, indicating that the valid address is put for next data; in this case, CSM goes to DATA state.

After the acquisition is complete, the disassembler reads the acquisition memory. Since each memory location contains i960 Hx data for a complete bus cycle, the disassembler is able to deduce the kind of bus activity that took place. For example, if an opcode fetch occurred, the disassembler converts the data bus into the opcode the data bus represents.

Clocking Options

The clocking algorithm for the i960 Hx microprocessor has two variations: DMA cycles included or DMA cycles excluded.

If HOLDA is active, then the i960 Hx microprocessor has given up the bus to another device. The design of the i960 Hx hardware affects what data will be logged in. The logic analyzer only samples signals at the i960 Hx pins. To properly log in bus activity, any buffers between the i960 Hx and the alternate bus driver must be enabled and pointed towards the i960 Hx. Possible i960 Hx hardware and clocking interactions are as follows:

- If the alternate device drives the same control lines as the i960 Hx and the i960 Hx sees these signals, alternate bus activity is logged in just like normal bus cycles except that HOLDA will be asserted.
- If none of the control lines are driven or if the i960 Hx cannot see them, the logic analyzer still logs in a DMA cycle. The information present on the bus one clock period prior to the deassertion of HOLDA is logged in as the DMA bus cycle.
- If some of the i960 Hx control signals are visible, but not all of them, the logic analyzer logs in what it determines is valid from the visible control signals and logs in the information previously present on the remaining bus signals one clock period prior to the deassertion of HOLDA. In all cases, HOLDA is logged in as high.

DMA Cycles Excluded. Whenever the logic analyzer is about to log in the first sample of a bus cycle and it detects that HOLDA is high, no data is logged in. No DMA cycles caused by HOLDA are logged in with this selection.

Synthesized Signals

The probe adapter must synthesize four signals in order to acquire valid data. Table 3–11 describes them. Refer to the previous discussions on including and excluding DMA cycles for a description of how these signals are used.

Table 3–11: Synthesized signals

Signal	Description
P_BTERM#	Derived from the DIP switches on the probe adapter. If the switch is open, P_BTERM# is the same as BTERM#. If the switch is closed, P_BTERM# is deasserted (high).
P_READY#	Derived from the DIP switches on the probe adapter. If the switch is open, P_READY# is the same as READY#. If the switch is closed, P_READY# is asserted (low).
A1	Grounded on the probe adapter
A0	Grounded on the probe adapter

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so that you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–5. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals Not on the Probe Adapter

Table 3–12 lists signals not accessible on the probe adapter.

Table 3–12: Signals not on the probe adapter

FAIL#	TDO	XINT0#	XINT4#
ONCE#	TDI	XINT1#	XINT5#
STEST	TMS	XINT2#	XINT6#
TCK	TRST#	XINT3#	XINT7#

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This chapter contains information on the following topics:

- Probe adapter circuit description
- How to replace a fuse

Probe Adapter Circuit Description

A 22V10 PAL, two 8-wide DIP switches, the upper four address lines A31–A28, and CLKIN are used to generate a signal named P_RDY_EN. The i960 Hx uses its upper four address lines to map its memory into 16 memory regions. Each region is software programmable.

The READY# and BTERM# inputs may be masked out in each of the regions. The user must open the DIP switch(s) that corresponds to region(s) where READY# and BTERM# are enabled. This causes P_RDY_EN to be high whenever the address is in a region where READY# and BTERM# are active. P_RDY_EN is combined with READY# and BTERM# to create P_READY# and P_BTERM#. In a region where READY# is enabled P_READY# will be the same as READY#. In regions where READY# is not enabled P_READY# will be low regardless of the value of READY#. In regions where BTERM# is enabled P_BTERM# will be the same as BTERM#. In regions where BTERM# is not enabled P_BTERM# will be high regardless of the value of BTERM#.

The 22V10 PAL is programmed for 21 inputs and one output. The PAL is programmed to decode the four address lines into 16 internal signals. Each signal is AND-ed with a DIP switch, then all of the AND gate outputs are OR-ed together. The OR output is clocked into a flip flop whose output becomes P_RDY_EN. When the DIP switch is open the input to the AND gate is high. When the DIP switch is closed the input to the AND gate is low.

The signal P_RDY_EN is combined with BTERM# in a 16L8PAL to generate P_BTERM#. P_RDY_EN is also combined with READY# in 16L8PAL to generate P_READY#.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replacing the Fuse

If the fuse on the i960 Hx probe adapter opens (burns out), you can replace it with a 5 A, 125 V fuse. Figure 4–1 shows the location of the fuse on the probe adapter.

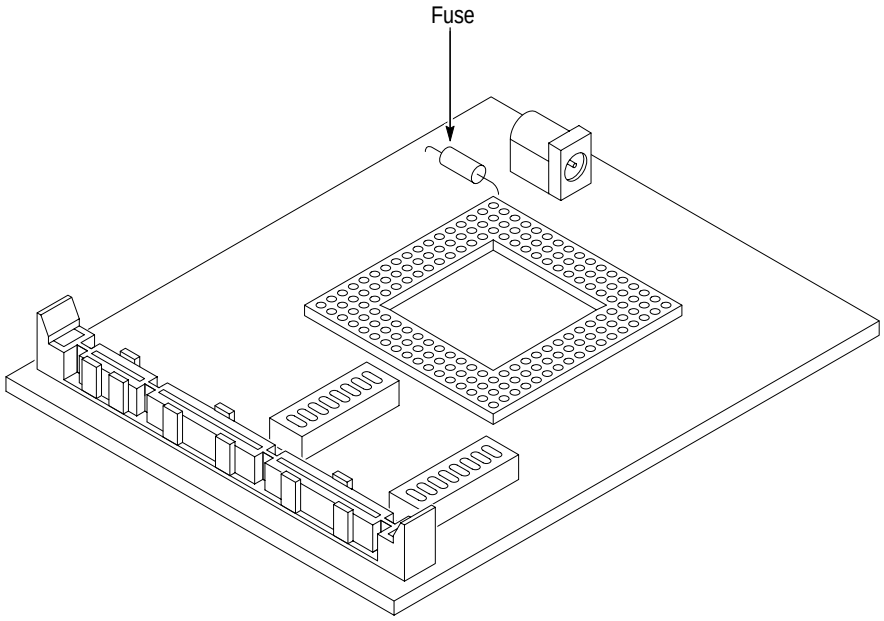


Figure 4–1: Location of the fuse

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 164 i960 Hx microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

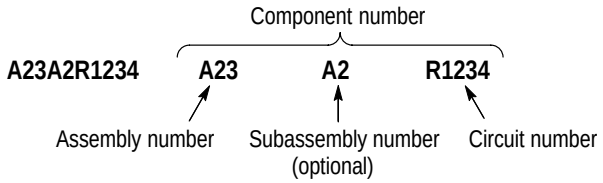
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
09353	C & K COMPONENTS CORP	15 RIVERDALE AVENUE	NEWTON, MA 02158
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG, MD 20879
61857	SAN–O INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK, NY 11741
63058	MCKENZIE TECHNOLOGY	910 PAGE AVE	FREMONT, CA 945387340
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	671-3931-00			CIRCUIT BD ASSY:I960HX,PGA-168, SOCKETED, 389-2157-00 WIRED,32/92DM19	80009	671-3931-00
A01F100	159-0059-00			FUSE,WIRE LEAD:5A,125V, FAST	61857	SP1-5A
A01J100	131-5527-00			JACK,POWER DC:PCB,MALE,RTANG,2MM PIN,11MM H(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWI	0LXM2	DJ005A
A01J510	131-5947-00			CONN,BOX:PCB,MICRO–STRIP,FEMALE,STR,100 POS,0.05 CTR,W/GRD PLANE,0.320 H X 0.125 TAIL,LAT	00779	121289–7
A01S420	260-5000-00			SWITCH,SLIDE:SPST,DIP8 POSITION,GOLD OVER NICKEL,3A,2PF,SEALED,90HBW08S,44MM T&R	09353	LD08HOSK1
A01S440	260-5000-00			SWITCH,SLIDE:SPST,DIP8 POSITION,GOLD OVER NICKEL,3A,2PF,SEALED,90HBW08S,44MM T&R	09353	LD08HOSK1
A01U330	136-1250-00			SOCKET,PGA:PCB,168 POS,17 X 17 MATRIX,0.1 CTR,0.173 H X 0.183 TAIL,GOLD,PHOS BRZ,PAT 1706 W	63058	PGA–168H–101B–176 9

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 164 i960 Hx microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
09353	C & K COMPONENTS CORP	15 RIVERDALE AVENUE	NEWTON, MA 02158
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG, MD 20879
61857	SAN–O INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK, NY 11741
63058	MCKENZIE TECHNOLOGY	910 PAGE AVE	FREMONT, CA 945387340
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable parts list

Fig. &index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
6–1	010-0600-00			1	PROBE ADAPTER:i960HX,SOCKETED	80009	010-0600-00
–1	174-3418-00			1	CA ASSY,RF:TLC,MICRO–STRIP,TLC,50 OHM	00779	1-340014-0
–2	159-0059-00			1	FUSE,WIRE LEAD:5A,125V, FAST	61857	SP1–5A
–3	131-5527-00			1	JACK,POWER DC:PCB,MALE,RTANG,2MM PIN,11MM H(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWI	0LXM2	DJ005A
–4	260-5000-00			2	SWITCH,SLIDE:SPST,DIP8 POSITION,GOLD OVER NICKEL,3A,2PF,SEALED,90HBW08S,44MM T&R	09353	LD08HOSK1
–5	671-3931-00			1	CIRCUIT BD ASSY:I960HX,PGA–168, SOCKETED, 389-2157-00 WIRED,32/92DM19	80009	671-3931-00
–6	136-1250-00			2	SOCKET,PGA:PCB,168 POS,17 X 17 MATRIX,0.1 CTR,0.173 H X 0.183 TAIL,GOLD,PHOS BRZ,PAT 1706 W	63058	PGA-168H-101B-1769
–7	131-5947-00			1	CONN,BOX:PCB,MICRO–STRIP,FEMALE,STR,100 POS,0.05 CTR,W/GRD PLANE,0.320 H X 0.125 TAIL,LAT	00779	121289–7
					STANDARD ACCESSORIES		
	070-9818-00			1	MANUAL,TECH:INSTRUCTION,i960HX	80009	070-9818-00
	070-9365-01			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA	80009	070-9365-01
	119-5061-01			1	POWER SUPPLY:25W;5V 5A,CONCENTRIC 2MM (NOT SHOWN)	14310	SW106KA002F01
	161-0104-00			1	CA ASSY,PWR 3,18 AWG,98 L, 250V/10AMP,98 IN., RTANG, IEC 320,RCPT X STR NEMA 15 –5P,W/ CORD GRIP,US	OB445	MC6–3CG86

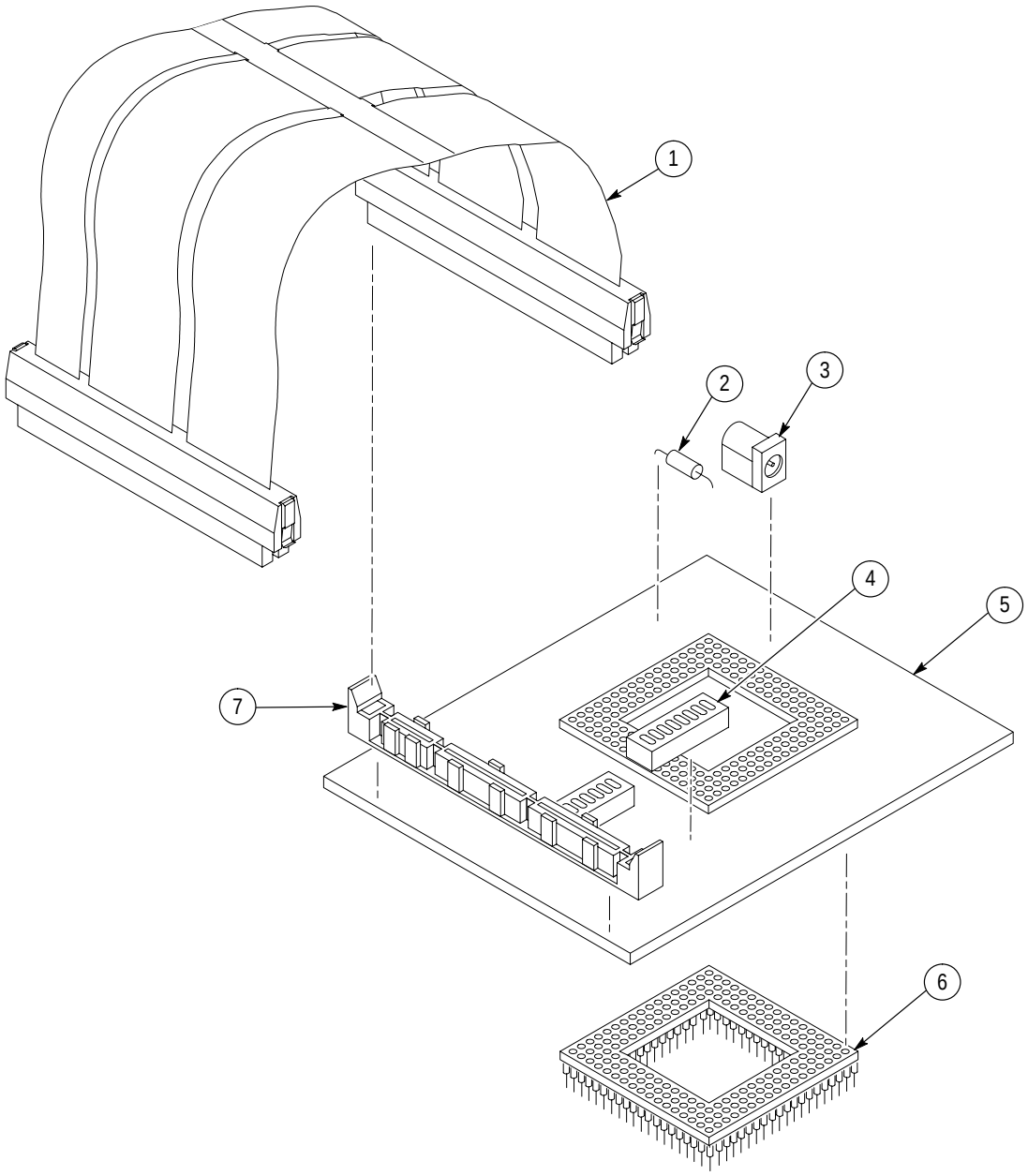


Figure 6–1: i960 Hx probe adapter exploded view

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