Instruction Manual

Tektronix

TMS 203
68030 & 68EC030 Microprocessor Support

070-9821-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

The common terminal is at ground potential. Do not connect the common terminal to elevated voltages.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Wear Eye Protection. Wear eye protection if exposure to high-intensity rays or laser radiation exists.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains information about the TMS 203 68030 microprocessor support and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor supports on the logic analyzer for which the TMS 203 68030 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor supports, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor supports is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- The TMS 203 68030 probe adapter

Manual Conventions

This manual uses the following conventions:

- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- The term XXX or P54C used in field selection and file name examples must be replaced with 68030. This is the name of the microprocessor in field selections and file names you must use to operate the 68030 support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.
- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to to a 102/136-channel or a 96-channel module.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The user manual provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics:

- The TMS 203 68030 microprocessor support
- Logic analyzer software compatibility
- Your 68030 system requirements
- 68030 support restrictions
- How to configure the probe adapter
- How to connect to the System Under Test (SUT)

Support Description

The TMS 203 microprocessor support disassembles data from systems that are based on the Motorola 68030 microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 96-channel module or a 102/136-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 203 microprocessor support.

Table 1–1 shows the microprocessors and packages from which the TMS 203 support can acquire and disassemble data.

Table 1–1: Supported microprocessors

Name	Package
68030	Socketed PGA
68EC030	Socketed PGA
68030	Soldered CQFP

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the following documents:

- The 68030 *MC68030 Microprocessor User's Manual*, Motorola, Inc.

- The *68030 Technical Summary*, Motorola, Inc.
- The *68EC030 Technical Summary*, Motorola, Inc.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the 68030 support, the Tektronix logic analyzer must be equipped with at least a 96-channel module or a 102/136-channel module. The module must be equipped with enough probes to acquire channel and clock data from signals in your 68030-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other 68030 support requirements and restrictions.

System Clock Rate. The microprocessor support product supports the 68030 microprocessor at speeds of up to 50 MHz[1] and the 68EC030 microprocessor at speeds up to 40 MHz[1].

Data Reads and Writes. The disassembler will not link data reads and writes with the instructions which cause them.

1 **Specification at time of printing. Contact your logic analyzer sales representative for current information on the fastest devices supported.**

Disabling the Instruction Cache. To disassemble acquired data, you must disable the internal instruction cache. Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled.

Configuring the Probe Adapter

Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled. The probe adapter contains CDIS jumper J190 (J1601 for the CQFP adapter) which you can use to disable the 68030 cache.

With the Cache jumper in the CACHE EN position, the SUT controls the cache and the CDIS~ signal is not affected.

With the Cache jumper in the CACHE OFF position, the CDIS~ signal connects to a 332 Ω pull-down resistor on the probe adapter which disables the cache. For the PGA probe adapter, you should also cut or remove pin H12 from the protective socket on the underside of the probe adapter to prevent contention with the driving signal. For the CQFP probe adapter, you should disable any devices on the SUT that drive the CDIS~ signal to prevent contention with the driving signal.

Figure 1–1 shows the location of J190 on the PGA probe adapter.

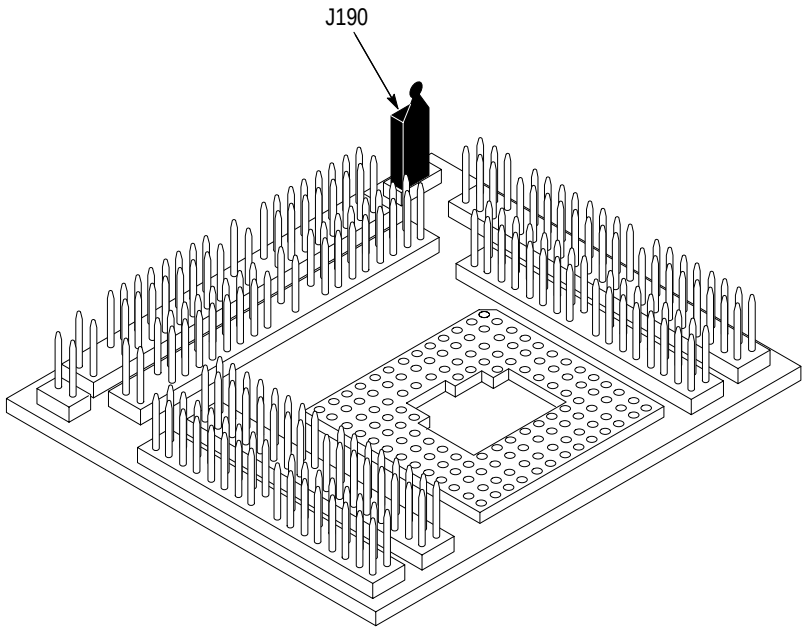


Figure 1–1: Cache jumper location on the PGA probe adapter

Figure 1–2 shows the location of J1601 on the CQFP probe adapter.

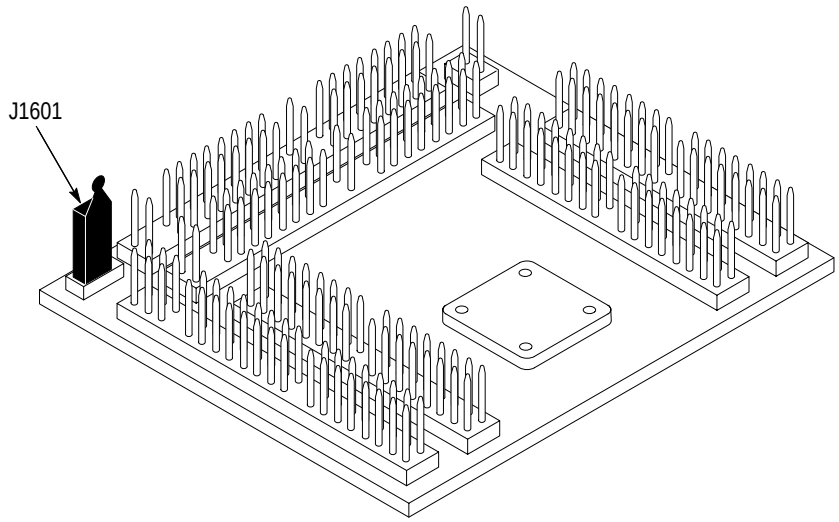


Figure 1–2: Cache jumper location on the CQFP probe adapter

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. Your probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

PGA Probe Adapter

To connect the logic analyzer to a SUT using a PGA probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–3. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the microprocessor from your SUT.
5. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–3.

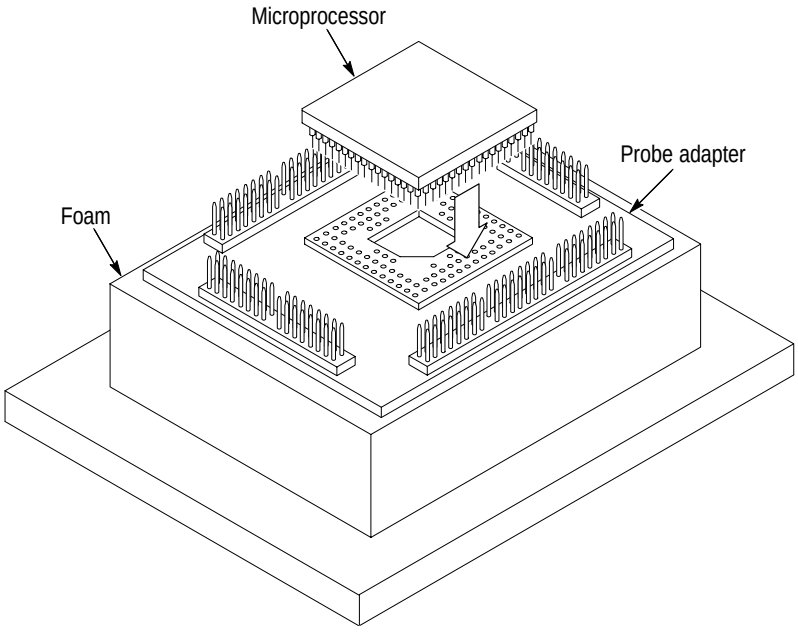


Figure 1–3: Placing a microprocessor into a PGA probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–4. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

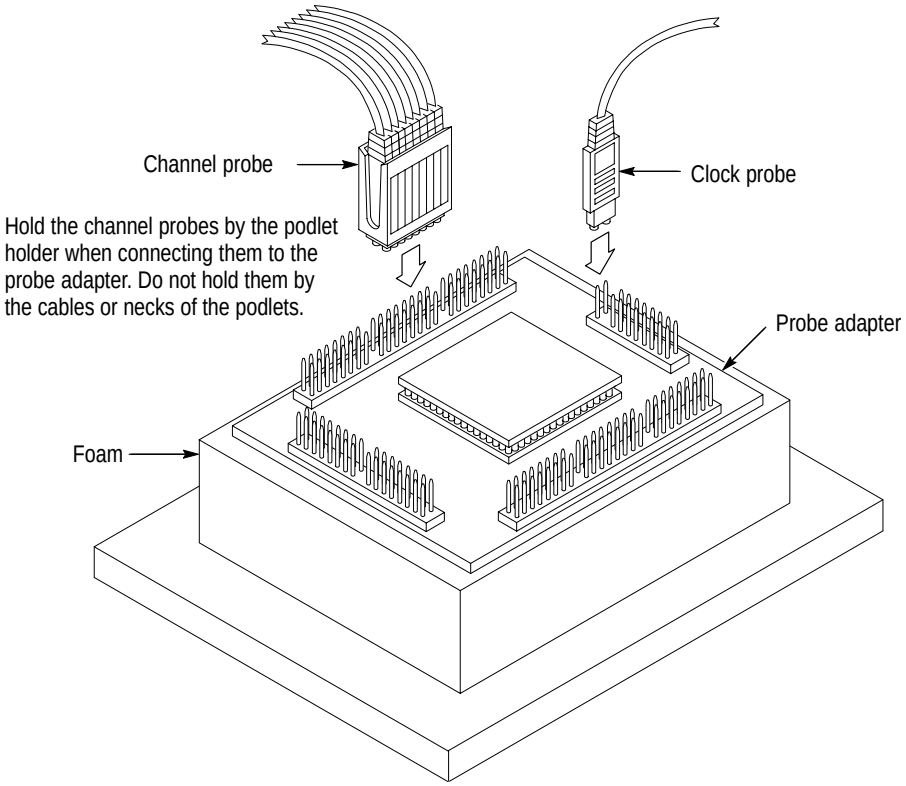


Figure 1–4: Connecting probes to a PGA probe adapter

8. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on your SUT.

9. Place the probe adapter onto the SUT as shown in Figure 1–5.

NOTE*. You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.*

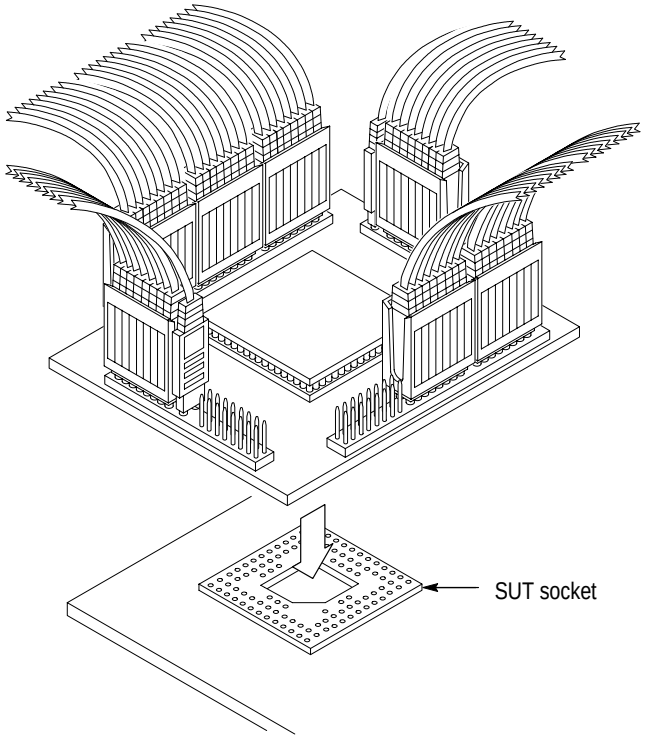


Figure 1–5: Placing a PGA probe adapter onto the SUT

CQFP Probe Adapter

To connect the logic analyzer to a SUT using a CQFP probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–6. This prevents the circuit board from flexing.
4. Connect the channel and clock probes to the probe adapter as shown in Figure 1–6. Match the channel groups and numbers on the probe labels to the

corresponding probe adapter pins. Match the ground pins on the probes to the corresponding pins on the probe adapter.

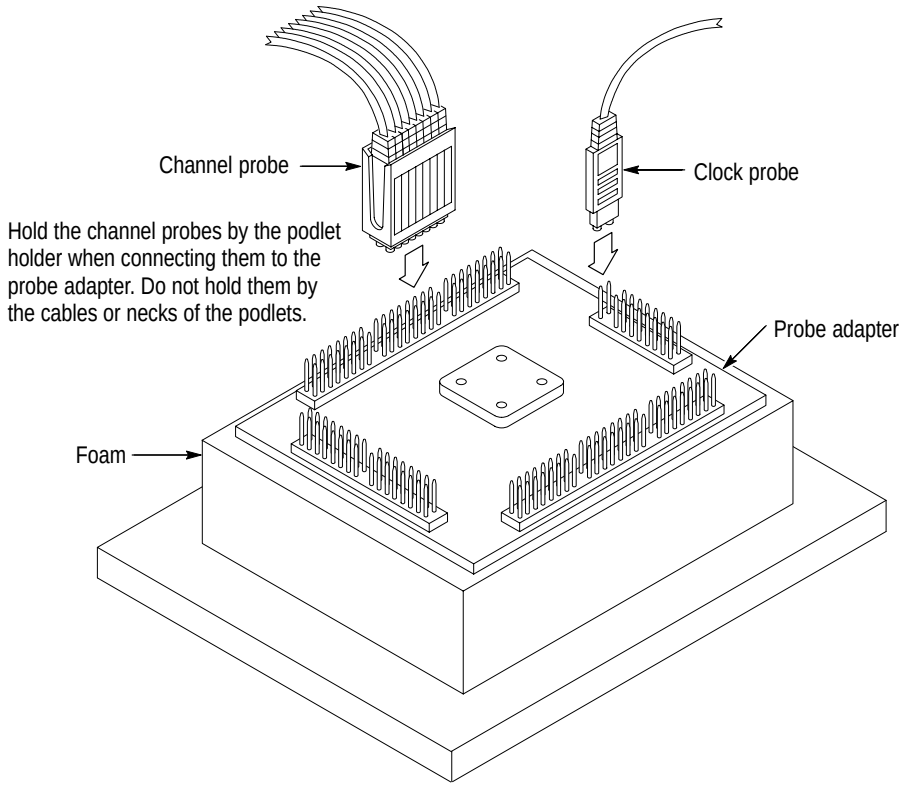


Figure 1–6: Connecting probes to a CQFP probe adapter

CAUTION. *This JEDEC (Quad Flat Pack) probe adapter has been equipped with a clip designed for tight tolerances.*

The clip supports only Quad Flat Pack devices that conform to the JEDEC M0-069 October 1990 specification. Attaching the clip to a device that does not conform to this JEDEC standard can easily damage the clip's connection pins and/or the microprocessor, causing the probe adapter to malfunction.

Please contact your IC manufacturer to verify that the microprocessor you are targeting conforms to the JEDEC specification.

For best performance and long probe life, use extreme care when connecting the probe adapter to the microprocessor.

5. Place a little glue on each corner of the CQFP-to-PQFP converter.

6. Place the CQFP-to-PQFP converter over your CQFP microprocessor as shown in Figure 1–7.

NOTE*. Do not allow the glue to touch the pins of your microprocessor. This might interfere with the connection between the microprocessor and the probe adapter. An open connection will cause errors.*

7. Allow the glue to dry.

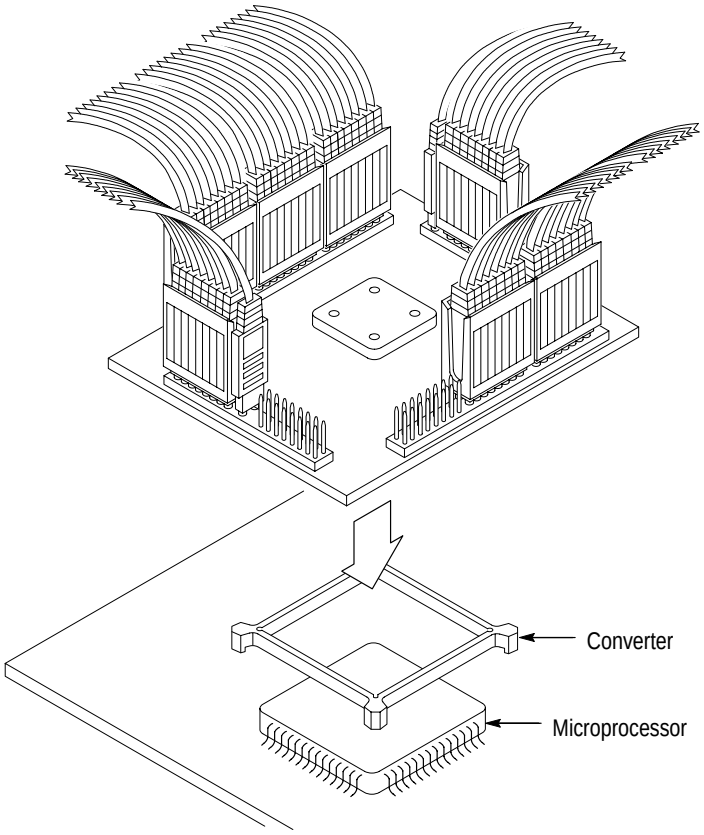


Figure 1–7: Placing a CQFP probe adapter onto the SUT

8. Line up the pin 1 indicator on CQFP clip on the probe adapter with the pin 1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the probe adapter onto the microprocessor might permanently damage all electrical components when power is applied.*

Center the clip on the microprocessor and apply an equal downward force on all four sides of the clip, slightly rocking the probe adapter in a clockwise circle.

Do not apply leverage to the probe adapter when installing or removing it.

9. Place the probe adapter onto the SUT as shown in Figure 1–7.

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to 68030 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

CAUTION. *Failure to place the SUT on a horizontal surface before connecting the test clip might permanently damage the pins on the microprocessor.*

3. Place the SUT on a horizontal static-free surface.

4. Use Table 1–2 to connect the channel probes to 68030 signal pins on the test clip or in the SUT.

Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Table 1–2: 68030 signal connections for channel probes

Section:channel	68030 signal	Section:channel	68030 signal
A3:7	A31	D3:7	D31
A3:6	A30	D3:6	D30
A3:5	A29	D3:5	D29
A3:4	A28	D3:4	D28
A3:3	A27	D3:3	D27
A3:2	A26	D3:2	D26
A3:1	A25	D3:1	D25
A3:0	A24	D3:0	D24
A2:7	A23	D2:7	D23
A2:6	A22	D2:6	D22
A2:5	A21	D2:5	D21
A2:4	A20	D2:4	D20
A2:3	A19	D2:3	D19
A2:2	A18	D2:2	D18
A2:1	A17	D2:1	D17
A2:0	A16	D2:0	D16
A1:7	A15	D1:7	D15
A1:6	A14	D1:6	D14
A1:5	A13	D1:5	D13
A1:4	A12	D1:4	D12
A1:3	A11	D1:3	D11
A1:2	A10	D1:2	D10
A1:1	A9	D1:1	D9
A1:0	A8	D1:0	D8
A0:7	A7	D0:7	D7
A0:6	A6	D0:6	D6
A0:5	A5	D0:5	D5
A0:4	A4	D0:4	D4
A0:3	A3	D0:3	D3
A0:2	A2	D0:2	D2
A0:1	A1	D0:1	D1
A0:0	A0	D0:0	D0
C3:7	DSACK0~	C2:7	SIZ1

Table 1–2: 68030 signal connections for channel probes (cont.)

Section:channel	68030 signal	Section:channel	68030 signal
C3:6	FC1	C2:6	SIZ0~
C3:5	FC0	C2:5	HALT~
C3:4	AS_B~	C2:4	BERR~
C3:3	RMC~	C2:3	BGACK~
C3:2	FC2	C2:2	R_W~
C3:1	DSACK1~	C2:1	STERM_L~*
C3:0	CLK~*	C2:0	CBACK~*
C1:7	REFILL~†	C0:7	STATUS~†
C1:6	IPL2~	C0:6	IPL0~*
C1:5	AVEC~†	C0:5	BR~†
C1:4	RESET~†	C0:4	DS~†
C1:3	CIIN~†	C0:3	CBREQ~†
C1:2	IPL1~*	C0:2	IPEND~†
C1:1	DBEN~†	C0:1	BG~†
C1:0	ECS~†	C0:0	STERM~†

* **Signal not required for disassembly.**

† **Signal not part of any channel group.**

Table 1–3 shows the clock probes, and the 68030 signal to which they must connect for disassembly to be correct.

Table 1–3: 68030 signal connections for clock probes

Section:channel	68030 signal
CK:3	CBREQ_B
CK:2	AS_B
CK:1	CLK_B~

5. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the 68030 microprocessor in your SUT and attach the clip to the microprocessor.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 203 68030 support on any compatible Tektronix logic analyzer. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify clocking and triggering setups as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The dissembler automatically defines the channel groups for the microprocessor. The channel groups for the 68030 microprocessor are: Address, Data, Control, DataSize, Misc, and Intr.

Clocking Options

The TMS 203 support offers a microprocessor-specific clocking mode for the 68030 microprocessor. This clocking mode is the default selection whenever you load the 68030 support.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these other clock selections with the microprocessor support products.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

DMA Cycles

A DMA cycle is defined as the 68030 microprocessor giving up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Symbols

The TMS 203 support supplies one symbol table file. The chip_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 lists the name, bit pattern, and meaning for the symbols in the file chip_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value			Meaning
	BGACK~ FC2 FC1 FC0	RMC~ AS_B~ R/W~	HALT~ BERR~ SIZ1 SIZ0	
ACK_ERROR	1 1 1 1	X 0 1	1 0 X X	CPU space acknowledgement error
B_ERR_RTY	X X X X	X X X	0 0 X X	Bus error retry
BUS_ERROR	X X X X	X X X	X 0 X X	Bus error
DMA_READ	0 X X X	X 0 1	X X X X	DMA read cycle
DMA_WRITE	0 X X X	X 0 0	X X X X	DMA write cycle
DMA*	0 X X X	X X X	X X X X	Any DMA cycle
CPU_RD	X 1 1 1	X 0 1	X X X X	CPU space read cycle
CPU_WR	X 1 1 1	X 0 0	X X X X	CPU space write cycle
CPU_SPACE*	X 1 1 1	X 0 X	X X X X	CPU space cycle
RMW_READ	X X X X	0 0 1	X X X X	Read of read-modify-write cycle
RMW_WRITE	X X X X	0 0 0	X X X X	Write of read-modify-write cycle
RMW*	X X X X	0 0 X	X X X X	Any read-modify-write cycle
DATA_RD	X X 0 1	X X X	X X X X	Read from data space
DATA_WR	X X 0 1	X 0 0	X X X X	Write to data space
PREFETCH?	1 X 1 0	X 0 1	X X X X	Read from program space
PROG_RD	X X 1 0	X 0 1	X X X X	Read from program space
PROG_WR	X X 1 0	X 0 0	X X X X	Write to program space
READ	X X X X	X 0 1	X X X X	Read
WRITE	X X X X	X 0 0	X X X X	Write
SUPER_DAT	X 1 0 1	X X X	X X X X	Supervisor data space
SUPER_PRG	X 1 1 0	X X X	X X X X	Supervisor program space
SUPERVISR*	X 1 X X	X X X	X X X X	Supervisor space
USER_DATA	X 0 0 1	X X X	X X X X	User data space
USER_PROG	X 0 1 0	X X X	X X X X	User program space
USER*	X 0 X X	X X X	X X X X	User space

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value BGACK~ FC2 FC1 FC0 / RMC~ AS_B~ R/W~ / HALT~ BERR~ SIZ1 SIZ0	Meaning
PRG_SPACE	X X 1 0 / X X X / X X X X	Program space access
DAT_SPACE	X X 0 1 / X X X / X X X X	Data space access
HALT_REQ*	X X X X / X X X / 0 1 X X	Processor halt request

*** Symbols used only for triggering; they do not appear in the Disassembly or State menus.**

Table 2–2 lists the name, bit pattern, and meaning for the symbols in the file 68030_Intr, the Interrupt group symbol table.

Table 2–2: Interrupt group symbol table definitions

Symbol	Interrupt group value IPL2~ IPL1~ IPL3~	Meaning
–	1 1 1	No interrupt
IPL_1	1 1 0	Level 1 interrupt request
IPL_2	1 0 1	Level 2 interrupt request
IPL_3	1 0 0	Level 3 interrupt request
IPL_4	0 1 1	Level 4 interrupt request
IPL_5	0 1 0	Level 5 interrupt request
IPL_6	0 0 1	Level 6 interrupt request
IPL_7	0 0 0	Level 7 interrupt request

Information on basic operations describes how to use symbolic values for triggering, and displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- How to change the way data is displayed
- How to change disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 68030 support, choose a clocking mode and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual, whichever is available.

Viewing Disassembled Data

You can view disassembled data in four different display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) or in the Processor Support submenu of the State table menu for the 80-channel module must be set correctly for your acquired data to be disassembled correctly.*

The default display format shows the Address, Data, Intr, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–3 shows the special characters and strings displayed by the 68030 disassembler and gives a definition of what they represent.

Table 2–3: Special characters in the display and meaning

Character or string displayed	Meaning
#	Indicates an immediate value
>	Indicates there is insufficient room on the screen to show all available data
t	Indicates the number shown is in decimal, such as #12t
**	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks will indicate the width of the data that is unavailable. Each two asterisks represent a byte
* ILLEGAL INSTRUCTION *	Decoded as an illegal instruction
A-LINE OPCODE	Displayed for an A-Line trap instruction
F-LINE OPCODE	Displayed for an F-Line trap instruction

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–4 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–4: Cycle type definitions

Cycle Type	Definition
(BREAKPOINT n)*	A breakpoint acknowledge cycle generated by execution of a BKPT instruction (n is the breakpoint number assigned in the BKPT command)
(BUS ERROR)	A bus cycle error
(BUS ERROR RETRY)	A bus cycle error retry
(COPROCESSOR #n READ REG: Rm)*	A read cycle accessing a coprocessor (n is the coprocessor number and Rm is the register number)
(COPROCESSOR #n WRITE REG: Rm)*	A write cycle accessing a coprocessor (n is the coprocessor number and Rm is the register number)
(CPU READ)	A data read in CPU space
(CPU SPACE BUS ERROR)	A bus error in CPU space
(CPU WRITE)	A data write in CPU space
(DMA)	A cycle in DMA mode
(DMA READ)	A read cycle in DMA mode
(DMA WRITE)	A write cycle in DMA mode
(EXTENSION)*	The second or subsequent fetch cycle of a multi-word instruction
(FLUSH)*	A fetch cycle that was flushed from the 68030's prefetch queue without execution

Table 2–4: Cycle type definitions (Cont.)

Cycle Type	Definition
(INTERRUPT ACK LEVEL: n)	Interrupt acknowledge cycle (n is the level of the interrupt being acknowledged)
(READ)	A data read cycle
(RMW READ)	The read portion of a read-modify-write cycle
(RMW WRITE)	The write portion of a read-modify-write cycle
(UNKNOWN)	The combination of control bits is unexpected and/or unrecognized
(WRITE)	A data write cycle

* **Computed cycle types.**

Figure 2–1 shows an example of the Hardware display.

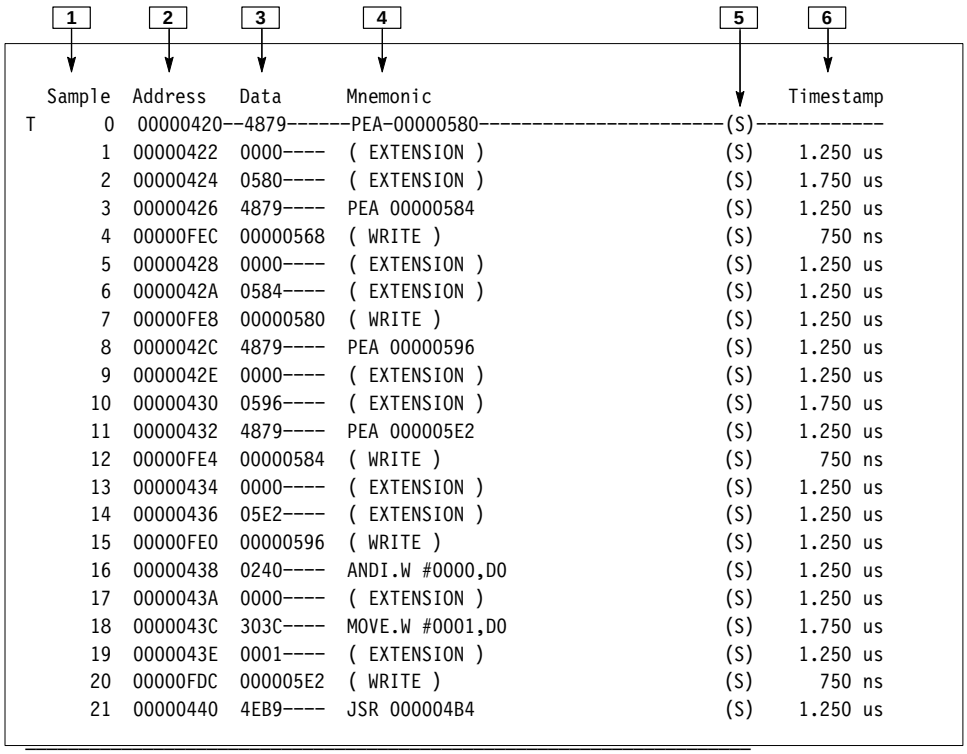


Figure 2–1: Hardware display

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the 68030 Address bus.

3 **Data Group.** Lists data from channels connected to the 68030 Data bus.

4 **Mnemonic Column.** Lists the disassembled instructions and cycle types.

5 The disassembler displays an (S) or (U) in the mnemonic column to indicate the mode in which the microprocessor is operating, Supervisor or User.

6 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

The Software display format also shows the following:

- Bus Error cycle
- CPU space Bus Error Cycle
- Emulated instructions that cause exceptions
- Special cycles: Breakpoint Ack, Int Ack, Internal Reg Access, Reset Vector
- Reads from the vector table that appear due to servicing interrupts or traps
- Illegal instructions
- UNKNOWN cycle types: the disassembler does not recognize the control group value

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

The Control Flow display format displays the following:

- Bus Error cycle
- CPU space Bus Error cycle
- Emulated instructions that cause exceptions
- Special cycles: Breakpoint Ack, Int Ack, Internal Reg Access
- Reset vector
- Reads from the vector table that appear due to servicing interrupts or traps
- Illegal instructions

- Unknown cycle types; the disassembler does not recognize the control group value

Instructions that generate an unconditional change in the flow of control in the 68030 microprocessor are as follows:

BKPT	BRA	BSR
ILLEGAL	JMP	JSR
RESET	RTD	RTE
RTR	RTS	STOP
TRAP		

Instructions that generate a conditional change in the flow of control in the 68030 microprocessor are displayed if they are determined to have been taken. These instructions are as follows:

Bcc	DBcc	FBcc
TRAPcc	TRAPV	

Instructions that might generate a change in the flow of control in the 68030 microprocessor are as follows:

CHK	CHK2	DIVS
DIVSL	DIVU	DIVUL

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

The Subroutine display format also displays the following:

- Bus Error Cycle
- CPU space Bus Error cycle
- Emulated instructions that cause exceptions
- Special cycles: Breakpoint Ack, Int Ack, Internal Reg Access
- Reset Vector
- Reads from the vector table that appear due to servicing interrupts or traps
- Illegal instructions
- Unknown cycle types; the disassembler does not recognize the control group value

Instructions that generate a subroutine call or a return in the 68030 microprocessor are as follows:

BKPT	BSR	ILLEGAL
JSR	RESET	RTD
RTE	RTR	RTS
STOP	TRAP	

Instructions that display if they cause an exception to occur in the 68030 microprocessor are as follows:

CHK	CHK2	DIVS
DIVSL	DIVU	DIVUL
TRAPcc	TRAPV	

Changing How Data is Displayed

There are fields and features that allow you to further modify displayed data to suit your needs. You can make selections unique to the 68030 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

Optional Display Selections

You can make optional display selections for acquired disassembled data to help you analyze the data. You can make these selections in the Disassembly property page (the Disassembled Format Definition overlay).

In addition to the common display options (described in the information on basic operations), you can change the displayed data in the following ways:

- Specify the starting address of the vector base register table
- Specify the size of the exception vector table

The 68030 support has two additional fields: Vector Base Register, and Vector Table Size. These fields appear in the area indicated in the information on basic operations.

Vector Base Register. You can specify the starting address of the vector table in hexadecimal. The default starting address is 0x00000000.

Vector Table Size. You can specify the size of the interrupt table in hexadecimal. The default size and maximum value is 400. Minimum value is 8. Size must be devisable by 4.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)
- Anything (any valid opcode, extension or flush)
- Read (marks a memory reference read as data)

Mark selections for a 32-bit bus are as follows:

```
OPCODE       Anything
OPCODE       OPCODE
OPCODE       Flush
Flush        Flush
Flush        OPCODE
Read         Read
Extension    Extension
Extension    OPCODE
Extension    Flush
```

Mark selections for an 8-bit and 16-bit bus are as follows:

```
OPCODE
Extension
Read
Flush

Undo marks on this cycle
```

You can also use the Mark Opcode function to specify the default segment size mode (16-bit or 32-bit) for the cycle. The segment size selection changes the cycle the cursor is on and the remaining cycles to the end of memory or to the next mark.

Information on basic operations contains more details on marking cycles.

Interrupt Vectors

The disassembler can display 68030 exception vectors.

You can relocate the table by entering the starting address in the Vector Base Register. The Vector Base Register field provides the disassembler with the offset address: enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception table. The Vector Table Size field lets you specify a three-digit hexadecimal size for the table.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Information on basic operations tells you where you can make optional display selections for the acquisition module.

Interrupt cycle types are computed and cannot be used to control triggering. When the 68030 microprocessor processes an interrupt, the disassembler displays the type of interrupt, if known.

Table 2–5 lists the 68030 interrupt vectors.

Table 2–5: Interrupt vectors

Exception number	Location in IV* table (in hexadecimal)	Displayed interrupt name
0	0000	RESET: STACK POINTER
1	0004	RESET: PROGRAM COUNTER
2	0008	BUS ERROR VECTOR
3	000C	ADDRESS ERROR VECTOR
4	0010	ILLEGAL INSTRUCTION VECTOR
5	0014	ZERO DIVIDE VECTOR
6	0018	CHK, CHK2 INSTR VECTOR
7	001C	TRAPcc, TRAPV VECTOR
8	0020	PRIV VIOLATION VECTOR
9	0024	TRACE VECTOR
10	0028	LINE 1010 EMULATOR VECTOR
11	002C	LINE 1111 EMULATOR VECTOR
12	0030	RESERVED VECTOR #12t
13	0034	COP PROT VIOLATION VECTOR
14	0038	FORMAT ERROR VECTOR
15	003C	UNINIT INTERRUPT VECTOR
16–23	0040–0060	RESERVED VECTOR #16t – #23t
24	0060	SPURIOUS INTERRUPT VECTOR
25	0064	IPL 1 AUTOVECTOR
26	0068	IPL 2 AUTOVECTOR
27	006C	IPL 3 AUTOVECTOR
28	0070	IPL 4 AUTOVECTOR
29	0074	IPL 5 AUTOVECTOR
30	0078	IPL 6 AUTOVECTOR
31	007C	IPL 7 AUTOVECTOR

Table 2–5: Interrupt vectors (cont.)

Exception number	Location in IV* table (in hexadecimal)	Displayed interrupt name
32-47	0080-0BC	TRAP #0t – #15t VECTOR
48	0C0	FPCP UNORDERED COND VECTOR
49	0C4	FPCP INEXACT RESULT VECTOR
50	0C8	FPCP ZERO DIVIDE VECTOR
51	0CC	FPCP UNDERFLOW VECTOR
52	0D0	FPCP OPERAND ERROR VECTOR
53	0D4	FPCP OVERFLOW VECTOR
54	0D8	FPCP SIGNALING NAN VECTOR
55	0DC	RESERVED VECTOR #55t
56	0E0	MMU CONFIGURATION ERROR VECTOR
57–63	0E4–0FC	RESERVED VECTOR #57t – #63t
64–255	100–3FC	USER INT VECTOR #64t – #255t

*** IV means interrupt vector.**

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your 68030 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use. You can view the system file without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires 68030 signals
- List of other accessible 68030 signals and extra acquisition channels

Probe Adapter Description

The probe adapter is a nonintrusive piece of hardware that allows the logic analyzer to acquire data from a 68030 microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a 68030 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

The 68030 PGA probe adapter accommodates the Motorola 68030 and 68EC030 microprocessors in a 128-pin PGA package. The 68030 CQFP probe adapter accommodates the 68030 microprocessor in a 132–pin CQFP package.

Configuring the Probe Adapter

Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled. The probe adapter contains CDIS jumper J190 (J1601 for the CQFP adapter) which you can use to disable the 68030 cache.

With the Cache jumper in the CACHE EN position, the SUT controls the cache and the CDIS~ signal is not affected.

With the Cache jumper in the CACHE OFF position, the CDIS~ signal connects to a 332 Ω pull-down resistor on the probe adapter which disables the cache. For the PGA probe adapter, you should also cut or remove pin H12 from the protective socket on the underside of the probe adapter to prevent contention with the driving signal. For the CQFP probe adapter, you should disable any devices on the SUT that drive the CDIS~ signal to prevent contention with the driving signal.

Table 3–1 shows the jumper positions.

Table 3–1: Jumper positions

Jumper	Positions
PGA (J190)	1–2 (CACHE EN) 2–3 (CACHE OFF)
CQFP (J1601)	1–2 (CACHE EN) 2–3 (CACHE OFF)

Figure 1–1 and 1–2 show the jumper locations on the probe adapters.

Specifications

These specifications are for a probe adapter connected to a compatible Tektronix logic analyzer, and the SUT. Table 3–2 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–2, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–2: Electrical specifications

Characteristics	Requirements
SUT DC power requirements	
Voltage	4.75-5.25 VDC
Current	I max (calculated) 87 mA I typ (measured) 56 mA
SUT clock	
Clock Rate	Min. 12.5 MHz Max. 40 MHz (68EC030) 50 MHz (68030)
Minimum setup time required*	
Data, STERM~, ECS~	4 ns

Table 3–2: Electrical specifications (Cont.)

Characteristics	Requirements	
AS~	5 ns	
All other signals	4 ns	
Minimum hold time required*		
Data, STERM~, ECS~	3 ns	
AS~	2 ns	
All other signals	3 ns	
	Specification	
	AC load	DC load
Measured typical SUT signal loading		
Address	7 pF + 1 podlet	1 podlet
Data	6 pF + 1 podlet	1 podlet
CLK	13 pF + 1 podlet	(1) 74As1004 + (1) 74F5074 in parallel with 1 podlet
ECS~, STERM~	11 pF + 1 podlet	(1) 74F5074 in parallel with 1 podlet
AS~	7 pF	(1) 74AS1004
CBREQ~	12 pF + 1 podlet	(1) 74AS1004
RESET~	16 pF + 1 podlet	1 podlet
CDIS~	13 pF + 1 podlet	1 podlet
Other Signals	10 pF + 1 podlet	1 podlet

*** Signal setup and hold times are in relation to the falling edge of CLK.**

Table 3–3 shows the environmental specifications.

Table 3–3: Environmental specification

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)*
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity†

Table 3–3: Environmental specification (cont.)

Characteristic	Description
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic Immunity	The probe adapter is static sensitive

*** Not to exceed 68030 thermal considerations. Forced air cooling may be required across the CPU.**

† **Designed to meet Tektronix standard 062-2847-00 class 5.**

Table 3–4 shows the certifications and compliances that apply to the probe adapter.

Table 3–4: Certifications and compliances

EC Compliance	There is no current European Directives that apply to this product.
Pollution Degree 2	Do not operate in environments where conductive pollutants might be present.

Figure 3–1 shows the dimensions of the probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

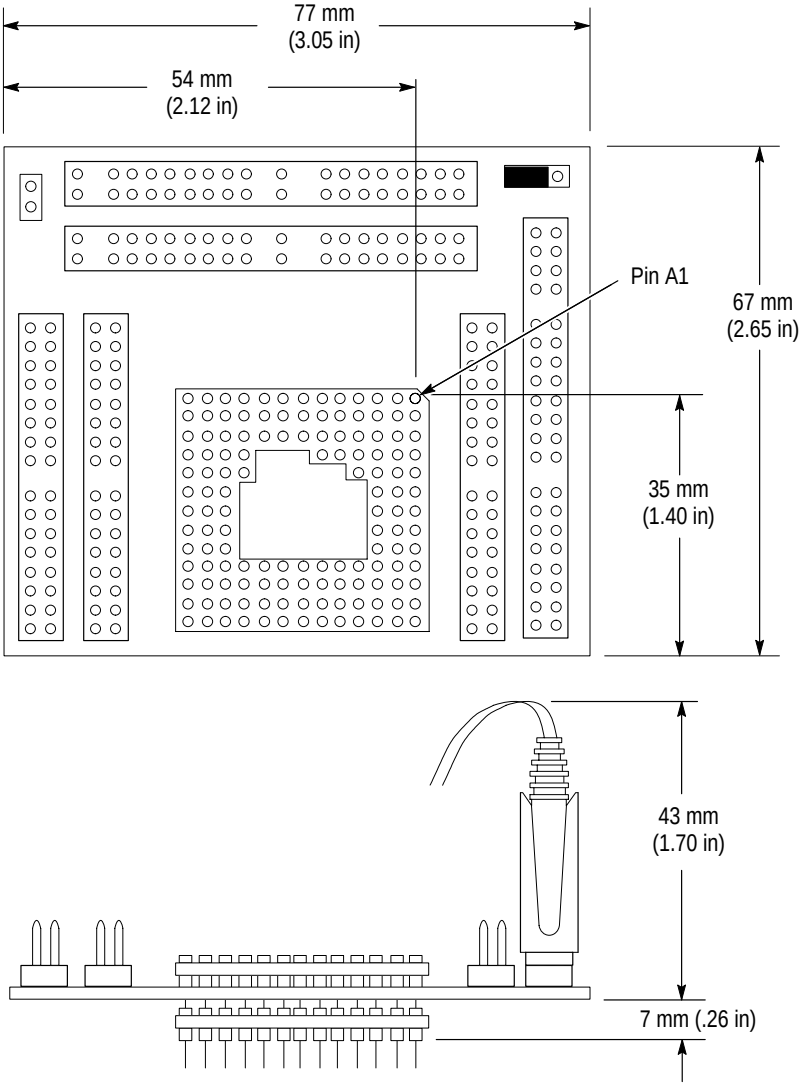


Figure 3–1: Dimensions of the probe adapter

Figure 3–2 shows the dimensions of the probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

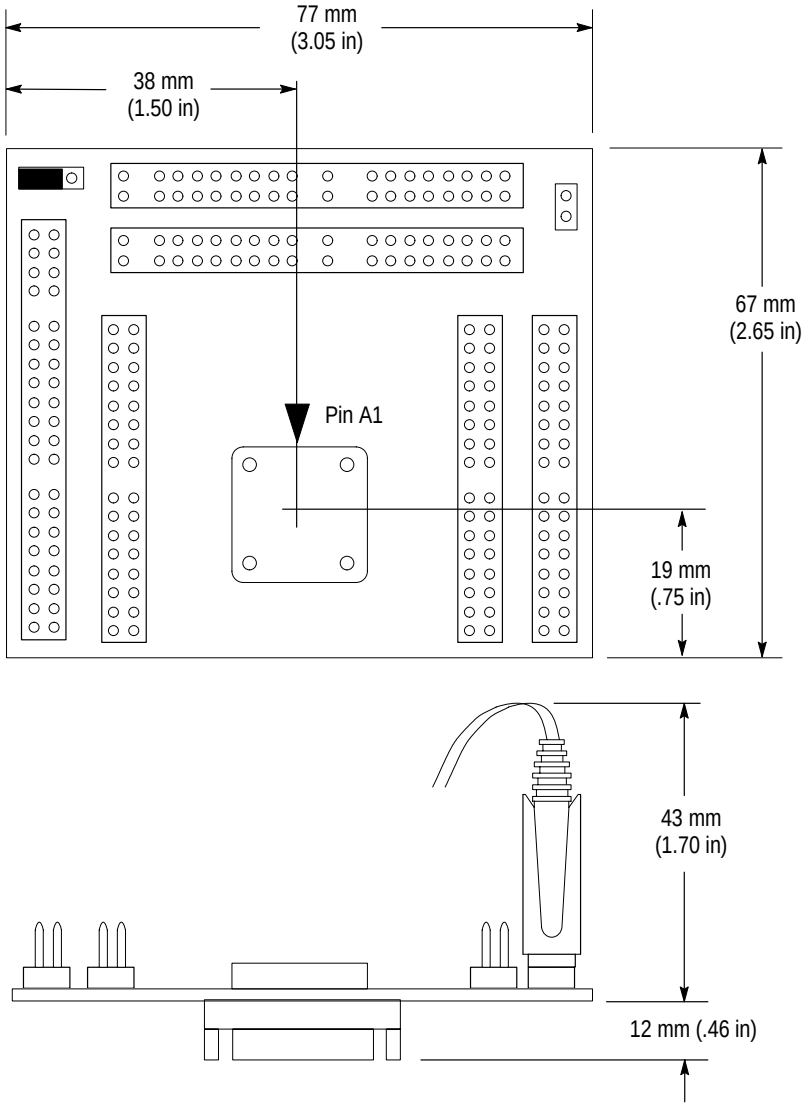


Figure 3–2: Dimensions of the probe adapter

Channel Assignments

Channel assignments shown in Table 3–5 through Table 3–11 use the following conventions:

- All signals are required by the support unless otherwise indicated.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for the 102/136-channel and 96-channel module unless otherwise indicated.
- A tilde (~) following a signal name indicates an active low signal.

Table 3–5 shows the probe section and channel assignments for the Address group, and the microprocessor signal to which each channel connects. By default this channel group is displayed in hexadecimal.

Table 3–5: TMS 203 address group channel assignments

Bit Order	Channel	68030 Signal Name
31	A3:7	A31
30	A3:6	A30
29	A3:5	A29
28	A3:4	A28
27	A3:3	A27
26	A3:2	A26
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10

Table 3–5: TMS 203 address group channel assignments

Bit Order	Channel	68030 Signal Name
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 3–6 shows the probe section and channel assignments for the Data group, and the microprocessor signal to which each channel connects. By default this channel group is displayed in hexadecimal.

Table 3–6: TMS 203 data group channel assignments

Bit Order	Channel	68030 Signal Name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15

Table 3–6: TMS 203 data group channel assignments

Bit Order	Channel	68030 Signal Name
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–7 shows the section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. By default this channel group is displayed symbolically.

Table 3–7: TMS 203 control group channel assignments

Bit Order	Channel	68030 Signal Name
10	C2:3	BGACK~
9	C3:2	FC2
8	C3:6	FC1
7	C3:5	FC0
6	C3:3	RMC~
5	C3:4	AS_B~
4	C2:2	R_W~
3	C2:5	HALT~
2	C2:4	BERR~
1	C2:7	SIZ1
0	C2:6	SIZ0~

Table 3–8 shows the section and channel assignments for the DataSize group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–8: TMS 203 DataSize group channel assignments

Bit Order	Channel	68030 Signal Name
1	C3:1	DSACK1~
0	C3:7	DSACK0~

Table 3–9 shows the section and channel assignments for the Misc group, and the microprocessor signal to which each channel connects. By default this channel group is not visible.

Table 3–9: TMS 203 Misc group channel assignments

Bit Order	Channel	68030 Signal Name
2	C3:0	CLK*
1	C2:1	STERM_L~
0	C2:0	CBACK~*

*** Signals not required for disassembly.**

Table 3–10 shows the section and channel assignments for the Intr group, and the microprocessor signal to which each channel connects. By default this channel group is displayed symbolically.

Table 3–10: TMS 203 Intr group channel assignments

Bit Order	Channel	68030 Signal Name
2	C1:6	IPL2~*
1	C1:2	IPL1~*
0	C0:6	IPL0~*

*** Signals not required for disassembly.**

Table 3–11 shows the acquisition probe section and channel assignments for the clock probes (not part of any group), and the 68030 signal to which each channel connects.

Table 3–11: TMS 203 clock channel assignments

Channel	68030 Signal Name
CK:3	CBREQ_B
CK:2	AS_B
CK:1	CLK_B~

These channels are used only to clock in data, they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–11, you must connect another channel probe to the signal. This technique is called double probing. An equals sign (=) following a signal name indicates that it is already doubled probed.

How Data is Acquired

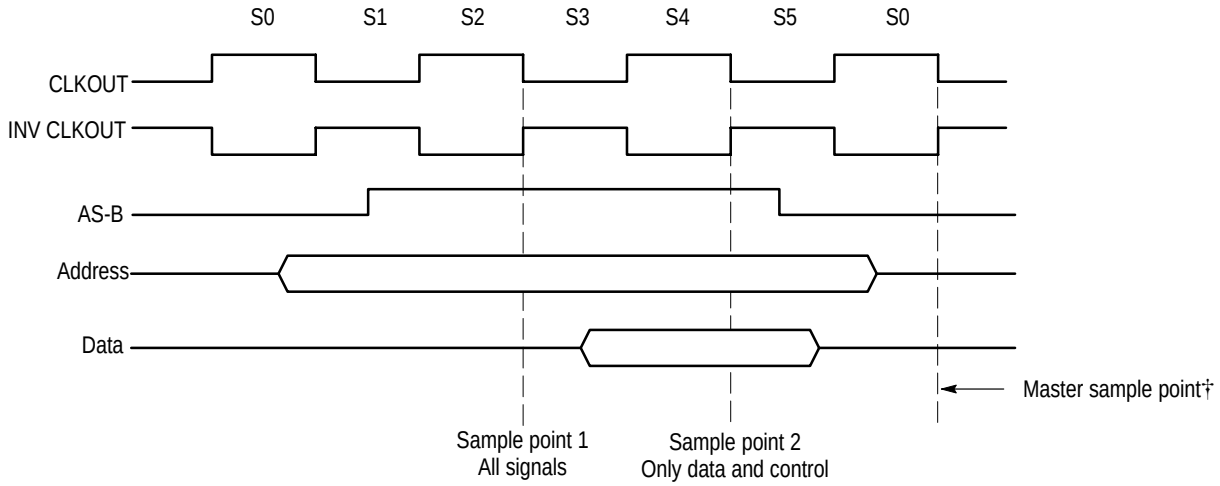
This part of this chapter explains how the module acquires 68030 signals using the TMS 203 support and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the 68030 support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the 68030 bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

Figure 3–3 shows the sample points and the master samples for a normal Read/Write (R/W) cycle.



†Channels not set up in a channel group by the TMS 203 software are logged with the Master sample.

Figure 3–3: 68030 bus timing for a normal Read/Write cycle

Clocking Options

The clocking algorithm for the 68030 microprocessor has two variations: DMA Cycles Excluded, and DMA Cycles Included.

DMA Cycles Excluded. DMA cycles are not logged in.

DMA Cycles Included. All bus cycles, including DMA cycles and backoff cycles, are logged in. If BGACK~ is true, the bus cycle will be considered a DMA cycle. To log in these cycles, the DS~ or AS_B signals must also be active true.

When the BGACK~ signal is low, the 68030 microprocessor has given up the bus to an alternate device. The design of the 68030 system affects what data is logged in. The 92C96 only samples the data at the pins of the 68030 microprocessor. To properly log in bus activity, any buffers between the 68030 microprocessor and the DMA must be enabled and pointing at the 68030 microprocessor.

There are three possible 68030 system designs and clocking interactions when a DMA has control of the bus. The three different possibilities are listed below:

- If the DMA drives the same control lines as the 68030 microprocessor, and the 68030 microprocessor “sees” these signals, the bus activity is logged in like normal bus cycles except that the BGACK~ signal is low.

- If none of the control lines are driven or if the 68030 microprocessor can not see them, the 68030 will still clock in a DMA cycle. The information on the bus, one clock prior to the BGACK~ signal going high, is logged in.
- If some of the 68030 microprocessor control lines are visible (but not all), the 68030 logs in what it determines is valid from the control signals and logs in the remaining bus signals one clock cycle prior to the BGACK~ signal going high.

Alternate Microprocessor Connections

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–7. Remember that these channels are already included in a channel group. If you connect these channels to other signals, you should set up another channel group for them.

Signals On the Probe Adapter

The probe adapter board contains pins for microprocessor signals that are not acquired by the TMS 203 support. You can connect extra channels to these pins, because they can be useful for general purpose analysis.

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

Table 3–12 shows the microprocessor signals available on J670 of the probe adapter.

Table 3–12 shows the microprocessor signals available on AUX.

Table 3–12: 68030 signals on AUX

Pin No.	Signal Name
8	OCS~
6	CIOUT~
4	CDIS~
2	MMUDIS

Table 3–13 shows the microprocessor signals available on the C0 and C1 8-channel probe pins on the probe adapter.

Table 3–13: 68030 signals on C0 and C1

C0 Pin number	Signal name	C1 Pin number	Signal name
C0:7	STATUS~	C1:7	REFILL~
C0:5	BR~	C1:5	AVEC~
C0:4	DS~	C1:4	RESET~
C0:3	CBREQ~	C1:3	CIIN~
C0:2	IPEND~	C1:1	DBEN~
C0:1	BG~	C1:0	ECS~
C0:0	STERM~		

Extra Channels

Table 3–14 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Table 3–14: Extra module sections and channels

Module	Section: channels
102-channels	C1:7-0, 5-3,1-0, C1:7, 5-3, 1-0, C0:7, 5-0
136-channels	E3:7-0, E2:7-0, E1:7-0, E0:7-0
96-channels	E3:7-0, E2:7-0, E1:7-0, E0:7-0

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This section contains information on the following topics:

- Probe adapter circuit description
- How to replace a fuse

Probe Adapter Circuit Description

On the probe adapters, STERM~ is latched by a 74F5074 on the rising clock and then is held for one complete clock cycle. The negative edge of this clock cycle logs the latched STERM~ into the logic analyzer.

AS~ is double-inverted for data. This ensures adequate AS hold time.

AS~ is single-inverted for clocking purposes. This decreases the AS~ hold time.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 203 68030 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

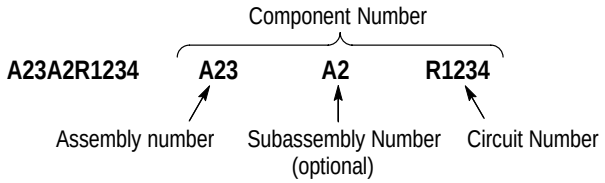
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2058	TDK CORPORATION OF AMERICA	1600 FEEHANVILLE DRIVE	MOUNT PROSPECT, IL 60056
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPY PO BOX 655303	DALLAS TX 75262–5303
1CH66	PHILIPS SEMICONDUCTORS	811 E ARQUES AVENUE PO BOX 3409	SUNNYVALE CA 94088–3409
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656–4548
5Y400	TRIAX METAL PRODUCTS INC DIV OF BEAVERTON PARTS MFG CO	1800 NW 216TH AVE	HILLSBORO OR 97124–6629
50139	ALLEN–BRADLEY CO ELECTRONIC COMPONENTS	1414 ALLEN BRADLEY DR	EL PASO TX 79936
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	010–0597–00			PROBE ADAPTER:80960JX,PGA–132,SOCKETED,32/92DM18	80009	010–0597–00
A01	671–3800–00			CIRCUIT BR ASSY:80960JX,PGA–132, SOCKETED,389–2212–00 WIRED, 32/92DM18	80009	671–3800–00
A01	671–2323–00			CIRCUIT BD ASSY:68030/68EC030,PROBE ADAPTER;	80009	671232300
A02	671–2509–00			CIRCUIT BD ASSY:68030,CQFP132,SOLDERED PROBE ADAPTER;	80009	671250900
A01	671–2323–00			CIRCUIT BD ASSY:68030/68EC030,PROBE ADAPTER;	80009	671232300
A01C300	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A01C420	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A01C440	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A01C460	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A01C640	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A01C740	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A01C750	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A01J100	————————			CONN,HDR:PCB,;MALE,STR,1 X 2,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD,TUBE,HIGH TEMP (SEE RMPL)		
A01J140	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J180	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		

A01J190	————————	CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION (SEE RMPL)		
A01J240	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J280	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J390	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J400	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J410	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J680	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J690	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J700	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J710	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J980	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A01J990		(SEE RMPL)		
A01R290	321–5012–00	RES,FXD:THICK FILM;332 OHM,1%,0.125W,TC=100	50139	BCK3320FT
A01U430	156–5908–00	IC,DIGITAL:FTTL,FLIP FLOP;DUAL D–TYPE, META STABLE IMMUNITY	1CH66	N74F5074D
A01U450	156–5178–00	IC,DIGITAL:ASTTL,GATE;HEX INV DRIVER	01295	SN74AS1004AD
A01U460	156–5908–00	IC,DIGITAL:FTTL,FLIP FLOP;DUAL D–TYPE, META STABLE IMMUNITY	1CH66	N74F5074D
A01U560	————————	SKT,PL–IN ELEK:13 X 13 MATRIX,128 PGA,0.275 (SEE RMPL)		
A01U560	136–1156–01	SOCKET,PGA:PCB,;124 POS,13 X 13,0.1 X0.1 CT R,0.17 H X 0.17 TAIL,GOLD,PAT1308	63058	PGA 63150–011
A02	671–2509–00	CIRCUIT BD ASSY:68030,CQFP132,SOLDERED PROBE ADAPTER;	80009	671250900
A02C1701	283–5004–00	CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A02C1702	283–5004–00	CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A02C1703	283–5004–00	CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A02C1711	283–5004–00	CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A02C1712	283–5004–00	CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A02C1801	283–5004–00	CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A02C1811	283–5004–00	CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A02J1601	131–4530–00	CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A02J1602	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A02J1611	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		

A02J1701	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A02J1702	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A02J1703	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A02J1704	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A02J1711	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A02J1712	131–4917–00	CONN,HDR:PCB,;MALE,STR,1 X 2,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD,TUBE,HIGH TEMP	00779	104714–3
A02J1801	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A02J1802	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A02J1811	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A02J1812	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A02J1813	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A02J1814	————————	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL)		
A02P1601	131–4356–00	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1	26742	9618–302–50
A02P2881	————————	CLIP,ELECTRICAL:ASSEMBLY,PQFP132 (NOT REPLACEABLE ORDER BY DESCBE,HIGH TEMP		
A02P2881	————————	PLATE,CMPNT MTG:SOCKET,ALUMINUM		
A02R1701	321–5012–00	RES,FXD:THICK FILM;332 OHM,1%,0.125W,TC=100	50139	BCK3320FT
A02U1701	156–5908–00	IC,DIGITAL:FTTL,FLIP FLOP;DUAL D–TYPE, METASTABLE IMMUNITY	1CH66	N74F5074D
A02U1711	156–5908–00	IC,DIGITAL:FTTL,FLIP FLOP;DUAL D–TYPE, META STABLE IMMUNITY	1CH66	N74F5074D
A02U1712	156–5178–00	IC,DIGITAL:ASTTL,GATE;HEX INV DRIVER	01295	SN74AS1004AD

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 203 68030 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2508	RICHEYCYPRESS ELECTRONICS INC	830 INDUSTRY DRIVE	SEATTLE, WA 98188
TK2548	XEROX BUSINESS SERVICES DIV OF XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON OR 97077
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656–4548
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0528–00			1	PROBE ADAPTER:68030/68EC030,PGA128 SOCKETED	80009	010052800
–1	131–4530–00			1	CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION (J190)	00779	104344–1
–2	131–4356–00			1	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR, 0.63 H,BLK,W/HANDLE,JUMPER (P190)	26742	9618–302–50
–3	131–5267–00			3	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J140,J180,J240,J280,J390,J400,J410,J680,J690,J700,J980, J990)	53387	2480–6122–TB
–4	671–2323–00			1	CIRCUIT BD ASSY:68030/68EC030,PROBE ADAPTER	80009	671232300
–5	136–1014–00			2	SKT,PL–IN ELEK:13 X 13 MATRIX,128 PGA,0.275LG LEAD (U560 68030)	63058	PGA128H115B113B
	136–1156–01			2	SOCKET,PGA:PCB,;124 POS,13 X 13,0.1 X0.1 CTR,0.17 H X 0.17 TAIL,GOLD,PAT1308 (U560 68EC030)	63058	PGA 63150–011
–6	131–4917–00			1	CONN,HDR:PCB,;MALE,STR,1 X 2,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD,TUBE,HIGH TEMP (J100)	00779	104714–3
					STANDARD ACCESSORIES		
	070–9821–00			1	MANUAL,TECH:INSTRUCTION,68030,DISSASEMBLER, TMS 203	80009	070–9821–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00
	161–0104–06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, EUROPEAN,SAFETY CONTROLLED (OPT A1)	S3109	ORDER BY DESCRIPTION
	161–0104–07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10AMP,2.5 METER, RTANG,IEC320,RCPT X 13A, FUSED, UK PLUG, (13A FUSE), UNITED KINGDOM,SAFETY CONTROL (OPT A2)	S3109	ORDER BY DESCRIPTION
	161–0104–05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, AUSTRALIA,SAFETY CONTROLLED (OPT A3)	S3109	ORDER BY DESCRIPTION
	161–0167–00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, SWISS,NO CORD GRIP, SAFETY CONTROLLED (OPT A5)	S3109	ORDER BY DESCRIPTION

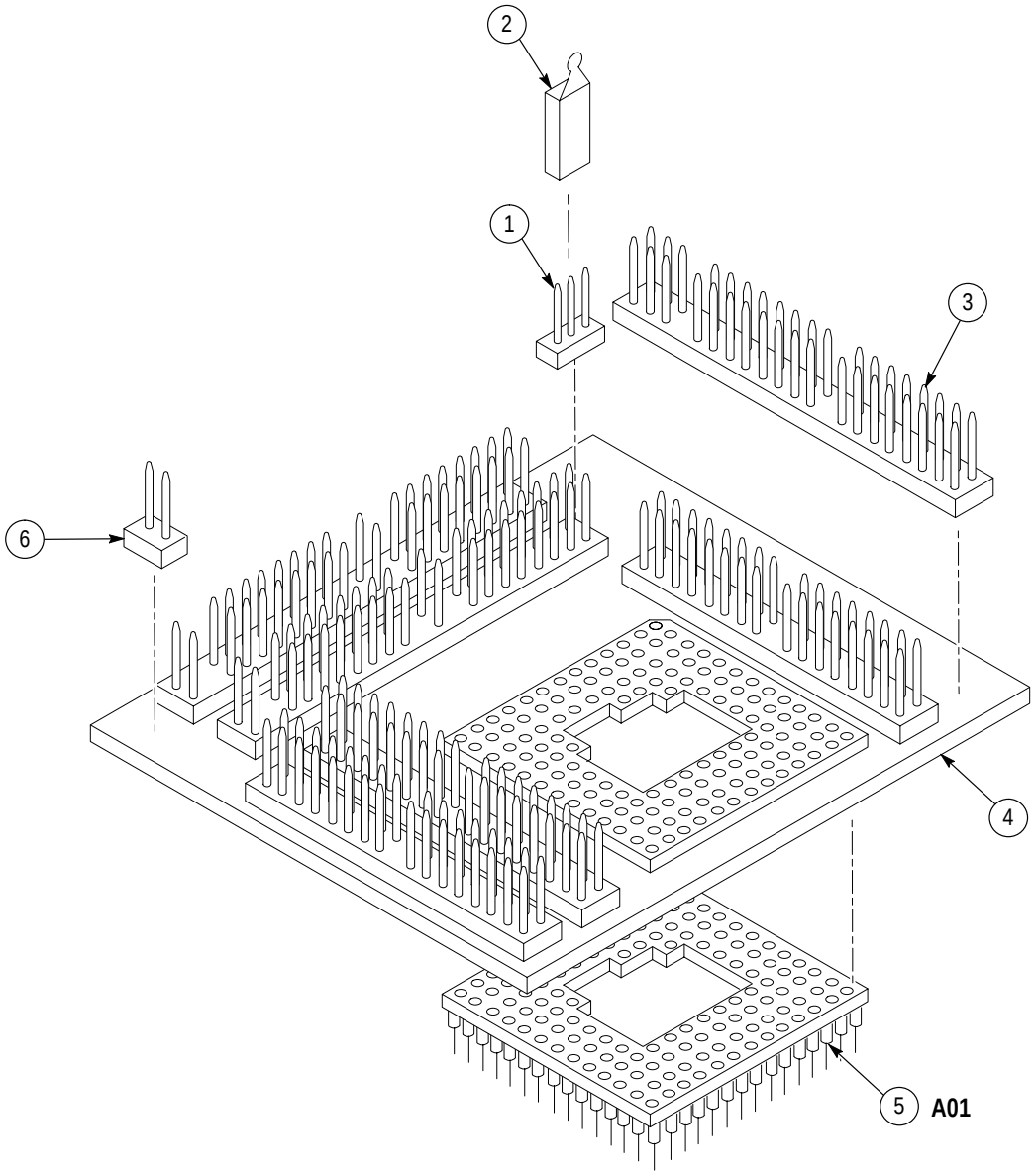


Figure 1: 68030 PGA probe adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
2–1	131–4530–00			1	CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION (J1601)	00779	104344–1
–2	131–4356–00			1	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR, 0.63 H,BLK,W/HANDLE,JUMPER (P1601)	26742	9618–302–50
–3	131–4917–00			1	CONN,HDR:PCB,;MALE,STR,1 X 2,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD,TUBE,HIGH TEMP (J1712)	00779	104714–3
–4	131–5267–00			2	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J1602,J1611,J1701,J1702,J1703,J1704,J1711,J1712,J1801, J1802,J1811,J1812,J1812,J1813,J1814)	53387	2480–6122–TB
–5	671–2509–00			1	CIRCUIT BD ASSY:68030,CQFP132,SOLDERED PROBE ADAPTER;	80009	671250900
					STANDARD ACCESSORIES		
	070–9821–00			1	MANUAL,TECH:INSTRUCTION,68030,DISSASEMBLER, TMS 203	80009	070–9821–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
	020–1983–00			1	ACCESSORY PKG:PKG OF 5 CQFP TO PQFP ADAPTER WITH INSTRUCTION SHEET	TK2508	ORDER BY DESC

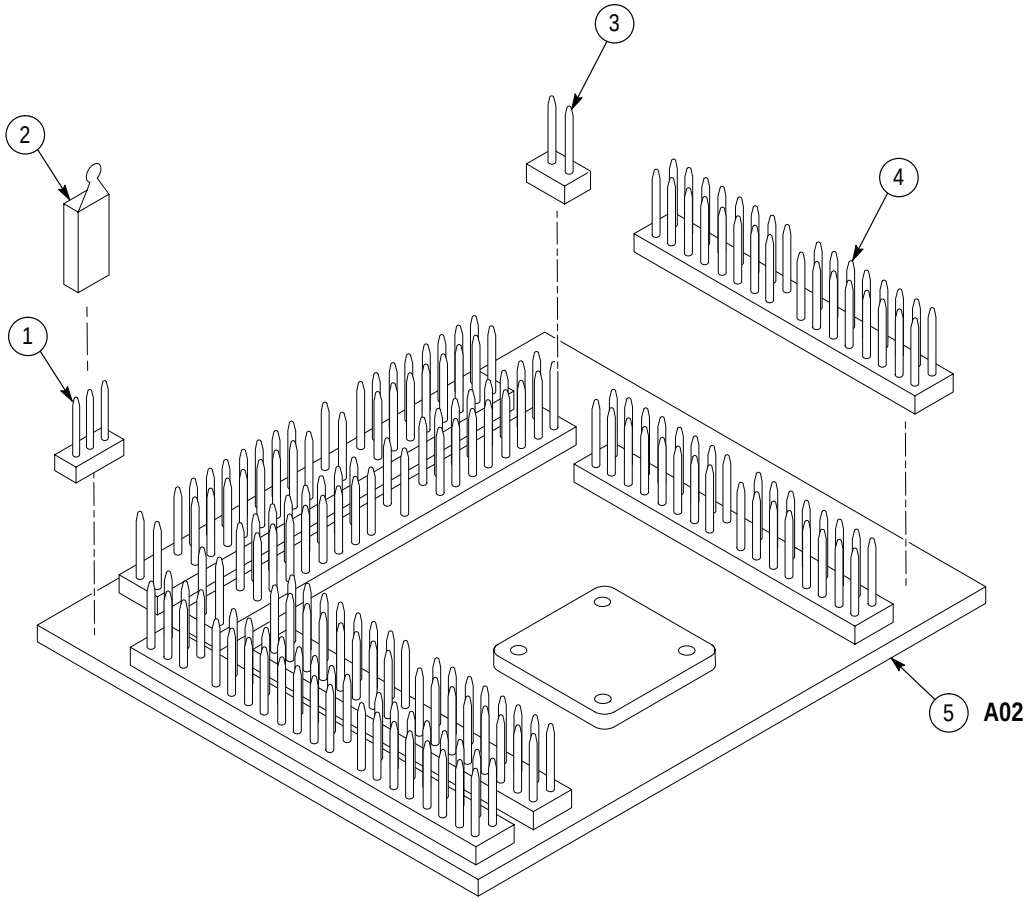


Figure 2: 68030 CQFP probe adapter exploded view

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