

Instruction Manual



TMS 261 68360 Microprocessor Support 070-9825-01

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning

The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:



WARNING. Warning statements identify conditions or practices that could result in injury or loss of life.



CAUTION. Caution statements identify conditions or practices that could result in damage to this product or other property.

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:



WARNING
High Voltage



Protective Ground
(Earth) Terminal



CAUTION
Refer to Manual



Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 261 68360 microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 261 68360 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names must be replaced with 68360. This is the name of the microprocessor in field selections and file names you must use to operate the 68360 support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 102/136-channel or a 96-channel module.
- 68360 refers to all supported variations of the 68360 microprocessor unless otherwise noted.
- An asterisk (*) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	<p>For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time</p> <p>Or, contact us by e-mail: tm_app_supp@tek.com</p> <p>For product support outside of North America, contact your local Tektronix distributor or sales office.</p>
Service Support	<p>Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations.</p> <p>http://www.tek.com</p>
For other information	<p>In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.</p>
To write us	<p>Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000</p>



Getting Started

Getting Started

This chapter provides information on the following topics and tasks:

- A description of the TMS 261 microprocessor support package
- Logic analyzer software compatibility
- Your system under test requirements
- Support restrictions
- How to configure the probe adapter
- How to connect to the system under test (SUT)
- How to apply power to and remove power from the probe adapter

Support Description

The TMS 261 microprocessor support package disassembles data from systems that are based on the Motorola 68360 microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 261 microprocessor support.

The TMS 261 supports the Motorola 68360 microprocessor in a 241-pin PGA package. Support for the QFP package is also available by purchasing a PGA-to-QFP converter clip from ITT Pomona (part number 5968) and using it with this probe adapter.

The product is intended to be used with the low-profile probe adapter to connect to the SUT. Descriptions of the conventional probe adapter are also included if you purchased an earlier version of the product.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *MC68360 Quad Integrated Communications Controller User's Manual*, Motorola, 1993.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the 68360 support, the Tektronix logic analyzer must be equipped with either a 102/136-channel module, or a 96-channel module at a minimum. The module must be equipped with enough probes to acquire channel and clock data from signals in your 68360-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other 68360 support requirements and restrictions.

System Clock Rate. The TMS 261 support can acquire data from the 68360 microprocessor at speeds of up to 33 MHz¹; it has been tested to 25 MHz.

DSACK Signals. The 68360 microprocessor allows 8-, 16-, and 32-bit data transfers. The DSACK group of signals, which indicate which bytes on the bus are valid, are not always asserted. When the DSACK signals are not asserted, the software disassembles data using the selection in the Int DSACKs Bus Width field. Refer to the *Operating Basics* section for more information on this field.

Valid Address Lines. The address bus is 28- or 32-bits wide. You can select either bus width in the Disassembly Format Definition overlay.

¹ Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.

Configuring the Probe Adapter

There are nine jumpers and one switch bank on the probe adapter. The jumpers and switch descriptions apply to both the low-profile and conventional probe adapters; the circuit numbers may differ, but the functionality is identical unless otherwise indicated.

Memory Size Jumper

If the SUT uses dynamic memory controlled by the 68360 microprocessor, you should place the Memory Size jumper in the position that corresponds to the memory size used. The jumper positions are: 128, 256, or 512 Kbytes, or 1, 2, 4, 8, 16, or 32 Mbytes.

If the SUT does not use dynamic memory, you can place the Memory Size jumper in any position.

You can also place the Memory Size jumper in any position if the RAS/Trans jumper is in the Trans position.

Figure 1–1 shows the location of the Memory Size jumper on the probe adapter.

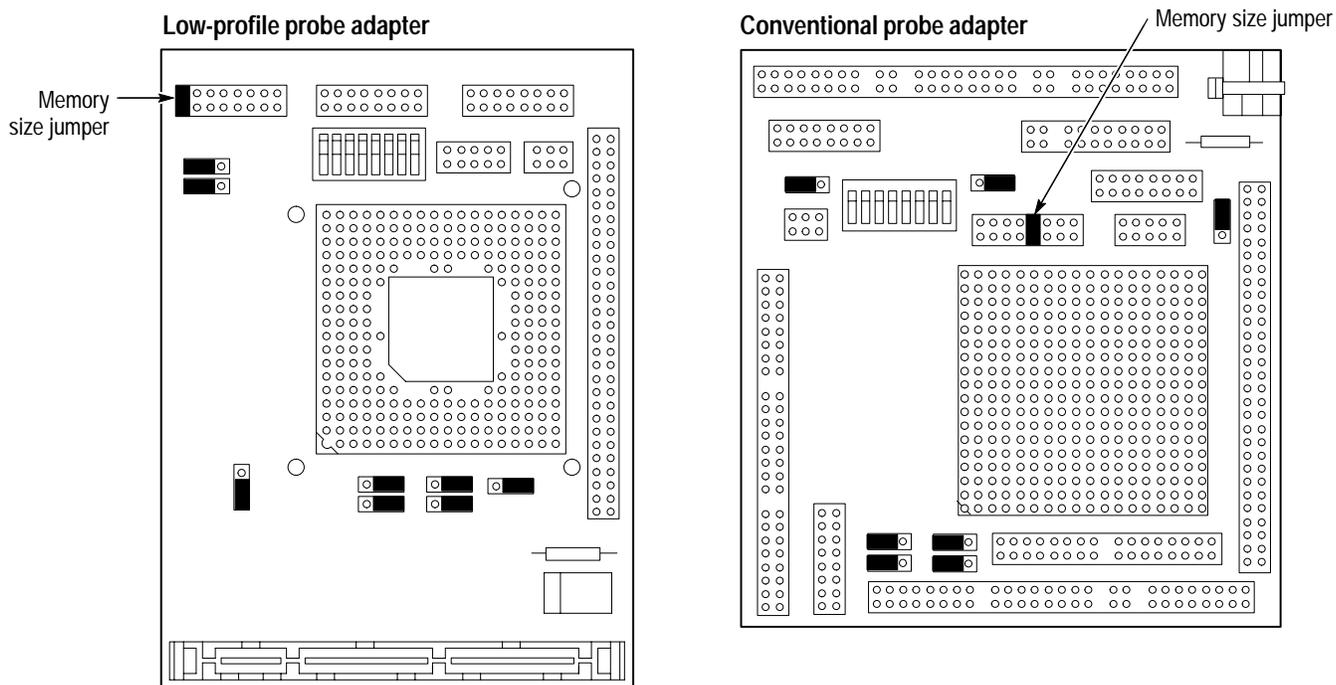


Figure 1–1: Memory Size jumper location

RAS/Trans Jumper

If your SUT does not use dynamic memory, or if you want to acquire data using Internal clocking (asynchronous), you should place the RAS/Trans Jumper in the Trans (transparent) position. This is the default setting.

If your SUT uses dynamic memory, you should place the RAS/Trans jumper in the RAS (row address strobe) position. This causes the probe adapter to rearrange the upper and lower bits of the Address group for disassembly during DRAM accesses.

If you do not know the size of the dynamic memory, or which RAS lines are used, then place the jumper in the Trans position.

NOTE. The RAS position meets Motorola's requirement that the complete address not be on the bus at the end of each RAS/CAS cycle. Observations on a limited set of microprocessors show that the complete address is on the bus at the end of each RAS/CAS cycle. If you find that the microprocessor does not place the complete address on the bus at the end of a RAS/CAS cycle (CAS part), then place the jumper in the RAS position.

Figure 1–2 shows the location of the RAS/Trans jumper.

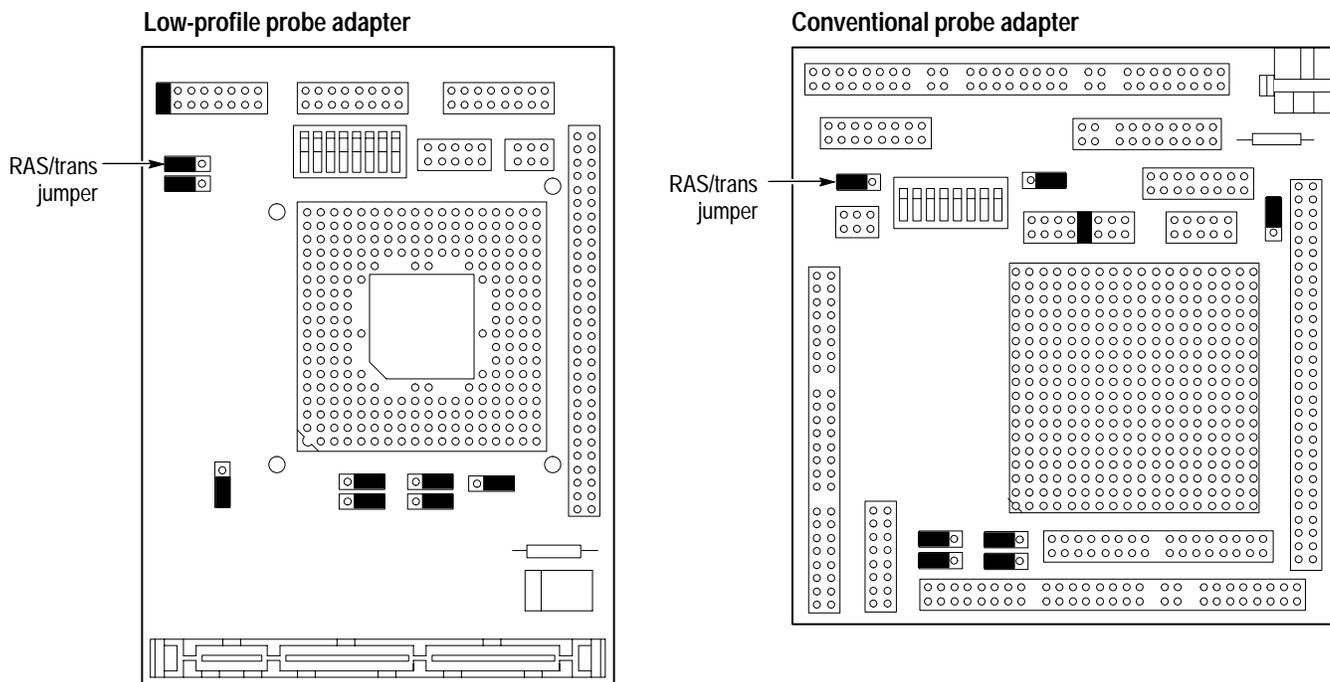


Figure 1-2: RAS/Trans jumper location

68360/68040 Clocking Jumper

If you want to acquire data using standard 68360 signals (such as AS* and DS*), you should place the 68360/68040 Clocking jumper in the 68360 position. This is the default setting.

If you want to acquire data using 68040-type signals (such as TS* and TA*), you should place the jumper in the 68040 position.

Figure 1–3 shows the location of this jumper.

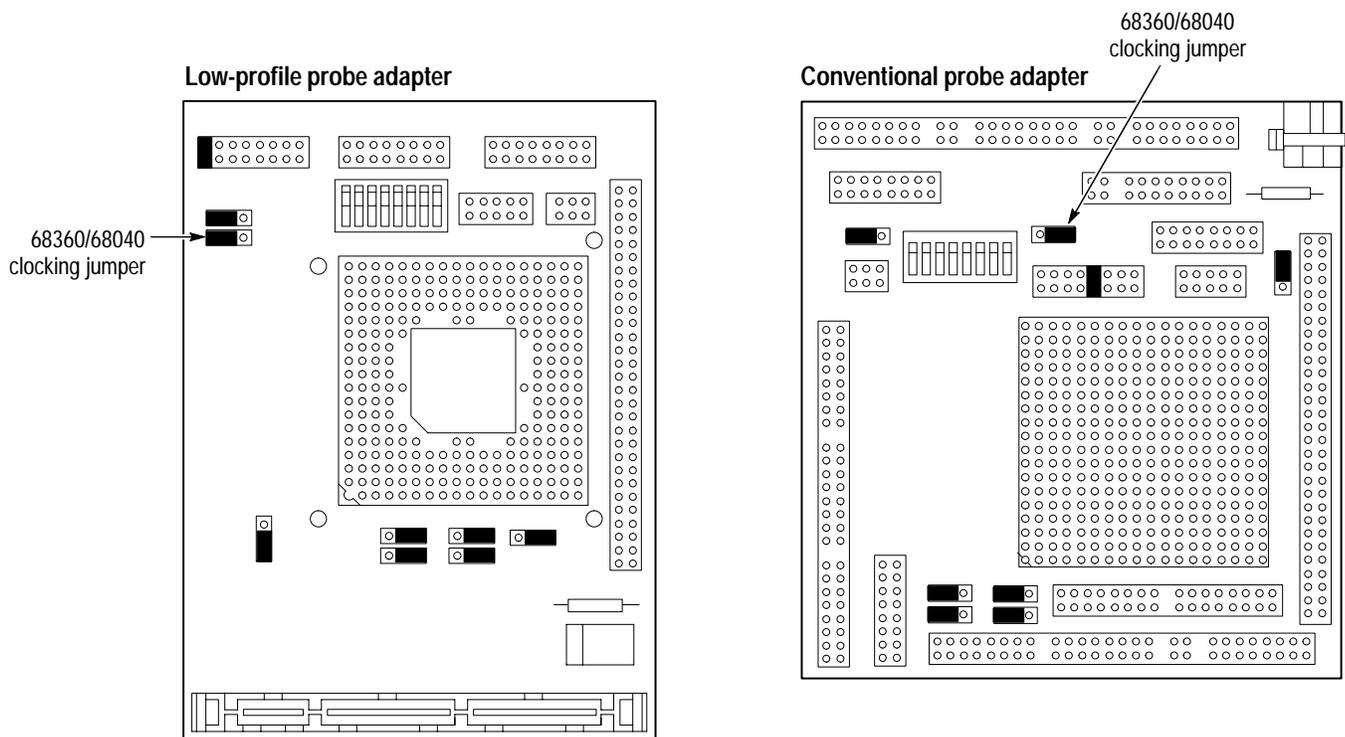


Figure 1–3: 68360/68040 clocking jumper location

CLK01/EXTAL Clock Jumper

Place the clock jumper in the CLK01 position when CLK01 is enabled in the CLKOCR register. Place the jumper in the EXTAL position when the EXTAL signal is driven with the system frequency.

Figure 1–4 shows the location of the CLK01/EXTAL jumper. This jumper is only available on the low-profile probe adapter.

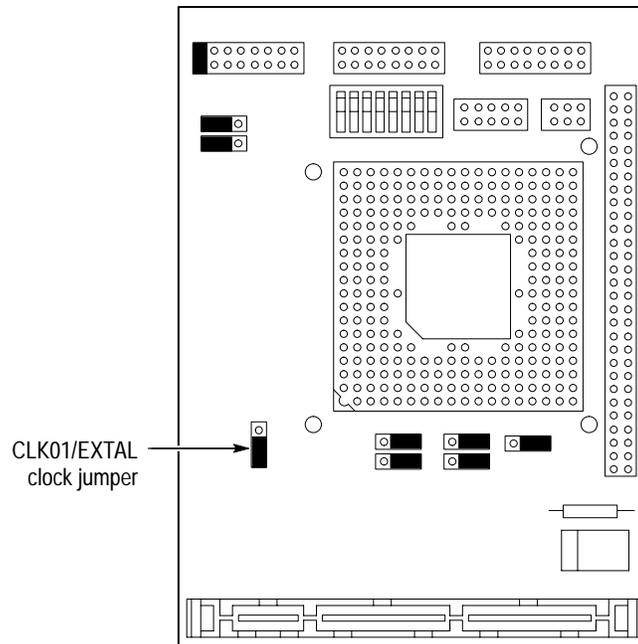


Figure 1–4: CLK01/EXTAL clock jumper location

A31-A28/WE3-WE0 Signal Jumpers

The 68360 microprocessor can be configured to use either the A31-A28 address signals or the WE3-WE0 signals. The probe adapter has four jumpers that you must set to match the configuration of your SUT.

If the SUT is configured to use A31-A28, you should place the jumpers in the A position. With the jumpers in the A position, the WE signals sent to the logic analyzer are held high.

If the SUT is configured to use WE3-WE0, you should place the jumpers in the WE position. With the jumpers in the WE position, the A31-A28 signals sent to the logic analyzer are held low.

Figure 1-5 shows the location of the A31-A28/WE3-WE0 jumpers.

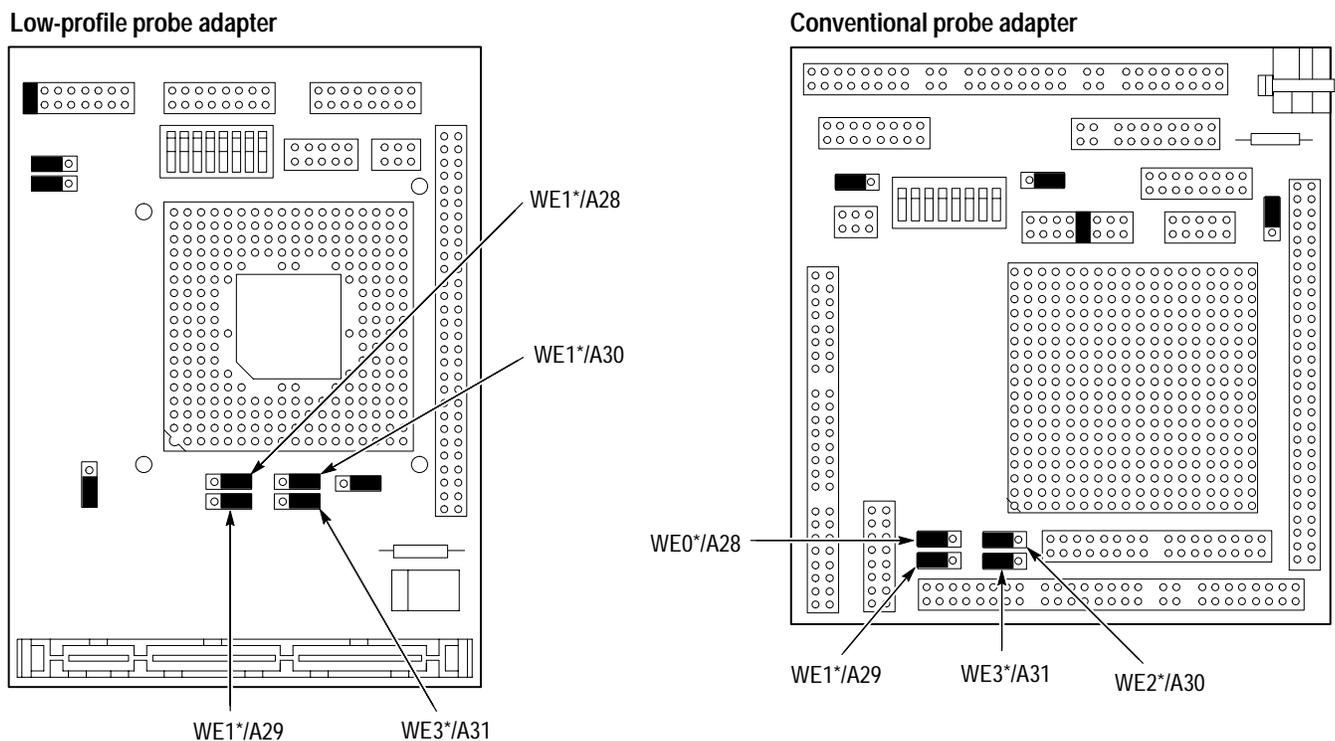


Figure 1-5: A31-A28/WE3-WE0 signal jumpers locations

Power Source Jumper

If your SUT has a +3 V 68360 microprocessor or you do not want your SUT to provide power to the 68360 probe adapter, you can use an alternate power source. If you use an alternate power source, you should set the Power Source jumper to the Ext Pwr position. This is the default setting.

If you do not use an alternate power source, you should set this jumper in the SUT position. In this position, the SUT provides power to the 68360 probe adapter.

For more information on using an alternate power source, refer to *Applying and Removing Power* in this chapter.

Figure 1–6 shows the location of the Power Source jumper.

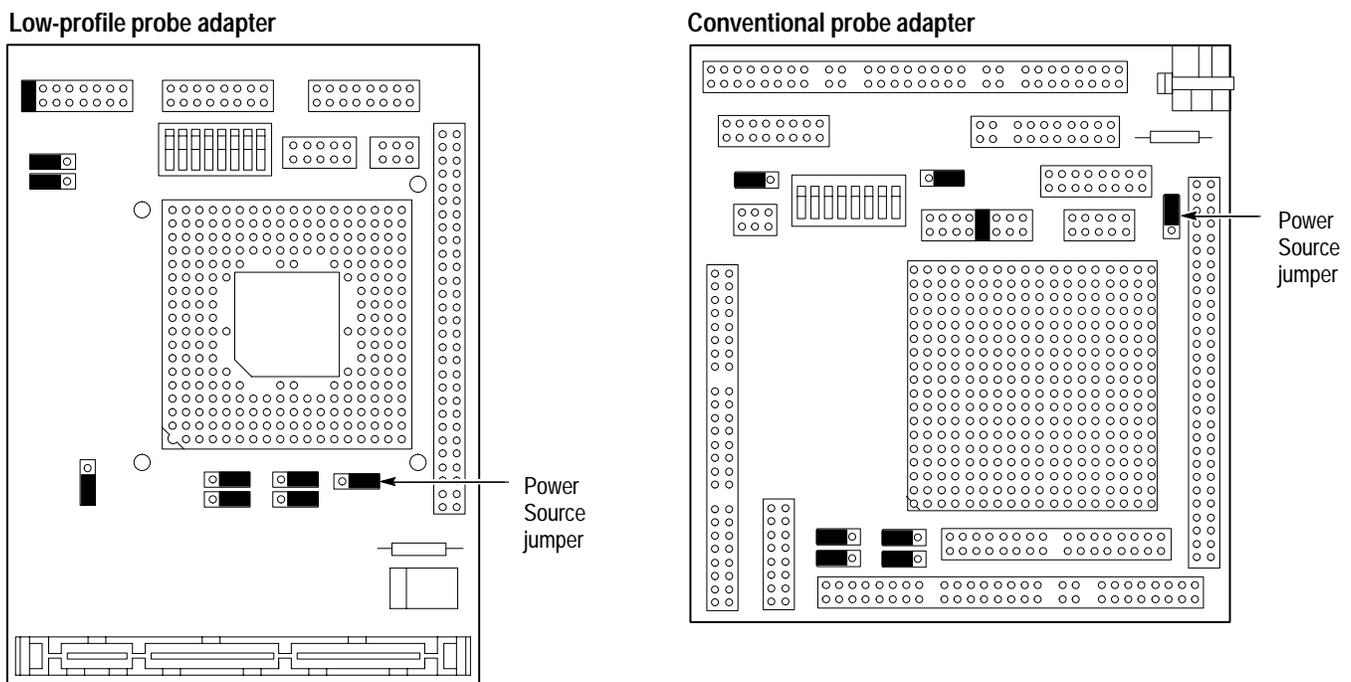


Figure 1–6: Power Source jumper location

CS/RAS Signal Selection Switch Block

The CS/RAS Signal Selection switch block has a switch for each RAS signal that the SUT might use. For each RAS signal used, you should close the corresponding switch on the RAS Signal Selection switch block. If the SUT does not use dynamic memory, you should open all the switches.

If you do not know which RAS lines are used by the SUT, you should open all the switches and place the RAS/Trans jumper in the Trans position.

Table 1–1 shows the switch numbers printed on the switch block and the CS or RAS signal that connects to each switch.

Table 1–1: Switch numbers and CS/RAS signals

Switch number	Signal name
1	CS0*/RAS0*
2	CS1*/RAS1*
3	CS2*/RAS2*
4	CS3*/RAS3*
5	CS4*/RAS4*
6	CS5*/RAS5*
7	CS6*/RAS6*
8	CS7*/RAS7*

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. The probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

Low-Profile Probe Adapter with a High-Density Probe

If a probe adapter has one or two high-density cables (probe adapter does not have pins to which the channel and clock probes connect), the probe adapter requires a high-density probe to make connections between the logic analyzer and a SUT.

To connect the logic analyzer to a SUT using the low-profile probe adapter and a high-density probe, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.



CAUTION. *Static discharge can damage the microprocessor, the low-profile probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and low-profile probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch the black foam on the underside of the probe adapter to discharge stored static electricity from the probe adapter.
3. Remove the microprocessor from the SUT.
4. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.



CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

5. Place the microprocessor into the probe adapter as shown in Figure 1–7.

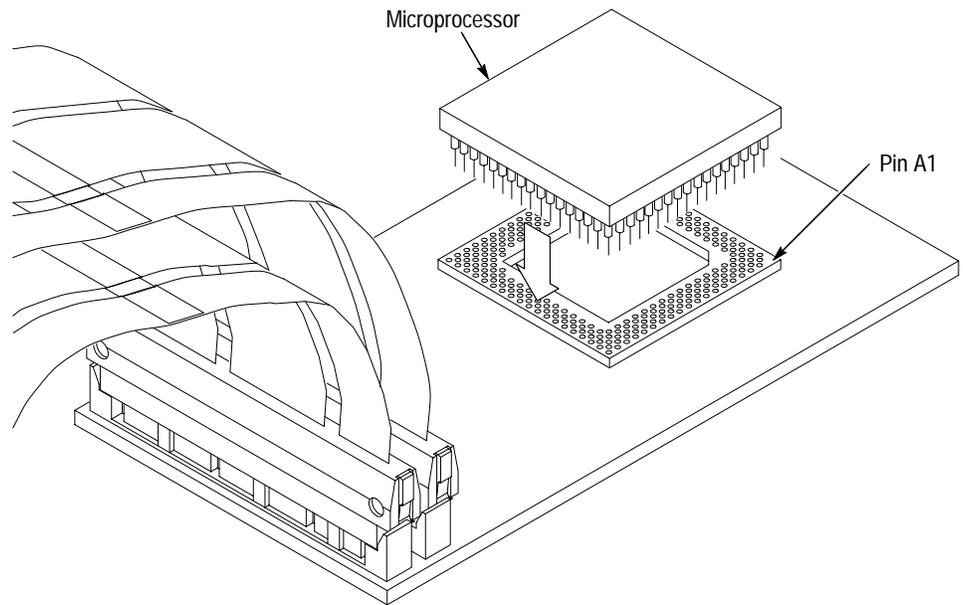


Figure 1-7: Placing a microprocessor into a PGA probe adapter

6. Remove the black foam from the underside of the probe adapter.
7. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the SUT.
8. Place the probe adapter onto the SUT as shown in Figure 1-8.

NOTE. You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind this might increase loading, which can reduce the electrical performance of the probe adapter.

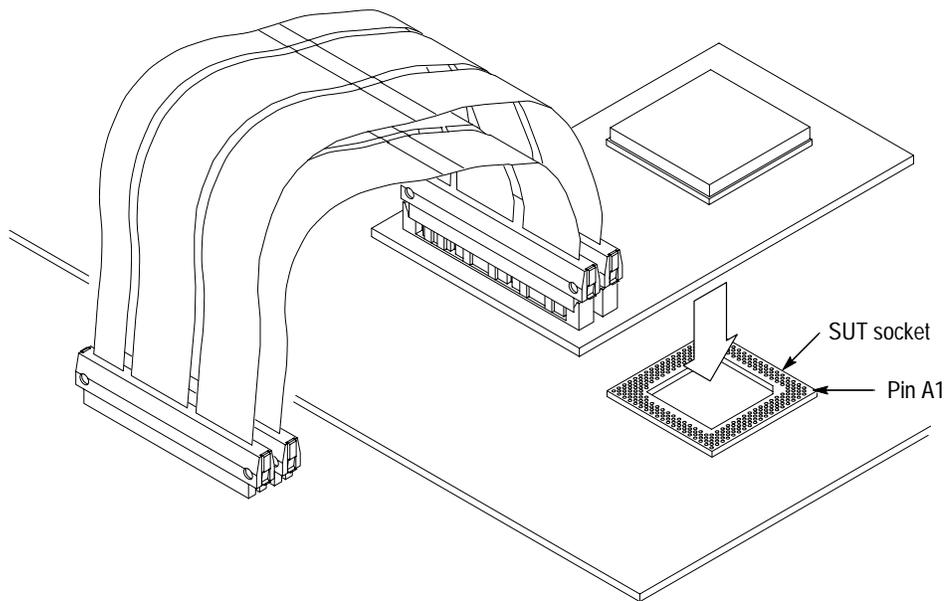


Figure 1-8: Placing a PGA probe adapter onto the SUT

9. Connect the channel and clock probes to the high-density probe as shown in Figure 1-9. Match the channel groups and numbers on the probe labels to the corresponding pins on the high-density probe. Match the ground pins on the probes to the corresponding pins on the probe adapter.

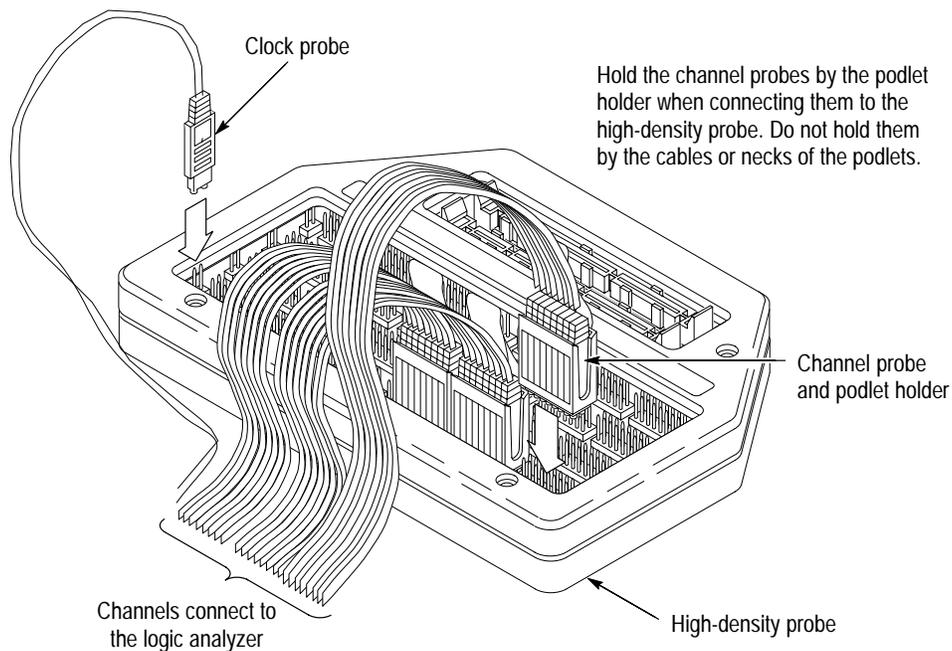


Figure 1-9: Connecting channel and clock probes to a high-density probe

- 10.** Align pin 1 on the LO cable connector, the end on the narrowest cable strip of the cable, with pin 1 on the LO connector on the high-density probe. Connect the cable to the connector as shown in Figure 1-10.

NOTE. The LO cable is 12 inches long; the HI cable is 13 inches long.

- 11.** Align pin 1 on the HI cable connector, the end on the narrowest cable strip of the cable, with pin 1 on the HI connector on the high-density probe. Connect the cable to the connector as shown in Figure 1-10.

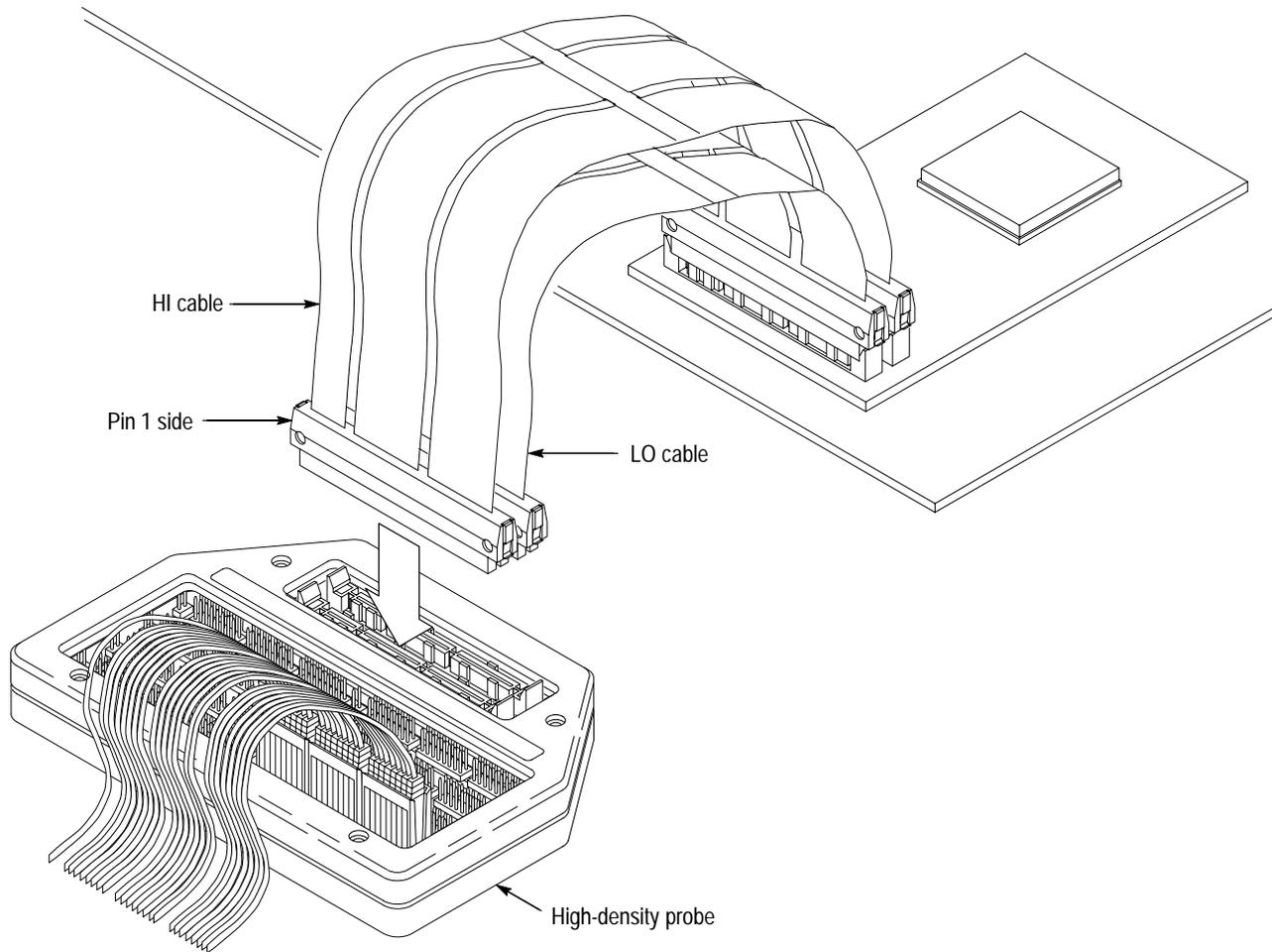


Figure 1-10: Connecting LO and HI cables to a high-density probe

Conventional Probe Adapter

To connect the logic analyzer to a SUT using a conventional probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.



CAUTION. Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–11. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the microprocessor from your SUT.
5. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.



CAUTION. Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.

6. Place the microprocessor into the probe adapter as shown in Figure 1–11.

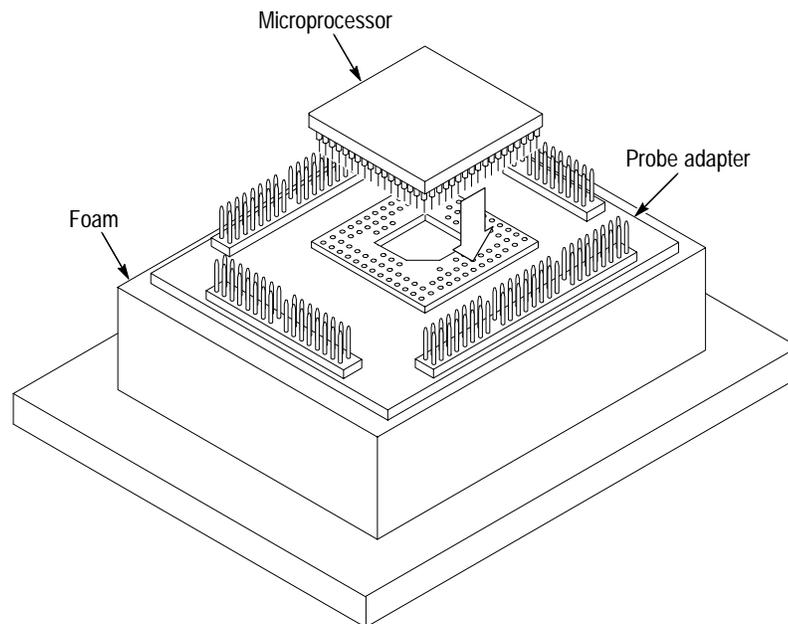


Figure 1–11: Placing a microprocessor into a PGA probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–12. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

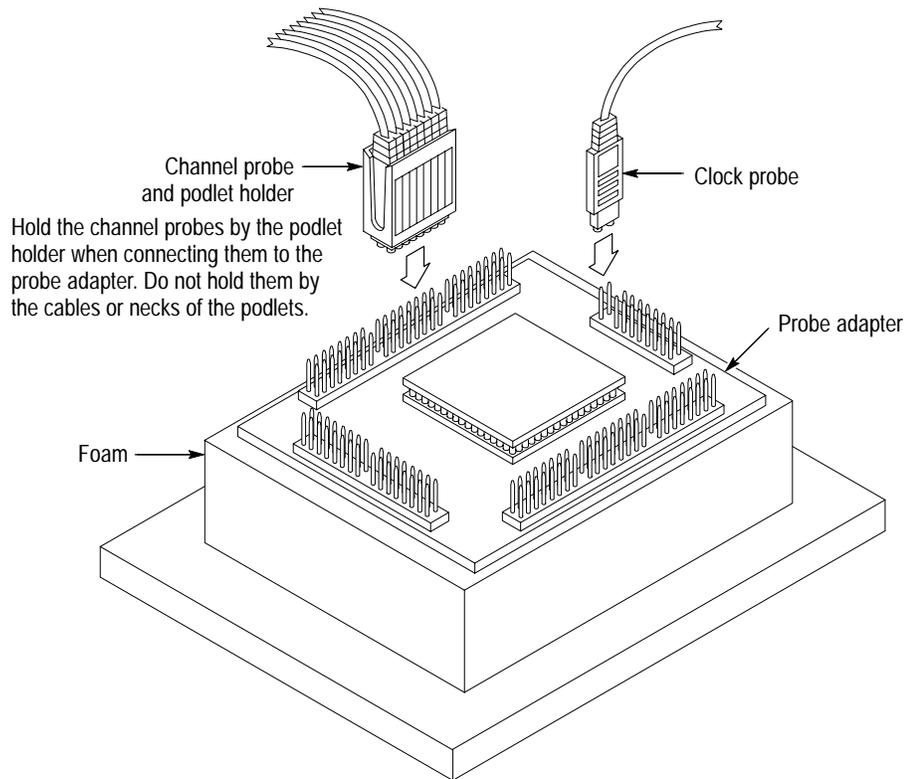


Figure 1-12: Connecting probes to a PGA probe adapter

8. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on your SUT.
9. Place the probe adapter onto the SUT as shown in Figure 1-13.

NOTE. You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.

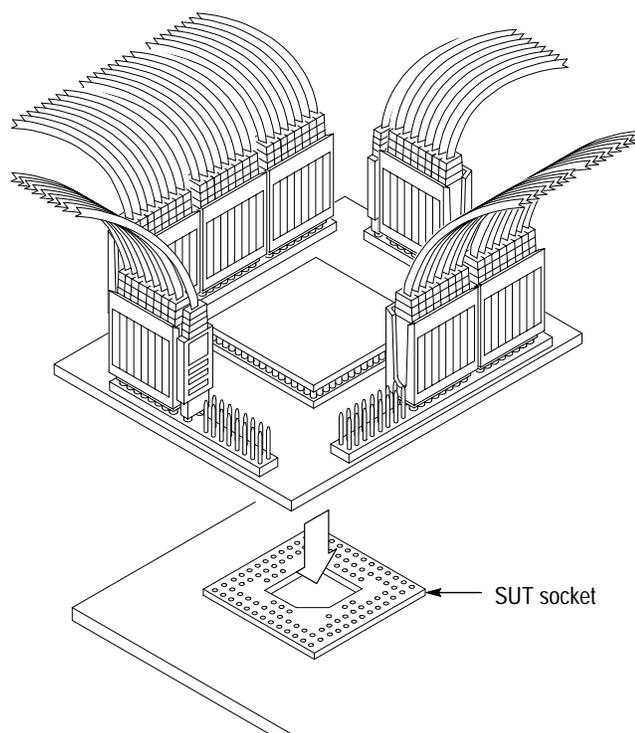


Figure 1-13: Placing a PGA probe adapter onto the SUT

Probe Names Printed on the Conventional Probe Adapter or High-Density Probe

The high-density probe, used with the low-profile probe adapter, has LO_ and HI_ designators. Table 1-2 shows the clock and channel probes you need to connect to the pins with the LO_ or HI_ designators on the conventional probe adapter or the high-density probe.

Table 1-2: Probe connections printed on the conventional probe adapter or high-density probe

Section: channel	Channel or clock probe designator		Section: channel	Channel or clock probe designator	
	High-density probe	Conventional probe adapter		High-density probe	Conventional probe adapter
A3	LO_A3	A3	C3	LO_C3	C3
A2	LO_A2	A2	C2	LO_C2	LO_C2
A1	LO_A1	A1	C1	LO_C1	C1/HI_D1
A0	LO_A0	A0	C0	LO_C0	C0/HI_D0
D3	LO_D3	D3	CK:3	LO_CK3	CK:3
D2	LO_D2	D2	CK:2	LO_CK2	CK:2
D1	LO_D1	D1	CK:1	LO_CK1	CK:1
D0	LO_D0	D0	CK:0	LO_CK0	CK:0

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT. To connect the probes to 68360 signals using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.



CAUTION. Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.
3. Use Table 1–3 to connect the channel probes to 68360 signal pins on the test clip or in the SUT.

Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip (or adapter).

Table 1–3: 68360 signal connections for channel probes

Section:channel	68360 signal	Section:channel	68360 signal
A3:7	A31	D3:7	D31
A3:6	A30	D3:6	D30
A3:5	A29	D3:5	D29
A3:4	A28	D3:4	D28
A3:3	A27	D3:3	D27
A3:2	A26	D3:2	D26
A3:1	A25	D3:1	D25
A3:0	A24	D3:0	D24
A2:7	A23	D2:7	D23
A2:6	A22	D2:6	D22
A2:5	A21	D2:5	D21
A2:4	A20	D2:4	D20
A2:3	A19	D2:3	D19
A2:2	A18	D2:2	D18
A2:1	A17	D2:1	D17

Table 1-3: 68360 signal connections for channel probes (cont.)

Section:channel	68360 signal	Section:channel	68360 signal
A2:0	A16	D2:0	D16
A1:7	A15	D1:7	D15
A1:6	A14	D1:6	D14
A1:5	A13	D1:5	D13
A1:4	A12	D1:4	D12
A1:3	A11	D1:3	D11
A1:2	A10	D1:2	D10
A1:1	A9	D1:1	D9
A1:0	A8	D1:0	D8
A0:7	A7	D0:7	D7
A0:6	A6	D0:6	D6
A0:5	A5	D0:5	D5
A0:4	A4	D0:4	D4
A0:3	A3	D0:3	D3
A0:2	A2	D0:2	D2
A0:1	A1	D0:1	D1
A0:0	A0	D0:0	D0
C3:7	FC0	C2:7	RMC*
C3:6	FC2	C2:6	BG*
C3:5	WE3†	C2:5	BGACK*
C3:4	SIZ1	C2:4	WE0†
C3:3	WE1†	C2:3	RESETH†
C3:2	FC1	C2:2	TA*
C3:1	WE2†	C2:1	DS*
C3:0	SIZ0	C2:0	Not connected
C1:7	FREEZE	C0:7	HALT*
C1:6	16MB*	C0:6	CONFIG1
C1:5	Not connected	C0:5	DSACK* TA*
C1:4	EXTAL†	C0:4	FC3
C1:3	AS*	C0:3	BERR*
C1:2	CONFIG0	C0:2	CONFIG2
C1:1	AVEC IACK5†	C0:1	DSACK* TBI
C1:0	IFETCH*	C0:0	R/W*

† Signal not required for disassembly.

Table 1–4 shows the clock probes and the 68360 signal to which they must connect for disassembly to be correct.

Table 1–4: 68360 signal connections for clock probes

Section:channel	68360 signal
CK:3	EXTAL or CLK01
CK:2	Not connected
CK:1	Not connected
CK:0	AS* (held high in 68040 mode)

4. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the 68360 microprocessor in your SUT and attach the clip.

Applying and Removing Power

If your microprocessor system cannot supply power to the 68360 probe adapter or your system has a +3.3 V 68360 microprocessor (probe adapters need +5 V), you must use an alternate power source. A +5 V power supply for the 68360 probe adapter is available. Refer to the *Replaceable Mechanical Parts* chapter for information on how to order a power supply.

The alternate power supply provides +5 volts to the 68360 probe adapter. The center connector of the power jack connects to Vcc.

To use the power supply, the Power Source jumper (Jxxx) on the probe adapter must be set in the EXT position.

NOTE. Whenever the SUT is powered off, be sure to remove power from the probe adapter.

To apply power to the 68360 probe adapter and SUT, follow these steps:



CAUTION. Failure to use the +5 V power supply provided by Tektronix might permanently damage the probe adapter and 68360 microprocessor. Do not mistake another power supply that looks similar for the +5 V power supply.

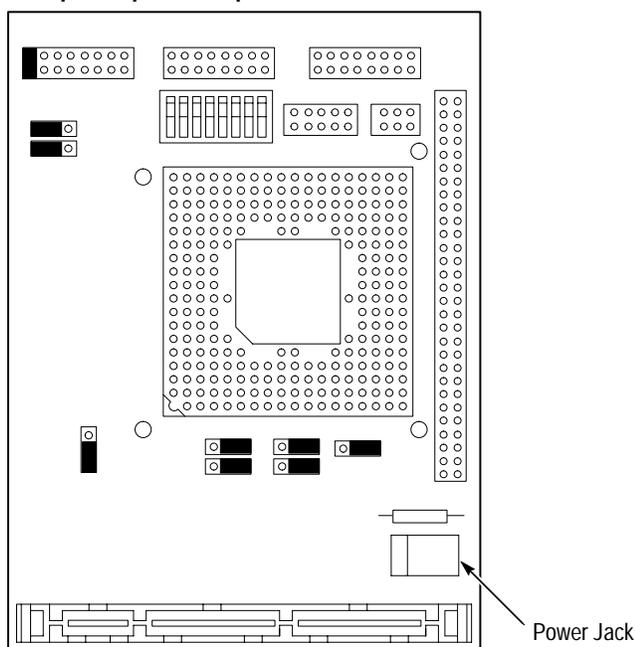
1. Connect the +5 V power supply to the jack on the probe adapter. Figure 1–14 shows the location of the jack on the adapter board.



CAUTION. Failure to apply power to the probe adapter before applying power to your SUT might permanently damage the 68360 microprocessor and SUT.

2. Plug the power supply for the probe adapter into an electrical outlet.
3. Power on the SUT.

Low-profile probe adapter



Conventional probe adapter

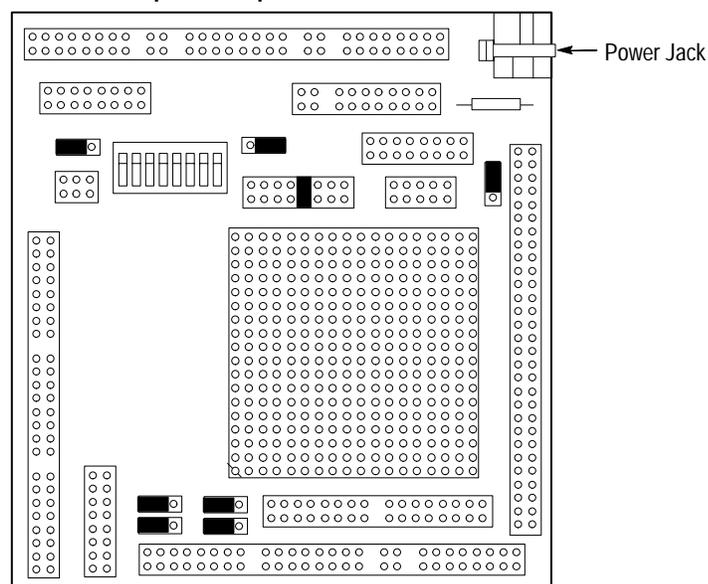


Figure 1-14: Location of the power jack

To remove power from the SUT and 68360 probe adapter, follow these steps:



CAUTION. Failure to power down your SUT before removing the power from the probe adapter might permanently damage the 68360 microprocessor and SUT.

1. Power off the SUT.
2. Unplug the power supply for the probe adapter from the electrical outlet.



Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 261 68360 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the 68360 support are Address, Data, Control, DataSize, and Misc. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–10.

Clocking Options

The TMS 261 support offers a microprocessor-specific clocking mode for the 68360 microprocessor. This clocking mode is the default selection whenever you load the 68360 support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking options for the TMS 261 application are: Probe Interface Type, Alternate Bus Master Cycles, and Refresh Cycles.

- Probe Interface Type** You can acquire data with or without using a probe adapter. If you do not use the 68360 probe adapter, keep the following in mind:
- The disassembler supports 68360 signal clocking. It does not support 68040 signal clocking.
 - Dynamic memory accesses may be unpredictable when the upper address bits are not stable at the end of a cycle.
 - Alternate Bus Master cycles are always acquired and displayed.
 - Refresh cycles are not acquired.
 - The CK2, CK1, C2:0, and C1:5 podlets must be tied low in your SUT.
 - The C2:2 podlet must be tied to Vcc in your SUT.
 - The Config2–Config0 and 16MB* signals must be connected to ground or Vcc (in your SUT) to match their values when the 68360 microprocessor reset is removed; these signals connect to C0:2, C0:6, C1:2, and C1:6 respectively.
 - If your SUT is configured to use the WE3-WE0 signals, you should connect the C3:5, C3:1, C3:3, and C2:4 podlets to the WE3-WE0 signals and the A31-A28 podlets (A3:7, A3:6, A3:5, and A3:4) to ground in your SUT.
 - If your SUT is configured to use the A31-A28 signals, you should connect the A3:7, A3:6, A3:5, and A3:4 podlets to the A31-A28 signals and the WE3-WE0 podlets (C3:5, C3:1, C3:3, and C2:4) to Vcc in your SUT.

Alternate Bus Master Cycles An alternate bus master cycle is defined as the 68360 microprocessor giving up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included. The default selection is Excluded.

Refresh Cycles A refresh cycle is defined as CAS before RAS when using dynamic memory. These types of cycles are acquired when you select Included. The default selection is Excluded.

Symbols

The TMS 261 support supplies one symbol table file. The 68360_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file 68360_Ctrl, the Control channel group symbol table.

Table 2-1: Control group symbol table definitions

Symbol	Control group value									Meaning										
	RESETH* FREEZE REFRESH TA_D*	BG_B* BGACK_B* BERR* HALT*	RMC* R_W* AS* DS_D*	IFETCH* CONFIG2 CONFIG1 CONFIG0	PORT32 S68040 FC3															
RESET	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reset				
B_GND_MD1	X	1	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X	X	X	Back ground mode; this is a dual function pin
B_GND_MD2	X	1	X	X	X	X	X	X	X	X	X	X	X	1	0	X	X	X	X	Back ground mode; this is a dual function pin
HALT	1	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	Halt
BUS_ERROR	1	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	Bus error
ALT_RD-1	1	X	X	X	1	X	X	X	X	1	X	X	X	X	1	0	X	X	X	BR* signal out. Alt bus master read
ALT_RD-2	1	X	X	X	1	X	X	X	X	1	X	X	X	0	0	X	X	X	X	BR* signal out. Alt bus master read
ALT_RD-3	1	X	X	X	0	X	X	X	X	1	X	X	X	1	0	X	X	X	X	BR* signal in. Alt bus master read
ALT_RD-4	1	X	X	X	0	X	X	X	X	1	X	X	X	X	1	1	X	X	X	BR* signal in. Alt bus master read
ALT_RD-5	1	X	X	X	X	0	X	X	X	1	X	X	X	1	0	X	X	X	X	BR* signal in. Alt bus master read
ALT_RD-6	1	X	X	X	X	0	X	X	X	1	X	X	X	X	1	1	X	X	X	BR* signal in. Alt bus master read
ALT_WR-1	1	X	X	X	1	X	X	X	X	0	X	X	X	X	1	0	X	X	X	BR* signal out. Alt bus master write
ALT_WR-2	1	X	X	X	1	X	X	X	X	0	X	X	X	0	0	X	X	X	X	BR* signal out. Alt bus master write
ALT_WR-3	1	X	X	X	0	X	X	X	X	0	X	X	X	1	0	X	X	X	X	BR* signal in. Alt bus master write
ALT_WR-4	1	X	X	X	0	X	X	X	X	0	X	X	X	X	1	1	X	X	X	BR* signal in. Alt bus master write
ALT_WR-5	1	X	X	X	X	0	X	X	X	0	X	X	X	1	0	X	X	X	X	BR* signal in. Alt bus master write
ALT_WR-6	1	X	X	X	X	0	X	X	X	0	X	X	X	X	1	1	X	X	X	BR* signal in. Alt bus master write
68040_RD	1	X	X	0	X	X	X	X	X	1	X	X	X	X	X	X	X	1	X	68040 signals used. Read
68040_WR	1	X	X	0	X	X	X	X	X	0	X	X	X	X	X	X	X	1	X	68040 signals used. Write
READ	1	X	X	X	X	X	X	X	1	1	0	X	1	X	X	X	X	0	0	Read
WRITE	1	X	X	X	X	X	X	X	1	0	0	X	X	X	X	X	X	0	0	Write
PREFETCH	1	X	X	X	X	X	X	X	X	1	0	X	0	X	X	X	X	0	0	Instruction Fetch

Table 2-1: Control group symbol table definitions (cont.)

Symbol	Control group value										Meaning
	RESETH* FREEZE REFRESH TA_D*	BG_B* BGACK_B* BERR* HALT*	RMC* R_W* AS* DS_D*	IFETCH* CONFIG2 CONFIG1 CONFIG0	PORT32 S68040 FC3						
SHOW_C_RD	1 X X X	X X X X	1 1 1 0	1 X X X	X 0 0						Show cycle read
SHOW_C_WR	1 X X X	X X X X	1 0 1 X	X X X X	X 0 0						Show cycle write
SHOW_FETH	1 X X X	X X X X	X 1 1 0	0 X X X	X 0 0						Show cycle fetch
SH_RMW_RD	1 X X X	X X X X	0 1 1 0	X X X X	X 0 0						Show cycle RMW read
SH_RMW_WR	1 X X X	X X X X	0 0 1 X	X X X X	X 0 0						Show cycle RMW write
BERR_RTRY ¹	1 X X X	X X 0 0	X X X X	X X X X	X 0 0						Bus Error Retry
RMW_READ	1 X X X	X X X X	0 1 0 0	X X X X	X 0 0						Read part of RMW cycle
RMW_WRITE	1 X X X	X X X X	0 0 0 X	X X X X	X 0 0						Write part of RMW cycle
RMW ¹	1 X X X	X X X X	0 X X X	X X X X	X 0 0						Read modify Write cycle
DMA	1 X X X	X X X X	X X 0 X	X X X X	X X 1						DMA access
REFRESH	1 X 1 X	X X X X	X X X X	X X X X	X X X						Refresh cycle

¹ Symbols used only for triggering; they do not appear in the Disassembly or State displays.

* Symbols used only for triggering; they are not displayed.

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- Changing the way data is displayed
- Changing disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 68360 support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to Changing How Data is Displayed on page 2–10.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows these special characters and strings, and gives a definition of what they represent.

Table 2-2: Meaning of special characters in the display

Character or string displayed	Meaning
>> or m	The instruction was manually marked as a program fetch
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.
#	Indicates an immediate value
t	Indicates the number shown is in decimal, such as #12t
(S) or (U)	Indicates the mode in which the microprocessor is operating, Supervisor or User
A-LINE OPCODE	Displayed for an A-Line trap instruction
F-LINE OPCODE	Displayed for an F-Line trap instruction

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2-3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2-3: Cycle type definitions

Cycle type	Definition
(68040 READ)	68040 signals used. Read
(68040 WRITE)	68040 signals used. Write
(ALT BUS MASTER: READ-1)	Another master has control of the bus and is doing a memory read
(ALT BUS MASTER: READ-2)	Another master has control of the bus and is doing a memory read
(ALT BUS MASTER: READ-3)	Another master has control of the bus and is doing a memory read
(ALT BUS MASTER: READ-4)	Another master has control of the bus and is doing a memory read
(ALT BUS MASTER: READ-5)	Another master has control of the bus and is doing a memory read
(ALT BUS MASTER: READ-6)	Another master has control of the bus and is doing a memory read
(ALT BUS MASTER: WRITE-1)	Another master has control of the bus and is doing a memory write
(ALT BUS MASTER: WRITE-2)	Another master has control of the bus and is doing a memory write

Table 2-3: Cycle type definitions (cont.)

Cycle type	Definition
(ALT BUS MASTER: WRITE-3)	Another master has control of the bus and is doing a memory write
(ALT BUS MASTER: WRITE-4)	Another master has control of the bus and is doing a memory write
(ALT BUS MASTER: WRITE-5)	Another master has control of the bus and is doing a memory write
(ALT BUS MASTER: WRITE-6)	Another master has control of the bus and is doing a memory write
(BACKGROUND READ)	A read has occurred while the processor is in background mode
(BACKGROUND WRITE)	A write has occurred while the processor is in background mode
(BUS ERROR)	External logic aborts current bus cycle
(DMA)	DMA access
(HALT)	HALT* asserted, processor stops
(READ)	Data read from memory
(READ RMW)	Read from memory during read-modify-write cycle
(REFRESH)	Refresh cycle
(RESET)	Processor asserts RESET* signal
(SHOW CYCLE READ)	This is an internal READ made visible on the external bus
(SHOW CYCLE WRITE)	This is an internal WRITE made visible on the external bus
(SHOW CYCLE READ RMW)	This is an internal READ made visible on the external bus (part of a RMC cycle)
(SHOW CYCLE WRITE RMW)	This is an internal WRITE made visible on the external bus (part of a RMC cycle)
(UNKNOWN)	An unrecognized combination of control values
(WRITE)	Data is written to memory
(WRITE RMW)	Write to memory during read-modify-write cycle
(BREAKPOINT ACK n) ¹	A19-A16 indicates type 0000, n is break number for a READ
(INT ACK LEVEL: n) ¹	A19-A16 indicates type 1111, n is level number for a READ
(INTERNAL REG ACCESS) ¹	A19-A16 indicates type 0011; this occurs at low power standby mode or a base address register access for a WRITE
(FLUSH) ¹	Pipeline flush; occurs when the processor branches to nonsequential address

Table 2–3: Cycle type definitions (cont.)

Cycle type	Definition
(EXTENSION) ¹	Extension fetched from program space

¹ Computed cycle types.

Figure 2–1 shows an example of the Hardware display.

	1	2	3	4	5
	Sample	Address	Data	Mnemonic	Timestamp
T	0	00084CE6	-----4E7A	--MOVEC-VBR,DO-----	(S)-----
	1	00084CEA	08012440	MOVEA.L D0,A2	(S) 280 ns
	2	00084CEC	257C0008	MOVE.L #00084E08,(00A8,A2)	(S) 360 ns
	3	00084CF0	4E0800A8	(EXTENSION)	(S) 480 ns
	4	00084CF4	227C0048	MOVEA.L #00480400,A1	(S) 360 ns
	5	004000A8	00084E08	(WRITE)	(S) 400 ns
	6	00084CFA	0400228F	MOVE.L A7,(A1)	(S) 320 ns
	7	00084CFC	48790008	PEA 00085C9A	(S) 840 ns
	8	00084D02	5C9A4879	PEA 00085CB2	(S) 360 ns
	9	00480400	004FFFE8	(WRITE)	(S) 360 ns
	10	00084D04	00085CB2	(EXTENSION)	(S) 320 ns
	11	004FFFE4	00085C9A	(WRITE)	(S) 400 ns
	12	00084D08	48790008	PEA 00085CB6	(S) 400 ns
	13	004FFFE0	00085CB2	(WRITE)	(S) 360 ns
	14	00084DOE	5CB64879	PEA 00085CC8	(S) 320 ns
	15	00084D10	00085CC8	(EXTENSION)	(S) 360 ns
	16	004FFFD8	00085CB6	(WRITE)	(S) 360 ns
	17	00084D14	48790008	PEA 00085D14	(S) 400 ns
	18	004FFFD4	00085CC8	(WRITE)	(S) 360 ns
	19	00084D1A	5D140240	ANDI.W #0000,D0	(S) 320 ns
	20	00084D1E	0000303C	MOVE.W #0001,D0	(S) 360 ns
	21	004FFFD4	00085D14	(WRITE)	(S) 360 ns

Figure 2–1: Hardware display format

- 1 **Sample Column.** Lists the memory locations for the acquired data.
- 2 **Address Group.** Lists data from channels connected to the 68360 address bus.
- 3 **Data Group.** Lists data from channels connected to the 68360 data bus.
- 4 **Mnemonics Column.** Lists the disassembled instructions and cycle types.
- 5 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

The Software display format also shows the following cycles:

- Reset cycle
- Halt cycle
- Bus Error cycle
- Special cycles: Breakpoint Ack, Int Ack, Internal Reg Access, Reset Vector
- Reads from the vector table that appear due to servicing exceptions or traps
- Illegal instructions
- (UNKNOWN) cycle types; the disassembler does not recognize the Control group value

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

The Control Flow display format also shows the following cycles:

- Reset cycle
- Halt cycle
- Bus Error cycle
- Special cycles: Breakpoint Ack, Int Ack, Internal Reg Access
- Reset vector
- Reads from the vector table that appear due to servicing exceptions
- Illegal instructions
- (UNKNOWN) cycle types; the disassembler does not recognize the Control group value

Instructions that generate a change in the flow of control in the 68360 microprocessor are as follows:

Bcc (conditional branches)		RTD
BGND	DIVSL	RTE
BKPT	DIVU	RTR
BRA	DIVUL	RTS
BSR	JMP	STOP

CHK	JSR	TRAP
CHK2	LPSTOP	TRAPcc
DBcc (test condition, decrement, and branch)		TRAPV
DIVS	RESET	

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

The Subroutine display format also shows the following cycles:

- Reset Cycle
- Halt Cycle
- Bus Error Cycle
- Special cycles: Breakpoint Ack, Int Ack, Internal Reg Access
- Reset Vector
- Reads from the vector table that appear due to servicing exceptions
- Illegal instructions
- (UNKNOWN) cycle types; the disassembler does not recognize the Control group value

Instructions that generate a subroutine call or a return in the 68360 microprocessor are as follows:

BGND	DIVS	LPSTOP	RTS
BKPT	DIVSL	RESET	STOP
BSR	DIVU	RTD	TRAP
CHK	DIVUL	RTE	TRAPcc
CHK2	JSR	RTR	TRAPV

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the 68360 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

- Choose to acquire A27-A0 or A31-A0 signals on the address bus.
- Specify the bus width when the DSACK signals are generated internally.
- Choose to display invalid bytes as dashes.
- Specify the starting address of the vector table.
- Specify the size of the vector table.

The 68360 microprocessor support product has five additional fields: Address Bus Width, Internal Bus Width of the DSACK Signals, Dash Invalid Bytes, Vector Base Register, and Vector Table Size. These fields appear in the area indicated in the basic operations user manual.

Address Bus Width. The address bus of the 68360 microprocessor can be 28- or 32-bits wide, inclusive. You should select the bus width that matches the width of the address bus in your SUT in the Address Lines A0 thru field. The choices are A27-A0 or A31-A0.

The disassembler ignores upper address bits that fall outside the selected range and displays them as 0.

If you create a symbol table for the Address group, be sure that the number of bits in the symbol table matches the bus width for the Address group.

Internal Bus Width of the DSACK Signals. The 68360 microprocessor allows 8-, 16-, and 32-bit wide data transfers. The DSACK signals, which indicate the valid bytes on the bus, are not always asserted.

For cycles when the DSACK signals are asserted, the disassembler uses the binary value on the DSACK signals for displaying the valid bytes and dashing invalid bytes (unless the field for dashing bytes is disabled).

For nonfetch Show cycles, the disassembler always displays 32 bits.

For cycles when the DSACK signals are not asserted, the disassembler uses the selection in the Int. DSACKs Bus Width field to determine the DSACK bus width. When Best Guess is selected, the disassembler will try to determine if the data transfer was 8-, 16-, or 32-bits wide by looking at the surrounding fetches. Data will be disassembled accordingly. This selection can be changed to an 8-bit, 16-bit, or 32-bit bus width.

Dash Invalid Bytes. The disassembler uses the DSACK signals to determine which bytes are valid for data transfers. When you select Yes in the Dash Invalid Bytes field, the disassembler displays dashes for invalid bytes.

Vector Base Register. The disassembler uses the vector base register (VBR) value (the base of the interrupt table) to compute the name of the interrupt or to determine if a conditional interrupt occurred. You can enter the VBR value, the starting address of the vector table, in the Vector Base Register field.

The disassembler ignores upper address bits that fall outside the selected range in the Address Lines A0 thru field.

A0 of the VBR must be set to 0.

The reset vector information must be located from address 0x0 to 0x7. It does not matter what the VBR is set to; the disassembler will always display the reset vector at 0 (0x00000000).

Vector Table Size. The disassembler uses the vector table size to compute the name of the interrupt whenever an exception occurs. The default vector table size is 400. Enter any value between 8 and 400. The value must be divisible by four.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)
- Anything (any valid opcode, extension or flush)

Mark selections are as follows:

Opcode	Anything
Opcode	Opcode
Opcode	Flush
Flush	Flush
Flush	Opcode
Extension	Extension
Extension	Opcode
Extension	Flush

Undo marks on this cycle

Information on basic operations contains more details on marking cycles and how to view the file.

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your 68360 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.



Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires 68360 signals
- List of other accessible microprocessor signals and extra probe channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a 68360 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

Circuitry on the probe adapter can be powered from either the SUT or an external power source. Refer to *Applying and Removing Power* in the *Getting Started* chapter on page 1–20 for information on using an external power source.

The probe adapter accommodates the Motorola 68360 microprocessor in a 241-pin PGA package. The low-profile probe adapter is designed to be used with the 192-Channel High Density Probe. The conventional probe adapter was available in earlier versions of the product.

Configuration

There are many jumpers on the probe adapter. Table 3–1 shows a summary of the jumpers, jumper positions, and functions for the low-profile. and conventional probe adapters.

Table 3–1: Jumper positions and functions

Jumper (low-profile probe adapter)	Jumper (conventional probe adapter)	Position	Function
J1120	J1260	Selectable	If the SUT uses dynamic memory controlled by the microprocessor, place the jumper in the position corresponding to the memory size used (128, 256, or 512 Kbytes, or 1, 2, 4, 8, 16, or 32 Mbytes). If the SUT does not use dynamic memory, place the jumper in any position. You can also place the jumper in any position if the RAS/Trans jumper (J1200) is in the Trans position (Pins 2, 3).
J1200	J1210	RAS ¹	Use if the SUT uses dynamic memory. Place the jumper in this position to rearrange the upper and lower bits of the Address group for disassembly.
		Trans	Use if the SUT does not use dynamic memory or if you want to acquire data using transitional clocking (asynchronous). This is the default jumper setting.
J1205	J1255	68360	Use when acquiring standard 68360 signals (such as AS* and DS*). This is the default jumper setting.
		68040	Use when acquiring 68040-type signals (such as TS* and TA*).
J1520	Not Present	CLK01	Use when CLK01 is enabled in the CLKOCR register.
		EXTAL	Use when EXTAL is driven with the system frequency.
J1540	J1630	WE0	Use when microprocessor is configured to use WE3–WE0 signals. The logic analyzer reads these signals as lows. This is the default position.
		A28	Use when microprocessor is configured to use A31–A28 address signals. The logic analyzer reads the WE3–WE0 signals as highs.
J1545	J1635	WE1	Use when microprocessor is configured to use WE3–WE0 signals. The logic analyzer reads these signals as lows. This is the default position.
		A29	Use when microprocessor is configured to use A31–A28 address signals. The logic analyzer reads the WE3–WE0 signals as highs.
J1550	J1640	WE2	Use when microprocessor is configured to use WE3–WE0 signals. The logic analyzer reads these signals as lows. This is the default position.
		A30	Use when microprocessor is configured to use A31–A28 address signals. The logic analyzer reads the WE3–WE0 signals as highs.
J1555	J1645	WE3	Use when microprocessor is configured to use WE3–WE0 signals. The logic analyzer reads these signals as lows. This is the default position.
		A31	Use when microprocessor is configured to use A31–A28 address signals. The logic analyzer reads the WE3–WE0 signals as highs.
J1560	J1290	EXT PWR	Use when the probe adapter is powered by an alternate power supply.
		SUT PWR	Use when the probe adapter is powered by the SUT. This is the default jumper setting.

¹ The RAS position meets Motorola's requirement that the complete address not be on the bus at the end of each RAS/CAS cycle. Observations on a limited set of microprocessors show that the complete address is on the bus at the end of each RAS/CAS cycle. If you find that the microprocessor does not place the complete address on the bus at the end of a RAS/CAS cycle (CAS part), then place the jumper in the RAS position.

Figure 3–1 shows the locations of the jumpers and switches on the probe adapters. Refer to Table 3–1 for descriptions of each jumper.

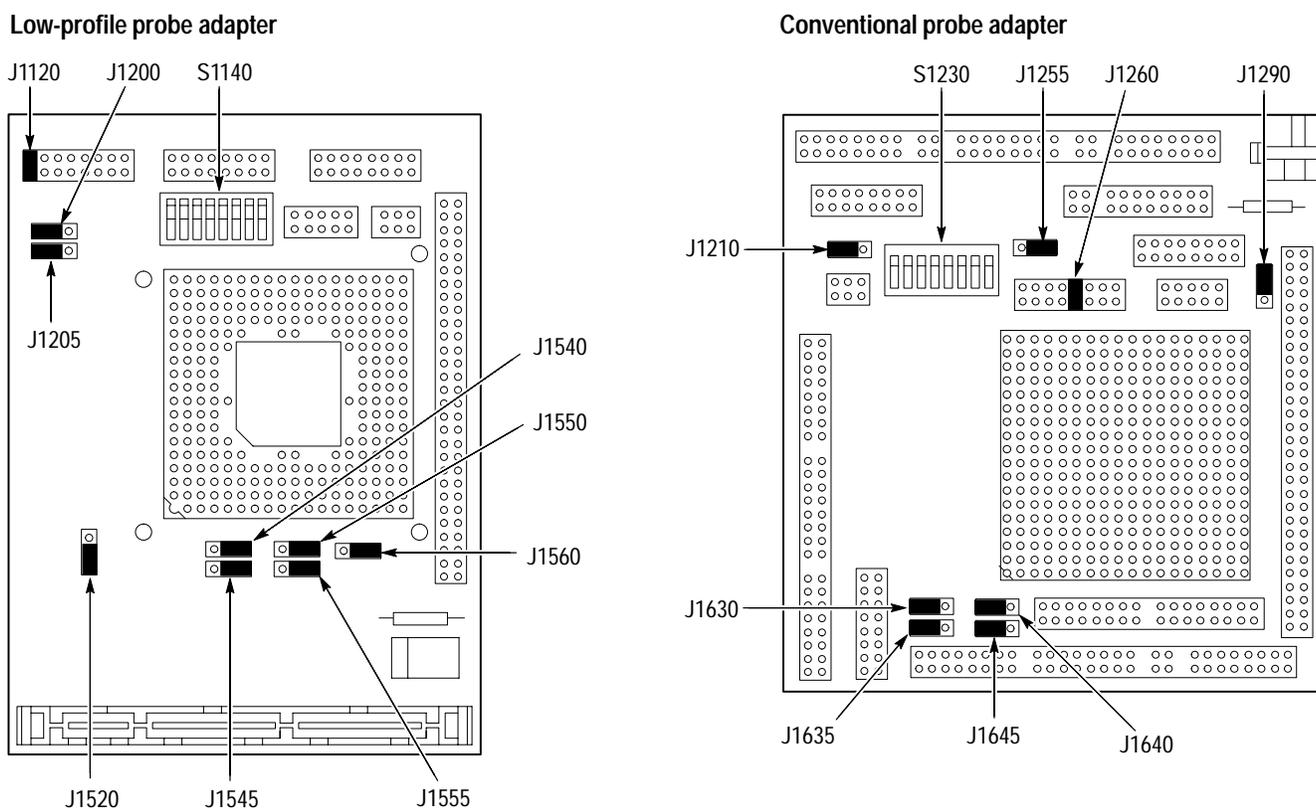


Figure 3–1: Jumper and switch locations on the probe adapters

The CS/RAS Signal Selection switch block (S1140 on the low-profile probe adapter or S1230 on the conventional probe adapter) has a switch for each RAS signal that the SUT might use. For each RAS signal used, close the corresponding switch on the switch block. If the SUT does not use dynamic memory, open all of the switches.

If you do not know which RAS lines are used by the SUT, open all of the switches and place the RAS/Trans jumper in the Trans position.

Table 3–2 shows the switch numbers printed on the switch block and the CS or RAS signal that connects to each switch.

Table 3–2: Switch numbers and CS/RAS signals

Switch number	Signal name
1	CS0*/RAS0*
2	CS1*/RAS1*
3	CS2*/RAS2*
4	CS3*/RAS3*
5	CS4*/RAS4*
6	CS5*/RAS5*
7	CS6*/RAS6*
8	CS7*/RAS7*

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–3 shows the electrical requirements for the low-profile probe adapter the SUT must produce for the support to acquire correct data.

In Table 3–3, for the 102/136-channel module, one podlet load is 20 k Ω in parallel with 2 pF. For the 96-channel module, one podlet load is 100 k Ω in parallel with 10 pF.

Table 3–3: Electrical specifications: Low-profile probe adapter

Characteristics	Requirements
Adapter DC power requirements	
Voltage	4.75-5.25 VDC
Current (power supplied by SUT)	I Maximum (calculated) 1.4 A I Typical (measured) 1.1 A
Power supply requirements	
Voltage	90-265 VAC
Current	1.1 A maximum at 100 VAC
Frequency	47-63 Hz
Power	25 W maximum
SUT clock	
Clock rate	Maximum. 33 MHz Tested 25 MHz
Minimum setup time required	
D0 – D31	8 ns worst case; 3 ns typical

Table 3–3: Electrical specifications: Low-profile probe adapter (cont.)

Characteristics	Requirements
All other signals	5 ns
Minimum hold time required	
IFETCH*, DSACK0–1*, AVEC*	8 ns
All other signals	1 ns
Without probe adapter	
Minimum setup time required, all signals	5 ns
Minimum hold time required, all signalst	0 ns

Table 3–4 lists the typical SUT loading you can expect when you use the low-profile probe adapter.

Table 3–4: Typical SUT signal loading: Low-profile probe adapter

Characteristics	AC load	DC load
A0–A14	11–15 pF	74FCT162501
A15, A20–A25	13–17 pF	20L8-10
A16–A19, A26, A27, BG*, BGACK*	13–17 pF	22V10-10
A28 (J1540 in WE0 position)	13 pF	74FCT162244ET
A28 (J1540 in A28 position)	15 pF	22V10-10
A29 (J1545 in WE1 position)	17 pF	74FCT162244ET
A29 (J1545 in A29 position)	19 pF	22V10-10
A30 (J1550 in WE2 position)	13 pF	74FCT162244ET
A30 (J1550 in A30 position)	21 pF	22V10-10
A31 (J1555 in WE3 position)	15 pF	74FCT162244ET
A31 (J1555 in A31 position)	15 pF	22V10-10
BCLRO*, PRTY3	9–11 pF	16V8-7
CAS0*–CAS3*	16–19 pF	20L8-5
DSACK1*	26 pF	20L8-5
AS*	23 pF	20L8-5
CLK01, EXTAL	4–16 pF ¹	20L8-5
CS0*–CS7*	5–19 pF ²	74F30
RMC*	26 pF	16V8-7
FREEZE	31 pF	16V8-7
DS*	12 pF	16V8-7

Table 3–4: Typical SUT signal loading: Low-profile probe adapter (cont.)

Characteristics	AC load	DC load
RESETH*	22 pF	16V8-7
Remaining Signals	8–15 pF	74FCT162244ET

¹ Loading varies with position of J1520 (CLK01/EXTAL jumper)

² Loading varies with positions of S1230 (CAS/RAS selection switch)

Table 3–5 shows the electrical requirements for the conventional probe adapter.

Table 3–5: Electrical specifications: Conventional probe adapter

Characteristics	Requirements
Adapter DC Power Requirements	
Voltage	4.75-5.25 VDC
Current (Power Supplied by SUT)	I maximum (calculated) 1.3 A I typical (measured) 1.0 A
Power supply requirements	
Voltage	90-265 VAC
Current	1.1 A maximum at 100 VAC
Frequency	47-63 Hz
Power	25 W maximum
SUT Clock	
Clock Rate	Min. DC Max. 33 MHz Tested 25 MHz
With Probe Adapter	
Minimum Setup Time Required	
D0 – D31	7 ns worst case; 3 ns typical
All Other Signals	4 ns
Minimum Hold Time Required	
IFETCH*, DSACK0–1*, AVEC*	7 ns
All Other Signals	0 ns
Without Probe Adapter	
Minimum Setup Time Required, All Signals	5 ns
Minimum Hold Time Required, All Signals	0 ns

Table 3–6 lists the typical SUT loading you can expect when you use the conventional probe adapter. In Table 3–6, for the module, one podlet load is 100 k Ω in parallel with 10 pF.

Table 3–6: Typical SUT signal loading: Conventional probe adapter

Characteristics	AC Load	DC Load
A0–A14	15 pF	74FCT
A15, A20–A25	15 pF	20L8–10
A16–A19, A26–A31, BG*, BGACK*	15 pF	22V10–10
BCLRO*, PRTY3	17 pF	16V4–15
CAS0–CAS3*, DSACK1*, AS*, EXTAL	20 pF	16L8–5
CS0*–CS7*		74F30 in parallel with 10K to V _{CC}
RMC*, FREEZE, DS*, RESETH*	20 pF + 1 podlet	1 podlet in parallel with 16V4
All Other Signals	20 pF + 1 podlet	1 podlet

Table 3–7 shows the environmental specifications.

Table 3–7: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

* Designed to meet Tektronix standard 062-2847-00 class 5.

† Not to exceed 68360 microprocessor thermal considerations. Forced air cooling might be required across the CPU.

Table 3–8 shows the certifications and compliances that apply to the probe adapter.

Table 3–8: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.
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Figure 3–2 shows the dimensions of the probe adapter. The figure also shows the minimum vertical clearance of the high-density probe cable.

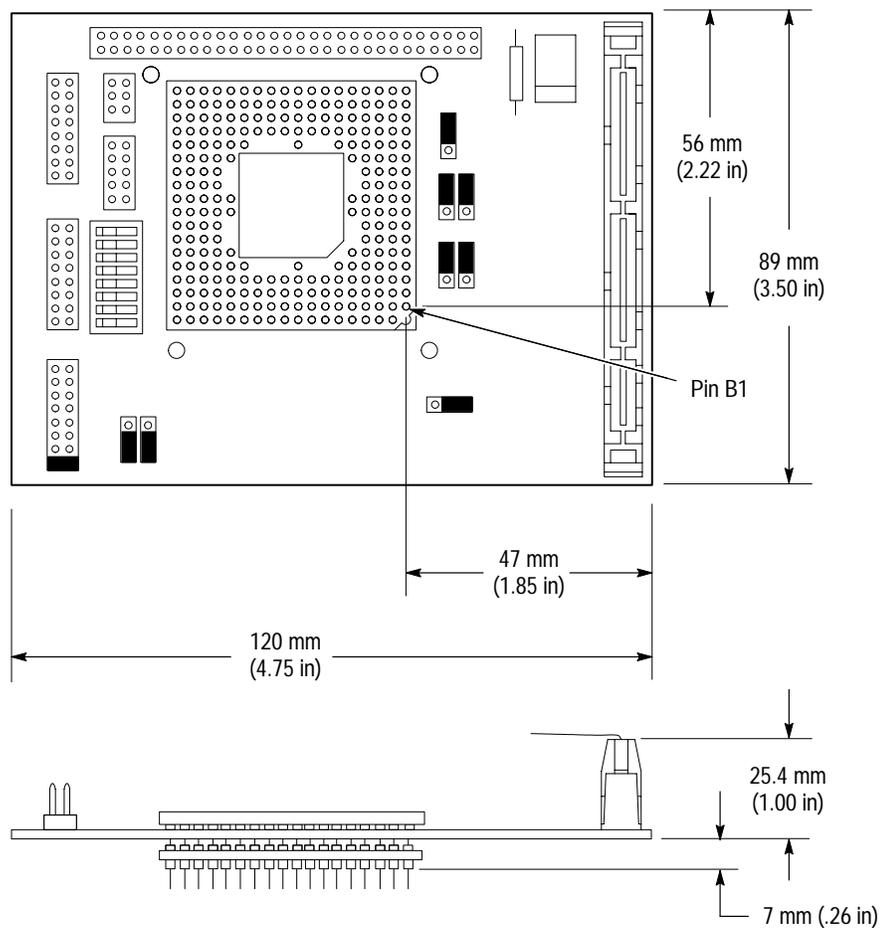


Figure 3–2: Dimensions of the low-profile probe adapter

Figure 3–3 shows the placement of tie-down holes on the probe adapter. If you purchase a converter clip (PGA-to-QFP) from ITT Pomona (part number 5968), you can use screws to secure the clip and probe adapter to the microprocessor in your system. The dimension of the holes is 0.110/0.116 inch.

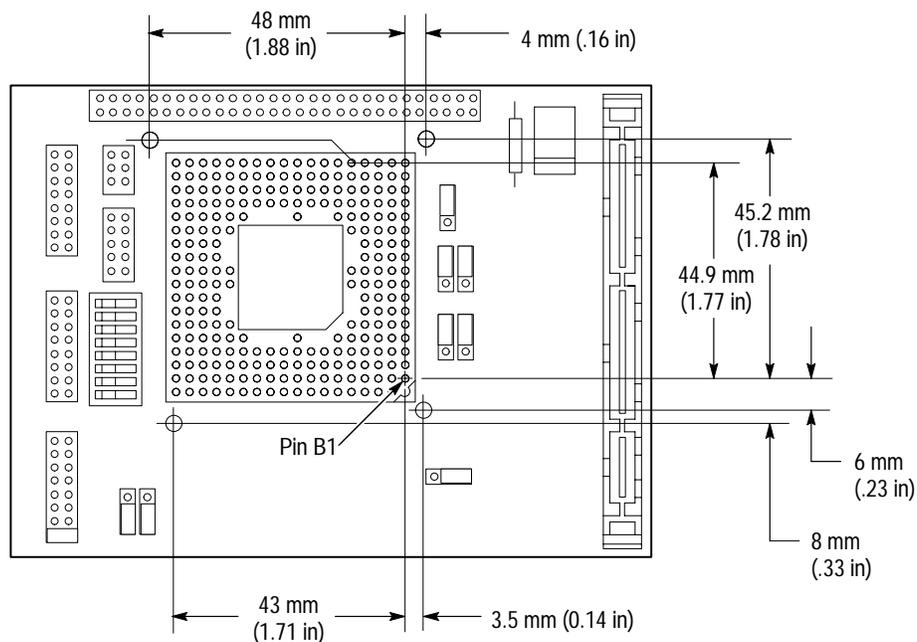


Figure 3-3: Tie-down hole placement on the low-profile probe adapter

Figure 3-4 shows the dimensions of the conventional probe adapter. The basic operations user manual shows the vertical clearance of the clock and channel probes when connected to a probe adapter under *Requirements and Restrictions* in the *Getting Started* chapter.

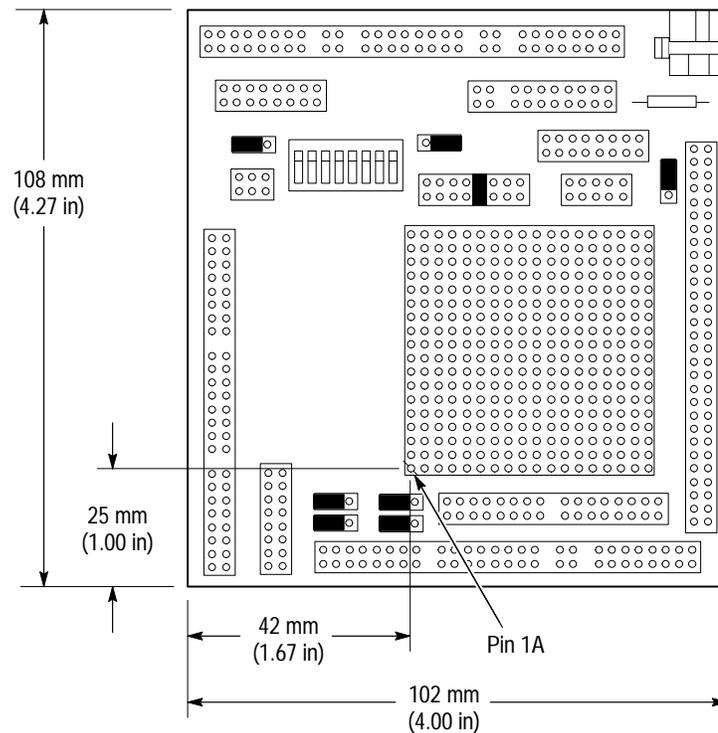


Figure 3-4: Dimensions of the conventional probe adapter

Channel Assignments

Channel assignments shown in Table 3-9 through Table 3-14 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- An asterisk following a signal name indicates an active low signal.
- An equals sign (=) following a signal name indicates that it is double probed.

Table 3-9 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–9: Address group channel assignments

Bit order	Section:channel	68360 signal name
31	A3:7	A31
30	A3:6	A30
29	A3:5	A29
28	A3:4	A28
27	A3:3	A27
26	A3:2	A26
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 3–10 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–10: Data group channel assignments

Bit order	Section:channel	68360 signal name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–11 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–11: Control group channel assignments

Bit order	Section:channel	68360 signal name	Logic analyzer signal name
18	C2:3	RESETH*	same
17	C1:7	FREEZE	same
16	C1:5	none	REFRESH
15	C2:2	TA*	TA_D*
14	C2:6	BG*	BG_B*
13	C2:5	BGACK*	BGACK_B*
12	C0:3	BERR*	same
11	C0:7	HALT*	same
10	C2:7	RMC*	same
9	C0:0	R_W*	same
8	C1:3	AS*	AS_B*
7	C2:1	DS*	DS_D*
6	C1:0	IFETCH*	same
5	C0:2	CONFIG2	CONFIG2 (at reset)
4	C0:6	CONFIG1	CONFIG1 (at reset)
3	C1:2	CONFIG0	CONFIG0 (at reset)
2	C1:6	16MB*	PORT32 (at reset)
1	C2:0	none	S68040
0	C0:4	FC3	same

Table 3–12 shows the probe section and channel assignments for the DataSize group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in symbolically.

Table 3–12: DataSize group channel assignments

Bit order	Section:channel	68360 signal name
6	C3:6	FC2
5	C3:2	FC1
4	C3:7	FC0
3	C0:5	DSACK*_TA*
2	C0:1	DSACK0*_TBI
1	C3:4	SIZ1
0	C3:0	SIZ0

Table 3–13 shows the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–13: Misc group channel assignments

Bit order	Section:channel	68360 signal name	Logic analyzer signal name
5	C3:5	WE3*†	same
4	C3:1	WE2*†	same
3	C3:3	WE1*†	same
2	C2:4	WE0*†	same
1	C1:1	AVEC*_IACK5†	same
0	C1:4	EXTAL†	SYSCLK_B†

† Signal not required for disassembly.

Table 3–14 shows the probe section and channel assignments for the clock probes (not part of any group) and the 68360 signal to which each channel connects.

Table 3–14: Clock channel assignments

Section: channel	68360 signal name	Logic analyzer signal name
CK:0	AS* (held high in 68040 mode)	AS_B*1
CK:1	none	REFRESH (CAS before RAS cycle) ¹
CK:2	none	ALT_D (derived signal – Config lines with BG* & BGACK*)
CK:3	EXTAL	SYSCLK_040*

¹ Channel is double probed.

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–14, you must connect another channel probe to the signal, a technique called double probing.

How Data is Acquired

This part of this chapter explains how the module acquires 68360 signals using the TMS 261 software and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra probe channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the 68360 support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the 68360 bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–5 shows the sample points and the master sample point for 68360 bus timing. Sample point 1 includes lower address signals latched on probe (RAS_CAS). Sample point 2 includes IFETCH*, SYSCLK_B, FC3, and R_W*. Sample point 3 includes all Address, Data and remaining control signals.

Figure 3–6 shows the sample points for 68040 microcontroller bus timing.

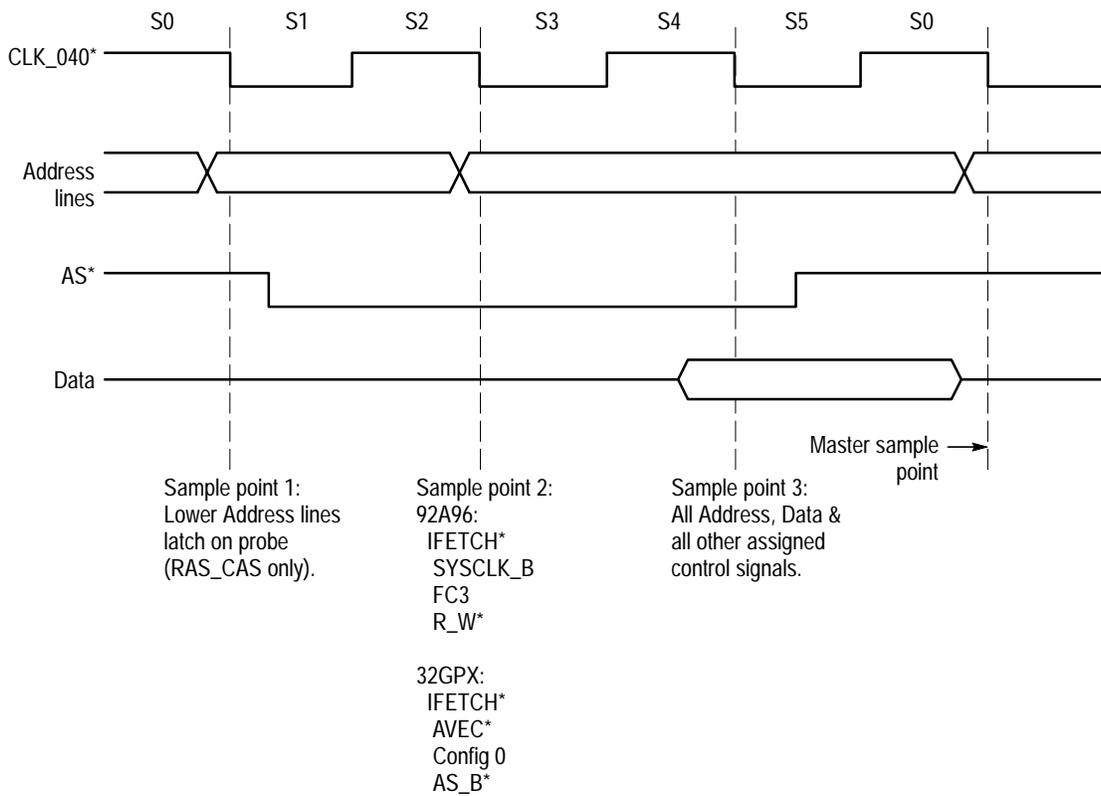


Figure 3-5: 68360 bus timing

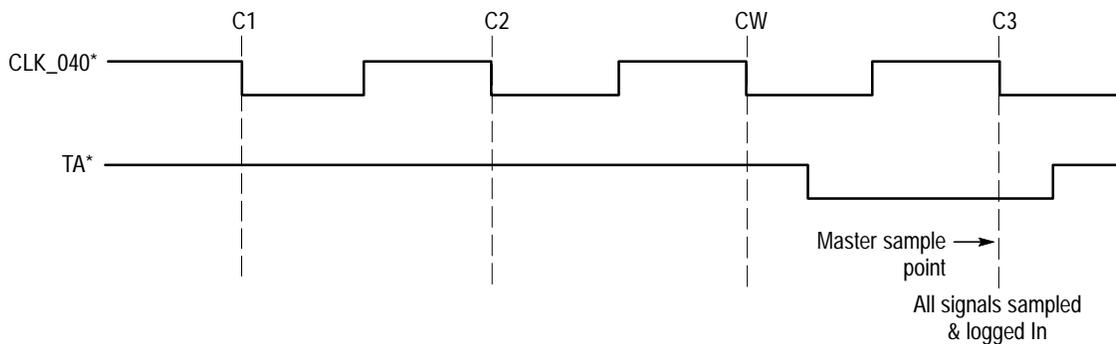


Figure 3-6: 68040 bus timing

Clocking Options

The clocking algorithm for the 68360 microprocessor support has the following variations: Probe Interface Type With Probe Adapter, Probe Interface Type Without Probe Adapter, Alternate Bus Master Cycles Excluded, Alternate Bus Master Cycles Included, Refresh Cycles Excluded, and Refresh Cycles Included.

Probe Interface Type. You can acquire data with or without using a probe adapter. Refer to the guidelines under *Probe Interface Type* on page 2–2 when acquiring data without a 68360 probe adapter.

Alternate Bus Master Cycles. An alternate bus master cycle is defined as the 68360 giving up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included. The default selection is Excluded.

Refresh Cycles. A refresh cycle is defined as CAS before RAS when using dynamic memory. These types of cycles are acquired when you select Included. The default selection is Excluded.

NOTE. *The RAS switches must be set correctly in order to detect Refresh cycles.*

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so that you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–10. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals On the Probe Adapter

The probe adapter board contains pins for microprocessor signals that are not acquired by the TMS 261 application. You can connect extra podlets to these pins, because they can be useful for general purpose analysis.

Table 3–15 shows the pin strip names and component designations (for example, J1180) for these miscellaneous 68360 signal connections. Table 3–16 through Table 3–23 show the pin number and signal name assignments for each pin strip.

Table 3–15: Pin strip names used for alternate connections

Pin strip name	Component designation	
	Low-profile probe adapter	Conventional probe adapter
AUX0	J1180	J1110
AUX	J1140	J1185
TIMERS	part of J1490	part of J1790
PORTA	part of J1490	part of J1790
PORTB	part of J1490	part of J1790
PORTC	part of J1490 </td <td>part of J1790</td>	part of J1790
JTAG	J1185	J1215
BDM	J1160	J1285

Figure 3–7 shows the locations of the miscellaneous pin strips you can use to make alternate connections.

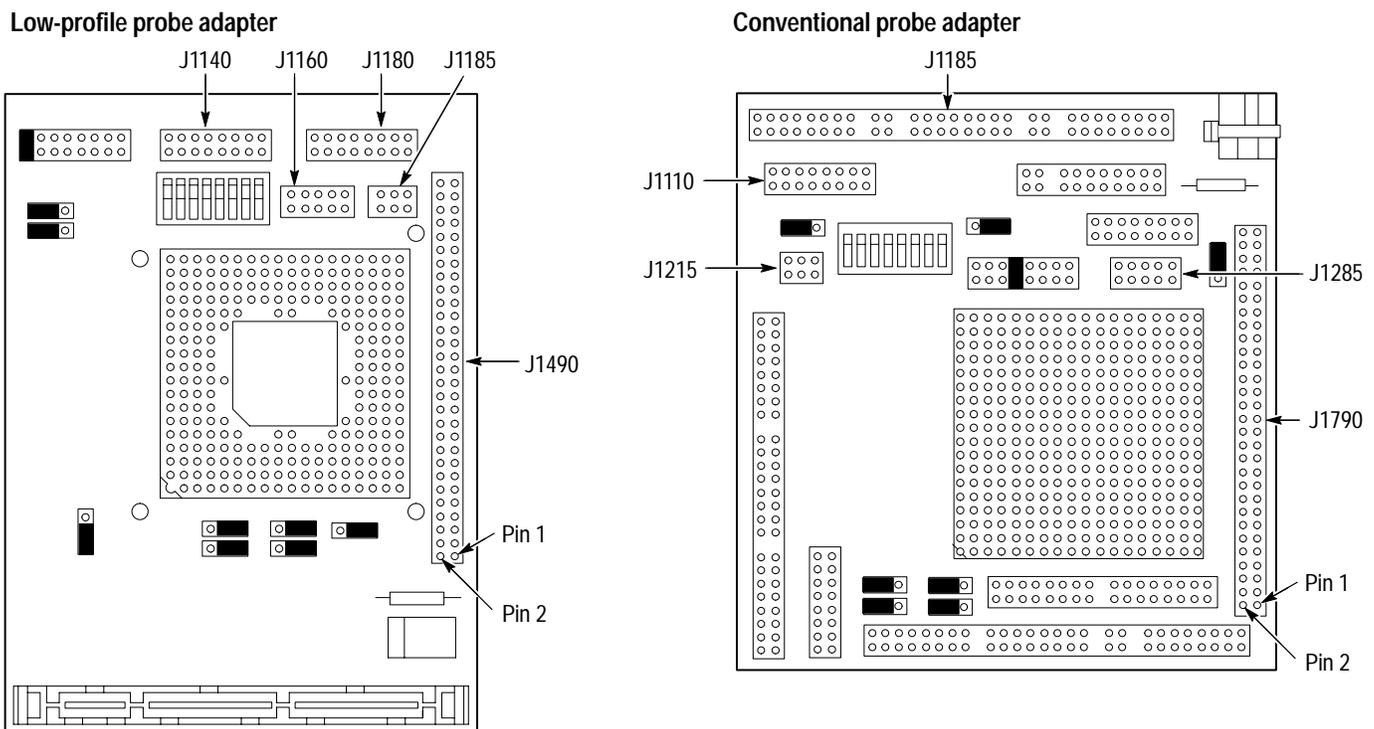


Figure 3–7: Miscellaneous pin strips for alternate connections

Table 3–16 shows the signals available on the AUX0 pin strip.

Table 3–16: AUX0 pin strip signals

J1180 pin (low-profile probe adapter)	J1110 pin (conventional probe adapter)	Channel	Signal name
1	1	GND	
2	2	AUX0:0	none
3	3	GND	
4	4	AUX0:1	BKPT*
5	5	GND	
6	6	AUX0:2	RESETS*
7	7	GND	
8	8	AUX0:3	OE*
9	9	GND	
10	10	AUX0:4	PRTY0
11	11	GND	
12	12	AUX0:5	PRTY1
13	13	GND	
14	14	AUX0:6	PRTY2
15	15	GND	
16	16	AUX0:7	PRTY3

Table 3–17 shows the signals available on the AUX pin strip.

Table 3–17: AUX pin strip signals

J1140 pin (low-profile probe adapter)	J1185 pin (conventional probe adapter)	Channel	Signal name
1	49	GND	
2	50	AUX:0	CS0*_RAS0*
3	51	GND	
4	52	AUX:1	CS1*_RAS1*
5	53	GND	
6	54	AUX:2	CS2*_RAS2*
7	55	GND	
8	56	AUX:3	CS3*_RAS3*
9	57	GND	
10	58	AUX:4	CS4*_RAS4*
11	59	GND	
12	60	AUX:5	CS5*_RAS5*
13	61	GND	
14	62	AUX:6	CS6*_RAS6*
15	63	GND	
16	64	AUX:7	CS7*_RAS7*_IACK7

Table 3–18 shows the signals available on the JTAG pin strip.

Table 3–18: JTAG pin strip signals

Pin number	Signal name
1	TCK
2	TMS
3	TDI
4	TDO
5	TRST*
6	TRIS*

Table 3–19 shows the signals available on the BDM pin strip.

Table 3–19: BDM pin strip signals

Pin number	Signal name
1	DS*
2	BERR*
3	GND
4	BKPT*
5	GND
6	FREEZE
7	RESETH*
8	IFETCH
9	VDD
10	IPIPEO

Table 3–20 shows the signals available on the Timers pin strip.

Table 3–20: Timers pin strip signals

Pin number	Signal name
13	GND
14	CLK1/PA8
15	CLK2/PA9
16	CLK3/PA10
17	CLK4/PA11
18	CLK5/PA12
19	CLK6/PA13
20	CLK7/PA14
21	CLK8/PA15
22	GND

Table 3–21 shows the signals available on the PortA pin strip.

Table 3–21: PortA pin strip signals

Pin number	Signal name
1	GND
2	RXD1/PA0
3	TXD1/PA1
4	RXD2/PA2
5	TXD2/PA3
6	RXD3/PA4
7	TXD3/PA5
8	RXD4/PA6
9	TXD4/PA7
10	GND
11	GND
12	GND

Table 3–22 shows the signals available on the PortB pin strip.

Table 3–22: PortB pin strip signals

Pin number	Signal name
23	GND
24	GND
25	GND
26	PB0
27	PB1
28	PB2
29	PB3
30	PB4
31	PB5
32	PB6
33	PB7
34	PB8
35	PB9
36	PB10
37	PB11
38	PB12
39	PB13
40	PB14
41	PB15
42	PB16
43	PB17
44	GND

Table 3–23 shows the signals available on the PortC pin strip.

Table 3–23: PortC pin strip signals

Pin number	Signal name
45	PC0
46	PC1
47	PC2
48	PC3
49	PC4
50	PC5
51	PC6
52	PC7
53	PC8
54	PC9
55	PC10
56	PC11
57	GND
58	GND

Signals Not On the Probe Adapter

The following is a list of microprocessor signals that are not accessible on either probe adapter or on the LAHDP2 probe.

- CLK02
- MODCK0
- MODCK1
- CLK01
- XTAL
- IPIPE1*
- CAS0–3* (IACK 1, 2, 3, 6)
- IRQ2,3,5,7*
- IRQ6*
- IRQ4*
- IRQ1*
- PERR*
- BCLR0*
- BR*
- XFC

Extra Channels

Table 3–24 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Table 3–24: Extra module sections and channels

Module	Section: channels
102-channels	Qual:1, Qual:0
136-channels	E3:7-0, E2:7-0, E1:7-0, E0:7-0, Qual:3-0
96-channels	None

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.



Maintenance

Maintenance

This chapter contains information on the following topics:

- Probe adapter circuit description
- How to replace a fuse

Probe Adapter Circuit Description

The following paragraphs provide descriptions of the PAL/gates on the probe adapter.

- MUX1–4. In CPU32+ mode, these PALs determine which lower address needs to be multiplexed onto a higher address line for RAS–CAS cycles. On cycles that are not RAS–CAS, or in Slave mode, the high order address line passes straight through.
- ALT–MUX. The MUX part of the PAL does the same job as the MUX1–4 PALs. The ALT part of the PAL determines when a cycle belongs to an alternate master and uses the output signal (ALT_D) for clocking only. To do this, it uses the BG* and BGACK* signals, and the BROUT signal from the LATCH PAL.
- LATCH. This PAL latches the Config and Port Size lines on RESET going away. These lines are then sent as data lines for the disassembler, and generate the BROUT signal for the ALT–MUX PAL.

The LATCH PAL also looks at the J68040 jumper and the Config lines to determine if 68040 type signals are being used. It places this information on the S68040 line to the RAS PAL.

- CONFIG. The 74F148 takes the memory space jumpers and turns them into three bits of gray code.
- RAS. This PAL determines CAS before RAS cycles and outputs a REFRESH signal. The AMS must ensure that only one REFRESH cycle is stored for each RAS cycle.

The PAL buffers the clock delay to the clock podlet. This will add from 1 to 5 ns of delay with a typical delay of 3 ns. This helps data setup time problems. When working with 68040 timing signals, the clock will be inverted when the S68040 signal for the LATCH PAL is high.

The AS* signal is held high when in 68040 signal mode and is buffered the rest of the time.

The DS* signal is held high when in 68040 signal mode and is buffered the rest of the time.

The TA_D* signal is held high in non 68040 timing modes and is buffered when in 68040 timing modes.

- RAS switches. Set these switches to indicate which RAS lines are being used. If you do not know the RAS lines or if they do not know the memory size when using dynamic memories, then you should move the RAS–CAS/Transparent jumper to the Transparent (Trans) position. This will turn off the multiplexing of address lines and send the address lines directly to the logic analyzer. Most observed microprocessors have the total address on the bus at the end of the cycle when the transparent position has no negative impact. If the RAS switches cannot be set up correctly, then no refresh cycles will be captured.

The transparent position (Trans) should also be used in timing mode.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

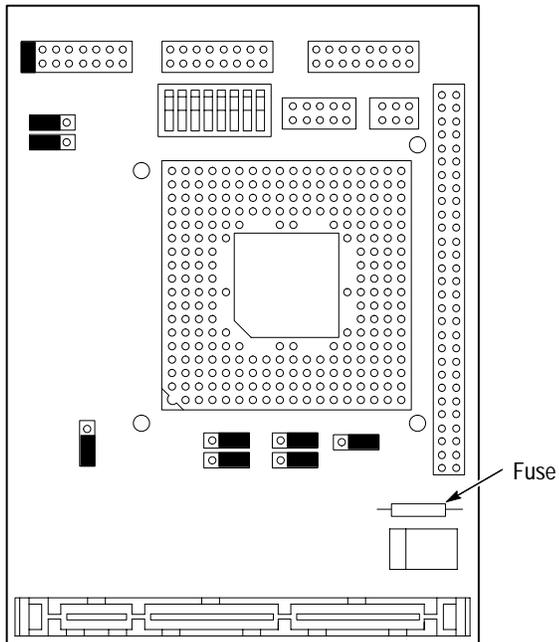
Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replacing the Fuse

If the fuse on the 68360 probe adapter opens (burns out), you can replace it with a 5 A, 125 V fuse. Figure 4–1 shows the location of the fuse on the probe adapter.

Low-profile probe adapter



Conventional probe adapter

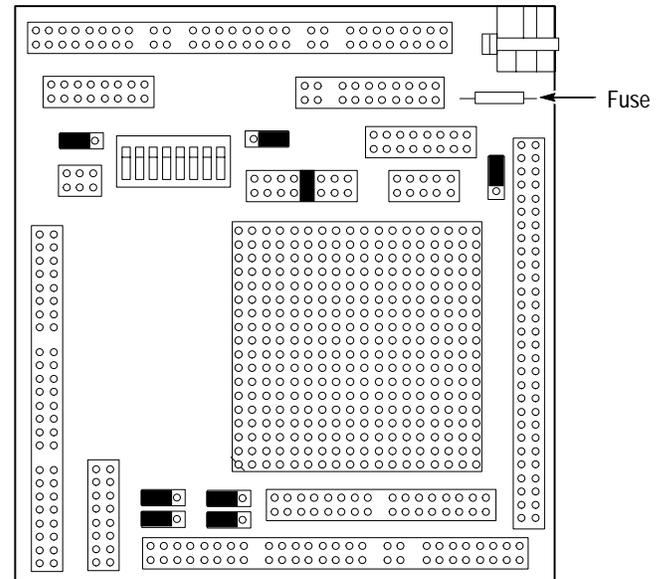


Figure 4–1: Location of the fuse



Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 261 68360 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105-3608
01295	TEXAS INSTRUMENTS INC	SEMICONDUCTOR GROUP 13500 N CENTRAL EXPRESSWAY PO BOX 655303	DALLAS, TX 75272-5303
04222	AVX/KYOCERA	PO BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA INC	SEMICONDUCTOR PRODUCTS SECTOR 5005 E MCDOWELL ROAD	PHOENIX, AZ 85008-4229
09969	DALE ELECTRONIC COMPONENTS	EAST HWY 50 P.O. BOX 180	YANKTON, SD 57078
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG, MD 20879
14310	AULT INC	7300 BOONE AVE NORTH BROOKLINE PARK	MINNEAPOLIS, MN 55428
26742	METHODE ELECTRONICS INC	BACKPLAIN DIVISION 7444 WEST WILSON AVE	CHICAGO, IL 60656-4548
34335	ADVANCED MICRO DEVICES INC	ONE AMD PLACE PO BOX 3453	SUNNYVALE, CA 94088-3453
50139	ALLEN-BRADLEY COMPANY	ELECTRONIC COMPONENTS DIVISION 1414 ALLEN BRADLEY DRIVE	EL PASO, TX 79936
50434	HEWLETT PACKARD	370 W TRIMBLE ROAD	SAN JOSE, CA 95131-1008
55420	DYSAN INTERNATIONAL	218 RAILROAD AVE	MILPITAS, CA 95035
61772	INTEGRATED DEVICE TECHNOLOGY	2975 STENDER WAY	SANTA CLARA, CA 95054
61857	SAN-O INDUSTRIAL CORP	91-3 COLIN DRIVE	HOLBROOK, NY 11741
63058	MCKENZIE TECHNOLOGY	910 PAGE AVE	FREMONT, CA 945387340
65786	CYPRESS SEMICONDUCTOR CORP	3901 N FIRST ST	SAN JOSE, CA 95134-1506
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077-0001
85480	BRADY USA	NAMEPLATE DIVISION P O BOX 571 346 ELIZABETH BRADY RD	HILLSBOROUGH, NC 27278
S3109	FELLER U.S. CORPORATION	72 VERONICA AVE UNIT #4	SOMERSET, NJ 08873
TK0875	MATSUO ELECTRONICS	2134 MAIN STREET SUITE 200	HUNTINGTON BEACH, CA 92648

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discontin'd	Name & description	Mfr. code	Mfr. part number
A02	671-3724-00			CIRCUIT BD ASSY:68360,PGA-241,SOCKETED, 32/92DM94	80009	671-3724-00
A02C1220	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C1300	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C1310	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C1320	290-5005-00			CAP,FXD,TANT:47UF,10%,10V,5.8MM X 4.6MM, 5846,SMD	TK0875	267M-1002-476-KR-533
A02C1325	290-5005-00			CAP,FXD,TANT:47UF,10%,10V,5.8MM X 4.6MM, 5846,SMD	TK0875	267M-1002-476-KR-533
A02C1345	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C1365	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C1445	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C1455	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C1580	290-5005-00			CAP,FXD,TANT:47UF,10%,10V,5.8MM X 4.6MM, 5846,SMD	TK0875	267M-1002-476-KR-533
A02C1600	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C1630	290-5005-00			CAP,FXD,TANT:47UF,10%,10V,5.8MM X 4.6MM, 5846,SMD	TK0875	267M-1002-476-KR-533
A02C1633	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C1650	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C1660	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C1700	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C2180	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C2290	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C2350	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C2390	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C2490	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C2590	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discount'd	Name & description	Mfr. code	Mfr. part number
A02C2640	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C2650	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02C2670	283-5114-00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD	04222	12065C104KAT (1A OR 3A)
A02CR1575	152-5045-00			DIODE,SIG:SCHTKY,20V,1.2PF,24 OHM	50434	HSMS-2810-T31
A02CR1620	152-5045-00			DIODE,SIG:SCHTKY,20V,1.2PF,24 OHM	50434	HSMS-2810-T31
A02CR1630	152-5045-00			DIODE,SIG:SCHTKY,20V,1.2PF,24 OHM	50434	HSMS-2810-T31
A02CR1635	152-5045-00			DIODE,SIG:SCHTKY,20V,1.2PF,24 OHM	50434	HSMS-2810-T31
A02F1670	159-0059-00			FUSE,WIRE LEAD:5A,125V	61857	SPI-5A
A02J1120	131-5267-00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR	00779	104326-4
A02J1140	131-5267-00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR	00779	104326-4
A02J1160	131-5267-00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR	00779	104326-4
A02J1180	131-5267-00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR	00779	104326-4
A02J1185	131-5267-00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR	00779	104326-4
A02J1200	131-4530-00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR	00779	104344-1
A02J1205	131-4530-00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR	00779	104344-1
A02J1490	131-5267-00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR	00779	104326-4
A02J1520	131-4530-00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR	00779	104344-1
A02J1540	131-4530-00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR	00779	104344-1
A02J1545	131-4530-00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR	00779	104344-1
A02J1550	131-4530-00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR	00779	104344-1
A02J1555	131-4530-00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR	00779	104344-1
A02J1560	131-4530-00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR	00779	104344-1
A02J1680	131-5527-00			JACK,POWER DC:PCB,MALE,RTANG,2MM PIN,11MM H(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWI	0LXM2	DJ005A
A02J1700	131-5947-00			CONN,BOX:PCB,MICRO-STRIP,FEMALE,STR,100 POS,0.05 CTR	00779	121289-7
A02P1120	131-4356-00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER	26742	9618-302-50
A02P1200	131-4356-00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER	26742	9618-302-50
A02P1205	131-4356-00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER	26742	9618-302-50
A02P1520	131-4356-00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER	26742	9618-302-50
A02P1540	131-4356-00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER	26742	9618-302-50

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A02P1545	131-4356-00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER	26742	9618-302-50
A02P1550	131-4356-00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER	26742	9618-302-50
A02P1555	131-4356-00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER	26742	9618-302-50
A02P1560	131-4356-00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER	26742	9618-302-50
A02R1100	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R1105	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R1110	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R1115	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R1215	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R1216	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R1218	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R1220	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R1410	321-5051-00			RES,FXD:THICK FILM,0 OHM,1%,0.125W	09969	CRCW1206 JUMPER
A02R1415	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R1420	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02R1535	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R1640	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R1650	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R1655	321-5030-00			RES,FXD:THICK FILM,10.0K OHM,1%,0.125W	50139	BCK1002FT
A02R2180	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02R2181	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02R2185	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02R2186	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02R2190	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02R2195	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02R2197	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02R2285	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02R2360	321-5002-00			RES,FXD:THICK FILM,15 OHM,1%,0.125W	50139	BCD15R0FT
A02R2380	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02R2385	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02R2387	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02R2388	321-5026-00			RES,FXD:THICK FILM,4.75K OHM,1%,0.125W	50139	BCK4751FT
A02S1140	260-1721-00			SWITCH,ROCKER:8,SPST,125MA,30VDC	00779	5-435166-3
A02U1120	156-5500-00			IC,DIGITAL:FTTL,GATES,8-INPUT NAND	01295	SN74F30D

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A02U1310	160-9952-00			IC,DIGITAL:STTL,PLD,PAL,20L8,210MA,10NS	80009	160-9952-00
A02U1420	156-6514-01			IC,DIGITAL:FCTCMOS,TRANSCEIVER,18-BIT REGISTERED,RESISTOR TERMINATED OUTPUTS	61772	IDT74FCT162501ATP V
A02U1510	163-0593-00			IC,DIGITAL:STTL,PLD,PAL,20L8,5NS,210MA	80009	163-0593-00
A02U1610	160-9951-01			IC,DIGITAL:CMOS,PLD,OTP,22V10,10NS,71MHZ,180MA	80009	160-9951-00
A02U1640	156-7112-00			IC DIGITAL:FCTCMOS,BUFFER,16-BIT, RESISTOR TERMINATED OUTPUTS,3-STATE	80009	156-7112-00
A02U1650	156-7112-00			IC DIGITAL:FCTCMOS,BUFFER,16-BIT, RESISTOR TERMINATED OUTPUTS,3-STATE	80009	156-7112-00
A02U1660	156-7112-00			IC DIGITAL:FCTCMOS,BUFFER,16-BIT, RESISTOR TERMINATED OUTPUTS,3-STATE	80009	156-7112-00
A02U2180	156-5253-00			IC,DIGITAL:FTTL,MUX/ENCODER,8-TO-3 LINE PRIORITY	04713	MC74F148D
A02U2350	160-9949-00			IC,DIGITAL:CMOS,PLD,EEPLD,16V8,7.5NS,130MA	80009	160-9949-00
A02U2390	160-9950-01			IC,DIGITAL:CMOS,PLD,OTP,22V10,10NS,71MHZ,180MA	80009	160-9950-00
A02U2490	156-6514-01			IC,DIGITAL:FCTCMOS,TRANSCEIVER,18-BIT REGISTERED,RESISTOR TERMINATED OUTPUTS	61772	IDT74FCT162501ATP V
A02U2590	160-9953-00			IC,DIGITAL:STTL,PLD,PAL,20L8,210MA,10NS	80009	160-9953-00
A02U2645	156-7112-00			IC DIGITAL:FCTCMOS,BUFFER,16-BIT, RESISTOR TERMINATED OUTPUTS,3-STATE	80009	156-7112-00
A02U2660	156-7112-00			IC DIGITAL:FCTCMOS,BUFFER,16-BIT, RESISTOR TERMINATED OUTPUTS,3-STATE	80009	156-7112-00
A02U2670	156-7112-00			IC DIGITAL:FCTCMOS,BUFFER,16-BIT, RESISTOR TERMINATED OUTPUTS,3-STATE	80009	156-7112-00
A02U2690	160-9954-00			IC,DIGITAL:STTL,PLD,PAL,20L8,210MA,10NS	80009	160-9954-00
A02W1700	174-3418-00			CA ASSY,RF:TLC,MICRO-STRIP,TLC,50 OHM	00779	1-340014-0

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATION

SYMBOLS

Graphic symbol and class designation letters are based on ANSI Y32.14, 1973 in terms of positive logic. Logic symbols are depicted according to the manufacturer's data book information (not according to function).

Letter symbols for quantities used in electrical science and electrical engineering are based on ANSI Y10.5, 1968.

Drafting practices, line conventions, and lettering conform to ANSI Y14.12, 1966 and ANSI Y14.2, 1973.

Abbreviations are based on ANSI Y1.1, 1972.

You can inquire about these ANSI standards by contacting:

American National Standard Institute
1430 Broadway
New York, New York 10018

COMPONENT VALUES

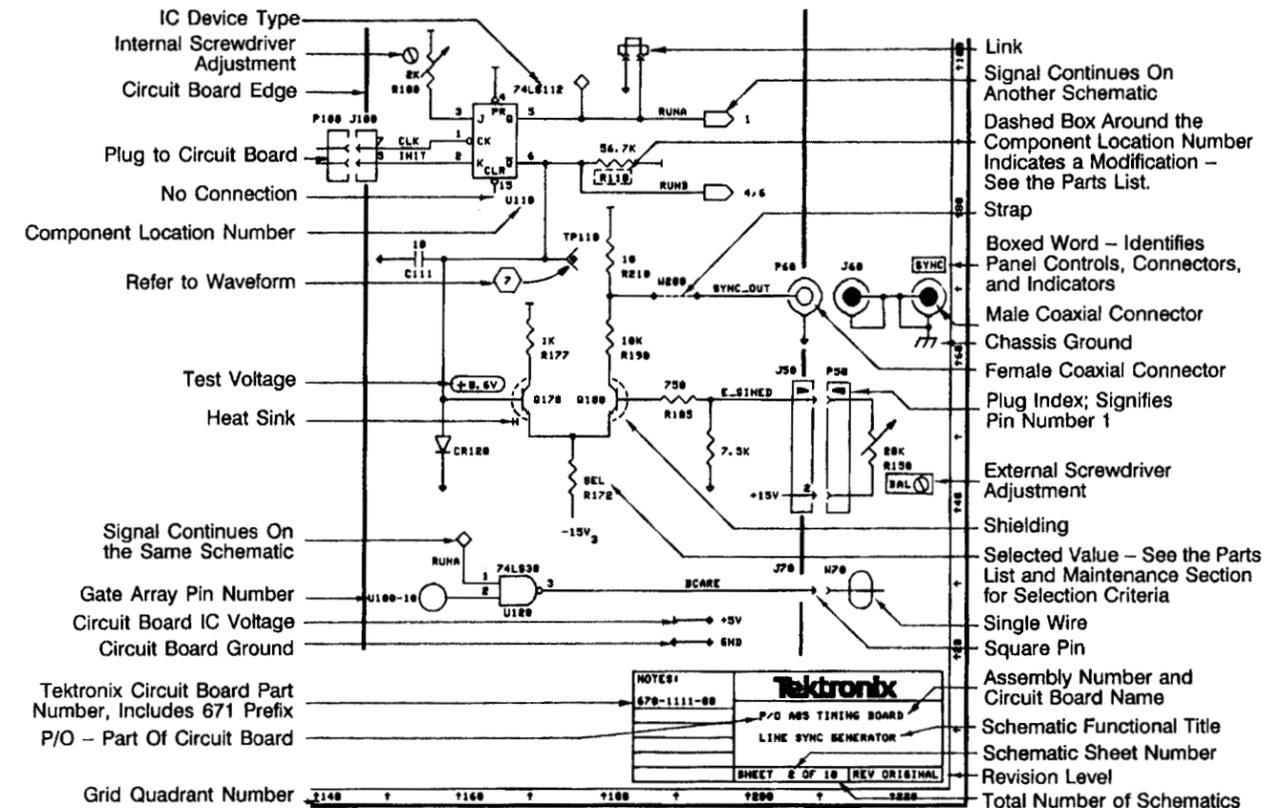
Electrical components shown on the diagram are in the following units unless noted otherwise:

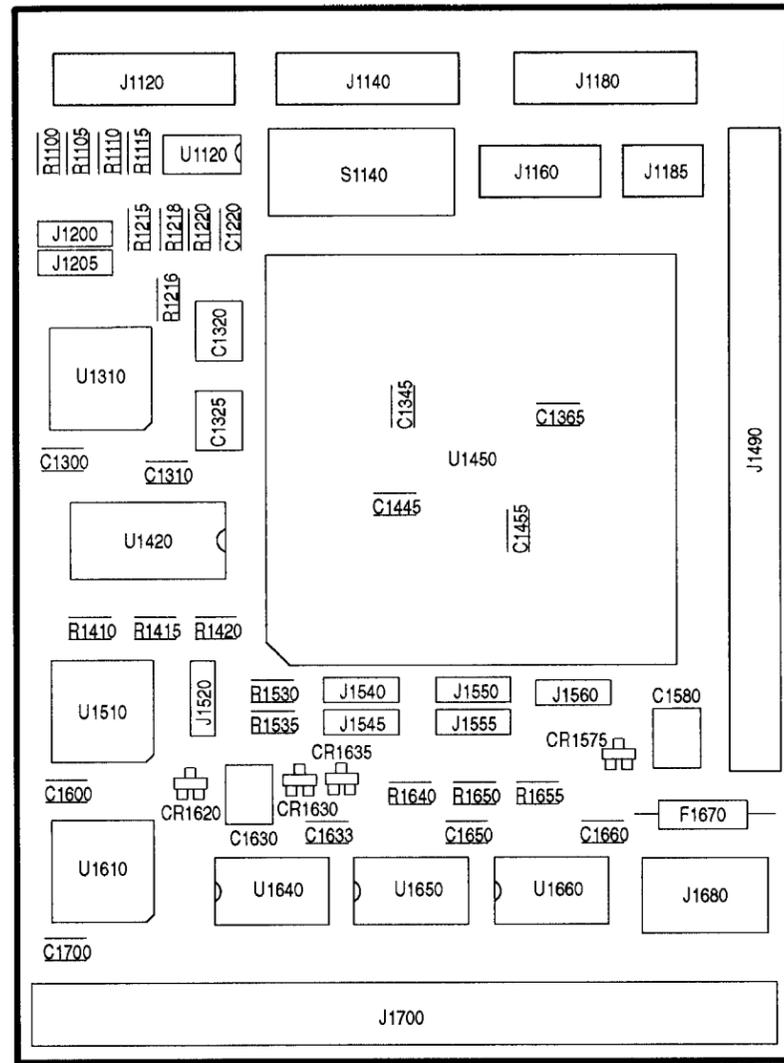
Capacitors = Values one or greater are in picofarads (pF)
Values less than one are in microfarads (μF)

Resistors = Ohms (Ω)

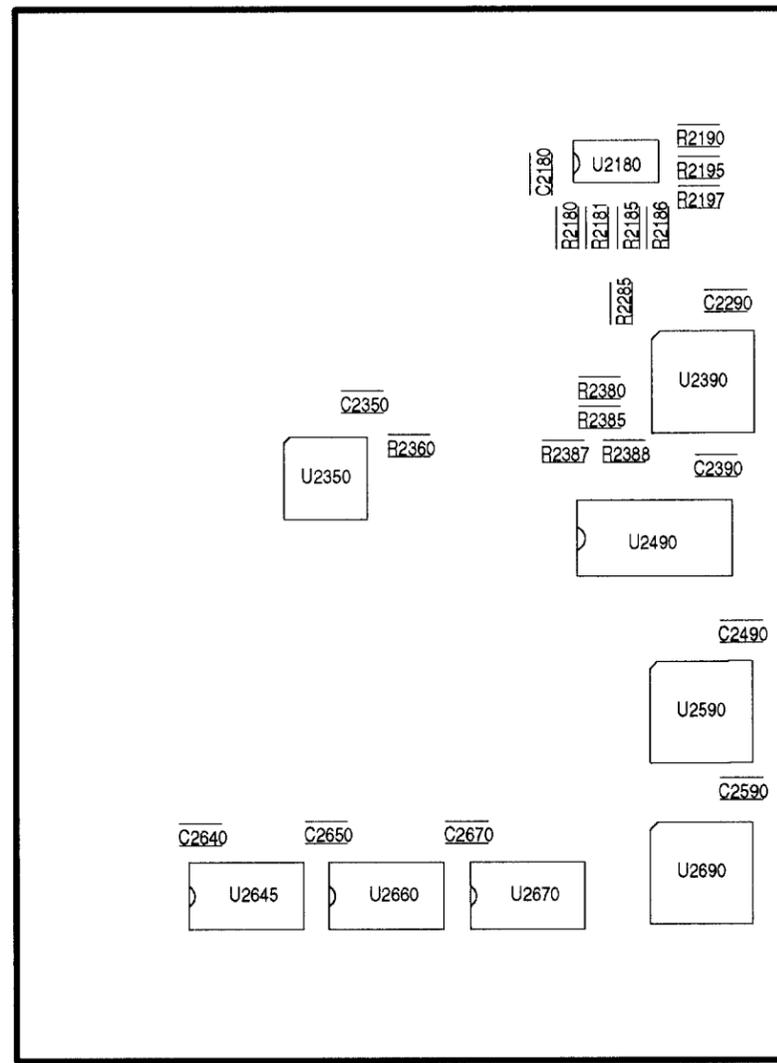
ACTIVE-LOW SIGNAL INDICATORS

A common convention used for indicating an active-low signal (a signal performing its intended function when it is in a low state) is an overbar, as shown in the signal name $\overline{\text{RESET}}$. The overbar may be used in this manual whenever a reference is given to an active-low signal. However, the same active-low signal is indicated on the schematic with a tilde (~), or a slash (/) following the signal name (e.g., RESET ~ or RESET*).



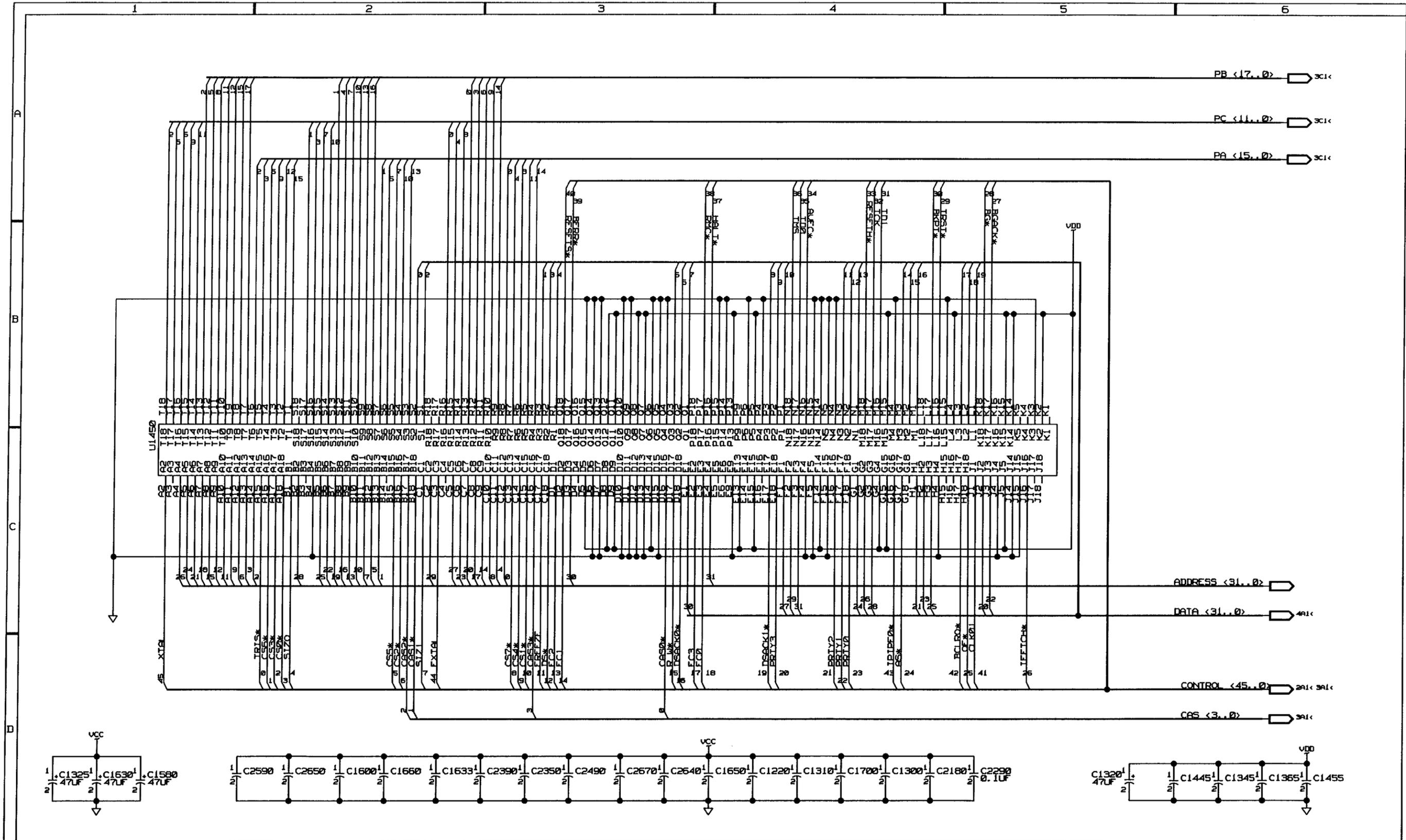


Front



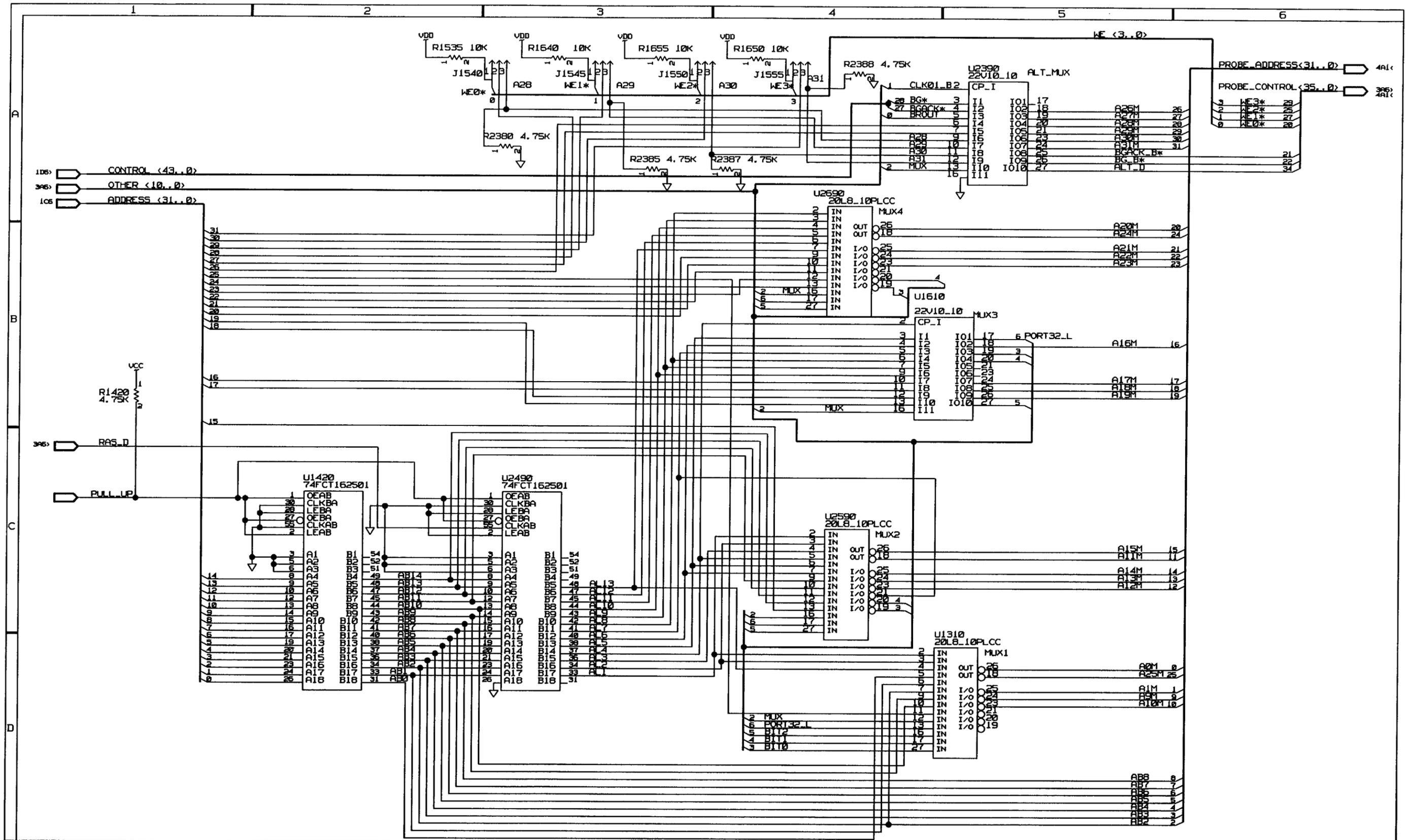
Back

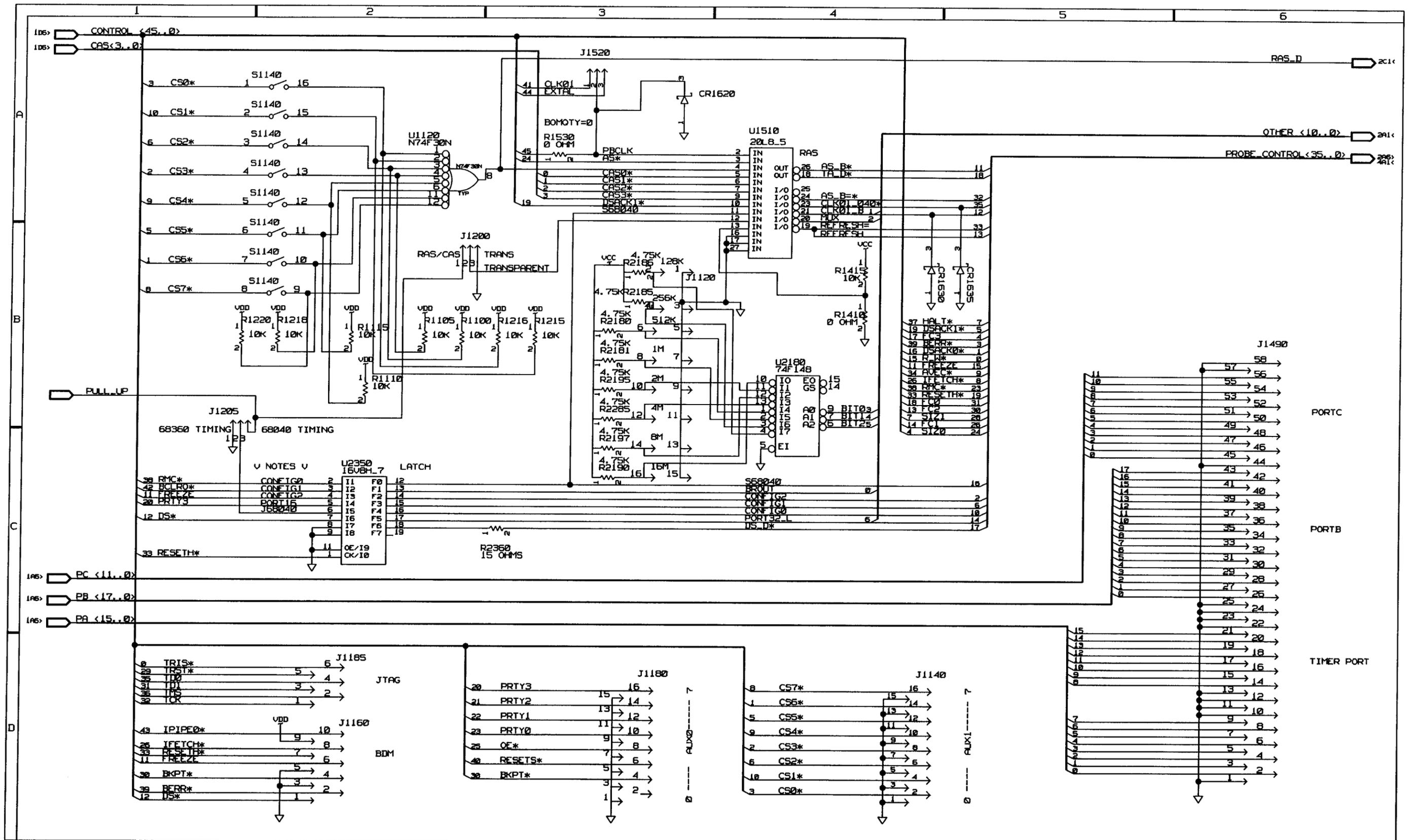
68360 probe adapter board component locations



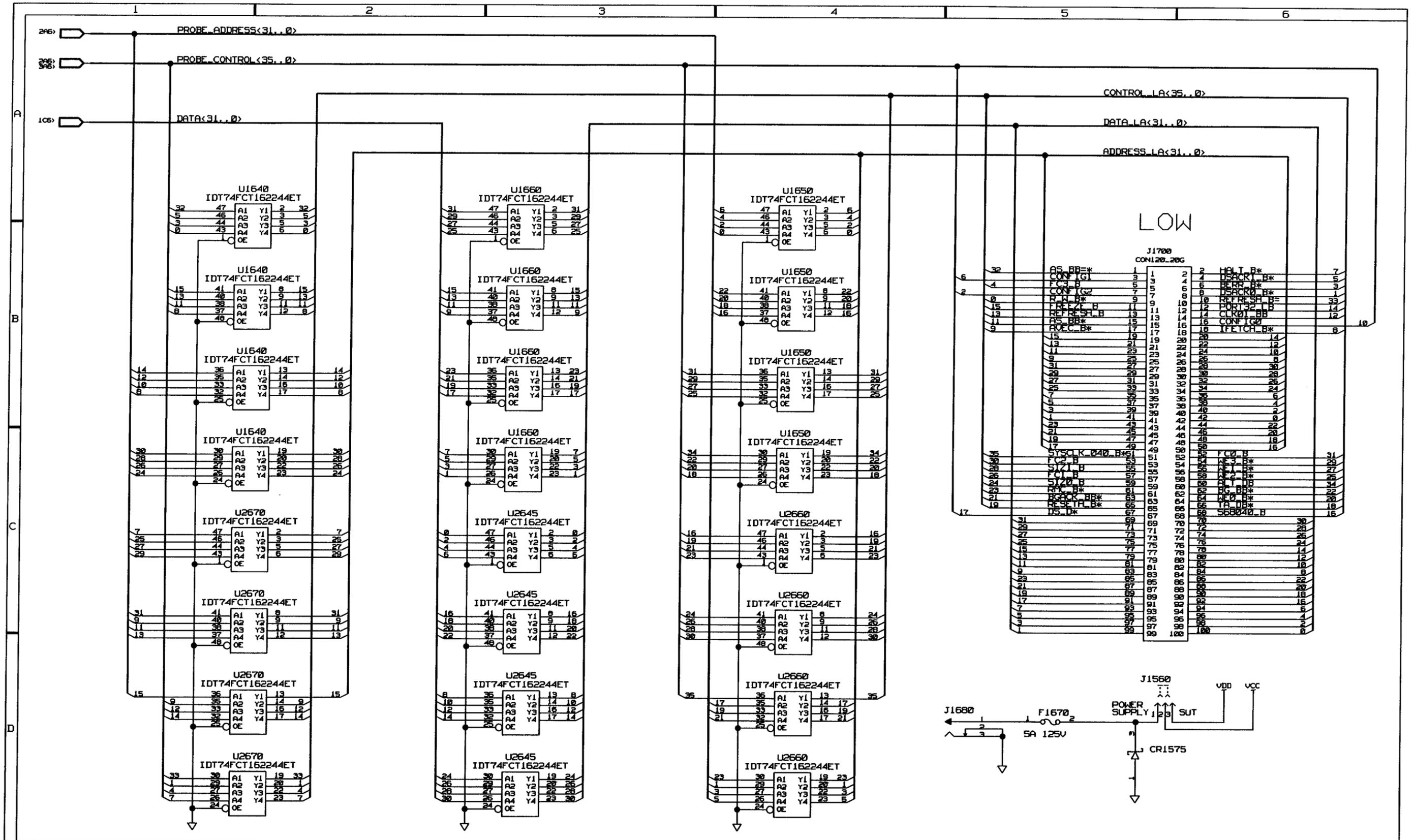
68360 PROBE ADAPTER

PROCESSOR SOCKET AND DECOUPLING A02





68350 PROBE ADAPTER



68360 PROBE ADAPTER

BUFFERS AND HIGH DENSITY CABLE HEADER A02



Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 261 68360 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1-1972.

Chassis Parts Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105-3608
01295	TEXAS INSTRUMENTS INC	SEMICONDUCTOR GROUP 13500 N CENTRAL EXPRESSWAY PO BOX 655303	DALLAS, TX 75272-5303
04222	AVX/KYOCERA	PO BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA INC	SEMICONDUCTOR PRODUCTS SECTOR 5005 E MCDOWELL ROAD	PHOENIX, AZ 85008-4229
09969	DALE ELECTRONIC COMPONENTS	EAST HWY 50 P.O. BOX 180	YANKTON, SD 57078
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG, MD 20879
14310	AULT INC	7300 BOONE AVE NORTH BROOKLINE PARK	MINNEAPOLIS, MN 55428
26742	METHODE ELECTRONICS INC	BACKPLAIN DIVISION 7444 WEST WILSON AVE	CHICAGO, IL 60656-4548
50139	ALLEN-BRADLEY COMPANY	ELECTRONIC COMPONENTS DIVISION 1414 ALLEN BRADLEY DRIVE	EL PASO, TX 79936
50434	HEWLETT PACKARD	370 W TRIMBLE ROAD	SAN JOSE, CA 95131-1008
61772	INTEGRATED DEVICE TECHNOLOGY	2975 STENDER WAY	SANTA CLARA, CA 95054
61857	SAN-O INDUSTRIAL CORP	91-3 COLIN DRIVE	HOLBROOK, NY 11741
63058	MCKENZIE TECHNOLOGY	910 PAGE AVE	FREMONT, CA 945387340
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077-0001
S3109	FELLER U.S. CORPORATION	72 VERONICA AVE UNIT #4	SOMERSET, NJ 08873
TK0875	MATSUO ELECTRONICS	2134 MAIN STREET SUITE 200	HUNTINGTON BEACH, CA 92648

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
-1-0	010-0594-00			1	PROBE ADAPTER:68360,SOCKETED,PROBE ADAPTER, TMS 261	80009	010-0594-00
-1	174-3418-00			1	CA ASSY,RF:TLC,MICRO-STRIP,TLC,50 OHM	00779	1-340014-0
-2	131-5267-00			2	CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J1120, J1160, J1185, J1140, J1180, J1490)	00779	104326-4
-3	260-1721-00			1	SWITCH,ROCKER:8,SPST,125MA,30VDC (S1140)	00779	5-435166-3
-4	671-3724-00			1	CIRCUIT BD ASSY:68360,PGA-241,SOCKETED	80009	671-3724-00
-5	136-1262-00			2	SOCKET,PGA:PCB,241 POS,18 X 18,0.1 CTR,0.165 H X 0.180 TAIL,GOLD/GOLD,PAT1849,ULTRA LOW IN	63058	PGA241H120B5-18 49R
-6	131-5947-00			1	CONN,BOX:PCB,MICRO-STRIP,FEMALE,STR,100 POS,0.05 CTR,W/GRD PLANE,0.320 H X 0.125 TAIL,LAT	00779	121289-7
-7	131-4530-00			8	CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION (J1200, J1205, J1520, J1540, J1545, J1550, J1555, J1560)	00779	104344-1
-8	131-4356-00			9	CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR, 0.63 H,BLK,W/HANDLE,JUMPER,	26742	9618-302-50
-9	131-5527-00			1	JACK,POWER DC:PCB,MALE,RTANG,2MM PIN	0LXM2	DJ005A
-10	159-0059-00			1	FUSE,WIRE LEAD:5A,125V (F1670)	61857	SPI-5A
					STANDARD ACCESSORIES		
	070-9825-01			1	MANUAL,TECH:INSTRUCTION,68360,DISSASSEMBLER, TMS 261	80009	070-9825-01
	070-9803-00			1	MANUAL,TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070-9803-00
					OPTIONAL ACCESSORIES		
	070-9802-00			1	MANUAL,TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070-9802-00
	119-5061-01			1	POWER SUPPLY:25W,5V 5A,CONCENTRIC 2MM,90-265V,47-63HZ (NOT SHOWN)	14310	SW106KA002F01
	161-0104-00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,98 INCH, RTANG,IEC320,RCPT X STR,NEMA 15-5P,W/CORD GRIP	S3109	ORDER BY DE- SCRIPTION
	161-0104-06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, EUROPEAN,SAFETY CONTROLLED (OPT A1)	S3109	ORDER BY DE- SCRIPTION
	161-0104-07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10AMP,2.5 METER, RTANG,IEC320,RCPT X 13A, FUSED, UK PLUG, (13A FUSE), UNITED KINGDOM,SAFETY CONTROL (OPT A2)	S3109	ORDER BY DE- SCRIPTION
	161-0104-05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, AUSTRALIA,SAFETY CONTROLLED (OPT A3)	S3109	ORDER BY DE- SCRIPTION
	161-0167-00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, SWISS,NO CORD GRIP, SAFETY CONTROLLED (OPT A5)	S3109	ORDER BY DE- SCRIPTION

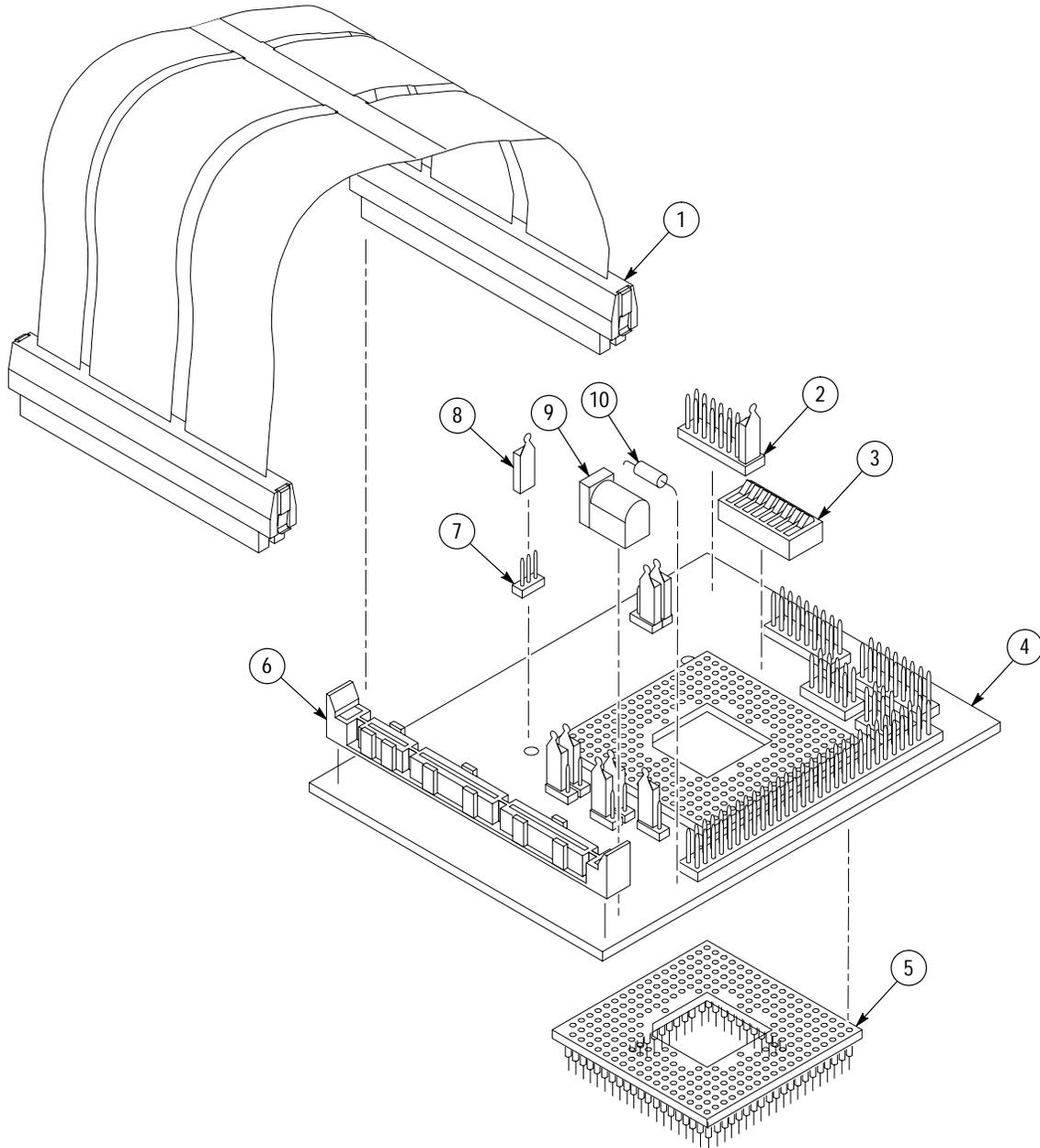


Figure 6-1: 68360 low-profile probe adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
2-0	010-0577-00			1	PROBE ADAPTER:68360,PGA241 SOCKETED, PROBE ADAPTER;TMS 261	80009	010057700
-1	131-4356-00			8	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2, 0.1 CTR, 0.630 H,BLK,W/HANDLE,JUMPER (P1210,P1255,P1260,P1290,P1630,P1635,P1640,P1645)	26742	9618-302-50
-2	131-4530-00			7	CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION,HIGH TEMP (J1210,J1255,J1290,J1630,J1635,J1640,J1645)	00779	104344-1
-3	343-0549-00			1	STRAP,TIEDOWN,E:0.098 W X 4.0 L,ZYTEL	TK1499	HW-047
-4	159-0059-00			1	FUSE,WIRE LEAD 5A,125V (F1)	61857	SPI-5A
-5	131-5148-00			1	JACK,POWER DC:PCB,;MALE,RTANG,2.0 MM DIA PIN, 7 MM H X 3.3 MM TAIL,3 COND,W/SWITCH, MTGPOST,DC PWR JACK,1 AMP@12V (JR1190)	TK2427	ADC-016
-6	260-1721-00			1	SWITCH,ROCKER:8,SPST,125MA,30VDC (S1230)	81073	76SB08S
-7	136-1262-00			2	SOCKET,PGA:PCB,;241 POS,18 X 18,0.1 CTR, 0.165 H X 0.180 TAIL,GOLD/GOLD,PAT1849,ULTRA LOW INSERTION (U1540)	80009	PGA241H120B5-18 49R
-8	671-3223-00			1	CIRCUIT BD ASSY:68360,PGA241,SOCKETED;	80009	671322300
-9	131-5267-00			5	CONN,HDR PCB,;MALE,STR,2 X 40,0.1 CTR,0.23,5 MLG X 0.110 TAIL,30GOLD; (J1110,J1180,J1185,J1215,J1260,J1280,J1285,J1300,J1520, J1650,J1730,J1790)	53387	N2480-6122-TB
STANDARD ACCESSORIES							
	070-9825-00			1	MANUAL, TECH:INSTRUCTION,68360,DISSASSEMBLER, TMS 261	80009	070-9825-00
	070-9803-00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070-9803-00
OPTIONAL ACCESSORIES							
	070-9802-00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070-9802-00
	119-5061-01			1	POWER SUPPLY:25W,5V 5A,CONCENTRIC 2MM,90-265V,47-63HZ (NOT SHOWN)	14310	SW106KA002F01
	161-0104-00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,98 INCH, RTANG,IEC320,RCPT X STR,NEMA 15-5P,W/CORD GRIP	S3109	ORDER BY DE- SCRIPTION
	161-0104-06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, EUROPEAN,SAFETY CONTROLLED (OPT A1)	S3109	ORDER BY DE- SCRIPTION
	161-0104-07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10AMP,2.5 METER, RTANG,IEC320,RCPT X 13A, FUSED, UK PLUG, (13A FUSE), UNITED KINGDOM,SAFETY CONTROL (OPT A2)	S3109	ORDER BY DE- SCRIPTION
	161-0104-05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, AUSTRALIA,SAFETY CONTROLLED (OPT A3)	S3109	ORDER BY DE- SCRIPTION
	161-0167-00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, SWISS,NO CORD GRIP, SAFETY CONTROLLED (OPT A5)	S3109	ORDER BY DE- SCRIPTION

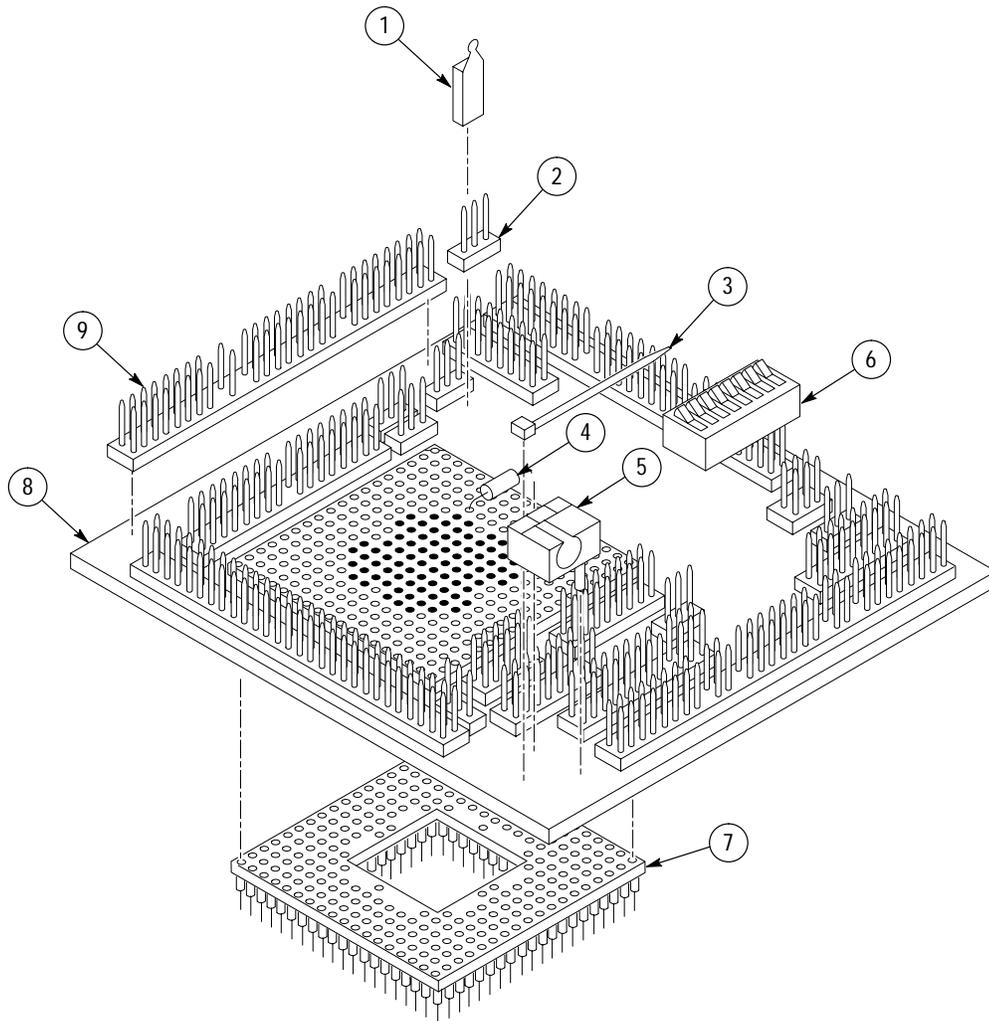


Figure 6-2: 68360 conventional probe adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
3-0	010-0582-00			1	ADAPTER,PROBE:192-CHANNEL,HIGH DENSITY PROBE	80009	010058200
-1	380-1095-00			1	HOUSING,HALF:UPPER,192 CHANNEL HIGH DENSITY PROBE	80009	380109500
-2	211-0152-00			4	SCR,ASSEM WSHR:4-40 X 0.625,PNH,BRS,NP,POZ	TK0435	ORDER BY DESC
-3	131-5947-00			2	CONN BOX:CPCB, MICRO-STRIP;FEMALE,STR,100 POS,0.05 CTR,W/GRD PLANE,0.320 H X 0.124 TAIL, LATCHING, 4 ROW, 0.05 PCB, STAGGER (J150, J250)	80009	131594700
-4	671-3395-00			1	CKT BD ASSY:192-CHANNELS,HIGH DENSITY PROBE	80009	671339500
-5	380-1096-00			1	HOUSING,HALF:LOWER,192 CHANNEL HIGH DENSITY PROBE	80009	380109600
-6	348-0070-01			2	PAD,CUSHIONING:2.03 X 0.69 X 0.18 SI RBR	85471	ORDER BY DESC
-7	131-4917-00			8	CONN,HDR CPCB,;MALE,STR,1 X 2,0.1 CTR,0.235 MLF X 0.110 TAIL,20 BOLD, TUBE, HIGH TEMP (J300,J340,J400,J440,J500,J640,J600)	53387	131491700
-8	131-5267-00			5	CONN,HDR CPCB,;MALE,STR,2 X 40.O.1 CTR,0.234 MLG X 0.110 TAIL, 30 GOLD (J310,J320,J330,J340,J350,J360,J370,J410,J420,J430,J450,J460,J470,J510,J520,J530,J550,J560,J570,J610,J620,J630,J650,J660,J670)	53387	131526700

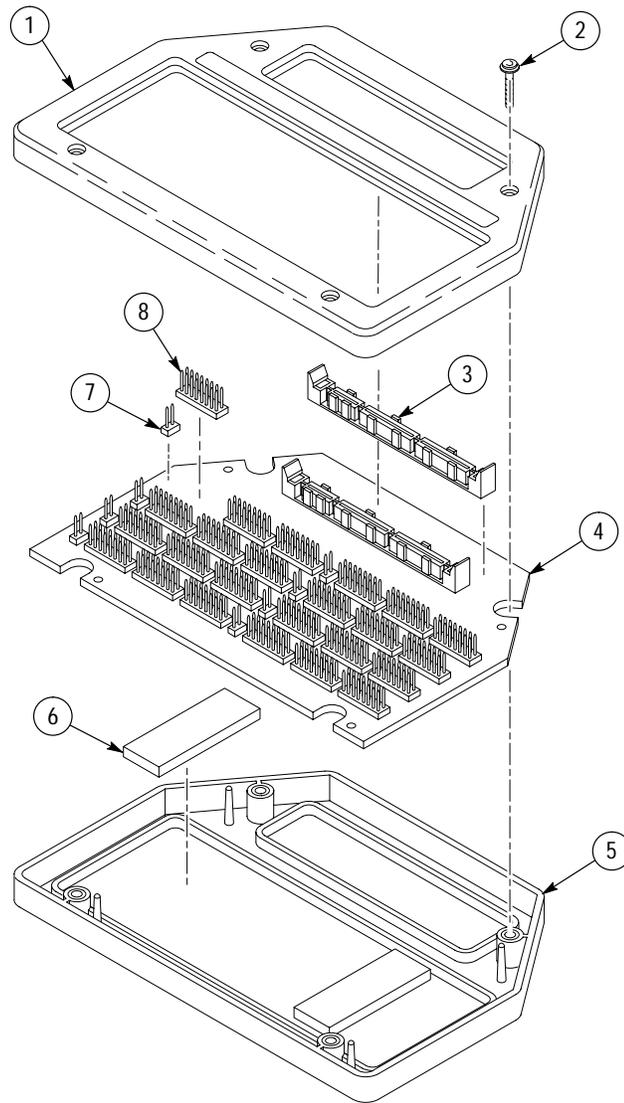


Figure 6-3: 192-Channel High-Density Probe exploded view



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