Instruction Manual

Tektronix

TMS 220
MCF5202/03 Microprocessor Support

070-9956-00

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 220 MCF5202/03 microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 220 MCF5202/03 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to your SUT (system under test)
- Setting up the logic analyzer to acquire data from your SUT
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- The term “5202/03” refers to all supported variations of the MCF5202/03 microprocessor unless otherwise noted.
- In the information on basic operations, the term “XXX” or “P54C” used in field selections and file names must be replaced with 5202/03. This is the name of the microprocessor in field selections and file names you must use to operate the MCF5202/03 support.

- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.
- The term “SUT” (system under test) refers to the microprocessor-based system from which data will be acquired.
- A tilde (~) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter contains information on the TMS 220 microprocessor support, and information on connecting your logic analyzer to your system under test.

Support Description

The TMS 220 microprocessor support package disassembles data from systems that are based on the Motorola MCF5202 and MCF5203 microprocessors.

The TMS 220 supports the MCF5202 and MCF5203 microprocessors in a 100-pin TQFP package.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the following documents:

- *Coldfire MCF5202/03 Specification*, Motorola High Performance Embedded Systems Division, 1995.
- *MCF5200 Family Programmer's Reference Manual*, Motorola, 1995.
- *MC68030 Enhanced 32-bit Microprocessor User's Manual*, Motorola, 1989.
- *MC68040 32-bit Microprocessor User's Manual*, Motorola, 1989.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

For use with a TLA 700 Series, the TMS 220 support requires a minimum of one 96-channel module.

For use with a DAS 9200 Series, the TMS 220 support requires a minimum of one 96-channel module.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other MCF5202/03 support requirements and restrictions.

System Clock Rate. The TMS 220 support can acquire data from the MCF5202/03 microprocessor at speeds of up to 33 MHz[1].

Hardware Reset. If a hardware reset occurs in your MCF5202/03 system during an acquisition, the disassembler may acquire an invalid sample.

Cache Invalidation. Correct disassembly is not guaranteed for microprocessor systems that run cache invalidations concurrent with burst cycles. Data for these cycles will not be disassembled and will be labeled as Cache Invalidation cycles.

Disabling the Internal Cache. To disassemble acquired data, you must disable the internal cache. Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled.

Big-Endian Byte Ordering. The disassembler always uses Big-Endian byte ordering for instruction disassembly. Big-Endian byte ordering is when the most significant data byte is located at the highest address.

Data Reads and Writes. The disassembler will not link data reads and writes with the instructions which cause them.

Connecting to a System Under Test With A Probe Adapter

To connect the logic analyzer to a SUT using the probe adapter and test clip, follow these steps:

1. Turn off power to your SUT.

   It is not necessary to turn off the logic analyzer.

1 **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the logic analyzer.

Connect The Test Clip To The Probe Adapter

To connect the test clip to the probe adapter follow these steps:

3. Line up pin 1 on the test clip, to pin 1 on the connector located on the bottom of the probe adapter circuit board, as shown in Figure 1–1.

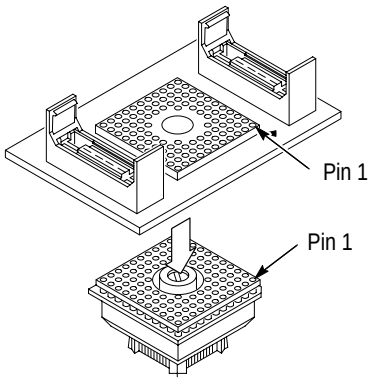


Figure 1–1: Connecting the test clip to the probe adapter

Connect the P6434 Probes To The Probe Adapter

To connect the P6434 probes to the probe adapter follow these steps:

CAUTION. *Incorrect handling of the P6434 probe while connecting it to the probe adapter can result in damage to the probe or to the mating connector on the probe adapter. To avoid damaging the probe and probe adapter, always position the probe perpendicular to the mating connector and gently connect the probe.*

4. Refer to Figure 1–2, and connect the P6434 probes to the probe adapter. Match the channel groups and numbers on the probe labels to the corresponding connectors on the probe adapter.

5. Position the probe tip perpendicular to the mating connector and gently connect the probe as shown in Figure 1–2.

6. When connected, push down the latch releases on the probe to set the latch.

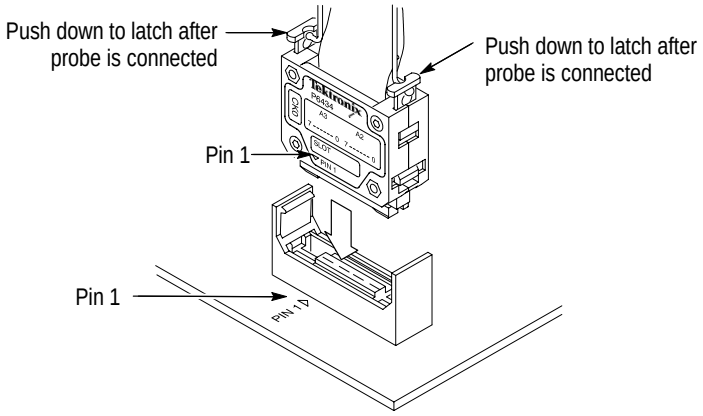


Figure 1–2: Connecting P6434 probes to the probe adapter

Connect The Probe Adapter Assembly To The System Under Test

To connect the probe adapter assembly (probe adapter and test clip) to your SUT follow these instructions:

7. Inspect the microcontroller on you SUT for bent or broken leads. Verify that the leads on the microcontroller are clean and free from dirt, dust, or any foreign material.
8. Inspect the pins of the test clip for bent or broken contacts. Verify that the leads on the test clip are clean and free from dirt, dust or any foreign material.
9. Verify that the locking devise on the test clip is not locked by turning the locking device with a small screwdriver counter-clockwise.
10. Place the probe adapter onto the SUT as shown in Figure 1–3.

CAUTION. *Failure to correctly place the probe adapter onto the microprocessor might permanently damage all electrical components when power is applied. Center the clip on the microprocessor and apply an equal downward force on all four sides of the clip. It is important to keep the TQFP test clip parallel to the microprocessor to avoid damage to the SUT or TQFP test clip.*
Do not apply leverage to the probe adapter when installing or removing it.

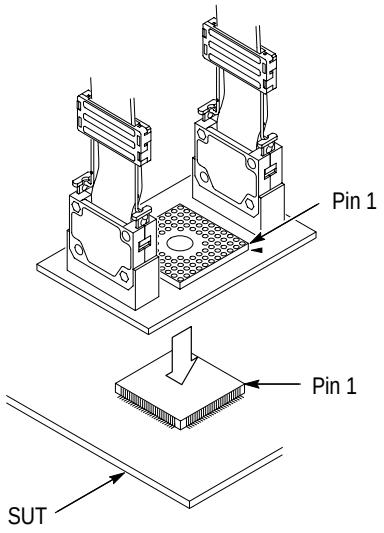


Figure 1–3: Placing the probe adapter onto the SUT

CAUTION. *The test clip was designed to be used on one and only one microprocessor. Because of the tight tolerances required for QFP test clip connectivity, the test clip that attaches to the microprocessor has a soft plastic collar that conforms to the unique shape of the target microprocessor.*

To avoid faulty and unreliable connections, do not use the test clip on any other microprocessor then the one it was originally connected to.

11. Lock the test clip to the microcontroller by turning the locking knob clockwise with a small screwdriver.

CAUTION. *The probe adapter board might slip off or slip to one side of the microprocessor because of the extra weight of the probes. This can damage the microprocessor and the SUT. To prevent this from occurring, stabilize the probe adapter by placing a non-conductive object (such as non-conductive foam) between the probe adapter and the SUT.*

Removing the Probe Adapter from the SUT

To remove the probe adapter from the sut follow these steps:

1. Unlock the test clip from the microcontroller by turning the locking knob counter-clockwise with a small screwdriver.

2. Gently lift and pull the probe adapter off of the microcontroller.

Connecting to a System Under Test Without A Probe Adapter

You can use the channel and clock probes and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT. To connect probes to MCF5202/03 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.
3. Table 1–1 through Table 1–8 shows the channel probes the MCF5202/03 signal pins on the test clip or in the SUT to connect to.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

NOTE*. Since the microprocessor multiplexes address A31-A0 and data D31-D0 (as the AD31-AD0 signals), the D3:7-0, D2:7-0, D1:7-0 and D0:7-0 channel probes do not need to be connected.*

These channels are not considered to be extra channels, even though they are not connected. Do not use them to make connections to other signals in your SUT.

4. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the MCF5202/03 microprocessor in your SUT and attach the clip.

Channel Assignments

The following channel assignment tables show the probe section and channel assignments, and the signal to which each channel connects. Channel assignments shown in Table 1–1 through Table 1–8 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.

By default, the Address group is displayed in hexadecimal.

Table 1–1: Address group channel assignments

Bit order	Section:channel	MCF5202/03 signal name
31	A3:7	AD31
30	A3:6	AD30
29	A3:5	AD29
28	A3:4	AD28
27	A3:3	AD27
26	A3:2	AD26
25	A3:1	AD25
24	A3:0	AD24
23	A2:7	AD23
22	A2:6	AD22
21	A2:5	AD21
20	A2:4	AD20
19	A2:3	AD19
18	A2:2	AD18
17	A2:1	AD17
16	A2:0	AD16
15	A1:7	AD15
14	A1:6	AD14
13	A1:5	AD13
12	A1:4	AD12
11	A1:3	AD11
10	A1:2	AD10
9	A1:1	AD9
8	A1:0	AD8

Table 1–1: Address group channel assignments (cont.)

Bit order	Section:channel	MCF5202/03 signal name
7	A0:7	AD7
6	A0:6	AD6
5	A0:5	AD5
4	A0:4	AD4
3	A0:3	AD3
2	A0:2	AD2
1	A0:1	AD1
0	A0:0	AD0

NOTE. *Since the microprocessor multiplexes address A31-A0 and data D31-D0 (as the AD31-AD0 signals), the D3:7-0, D2:7-0, D1:7-0 and D0:7-0 channel probes do not need to be connected.*

These channels are not considered to be extra channels, even though they are not connected. Do not use them to make connections to other signals in your SUT.

By default, the Data group is displayed in hexadecimal.

Table 1–2: Data group channel assignments

Bit order	Section:channel	MCF5202/03 signal name
31	D3:7	AD31
30	D3:6	AD30
29	D3:5	AD29
28	D3:4	AD28
27	D3:3	AD27
26	D3:2	AD26
25	D3:1	AD25
24	D3:0	AD24
23	D2:7	AD23
22	D2:6	AD22
21	D2:5	AD21
20	D2:4	AD20
19	D2:3	AD19
18	D2:2	AD18
17	D2:1	AD17
16	D2:0	AD16

Table 1–2: Data group channel assignments (cont.)

Bit order	Section:channel	MCF5202/03 signal name
15	D1:7	AD15
14	D1:6	AD14
13	D1:5	AD13
12	D1:4	AD12
11	D1:3	AD11
10	D1:2	AD10
9	D1:1	AD9
8	D1:0	AD8
7	D0:7	AD7
6	D0:6	AD6
5	D0:5	AD5
4	D0:4	AD4
3	D0:3	AD3
2	D0:2	AD2
1	D0:1	AD1
0	D0:0	AD0

By default, the Control group is displayed symbolically.

Table 1–3: Control group channel assignments

Bit order	Section:channel	MCF5202/03 signal name
8	C3:7	BD~
7	C3:6	TT1
6	C3:2	TT0
5	C2:3	TS~
4	C3:3	ATM
3	C2:5	ATM=
2	C3:1	DTIP~
1	C2:6	R/W~
0	C2:2	TEA~

By default, the DataSize group is displayed symbolically.

Table 1–4: DataSize group channel assignments

Bit order	Section:channel	MCF5202/03 signal name
4	C2:0	DA1~
3	C2:1	DA0~
2	C3:0	SIZ1
1	C3:4	SIZ0
0	C3:5	TBI~

By default, the Intr group is not visible.

Table 1–5: Intr group channel assignments

Bit order	Section:channel	MCF5202/03 signal name
3	C1:5	AVEC~ †
2	C1:6	IPL2~ †
1	C1:2	IPL1~ †
0	C0:6	IPL0~ †

† **Signal not required for disassembly.**

By default, the Misc group is not visible.

Table 1–6: Misc group channel assignments

Bit order	Section:channel	MCF5202/03 signal name
8	C2:7	CLK †
7	C0:5	RST~ †
6	C1:4	MTMOD2 †
5	C1:3	MTMOD1 †
4	C1:1	MTMOD0 †
3	C1:7	HIZ~ †
2	C1:0	AA~ †
1	C0:4	BR~ †
0	C2:4	BG~ †

† **Signal not required for disassembly.**

By default, the Test group is not visible.

Table 1–7: Test group channel assignments

Bit order	Section:channel	MCF5202/03 signal name
4	C0:7	TCK †
3	C0:3	PST3 †
2	C0:2	PST2 †
1	C0:1	PST1 †
0	C0:0	PST0 †

† **Signal not required for disassembly.**

Table 1–8 lists the probe section and channel assignments for the clock probes. The clock probes are not part of any group.

Table 1–8: Clock channel assignments

Section:channel	MCF5202/03 signal name
CK:3	CLK=
CK:1	BD~=
CK:0	DTIP~=

CPU To Mictor Connections

To probe the microprocessor you will need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the P6434 Mass Termination Probe manual, Tektronix part number 070-9793-xx, for more information on mechanical specifications. Table 1–9 through Table 1–10 show the CPU pin to Mictor pin connections.

Table 1–9: CPU to Mictor connections for Mictor A pins

Mictor A pin	LA channel	MCF5202/03 signal name	Pin number
1	NC		
2	NC		
3	CLOCK:0		47
4	A3:7	AD31	34
5	A3:6	AD30	33
6	A3:5	AD29	30
7	A3:4	AD28	29
8	A3:3	AD27	28
9	A3:2	AD26	27
10	A3:1	AD25	26
11	A3:0	AD24	23
12	A2:7	AD23	22
13	A2:6	AD22	21
14	A2:5	AD21	20
15	A2:4	AD20	17
16	A2:3	AD19	16
17	A2:2	AD18	15
18	A2:1	AD17	14
19	A2:0	AD16	11
20	A0:0	AD0	89
21	A0:1	AD1	90
22	A0:2	AD2	91
23	A0:3	AD3	92
24	A0:4	AD4	95
25	A0:5	AD5	96
26	A0:6	AD6	97
27	A0:7	AD7	98
28	A1:0	AD8	1
29	A1:1	AD9	2
30	A1:2	AD10	3
31	A1:3	AD11	4
32	A1:4	AD12	5
33	A1:5	AD13	8
34	A1:6	AD14	9
35	A1:7	AD15	10
36	CLOCK:1	BD~=	49

Table 1–9: CPU to Mictor connections for Mictor A pins (cont.)

Mictor A pin	LA channel	MCF5202/03 signal name	Pin number
37	NC		
38	NC		
39	GND	GND	
40	GND	GND	
41	GND	GND	
42	GND	GND	
43	GND	GND	

Table 1–10: CPU to Mictor connections for Mictor C pins

Mictor C pin	LA channel	MCF5202/03 signal name	Pin number
1	NC		
2	NC		
3	CLOCK:3	CLK=	87
4	C3:7	BD~	49
5	C3:6	TT1~	36
6	C3:5	TBI~	54
7	C3:4	SIZ0	41
8	C3:3	ATM	63
9	C3:2	TT0~	35
10	C3:1	DTIP~	47
11	C3:0	SIZ1	42
12	C2:7	CLK	87
13	C2:6	R/W~	39
14	C2:5	ATM=	63
15	C2:4	BG~	51
16	C2:3	TS~	40
17	C2:2	TEA~	55
18	C2:1	DA0~	43
19	C2:0	DA1~	44
20	C0:0	PST0	56
21	C0:1	PST1	57
22	C0:2	PST2	58
23	C0:3	PST3	59
24	C0:4	BR~	50
25	C0:5	RST~	67

Table 1–10: CPU to Mictor connections for Mictor C pins (cont.)

Mictor C pin	LA channel	MCF5202/03 signal name	Pin number
26	C0:6	IPL0~	64
27	C0:7	TCK	74
28	C1:0	AA~	48
29	C1:1	MTMOD0	76
30	C1:2	IPL1~	65
31	C1:3	MTMOD1	77
32	C1:4	MTMOD2	78
33	C1:5	AVEC~	79
34	C1:6	IPL2~	66
35	C1:7	HIZ~	75
36	NC		
37	NC		
38	NC		
39	GND	GND	
40	GND	GND	
41	GND	GND	
42	GND	GND	
43	GND	GND	

Operating Basics

Setting Up the Support

The information in this section is specific to the operations and functions of the TMS 220 MCF5202/03 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the MCF5202/03 support are Address, Data, Control, DataSize, Intr, Misc, and Test. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 1–7.

How Data is Acquired

This part of the chapter explains how the module acquires MCF5202/03 signals using the TMS 220 software. This part also provides additional information on extra probe channels available for you to use for additional connections.

Clocking Options

The TMS 220 support offers a microprocessor-specific clocking mode for the MCF5202/03 microprocessor. This clocking mode is the default selection whenever you load the 5202/03 support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking option for the TMS 220 support is Alternate Bus Master Cycles. An alternate bus master cycle is defined as the cycle in which the MCF5202/03 microprocessor gives up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Custom Clocking

A special clocking program is loaded to the module every time you load the 5202/03 support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the MCF5202/03 bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module clocking state machine generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Address Phase. The assertion of the TS~ signal indicates an Address phase (Ta). The clocking program checks whether the cycle is a potential bus master cycle or an Alternate Bus Master cycle. If Excluded is selected as the Alternate Bus Master Cycles clocking option, the disassembler waits for the potential bus maser cycle. Otherwise, when TS~ is deasserted while the DTIP~ and TEA~ signals are deasserted, then the A31-A0, BD~, ATM, CLK, and TS~ signals are acquired.

Data Phase. The assertion of the DTIP~ signal indicates a Data phase (Td). When the DA0~ or DA1~ signals are asserted, the D31-D0, TEA~, DA0~, DA1~, TT0, TT1, SIZ0, SIZ1, DTIP~, CLK, R/W~, ATM=, and BD~ signals are acquired.

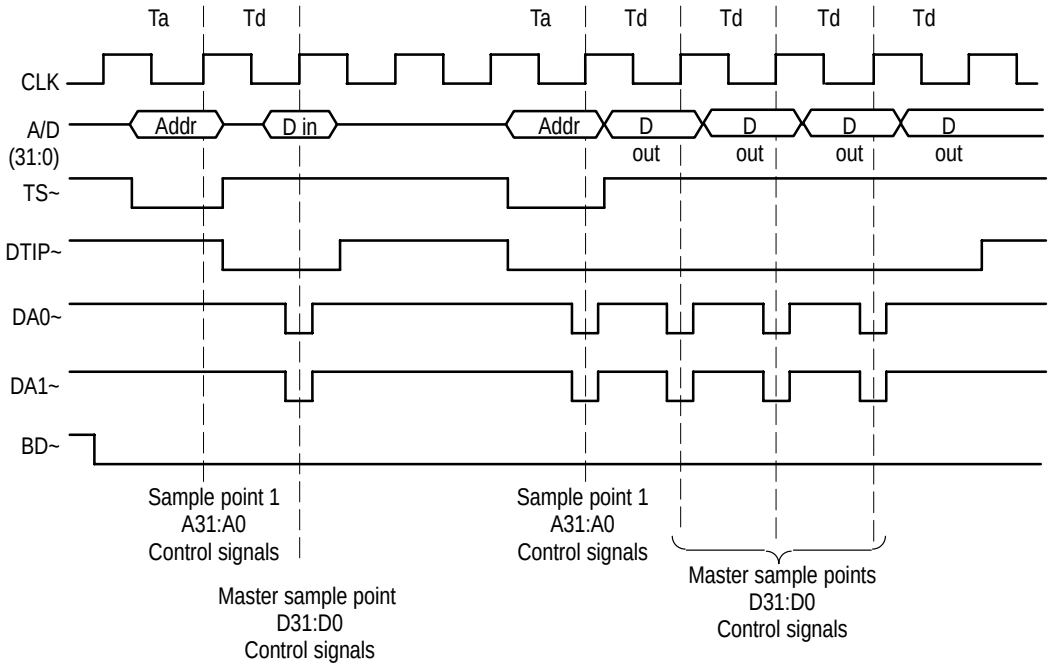


Figure 2–1: MCF5202/03 bus timing

Clocking Options

The clocking algorithm for the MCF5202/03 support has two variations: Alternate Bus Master Cycles Excluded and Alternate Bus Master Cycles Included.

Alternate Bus Master Cycles Excluded. Whenever the BD~ signal is high, no bus cycles are logged in. Only bus cycles initiated by the MCF5202/03 microprocessor (BD~ low) will be logged in.

Alternate Bus Master Cycles Included. All bus cycles, including Alternate Bus Master cycles, are logged in.

Symbols

The TMS 220 support supplies three symbol table files. Each file replaces specific channel group values with symbolic values when Symbolic is the radix for the channel group.

Symbol tables are generally not for use in timing or 5202/03_T support disassembly.

Table 2–1 lists the name, bit pattern, and meaning for the symbols in the file 5202/03_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value			Description
	BD~ TT1 TT0	TS~ ATM ATM=	DTIP~ R/W~ TEA~	
S_DATA_RD	0 0 0	0 0 1	0 1 1	Supervisor mode Data Read; Normal Access
S_DATA_WR	0 0 0	0 0 1	0 0 1	Supervisor mode Data Write; Normal Access
S_FETCH	0 0 0	0 1 1	0 1 1	Supervisor mode Instruction Fetch; Normal Access
S_CPU_RD	0 1 1	0 0 1	0 1 1	Supervisor mode Data Read; CPU Access
S_CPU_WR	0 1 1	0 0 1	0 0 1	Supervisor mode Data Write; CPU Access
S_EMT_RD	0 1 0	0 0 1	0 1 1	Supervisor mode Data Read; Emulator Access
S_EMT_WR	0 1 0	0 0 1	0 0 1	Supervisor mode Data Write; Emulator Access
U_DATA_RD	0 0 0	0 0 0	0 1 1	User mode Data Read; Normal Access
U_DATA_WR	0 0 0	0 0 0	0 0 1	User mode Data Write; Normal Access

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value BD~ TT1 TT0	 TS~ ATM ATM=	 DTIP~ R/W~ TEA~	Description
U_FETCH	0 0 0	0 1 0	0 1 1	User mode Instruction Fetch; Normal Access
U_CPU_RD	0 1 1	0 0 0	0 1 1	User mode Data Read; CPU Access
U_CPU_WR	0 1 1	0 0 0	0 0 1	User mode Data Write; CPU Access
U_EMT_RD	0 1 0	0 0 0	0 1 1	User mode Data Read; Emulator Access
U_EMT_WR	0 1 0	0 0 0	0 0 1	User mode Data Write; Emulator Access
ALT_RD	1 X X	0 0 X	0 1 1	Alternate Master data read
ALT_WR	1 X X	0 0 X	0 0 1	Alternate Master data write
ALT_FETCH	1 X X	0 1 X	0 1 1	Alternate Master instruction fetch
BUS_ERROR	X X X	X X X	X X 0	Bue Error cycle
UNKNOWN	X X X	X X X	X X X	Unknown data cycle

Table 2–2 lists the name, bit pattern, and meaning for the symbols in the file 5202/03_Size, the data transfer size channel group symbol table.

Table 2–2: DataSize group symbol table definitions

Symbol	DataSize group value DA1~	 DA0~ SIZ1 SIZ0 TBI~	Description
LWORD	0	0 0 0 X	Long Word Transfer
WORD	0	X 1 0 X	Word Transfer
BYTE	X	X 0 1 X	Byte Transfer
4_LWD_BST	0	0 1 1 X	4-Long Word Burst Transfer
2_WD_BST	0	1 0 0 X	2-Word Burst Transfer
8_WD_BST	0	1 1 1 X	8-Word Burst Transfer
4_BTE_BST	1	0 0 0 X	4–Byte Burst Transfer
2_BTE_BST	1	0 1 0 X	2–Byte Burst Transfer
16_BTE_BST	1	0 1 1 X	16–Byte Burst Transfer

Table 2–3 lists the name, bit pattern, and meaning for the symbols in the file 5202/03_Intr, the Interrupt channel group symbol table.

Table 2–3: Intr group symbol table definitions

Symbol	Intr group value (AVEC~ IPL2~ IPL1~ IPL0~)	Description
IPL_1	X 1 1 0	Level 1 interrupt request
IPL_2	X 1 0 1	Level 2 interrupt request
IPL_3	X 1 0 0	Level 3 interrupt request
IPL_4	X 0 1 1	Level 4 interrupt request
IPL_5	X 0 1 0	Level 5 interrupt request
IPL_6	X 0 0 1	Level 6 interrupt request
IPL_7	X 0 0 0	Level 7 interrupt request
NO_INTR	X 1 1 1	No interrupt

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

Acquiring Data

Once you load the 5202/03 support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

***NOTE**. Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–11*.

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–4 lists these special characters and strings, and gives a definition of what they represent.

Table 2–4: Meaning of special characters in the display

Character or string displayed	Description
>> On the TLA 700 m On the DAS 9200	The instruction was manually marked as a program fetch
****	Indicates there is insufficient data available for complete disassembly of the instruction: the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.
#	Indicates an immediate value
t	Indicates the number shown is in decimal, such as #12t
(S) or (U)	Indicates the mode in which the microprocessor is operating, Supervisor or User

Table 2–4: Meaning of special characters in the display (cont.)

Character or string displayed	Description
A-LINE OPCODE	Displayed for an A-Line trap instruction
F-LINE OPCODE	Displayed for an F-Line trap instruction

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–5 lists these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–5: Cycle type definitions

Cycle type	Description
(BUS ERROR)	Bus cycle error
(ALT FETCH)	ALT microprocessor fetch cycle
(ALT READ)	ALT microprocessor read cycle
(ALT WRITE)	ALT microprocessor write cycle
(CPU SUP READ)	Read from CPU space: Supervisor access
(CPU SUP WRITE)	Write to CPU space: Supervisor access
(CPU USR READ)	Read from CPU space: User access
(CPU USR WRITE)	Write to CPU space: User access
(DATA SUP READ)	Read cycle: Supervisor access
(DATA SUP WRITE)	Write cycle: Supervisor access
(DATA USR READ)	Read cycle: User access
(DATA USR WRITE)	Write cycle: User access
(EMUL SUP READ)	Read cycle: Emul Access in Supervisor mode
(EMUL SUP WRITE)	Write cycle: Emul Access in Supervisor mode
(EMUL USR READ)	Read cycle: Emul Access in User mode
(EMUL USR WRITE)	Write cycle: Emul Access in User mode
(UNKNOWN)	The combination of control bits is unexpected and/or unrecognized
(PREFETCH IGNORED)§	Instruction Burst Fill to the cache that is not executed
(CACHE BURST FILL)§	Data burst fill to the cache
(INTERRUPT ACK LEVEL: n)§	Interrupt acknowledge
(EXTENSION)§	A fetch cycle computed to be an opcode extension

Table 2–5: Cycle type definitions (cont.)

Cycle type	Description
(FLUSH)§	A fetch cycle computed to be an opcode flush

§ **Computed cycle types.**

Figure 2–2 shows an example of the Hardware display.

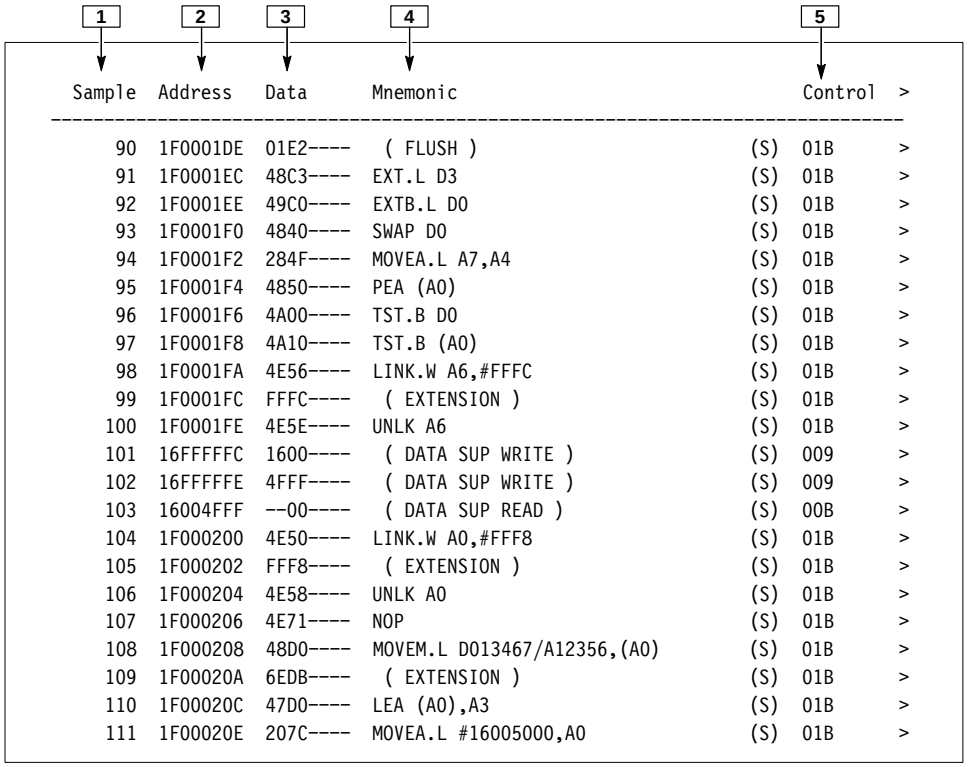


Figure 2–2: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the MCF5202/03 address bus.

3 **Data Group.** Lists data from channels connected to the MCF5202/03 data bus.

4 **Mnemonics Column.** Lists the disassembled instructions and cycle types.

5 **Control Group.** Lists data from channels connected to MCF5202/03 microprocessor control signals (shown symbolically).

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

The Software display format also shows the following cycles:

- CPU Space Bus Error cycle
- Bus Error cycle
- Special cycles: Breakpoint Ack, Int Ack, access register reads and writes
- Emulated instructions which cause exceptions
- Reset vector
- Reads from the interrupt table that appear due to servicing exceptions, provided the Vector Base Register field matches your SUT
- Illegal instructions
- (UNKNOWN) cycle types: the disassembler does not recognize the Control group value

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

The Control Flow display format also shows the following cycles:

- CPU Space Bus Error cycle
- Bus Error cycle
- Special cycles: Breakpoint Ack, Int Ack, access register reads and writes
- Emulated instructions which cause exceptions
- Reset vector
- Reads from the interrupt table that appear due to servicing exceptions, provided the Vector Base Register field matches your SUT
- Illegal instructions
- (UNKNOWN) cycle types: the disassembler does not recognize the Control group value

Instructions that generate a change in the flow of control in the MCF5202/03 microprocessor are as follows:

BRA	JSR	STOP	BSR
RTE	TRAP	JMP	RTS

The instruction that might generate a change in the flow of control in the MCF5202/03 microprocessor is Bcc.

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

The Subroutine display format also shows the following cycles:

- CPU Space Bus Error cycle
- Bus Error cycle
- Special cycles: Breakpoint Ack, Int Ack, access register reads and writes
- Emulated instructions which cause exceptions
- Reset vector
- Reads from the interrupt table that appear due to servicing exceptions, provided the Vector Base Register field matches your SUT
- Illegal instructions
- (UNKNOWN) cycle types: the disassembler does not recognize the Control group value

Instructions that generate a subroutine call or a return in the MCF5202/03 microprocessor are as follows:

BSR	RTE	STOP
JSR	RTS	TRAP

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the MCF5202/03 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

There are no optional fields for this support package. Refer to the information on basic operations for descriptions of common fields.

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

- Select the microprocessor from which to acquire data
- Specify the starting address of the vector base register
- Specify the size of the vector base register

The MCF5202/03 microprocessor support product has three additional fields: Processor Select, Vector Base Register, and Vector Table Size.

Processor Select. You can select which microprocessor from which to acquire data, the MCF5202 or the MCF5203.

Vector Base Register. You can specify the starting address of the vector base register in hexadecimal, by increments of two. The default starting address is 0x00000000.

Vector Table Size. You can specify the size of the interrupt table in hexadecimal. The default size is 0x400. The minimum size allowed is 8. The size must be divisible by 4.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)
- Anything (any valid opcode, extension or flush)

Mark selections for a 32-bit bus are as follows:

```
Opcode      Anything
Opcode      Opcode
Opcode      Flush
Flush       Flush
Flush       Opcode
Extension   Extension
Extension   Opcode
Extension   Flush

Undo mark
```

Mark selections for an 8- and 16-bit bus are as follows:

```
Opcode
Extension
Flush

Undo mark
```

Displaying Exception Vectors

The disassembler can display exception vectors.

You can relocate the table by entering the starting address in the Vector Base Register field. The Vector Base Register field provides the disassembler with the offset address. Enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception table. The Vector Table Size field lets you specify a three-digit hexadecimal size for the table.

These fields are located in the Disassembly property page (Disassembly Format Definition overlay).

Table 2–6 lists the MCF5202/03 exception vectors.

Table 2–6: Exception vectors

Exception number	Location in table (in hexadecimal)	Displayed exception name
0	000	(INITIAL STACK POINTER)
1	004	(INITIAL PROGRAM COUNTER)
2	008	(ACCESS ERROR VECTOR)
3	00C	(ADDRESS ERROR VECTOR)
4	010	(ILLEGAL INSTRUCTION VECTOR)
5-7	014-01C	(RESERVED VECTOR #14H-#1CH)
8	020	(PRIV VIOLATION VECTOR)
9	024	(TRACE VECTOR)
10	028	(UNIMPLEMENTED LINE-A OPCODE)

Table 2–6: Exception vectors (cont.)

Exception number	Location in table (in hexadecimal)	Displayed exception name
11	02C	(UNIMPLEMENTED LINE-F OPCODE)
12	030	(DEBUG INTERRUPT VECTOR)
13	034	(RESERVED VECTOR #34H)
14	038	(FORMAT ERROR VECTOR)
15	03C	(UNINIT INTERRUPT VECTOR)
16-23	040-05C	(RESERVED VECTOR #40H-#5CH)
24	060	(SPURIOUS INTERRUPT VECTOR)
25-31	064-07C	(ILP 1-7 AUTOVECTOR)
32-47	080-08C	(TRAP #0t-#15t VECTOR)
48-63	0C0-0FC	(RESERVED VECTOR #C0-#FC)
64-255	100-3FC	(USER INT VECTOR #64t-#255t)

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your MCF5202/03 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Specifications

Specifications

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little or no effect on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a MCF5202/03 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

The probe adapter accommodates the Motorola MCF5202/03 microprocessor in a 100-pin TQFP package.

Specification Tables

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 lists the electrical requirements the SUT must produce for the support to acquire correct data. Table 3–2 lists the environmental specifications.

Figure 3–1 shows the dimensions of the probe adapter. Figure 3–2 shows the dimensions of the test clip.

Table 3–1: Electrical specifications

Characteristics	Requirements
SUT clock	
Maximum clock rate	33 MHz
Minimum setup time required	
TLA 700	2.5 ns
DAS 9200	5 ns
Minimum hold time required	
TLA 700	0 ns
DAS 9200	0 ns

Table 3–1: Electrical specifications (cont.)

Characteristics	Requirements	
	Specification	
Measured typical SUT signal loading	**AC load**	**DC load**
AD0–AD31	16 pF + 1 podlet	1 podlet
CLK	11.5 pF + 2 podlets	2 podlets
DTIP~	18.4 pF + 2 podlets	2 podlets
BD~	21.4 pF + 2 podlets	2 podlets
ATM	10.5 pF + 2 podlets	2 podlets
PST0, PST1, PST2, PST3, BR~, RST~, IPL0~, IPL1~, IPL2~, TCK, AA~, MTMOD0, MTMOD1, MTMOD2, AVEC~, HIZ~	10 pF + 1 podlet	1 podlet
Loading		
TLA 700 podlet load	20 KΩ in parallel with 2 pF	
TLA 700 Mictor load	20 KΩ in parallel with 2 pF	
DAS 9200 podlet load	100 KΩ in parallel with 10 pF	
DAS 9200 Mictor load	100 KΩ in parallel with 12 pF	

Table 3–2: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F) †
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed MCF5202/03 microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

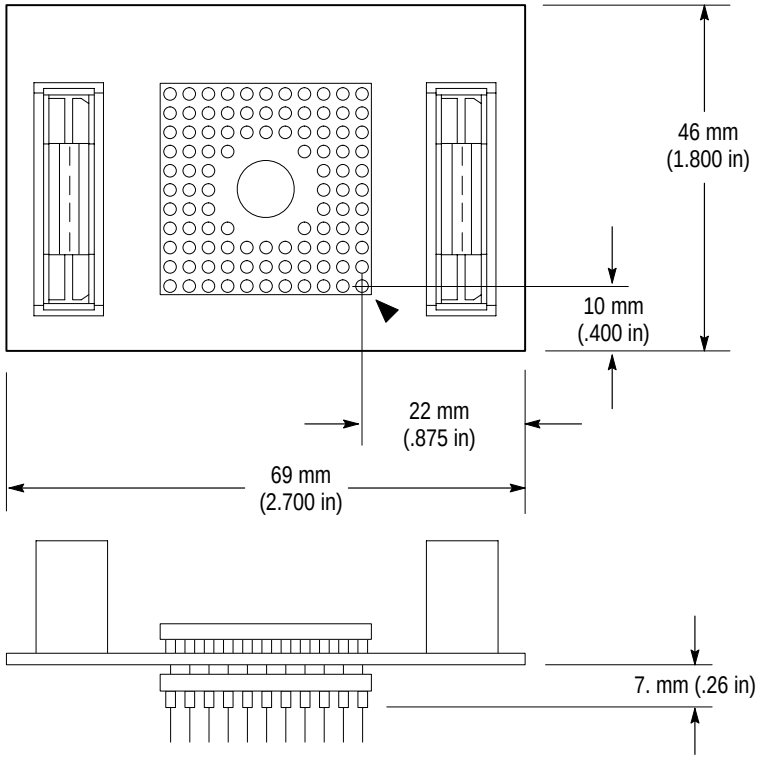


Figure 3–1: Dimensions of the probe adapter

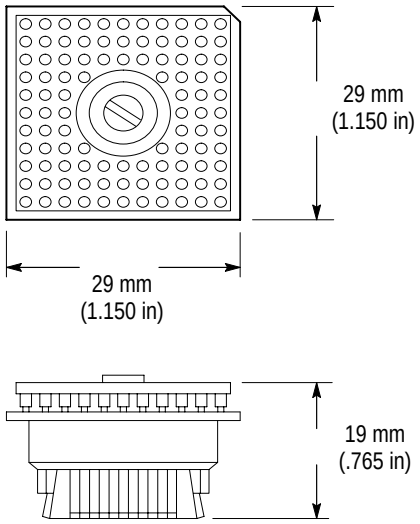


Figure 3–2: Dimensions of the test clip

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 220 MCF5202/03 microprocessor support.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

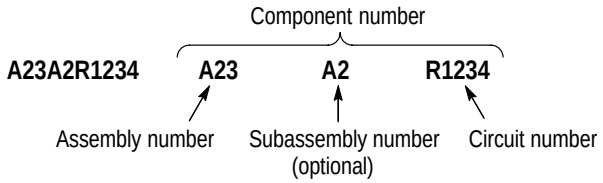
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
05276	ITT POMONA ELECTRONICS	1500 E NINTH ST	POMONA, CA 91766–3835
63058	BERG ELECTRONICS INC.	MCKENZIE SOCKET DIV 910 PAGE AVE	FREMONT, CA 94538–7340
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
–	010–0609–00			ADATPER,PROBE:MCF5202/03,PGA–100 SOCKETED,TMS220 11	80009	010–0609–00
–	103–0411–00			ADAPTER,TQFP:TEST CLIP,100 PIN TQFP,0.50 MM LEAD PITCH,MCF5202/03,100 POS,	05276	MODEL 6150
–	136–1316–00			SOCKET,PGA:PCB,FEMALE,STR,100 POS,11 X 11,0.173 H X 0.183 TAIL,G/G,PAT 114,OPEN CENTER,SHO	63058	PGA100H101B1–1149 F
–	671–4151–00			CIRCUIT BD ASSY:PGA–100 BD,SOCKETED,389–2425–00 WIRED,TMS220 OPT 11	80009	671–4151–00

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 220 MCF5202/03 microprocessor support.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
05276	ITT POMONA ELECTRONICS	1500 E NINTH ST	POMONA, CA 91766–3835
63058	BERG ELECTRONICS INC.	MCKENZIE SOCKET DIV 910 PAGE AVE	FREMONT, CA 94538–7340
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
1–0	671–4151–00			1	CIRCUIT BD ASSY: PGA–100 BD, SOCKETED, 389–2425–00 WIRED, TMS220 OPT 11	80009	671–4151–00
–1	010–0609–00			1	ADATPER, PROBE: MCF5202/03, PGA–100 SOCKETED, TMS220 11	80009	010–0609–00
–2	131–6134–01			3	CONN, RCPT: SMD, MICTOR, PCB, STR, 38 POS, FEMALE, 0.025 CTR, 0.240 H, W/0.108 PCB HOLD DOWN	00779	767054–1
–3	105–1089–00			3	LATCH ASSY: LATCH HOUSING ASSY, VERTICAL MOUNT, 0.48 H X 1.24 L, W/PCB SINGLE CLIP, P6434	60381	105–1089–00
–4	136–1316–00			1	SOCKET, PGA: PCB, FEMALE, STR, 100 POS, 11 X 11, 0.173 H X 0.183 TAIL, G/G, PAT 114, OPEN CENTER, SHO	63058	PGA100H101B1–1149 F
–5	103–0411–00			1	ADAPTER, TQFP: TEST CLIP, 100 PIN TQFP, 0.50 MM LEAD PITCH, MCF5202/03, 100 POS	05276	MODEL 6150
	070–9803–00			1	MANUAL, TECH: INSTRUCTION, MICROPROCESSOR SUPPORT, PKG INSTALLATION, TLA700 SERIES, LOGIC ANALYZER	TK2548	070–9803–00
	070–9842–00			1	MANUAL, TECH: INSTRUCTION MANUAL, MCF5202/03, TMS220	TK2548	070–9842–00
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00

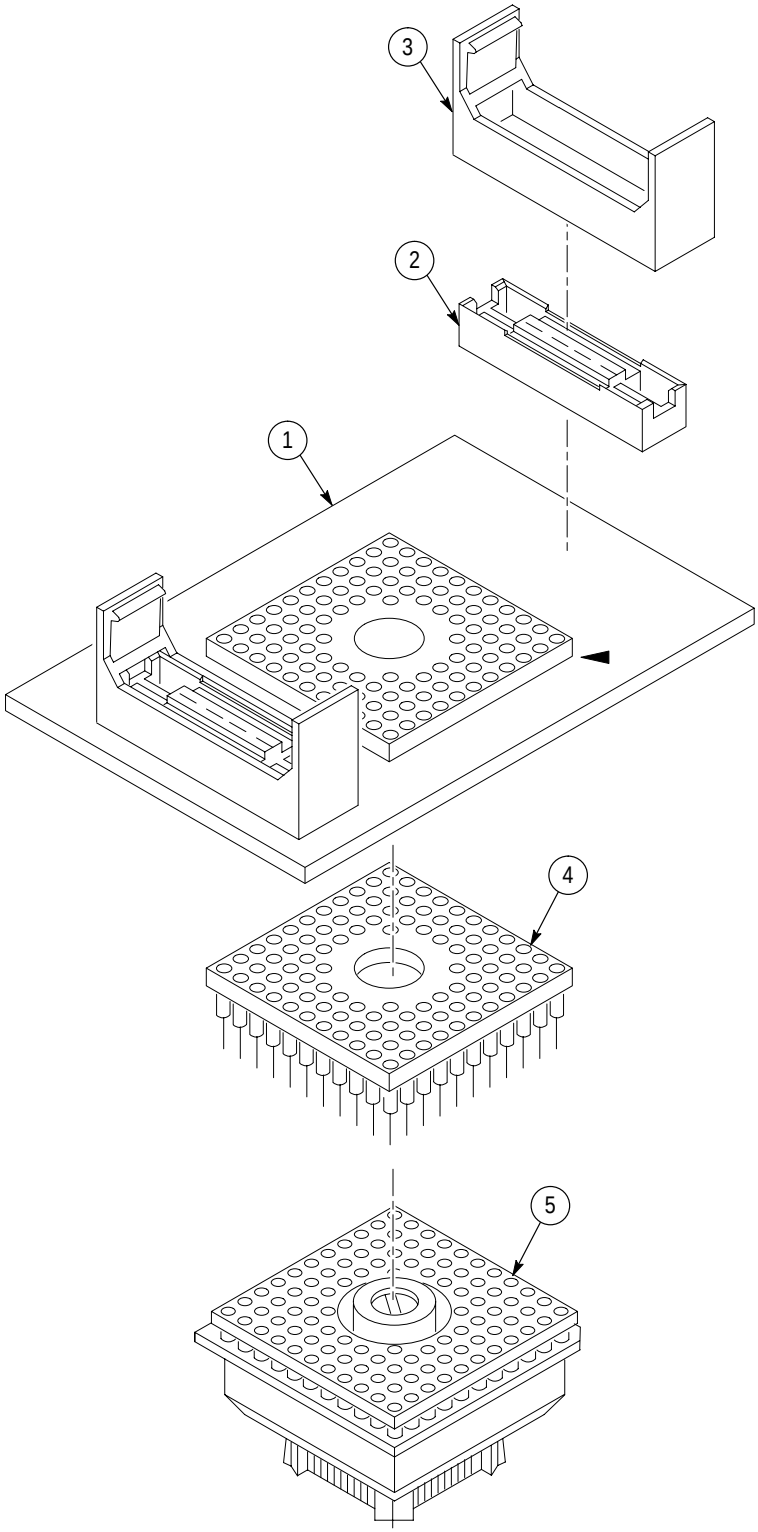


Figure 1: MCF5202/03 probe adapter exploded view

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