Instruction Manual

Tektronix

TMS 531
PPC 403GX Microprocessor Support

071-0494-00

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

SOFTWARE WARRANTY

Tektronix warrants that the media on which this software product is furnished and the encoding of the programs on the media will be free from defects in materials and workmanship for a period of three (3) months from the date of shipment. If a medium or encoding proves defective during the warranty period, Tektronix will provide a replacement in exchange for the defective medium. Except as to the media on which this software product is furnished, this software product is provided “as is” without warranty of any kind, either express or implied. Tektronix does not warrant that the functions contained in this software product will meet Customer’s requirements or that the operation of the programs will be uninterrupted or error-free.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period. If Tektronix is unable to provide a replacement that is free from defects in materials and workmanship within a reasonable time thereafter, Customer may terminate the license for this software product and return this software product and any associated materials for credit or refund.

THIS WARRANTY IS GIVEN BY TEKTRONIX IN LIEU OF ANY OTHER WARRANTIES, EXPRESS OR IMPLIED. TEKTRONIX AND ITS VENDORS DISCLAIM ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. TEKTRONIX’ RESPONSIBILITY TO REPLACE DEFECTIVE MEDIA OR REFUND CUSTOMER’S PAYMENT IS THE SOLE AND EXCLUSIVE REMEDY PROVIDED TO THE CUSTOMER FOR BREACH OF THIS WARRANTY. TEKTRONIX AND ITS VENDORS WILL NOT BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES IRRESPECTIVE OF WHETHER TEKTRONIX OR THE VENDOR HAS ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Table of Contents

List of Tables

General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Preface

This instruction manual contains specific information about the TMS 531 PPC 403GX microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 531 PPC 403GX support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to your online help.
- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or visit our web site for a listing of worldwide service locations. tektronix.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter contains information on the TMS 531 PPC 403GX microprocessor support package.

Support Package Description

The TMS 531 PPC 403GX microprocessor support package displays disassembled data from systems based on the PPC 403GX IBM microprocessor. The support runs on a compatible Tektronix logic analyzer.

To use this support efficiently, refer to information on basic operations and the following documents:

- *PowerPC 403GA Data Sheet, IBM Microelectronics, 9–97*
- *PowerPC 403GC Data Sheet, IBM Microelectronics, 9–97*
- *PowerPC 403GCX Data Sheet, IBM Microelectronics, 3–98*
- *PowerPC 403GA User Manual, IBM Microelectronics, 3–95*
- *PowerPC 403GC User Manual, IBM Microelectronics, 3–95*
- *PowerPC 403GCX User Manual, IBM Microelectronics, 5–98*

The following is a list of microprocessors the TMS 531 PPC 403GX support can acquire and display as disassembled data:

PPC 403GA
PPC 403GC
PPC 403GCX

Logic Analyzer Software Compatibility

The version of logic analyzer software that is compatible with this support is listed on the label of the floppy disk.

Logic Analyzer Configuration

The TMS 531 PPC 403GX support requires a minimum of a 102-channel module.

Requirements and Restrictions

Review the electrical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, and the following descriptions of other PPC 403GX support requirements and restrictions.

Hardware Reset. If a hardware reset occurs in your PPC 403GX system during an acquisition, the application disassembler might acquire an invalid sample.

System Clock Rate. The PPC 403GX microprocessor support can acquire data from the PPC 403GX microprocessor operating at speeds of up to 40 MHz. The PPC 403GX microprocessor support has been tested to the 33 MHz clock rates. The operating clock rate specifications were measured at the time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.

Disabling the Instruction Cache. To display disassembled acquired data, you must disable the internal instruction cache. Disabling the cache makes all instruction prefetches visible on the bus so that they can be acquired and displayed disassembled.

Disabling the Data Cache. To display acquired data, you must disable the data cache. Disabling the data cache makes visible all loads and stores to memory on the bus, including data reads and writes, so the software can acquire and display them.

Nonintrusive Acquisition. The PPC 403GX microprocessor will not intercept, modify, or present signals back to the system under test.

Support Software. The PPC 403GX Support Software is not tested for DRAM Data Read on CAS mode or EDO (2-1-1-1) mode.

MMU Address Translation. The MMU address translation must be turned off for proper disassembly.

Functionality Not Supported

Real Time Debug. You must enable the PPC 403GX microprocessor Real Time Debug trace signals for the TMS 531 PPC 403GX support to disassemble data. When enabled the debug trace signals generate the Program Status and Bus Status signals. This also makes available qualifiers for the CSM and Instruction/ Data signals for disassembly.

Bus Status Mode must be enabled in the IOCR (Input/output configuration register). To enable the Bus Status Mode, the ReaL-Time Debug Mode bits (IOCR [RDM]) must be set to 01 in IOCR register.

NonDRAM. NonDRAM cycles may not be acquired correctly when Data Read on CAS mode or EDO (Other) mode are selected.

Byte Enable. You can choose to configure Byte Enable signals as either Write Enable or Byte Enable for both reads and writes. If the Byte Enable signals are not configured for both reads and writes, the byte invalidation for reads and writes is not executed.

Interrupt Signals. The interrupt signals are not acquired by the TMS 531 PPC 403GX support software; however, the interrupt signals are identified when looking at the address displayed for the interrupt service.

Extra Acquisition Channels. Extra Acquisition Channels are not available.

Show Cycle. The show cycle signals are not acquired by the TMS 531 PPC 403GX support software.

External Master Cycles. Asynchronous External Master cycles are not acquired.

Connecting the Logic Analyzer to a System Under Test

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your system under test.

To connect the probes to PPC 403GX signals in the system under test using a test clip, follow these steps:

1. Power down your system under test. It is not necessary to power down the logic analyzer.

CAUTION. *To prevent static damage, handle these components only in a static-free environment. Static discharge can damage the microprocessor, the probes, and the logic analyzer module.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from the test clip.
3. Place the system under test on a horizontal, static-free surface.
4. Refer to Tables 1–1 through 1–6, and connect the channel probes to PPC 403GX signal pins on the test clip or in the system under test.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Channel Assignments

Channel assignments listed in Tables 1–1 through 1–6 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are listed starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- An tilde symbol (~) following the signal name indicates an active low signal.

Table 1–1 lists the probe section and channel assignments for the Address group and the microprocessor signal for each channel connect. By default, this channel group is displayed in hexadecimal.

Table 1–1: Address channel group assignments

Bit order	Section:channel	PPC 403GX signal name
27	A3:3	WBE0~/A4/BE0~
26	A3:2	WBE1~/A5/BE1~
25	A3:1	A6
24	A3:0	A7
23	A2:7	A8
22	A2:6	A9

Table 1–1: Address channel group assignments (Cont.)

Bit order	Section:channel	PPC 403GX signal name
21	A2:5	A10
20	A2:4	A11
19	A2:3	A12
18	A2:2	A13
17	A2:1	A14
16	A2:0	A15
15	A1:7	A16
14	A1:6	A17
13	A1:5	A18
12	A1:4	A19
11	A1:3	A20
10	A1:2	A21
9	A1:1	A22
8	A1:0	A23
7	A0:7	A24
6	A0:6	A25
5	A0:5	A26
4	A0:4	A27
3	A0:3	A28
2	A0:2	A29
1	A0:1	WBE2~/A30/BE2~
0	A0:0	WBE3~/A31/BE3~

Table 1–2 lists the probe section and channel assignments for the Data group and the microprocessor signal for each channel connect. By default, this channel group is displayed in hexadecimal.

Table 1–2: Data channel group assignments

Bit order	Section:channel	PPC 403GX signal name
31	D3:7	D0
30	D3:6	D1
29	D3:5	D2
28	D3:4	D3
27	D3:3	D4
26	D3:2	D5

Table 1–2: Data channel group assignments (Cont.)

Bit order	Section:channel	PPC 403GX signal name
25	D3:1	D6
24	D3:0	D7
23	D2:7	D8
22	D2:6	D9
21	D2:5	D10
20	D2:4	D11
19	D2:3	D12
18	D2:2	D13
17	D2:1	D14
16	D2:0	D15
15	D1:7	D16
14	D1:6	D17
13	D1:5	D18
12	D1:4	D19
11	D1:3	D20
10	D1:2	D21
9	D1:1	D22
8	D1:0	D23
7	D0:7	D24
6	D0:6	D25
5	D0:5	D26
4	D0:4	D27
3	D0:3	D28
2	D0:2	D29
1	D0:1	D30
0	D0:0	D31

Table 1–3 lists the probe section and channel assignments for the ChipSel group and the microprocessor signal for each channel connect. By default, this channel group is not visible.

Table 1–3: ChipSel channel group assignments

Bit order	Section:channel	PPC 403GX signal name
7	C3:7	CS7~/RAS0~
6	C3:6	CS6~/RAS1~

Table 1–3: ChipSel channel group assignments (Cont.)

Bit order	Section:channel	PPC 403GX signal name
5	C3:5	CS5~/RAS2~
4	C3:4	CS4~/RAS3~
3	C3:3	CS3~
2	C3:2	CS2~
1	C3:1	CS1~
0	C3:0	CS0~

Table 1–4 lists the probe section and channel assignments for the ByteEnbl group and the microprocessor signal for each channel connect. By default, this channel group is not visible.

Table 1–4: ByteEnbl channel group assignments

Bit order	Section:channel	PPC 403GX signal name
3	A3:3	WBE0~/A4/BE0~
2	A3:2	WBE1~/A5/BE1~
1	A0:1	WBE2~/A30/BE2~
0	A0:0	WBE3~/A31/BE3~

Table 1–5 lists the probe section and channel assignments of the Control group and the microprocessor signal for each channel connect. The default radix of the Control group is SYMBOLIC. The symbol table file name is 403GX_Ctrl. By default, this channel group is displayed as symbols.

Table 1–5: Control channel group assignments

Bit order	Section:channel	PPC 403GX signal name
11	C2:7	Reset~
10	C2:6	Halt~
9	C2:5	Error
8	C2:1	TS4
7	C2:4	BusError~
6	Clock 0	HoldAck
5	C2:3	AMuxCAS
4	C1:3	R/W~
3	C2:0	TS6

Table 1–5: Control channel group assignments (Cont.)

Bit order	Section:channel	PPC 403GX signal name
2	Clock:2	DRAMOE~
1	Clock:3	DRAMWE~
0	C0:7	TS5

Table 1–6 lists the probe section and channel assignments for the Misc group and the microprocessor signal for each channel connect. By default, this channel group is not visible.

Table 1–6: Misc channel group assignments

Bit order	Section:channel	PPC 403GX signal name
13	C2:2	TS3
12	C1:2	BootW
11	C1:1	OE~
10	C1:0	Ready
9	C0:5	CINT~
8	C0:4	INT0
7	C0:3	INT1
6	C0:2	INT2
5	C0:1	INT3
4	C0:0	INT4
3	C1:4	CAS0~
2	C1:5	CAS1~
1	C1:6	CAS2~
0	C1:7	CAS3~

Table 1–7 lists the probe section and channel assignments for the clock probes (not part of any group) and the PPC 403GX signal to which each channel connects.

Table 1–7: Clock and qualifier channel assignments

LA section and probe	PPC 403GX signal name	Description
CLK:0	HoldAck	Clock used as Qualifier
CLK:1	SysClk	Clock used as clock
CLK:2	DRAMOE~	Clock used as Qualifier

Table 1–7: Clock and qualifier channel assignments (Cont.)

LA section and probe	PPC 403GX signal name	Description
CLK:3	DRAMWE~	Clock used as Qualifier
C2:0	TS6	Qualifier
C2:1	TS4	Qualifier
C2:2	TS3	——
C2:3	AMuxCAS	Qualifier
QUAL:0	[1]	102 & 136 channel
QUAL:1	[1]	102 & 136 channel
QUAL:2	[1]	136 channel only
QUAL:3	[1]	136 channel only

[1] **Indicates unused channels**

NOTE*. The CLK channels and QUAL channels are stored as acquisition data, and can be used for triggering.*

Table 1–8 lists channel groups not required for clocking and disassembly by the PPC 403GX microprocessor support.

Table 1–8: Channel groups not required for clocking and disassembly

PPC 403GX Signal Name	TLA 700 Channel
BootW	C1:2
OE~	C1:1
Ready	C1:0
CINT~	C0:5
INT0	C0:4
INT1	C0:3
INT2	C0:2
INT3	C0:1
INT4	C0:0

The following channels may be connected to other signals of interest to you. If connected to other signals, these channels will be logged in on the Master Strobe.

PPC 403GX Signal Name	TLA 700 Channel
	A3:7
	A3:6
	A3:5
	A3:4

Acquisition Setup. The PPC 403GX support will affect the logic analyzer setup menus and submenus by modifying existing fields and adding micro-specific fields.

The PPC 403GX support will add the selection PPC 403GX to the Load Support Package dialog box, located under the File pulldown menu. Once that PPC 403GX support has been loaded, the Custom clocking mode selection in the module Setup menu is also enabled.

CPU To Mictor Connections

To probe the microprocessor you will need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the P6434 Mass Termination Probe manual, Tektronix part number 070-9793-xx, for more information on mechanical specifications. Tables 1–1 through 1–11 show the CPU pin to Mictor pin connections.

Tektronix uses a counterclockwise pin assignment. Pin-1 is located at the top left, and pin-2 is located directly below it. Pin-20 is located on the bottom right, and pin-21 is located directly above it.

AMP uses an odd side-even side pin assignment. Pin-1 is located at the top left, and pin-3 is located directly below it. Pin-2 is located on the top right, and pin-4 is located directly below it (see Figure 1–1).

NOTE. *When designing Mictor connectors into your system under test, always follow the Tektronix pin assignment.*

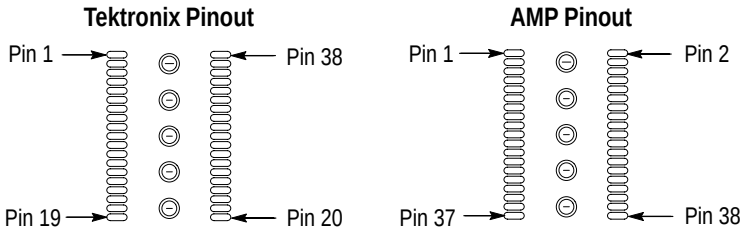

Figure 1–1: Pin assignments for a Mictor connector (component side)

CAUTION. *To protect the CPU and the inputs of the module, it is recommended that a 180 Ω resistor be connected in series between each ball pad of the CPU and each pin of the Mictor connector. The resistor must be within 1/2-inch of the ball pad of the CPU.*

Table 1–9: CPU to Mictor connections for Mictor A pins

Tektronix Mictor A pin number	AMP Mictor A pin number	LA Channel	PPC 403GX signal name	PPC 403GX pin number
1	1	GND	GND	GND
2	3	GND	GND	GND
3	5	CLK:0	HoldAck	134
4	7	A3:7	NC	NC
5	9	A3:6	NC	NC
6	11	A3:5	NC	NC

Table 1–9: CPU to Mictor connections for Mictor A pins (Cont.)

Tektronix Mictor A pin number	AMP Mictor A pin number	LA Channel	PPC 403GX signal name	PPC 403GX pin number
7	13	A3:4	NC	NC
8	15	A3:3	WBE0~/A4/BE0~	122
9	17	A3:2	WBE1~/A5/BE1~	123
10	19	A3:1	A6	92
11	21	A3:0	A7	93
12	23	A2:7	A8	94
13	25	A2:6	A9	95
14	27	A2:5	A10	96
15	29	A2:4	A11	97
16	31	A2:3	A12	98
17	33	A2:2	A13	99
18	35	A2:1	A14	103
19	37	A2:0	A15	104
20	38	A0:0	WBE3~/A31/BE3~	125
21	36	A0:1	WBE2~/A30/BE2~	124
22	34	A0:2	A29	119
23	32	A0:3	A28	118
24	30	A0:4	A27	117
25	28	A0:5	A26	116
26	26	A0:6	A25	115
27	24	A0:7	A24	114
28	22	A1:0	A23	113
29	20	A1:1	A22	112
30	18	A1:2	A21	110
31	16	A1:3	A20	109
32	14	A1:4	A19	108
33	12	A1:5	A18	107
34	10	A1:6	A17	106
35	8	A1:7	A16	105
36	6	CLK:1	SysClk	22
37	4	GND	GND	GND
38	2	GND	GND	GND
39	39	GND	GND	GND
40	40	GND	GND	GND
41	41	GND	GND	GND

Table 1–9: CPU to Mictor connections for Mictor A pins (Cont.)

Tektronix Mictor A pin number	AMP Mictor A pin number	LA Channel	PPC 403GX signal name	PPC 403GX pin number
42	42	GND	GND	GND
43	43	GND	GND	GND
44	44	GND	GND	GND

Table 1–10: CPU to Mictor connections for Mictor D pins

Tektronix Mictor D pin number	AMP Mictor D pin number	LA Channel	PPC 403GX signal name	PPC 403GX pin number
1	1	GND	GND	GND
2	3	GND	GND	GND
3	5	QUAL:0	NC	NC
4	7	D3:7	D0	42
5	9	D3:6	D1	43
6	11	D3:5	D2	44
7	13	D3:4	D3	45
8	15	D3:3	D4	46
9	17	D3:2	D5	47
10	19	D3:1	D6	48
11	21	D3:0	D7	51
12	23	D2:7	D8	52
13	25	D2:6	D9	53
14	27	D2:5	D10	54
15	29	D2:4	D11	55
16	31	D2:3	D12	56
17	33	D2:2	D13	57
18	35	D2:1	D14	58
19	37	D2:0	D15	62
20	38	D0:0	D31	82
21	36	D0:1	D30	79
22	34	D0:2	D29	78
23	32	D0:3	D28	77

Table 1–10: CPU to Mictor connections for Mictor D pins (Cont.)

Tektronix Mictor D pin number	AMP Mictor D pin number	LA Channel	PPC 403GX signal name	PPC 403GX pin number
24	30	D0:4	D27	76
25	28	D0:5	D26	75
26	26	D0:6	D25	74
27	24	D0:7	D24	73
28	22	D1:0	D23	72
29	20	D1:1	D22	71
30	18	D1:2	D21	68
31	16	D1:3	D20	67
32	14	D1:4	D19	66
33	12	D1:5	D18	65
34	10	D1:6	D17	64
35	8	D1:7	D16	63
36	6	CLK:2	DRAMOE~	137
37	4	GND	GND	GND
38	2	GND	GND	GND
39	39	GND	GND	GND
40	40	GND	GND	GND
41	41	GND	GND	GND
42	42	GND	GND	GND
43	43	GND	GND	GND
44	44	GND	GND	GND

Table 1–11: CPU to Mictor connections for Mictor C pins

Tektronix Mictor C pin number	AMP Mictor C pin number	LA Channel	PPC 403GX signal name	PPC 403GX pin number
1	1	GND	GND	GND
2	3	GND	GND	GND
3	5	CLK:3	DRAMWE~	138
4	7	C3:7	CS7~/RAS0~	146
5	9	C3:6	CS6~/RAS1~	147

Table 1–11: CPU to Mictor connections for Mictor C pins (Cont.)

Tektronix Mictor C pin number	AMP Mictor C pin number	LA Channel	PPC 403GX signal name	PPC 403GX pin number
6	11	C3:5	CS5~/RAS2~	148
7	13	C3:4	CS4~/RAS3~	151
8	15	C3:3	CS3~	152
9	17	C3:2	CS2~	153
10	19	C3:1	CS1~	154
11	21	C3:0	CS0~	155
12	23	C2:7	Reset~	91
13	25	C2:6	Halt~	9
14	27	C2:5	Error	136
15	29	C2:4	BusError~	12
16	31	C2:3	AMuxCAS	139
17	33	C2:2	TS3	86
18	35	C2:1	TS4	85
19	37	C2:0	TS6	84
20	38	C0:0	INT4	35
21	36	C0:1	INT3	34
22	34	C0:2	INT2	33
23	32	C0:3	INT1	32
24	30	C0:4	INT0	31
25	28	C0:5	CINT~	36
26	26	C0:6	–	134
27	24	C0:7	TS5	83
28	22	C1:0	Ready	13
29	20	C1:1	OE~	126
30	18	C1:2	BootW	139
31	16	C1:3	R/W~	11
32	14	C1:4	CAS0~	142
33	12	C1:5	CAS1~	143
34	10	C1:6	CAS2~	144
35	8	C1:7	CAS3~	145
36	6	Qual:1	–	–
37	4	GND	GND	GND
38	2	GND	GND	GND
39	39	GND	GND	GND
40	40	GND	GND	GND

Table 1–11: CPU to Mictor connections for Mictor C pins (Cont.)

Tektronix Mictor C pin number	AMP Mictor C pin number	LA Channel	PPC 403GX signal name	PPC 403GX pin number
41	41	GND	GND	GND
42	42	GND	GND	GND
43	43	GND	GND	GND
44	44	GND	GND	GND

Operating Basics

Setting Up the Support

Information in this section covers channel group definitions, Clocking and Symbol table files.

The information in this section is specific to the operations and functions of the TMS 531 PPC 403GX support on any Tektronix logic analyzer. Information on basic operations describes general tasks and functions.

Before you acquire and display disassembled data, you need to load the support and specify the setups for clocking and triggering as described in the information on basic operations in your online help. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the PPC 403GX support are Address, Data, ChipSel, Byte Enbl, Control, and Misc. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 1–4.

Clocking

Custom Clocking

Custom clocking works only when the PPC 403GX real time debug port is configured for Bus Status and Execution Status (by setting the RDM field in IOCR register to 0b01). Then a special clocking program is loaded to the module every time you load the PPC 403GX support. This special clocking is called Custom.

When Custom is selected, the Custom Clocking Options menu has the subtitle PPC 403GX Microprocessor Clocking Support added, and clocking options are displayed.

Clocking Options

The TMS 531 PPC 403GX support offers a microprocessor-specific clocking mode for the PPC 403GX microprocessor. This clocking mode is the default selection whenever you load the PPC 403GX support.

Disassembly will not be correct if you select Internal or External clocking modes. Information on basic operations in your online help describes how to use these clock selections for general-purpose analysis.

There are two clocking options:

DRAM Type. You can select four types of DRAM accesses. The default is in effect when the system under test does not contain any DRAM or the DRAM is in the normal configuration (IOCR.DRC = 0, IOCR.EDO=0).

Normal (default)
Data Read on CAS
EDO (2-1-1-1)
EDO (Other)

If the processor is configured to read DRAM Data on rising CAS (IOCR.DRC=1) instead of rising SysClk, Data Read on the CAS option must be selected for the DRAM type. This is handled by adjusting the setup/hold window of the logic analyzer. In the Data Read on CAS option, because of the setup/hold adjustment, nonDRAM accesses may not by acquired correctly.

The EDO (2-1-1-1) option must be selected when the system under test contains EDO DRAM in 2–1–1–1 timing or nonpaged EDO DRAM. In this case, PPC 403GX support reads the data at the falling edge of the clock.

The EDO (Other) option must be selected for EDO DRAM not mentioned above. In this case, the PPC 403GX support adjusts the setup/hold window of the logic analyzer such that the data is sampled at the falling edge of the CAS. Due to the setup/hold adjustment nonDRAM accesses may not be acquired correctly.

Alternate Master Cycles. You can select Excluded and the alternate master cycles are not acquired. If you select Included, the alternate master cycles are acquired and not disassembled.

Excluded (default)
Included

Alternate Master Cycles, for example on-chip DMA controller accesses (indicated by TS4 asserting low), and external master accesses (indicated by HoldAck assertion) are not acquired or are acquired based on this selection.

Bus Timing Diagram Figures 2–1 through 2–6 shows Timing diagrams.

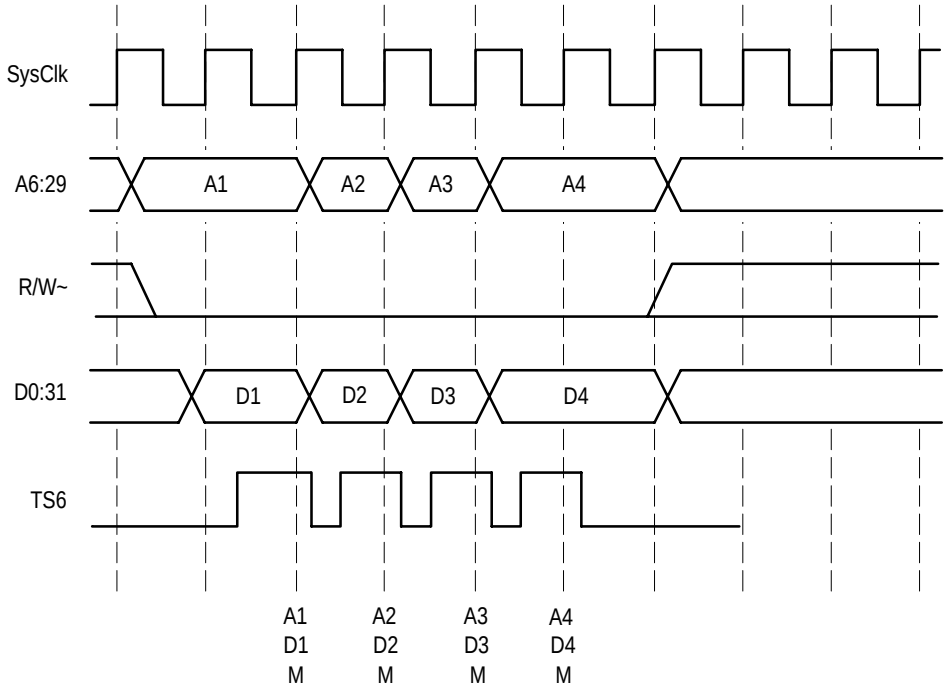

Figure 2–1: SRAM, ROM Write timing diagram

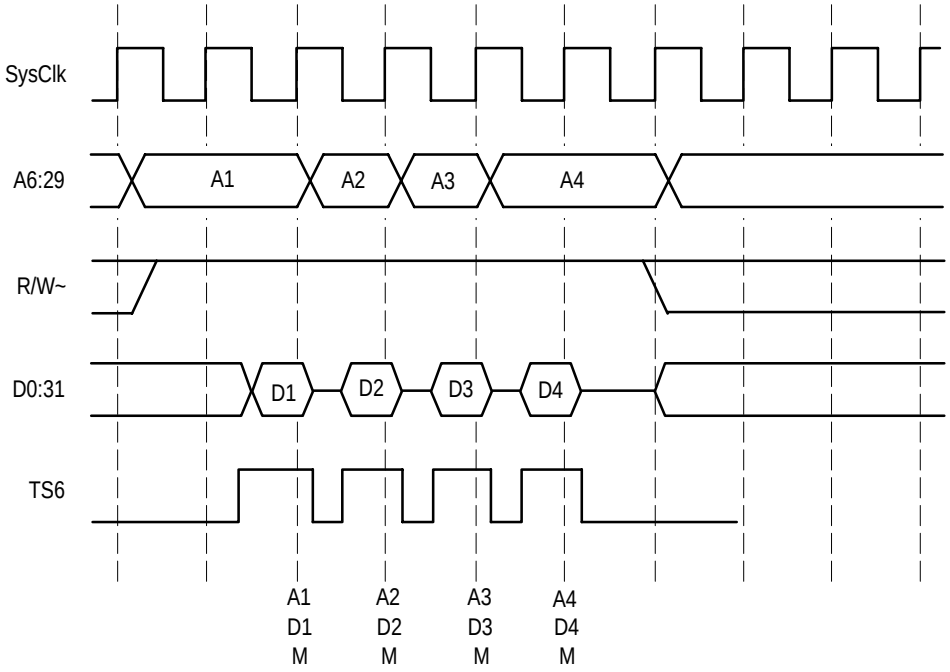

Figure 2–2: SRAM, ROM Read timing diagram

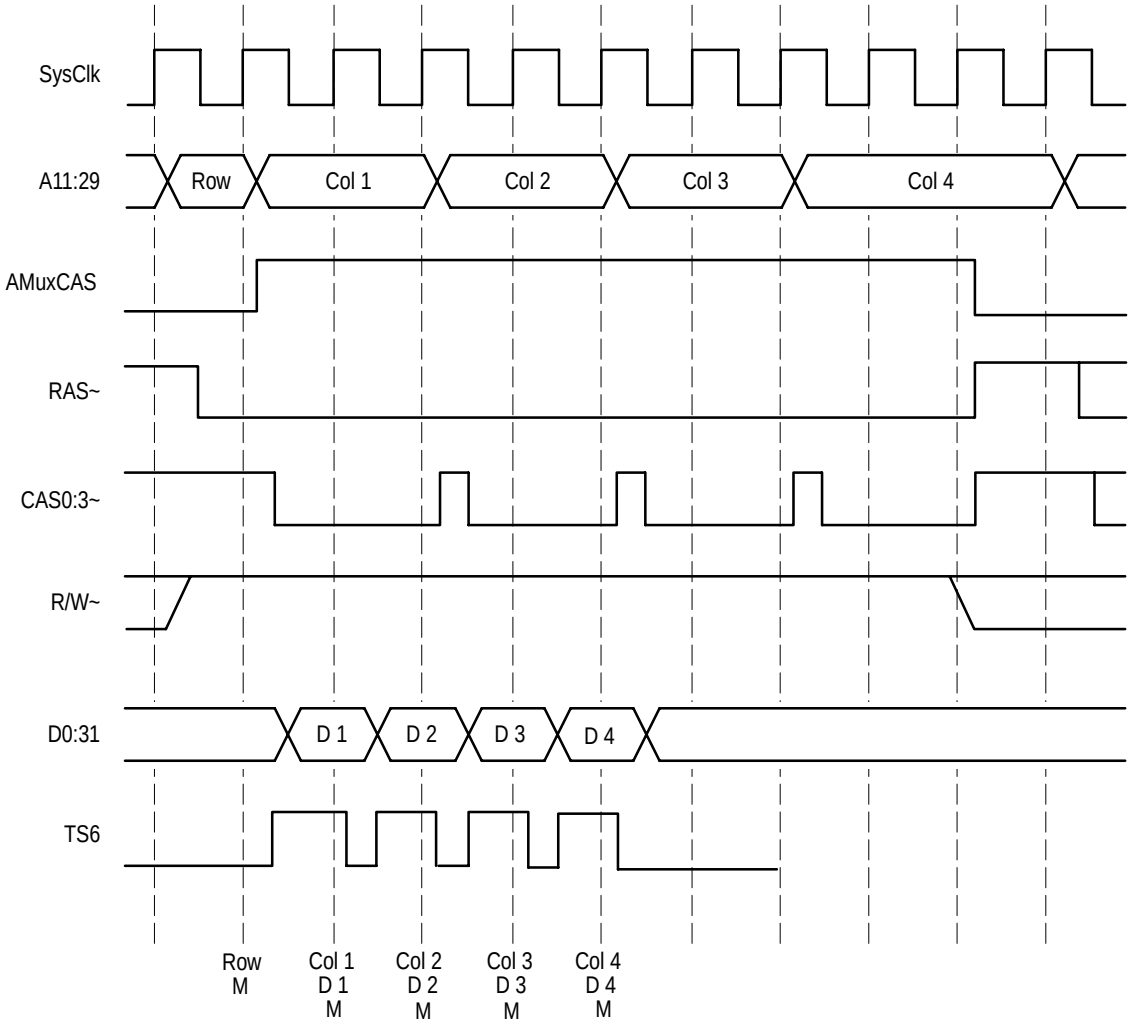

Figure 2–3: DRAM Write timing diagram

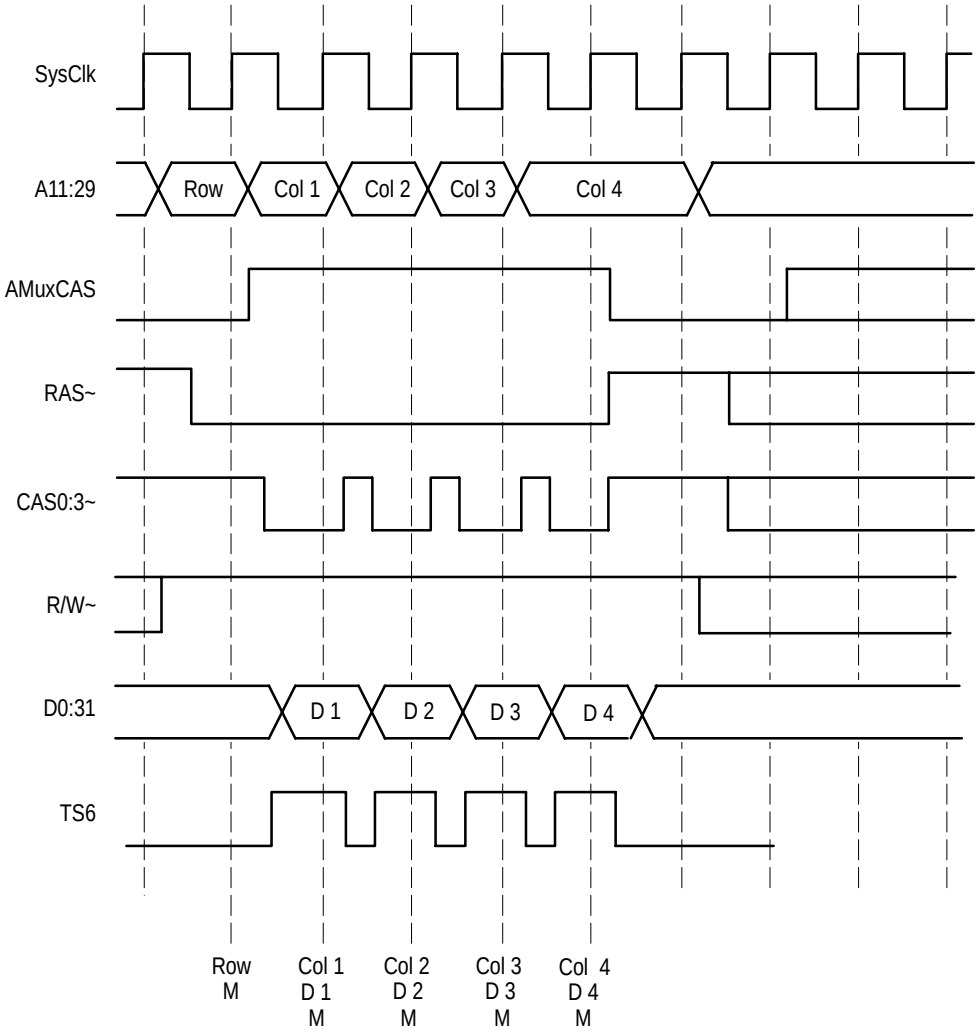

Figure 2–4: DRAM 2-1-1-1 Read timing diagram

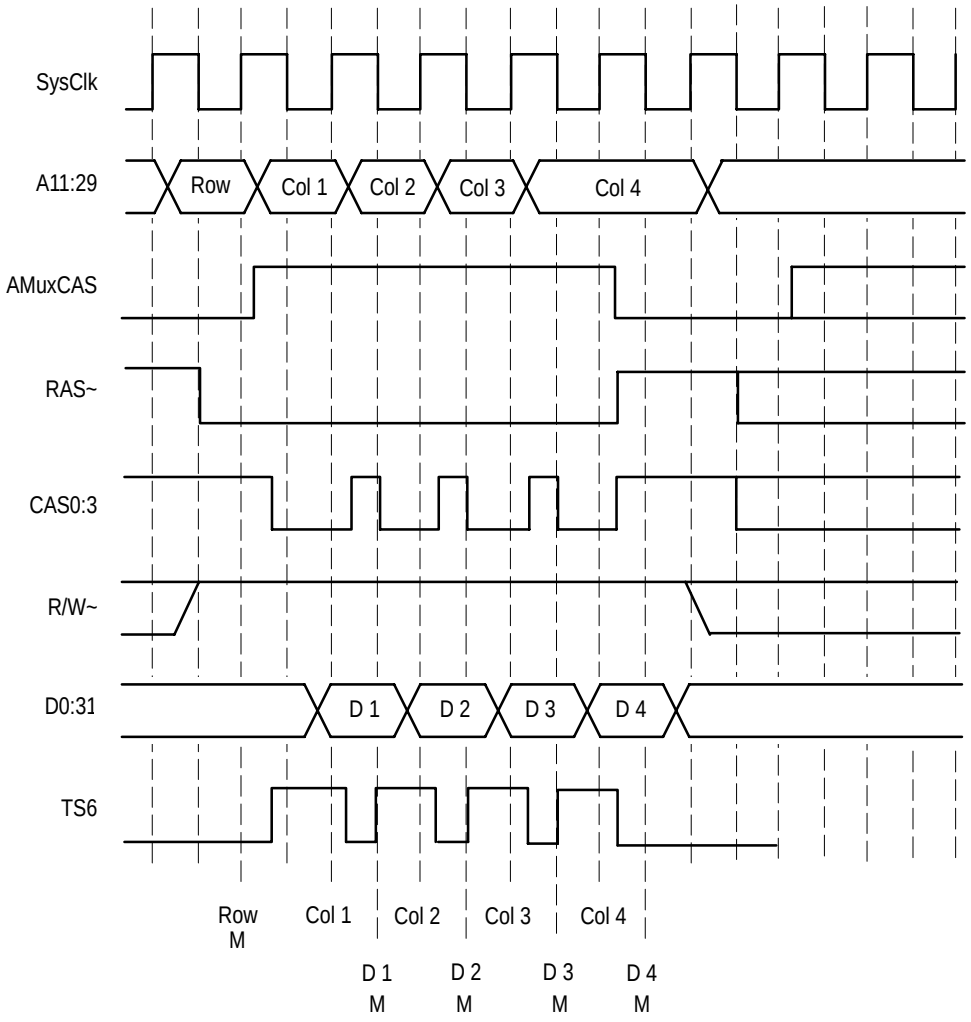

Figure 2–5: EDO DRAM 2-1-1-1 Read timing diagram

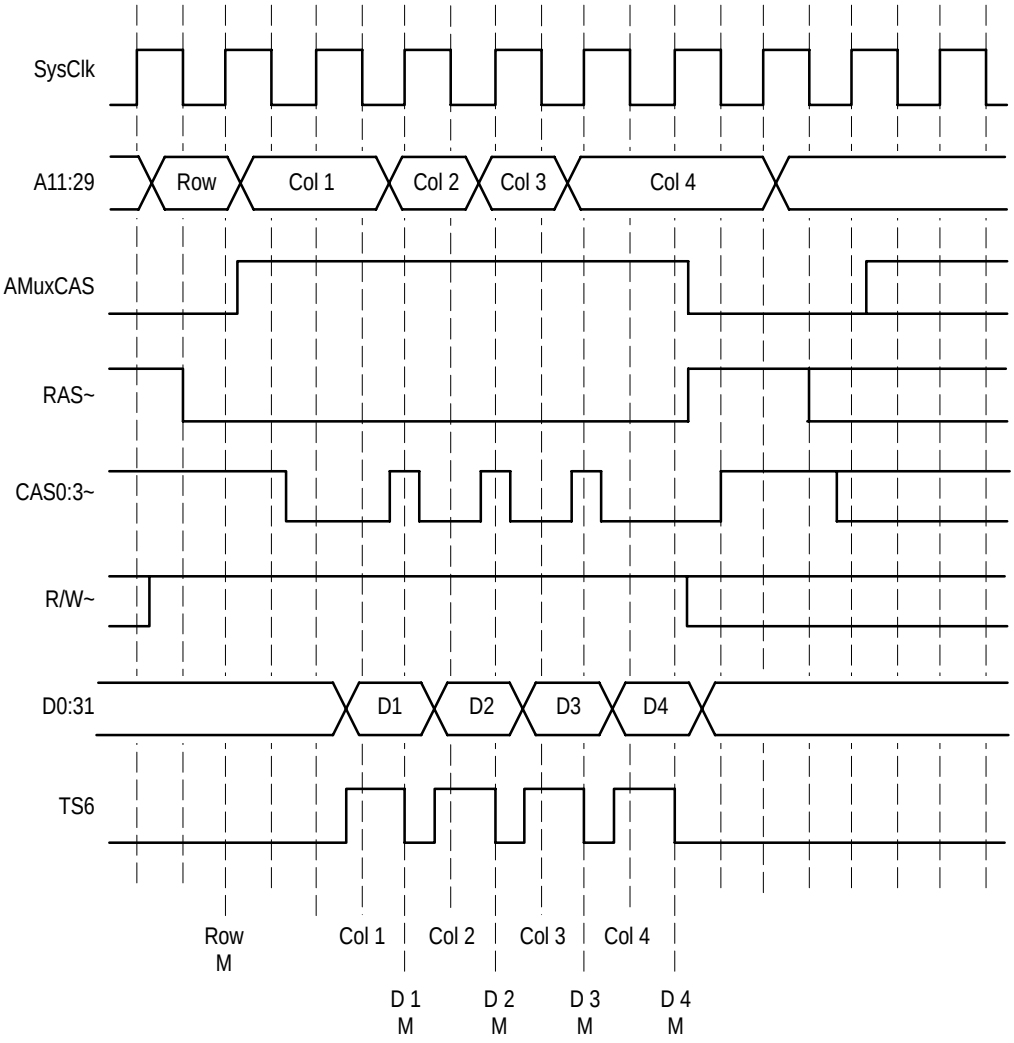

Figure 2–6: EDO DRAM 3-1-1-1 Read timing diagram

Symbols

The TMS 531 PPC 403GX support provides a symbol-table file. The 403GX_Ctrl file replaces specific control channel group values with symbolic values when Symbolic is the radix for the channel group.

Symbol tables are generally not used in timing or 403GX_T support disassembly.

Table 2–1 lists the name, bit pattern, and description for the symbols in the file, 403GX_Ctrl, in the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value Reset~ Halt~ Error TS4 / BusError~ HoldAck [1] AmuxCAS [2] R/W~ [3] / TS6 I/O [4] DRAMOE~ [5] DRAMWE~ [6] TS5 [7]	Description
Reset	0 X X X / X X X X / X X X X	Processor in Reset
Halt	1 0 X X / X X X X / X X X X	Halt command from ext debugger
System Error	1 1 1 X / X X X X / X X X X	Machine check error detected
Bus Error	1 1 0 X / 0 X X X / X X X X	Error in bus transaction
Alt Master Cycle	1 1 0 X / 1 1 X X / 1 X X X	External Master in control of bus
DMA Cycle	1 1 0 0 / 1 0 X X / 1 X X X	DMA Cycle
Row Address	1 1 0 1 / 1 0 0 X / 0 X X X	Row address for DRAM access
Inst Fetch	1 1 0 1 / 1 0 X 1 / 1 X X 1	Instruction Fetch Cycle
Data Read	1 1 0 1 / 1 0 X 1 / 1 X X 0	Data Read cycle
Data Write	1 1 0 1 / 1 0 X 0 / 1 X X 0	Data Write cycle
DRAM Read	1 1 0 1 / 1 0 1 1 / 1 0 1 0	DRAM Data cycle [8]
DRAM Write	1 1 0 1 / 1 0 1 0 / 1 1 0 0	DRAM Write cycle [8]

1 **Hold Acknowledge**

2 **DRAM Address mux select**

3 **Read/Write**

4 **Transfer Valid**

5 **DRAM Output Enable**

6 **DRAM Write Enable**

7 **Fetch/Read**

8 **These symbols are for triggering only; they will not be seen in the data display.**

Acquiring and Viewing Disassembled Data

The information in this section covers acquiring data, viewing disassembled data, and changing how data is displayed.

Acquiring Data

Once you load the PPC 403GX support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help.

Viewing Disassembled Data

You can view disassembled data in six display formats: Timing, State, Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–15.*

The default display format displays the Address, Data, and Control channel group values for each sample of acquired data.

If a channel group is not visible, you must use the Disassembly property page to make the group visible.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 lists these special characters and strings, and gives a definition of what they represent.

Table 2–2: Description of special characters in the display

Character or string displayed	Definition
#	The pound sign is used to indicate an immediate value. This value is dependent upon the target microprocessor assembler notation.
>	There is insufficient room on the screen to show all available data.
>>	Instruction fetch cycle has been manually marked by the user.
T	This indicates the given number is in decimal. Example: #12t (for 0xC in hexadecimal)
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.

State-Listing Display Format

In the State-Listing display format, bus cycles are displayed and not disassembled.

Hardware Display Format

In Hardware display format, all valid opcode fetch bus cycles are disassembled and displayed. Table 2–3 lists certain cycle-type labels in parentheses that the disassembler displays.

Table 2–3: Cycle-type labels for sequences and definitions

Label	Description
(DATA READ)	Data read from SRAM, ROM and EPROM
(DATA WRITE)	Data write to SRAM, ROM and EPROM
(DRAM DATA READ)	Data read from DRAM
(DRAM DATA WRITE)	Data write to DRAM
(D-CACHE FILL)	Data cache fill cycle
(I-CACHE FILL)	Instruction cache fill cycle
(ROW ADDRESS)	Row address of the DRAM access
(RESET)	Reset cycle
(HALT)	Halt state

Table 2–3: Cycle-type labels for sequences and definitions (cont.) (Cont.)

Label	Description
(DMA CYCLE)	DMA cycle
(SYSTEM ERROR)	System error
(ALTERNATE MASTER CYCLE)	Alternate master cycle
(BUS ERROR)	Error in bus transaction
(FLUSH)	This cycle was fetched but not executed
(EXTENSION)	This cycle is a extension to a preceding instruction opcode
(UNKNOWN)	This combination of control bits is unexpected and unrecognized

Figure 2–7 shows an example of the Hardware display.

Sample	403gx Address	403gx Data	403gx Mnemonics	403gx Control	Timestamp
85	7FFE25D5	E1------	(EXTENSION)	Inst Fetch	-1.920,50C
86	7FFE25D6	00------	(EXTENSION)	Inst Fetch	-1.800,50C
87	7FFE25D7	7C------	(EXTENSION)	Inst Fetch	-1.680,50C
88	7FFE25D8	80------	lwz r1,0x4(r1)	Inst Fetch	-1.530,50C
89	7FFE25D9	21------	(EXTENSION)	Inst Fetch	-1.410,50C
90	7FFE25DA	00------	(EXTENSION)	Inst Fetch	-1.290,50C
91	7FFE25DB	04------	(EXTENSION)	Inst Fetch	-1.170,50C
92	7FFE25DC	4C------	rfi	Inst Fetch	-1.020,50C
93	7FFE25DD	00------	(EXTENSION)	Inst Fetch	-900.50C
94	7FFE25DE	00------	(EXTENSION)	Inst Fetch	-780.50C
95	7FFE25DF	64------	(EXTENSION)	Inst Fetch	-660.50C
96	7FFE25E0	3C------	(FLUSH)	Inst Fetch	-510.50C
97	7FFE25E1	20------	(FLUSH)	Inst Fetch	-390.50C
98	7FFE25E2	00------	(FLUSH)	Inst Fetch	-270.50C
99	7FFE25E3	00------	(FLUSH)	Inst Fetch	-150.50C
100	00001000	--------	(ROW ADDRESS)	Row Address	-43.00C
101	00001000	70410000	andi. r1,r2,0x0	Inst Fetch	C
102	00001000	--------	(ROW ADDRESS)	Row Address	107.50C
103	BEGIN	3C608000	addis r3,r0,0x80000000	Inst Fetch	149.50C
104	00001000	--------	(ROW ADDRESS)	Row Address	257.50C
105	BEGIN+4	38C30100	addi r6,r3,0x100	Inst Fetch	299.50C
106	00001000	--------	(ROW ADDRESS)	Row Address	407.50C
107	BEGIN+8	81860000	lwz r12,0x0(r6)	Inst Fetch	450.00C
108	00001000	--------	(ROW ADDRESS)	Row Address	557.50C
109	BEGIN+C	85A60004	lwzu r13,0x4(r6)	Inst Fetch	600.00C
110	00000000	--------	(ROW ADDRESS)	Row Address	677.50C
111	00000100	FFFFFEFF	(DRAM DATA READ)	Data Read	719.50C
112	00001000	--------	(ROW ADDRESS)	Row Address	797.50C
113	BEGIN+10	7DCC6BD6	diww r14,r12,r13	Inst Fetch	840.50C

Figure 2–7: Example of the hardware display format

Software Display Format

The Software display format displays only the first fetch of executed instructions. Flushed cycles and extensions are not displayed, even though they are part of the executed instruction. Data reads and writes are not displayed. Special cycles are shown here, if they were displayed in Control Flow or Subroutine display formats.

Control Flow Display Format

The Control Flow display format displays only the first fetch of instructions that changes the flow of control.

Instructions that generate a change in the flow of control in the PPC 403GX microprocessor are as follows:

b ba bl bla rfi sc

Instructions that might generate a change in the flow of control in the PPC 403GX microprocessor are as follows:

bc	bca	bcl	bcla
bcctr	bcctrl	bclr	bclrl
tw	twi		

Instructions that generate an exception in the PPC 403GX microprocessor are as follows:

rfci	twi	twi

NOTE. *Special cycles displayed in Subroutine display format are also displayed in the Control Flow Display Format.*

Subroutine Display Format

The Subroutine display format displays only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the PPC 403GX microprocessor are as follows:

sc rfi

Instructions that might generate a subroutine call or a return in the PPC 403GX microprocessor are as follows:

tw twi

Instructions that generate an exception in the PPC 403GX microprocessor are as follows:

rfci	rfi	tw	twi

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the PPC 403GX support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception cycles

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

For the TLA 700 Series:

Show:	Hardware (default) Software Control Flow Subroutine
Highlight:	Software (default) Control Flow Subroutine None
Disasm Across Gaps:	Yes No (default)

Micro Specific Fields

Byte Ordering. Select one of the following options for Byte ordering.

Byte Order:	Big Endian (default) PCC Little Endian

Exception Vector Prefix. Enter an Exception prefix, depending on the system configuration.

Exception Prefix :	0000 (default)

Byte Enable. Select one of the following options for Byte Enable. If byte enable is selected as Write Only, Byte invalidation is not done for read cycles.

Byte Enable:	Read/Write (default) Write Only

DRAM Addr Mux. Select one of the following options for DRAM Addr Mux. If Internal is selected, address calculation is done.

DRAM Addr Mux:	Internal (default) External

MMU Address Translation. Select one of the following options for MMU Address Translation.

MMU Address Translation:	Disabled (default) Enabled

Bank Size [7-0]. You can enter one hexadecimal digit for each bank in the Bank Size field. The default is zero when a bank input field is not used.

Bank Size = One hexadecimal digit:

0 – 1 MB bank
1 – 2 MB bank
2 – 4 MB bank
3 – 8 MB bank
4 – 16 MB bank
5 – 32 MB bank
6 – 64 MB bank

The following is an example of Bank Size [7-0] field input

0 – 64 MB bank
1 – 64 MB bank
2 – 32 MB bank
3 – 16 MB bank
4 – 8 MB bank
5 – 4 MB bank
6 – 2 MB bank
7 – 1 MB bank

The following entry is displayed in the Bank Size [7-0] field for the previous example of different banks:

Bank	7 6 5 4 3 2 1 0
Bank Size [7-0]	0 1 2 3 4 5 6 6

Bus Width [7-0]. You can enter one hexadecimal digits for each bank in the Bus Width field. The default is zero when a bank input field is not used.

Bus Width = One hexadecimal digit:

0 – 8 bus width
1 – 16 bus width
2 – 32 bus width

The following is an example of Bus Width [7-0] field input:

0 – 32 MB bank
1 – 32 MB bank
2 – 32 MB bank
3 – 8 MB bank
4 – 8 MB bank
5 – 8 MB bank
6 – 16 MB bank
7 – 16 MB bank

The following entries are displayed in the Bus Width [7-0] field for the previous example for different banks

Bank	7 6 5 4 3 2 1 0
Bus Width [7-0]	1 1 0 0 0 2 2 2

NOTE*. The Bank Address is the same base register information you entered in the BRX register, which went into address bits A4 to A11 of the bus. Address bit A0 is always assumed to be 0, address bits A1 to A4 are 000 for DRAM and 111 for SRAM.*

Bank 0 Base Address. The Bank 0 Base Address contains the Base Address; it is an 8 bit field (2 hexadecimal digits).

The Default value is: 00

Bank 1 Base Address. The Bank 1 Base Address contains the Base Address; it is an 8 bit field (2 hexadecimal digits).

The Default value is: 00

Bank 2 Base Address. The Bank 2 Base Address contains the Base Address; it is an 8 bit field (2 hexadecimal digits).

The Default value is: 00

Bank 3 Base Address. The Bank 3 Base Address contains the Base Address; it is an 8 bit field (2 hexadecimal digits).

The Default value is: 00

Bank 4 Base Address. The Bank 4 Base Address contains the Base Address; it is an 8 bit field (2 hexadecimal digits).

The Default value is: 00

Bank 5 Base Address. The Bank 5 Base Address contains the Base Address; it is an 8 bit field (2 hexadecimal digits).

The Default value is: 00

Bank 6 Base Address. The Bank 6 Base Address contains the Base Address; it is an 8 bit field (2 hexadecimal digits).

The Default value is: 00

Bank 7 Base Address. The Bank 7 Base Address contains the Base Address; it is an 8 bit field (2 hexadecimal digits).

The Default value is: 00

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it.

NOTE. *The TMS 531 PPC 403GX support will only allow marking of instruction fetch cycles that also includes read extensions and flush cycles.*

Marks are placed by using the Mark Opcode button. The Mark Opcode button will always be available. If the sample being marked is not an Address cycle or

Data cycle of the potential bus master, the Mark Opcode selections will be replaced by a note indicating that an Opcode Mark cannot be placed at the selected data sample.

When a cycle is marked, the character >> is displayed immediately to the left of the Mnemonics column. Cycles can be unmarked by using the Undo Mark selection, which will remove the character >> (see Table 2–4).

Table 2–4: Mark selections and definitions

Mark selection or combination†	Definition
Opcode	Marks cycle as an instruction opcode
Flush	Marks cycle as a flushed cycle
Undo Mark	Removes all marks

Displaying Exception Labels

The disassembler can display PPC 403GX exception labels. The exception table must reside in external memory for interrupt and exception cycles to be visible to the disassembler.

Select the table prefix in the Exception Prefix field. The Exception Prefix field provides the disassembler with the prefix value. Select a three-digit hexadecimal value from the two values provided, corresponding to the prefix of the exception table.

These fields are located in the Disassembly property page (Disassembly Format Definition overlay) (see Table 2–5).

Table 2–5: Interrupt and exception labels

Offset	Displayed interrupt or exception name
0x0100	(CRITICAL INTERRUPT)
0x0200	(MACHINE CHECK)
0x0300	(DATA STORAGE EXCEPTION)
0x0400	(INSTRUCTION STORAGE EXCEPTION)
0x0500	(EXTERNAL INTERRUPT)
0x0600	(ALIGNMENT ERROR)
0x0700	(PROGRAM)
0x0C00	(SYSTEM CALL)
0x1000	(PROGRAM INTERVAL TIMER)
0x1010	(FIXED INTERVAL TIMER)
0x1020	(WATCHDOG TIMER)
0x1100	(DATA TLB MISS)

Table 2–5: Interrupt and exception labels (cont.)

Offset	Displayed interrupt or exception name
0x1200	(INSTRUCTION TLB MISS)
0x2000	(DEBUG EXCEPTION)

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your PPC 403GX microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your system under test.

Information on basic operations in your online help describes how to view the file.

Specifications

Specifications

This chapter contains the specifications for the TMS 531 PPC 403GX support.

Specification Tables

Table 3–1 lists the electrical requirements the system under test must produce for the support to acquire correct data.

Table 3–1: Electrical specifications

Characteristics	Requirements
System under test clock rate	
Specified clock rate	40 MHz Maximum
Tested clock rate	33 MHz
Minimum setup time required	2.5 ns
Minimum hold time required	0 ns

Replaceable Parts List

Replaceable Parts

This section contains a list of the replaceable parts for the TMS 531 PPC 403GX microprocessor support product.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
	071–0494–00			1	MANUAL,TECH INSTRUCTIONS,PPC403GX SUPPORT;TMS531	80009	071–0494–00

Index

A

B

C

D

E

F