Instruction Manual

Tektronix

TMS 871
1394 Bus Support Package

071-0637-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Connect the probe output to the measurement instrument before connecting the probe to the circuit under test. Disconnect the probe input from the circuit under test before disconnecting the probe from the measurement instrument.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This instruction manual contains specific information about the TMS 871 1394 Bus support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating support packages on the logic analyzer for which the TMS 871 1394 Bus support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Each logic analyzer has basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual. For complete information on packet types and field descriptions, refer to the *IEEE 1394_1995 Standard and the IEEE 1394a supplement*.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term “system under test (SUT)” refers to the 1394 Bus system from which data will be acquired.
- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.
- The term “module” refers to the Tektronix logic analyzer module for which this product was purchased.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For questions about using Tektronix measurement products, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Tektronix offers extended warranty and calibration programs as options on many products. Contact your local Tektronix distributor or sales office. For a listing of worldwide service centers, visit our web site.
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000 USA
Website	Tektronix.com

Getting Started

This chapter provides information on the following topics and tasks:

- A description of the TMS 871 1394 Bus support package
- Logic analyzer software compatibility
- Options and accessories
- Support restrictions
- How to connect to the system under test

Figure 1–1 shows components of the TMS 871 1394 Bus support package.

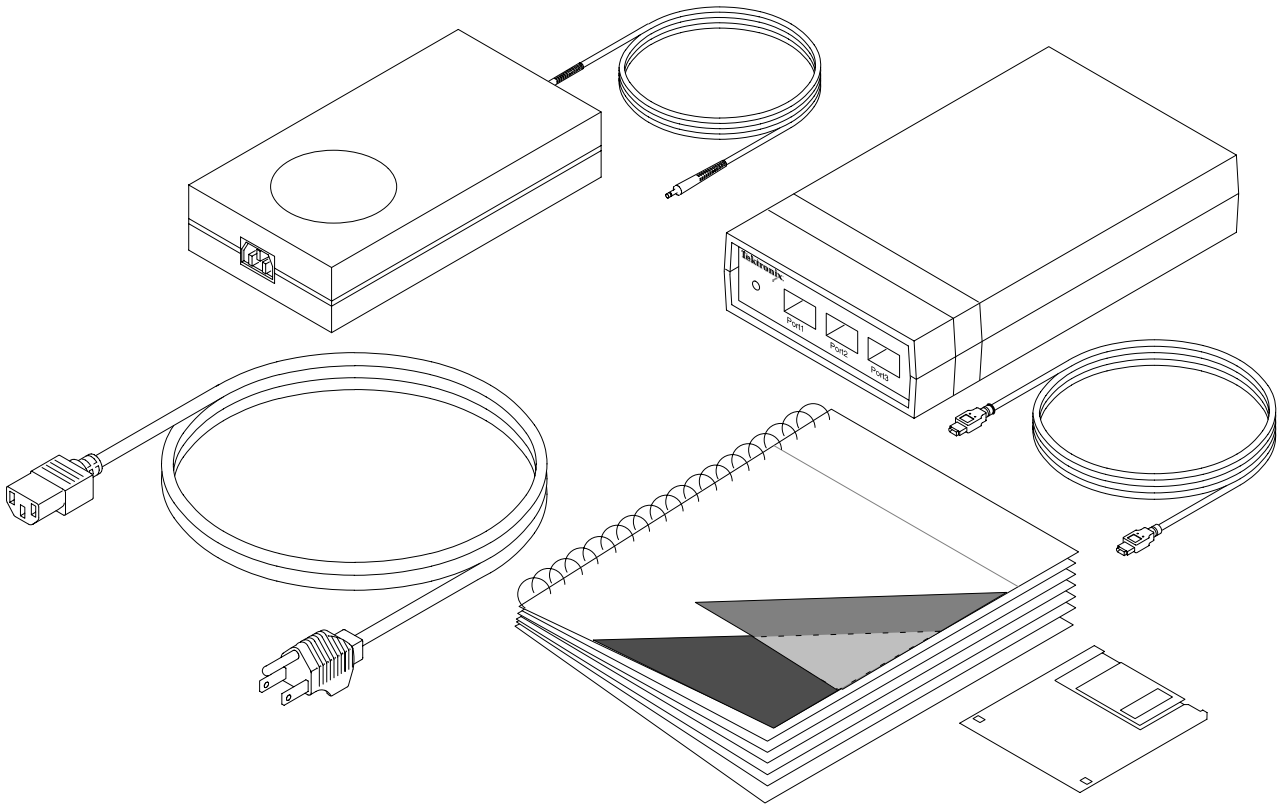

Figure 1–1: TMS 871 support package

Support Description

The TMS 871 1394 Bus support package displays data from the IEEE 1394 High Performance Serial Bus. The support runs on a compatible Tektronix logic analyzer equipped with a 68-channel or wider module, and requires two P6434 probes.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

Logic Analyzer Software Compatibility

The TMS 871 application software requires Version 3.0 and higher of TLA 700 System software running on the logic analyzer, and Version 3.0 and higher of TLA 700 LA module firmware on the modules you will be using.

Standard Accessories

The probe adapter is shipped with the following standard accessories:

- TMS 871 Support SW Disk
- TMS 871 Support Instruction Manual
- 1394 cable
- 5V power supply
- North American power cord

Options

The following options are available when ordering the TMS 871 Support:

- Option A1 Power Cord, Europe, 230 V
- Option A2 Power Cord, United Kingdom, 230 V
- Option A3 Power Cord, Australia, 230 V
- Option A5 Power Cord, Switzerland, 230 V
- Option 21 Add 2 P6434 Probes

Requirements and Restrictions

You should review the general requirements and restrictions of 1394 Bus support in the information on basic operations.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other support requirements and restrictions.

System Clock Rate

The TMS 871 support package can acquire data from the 1394 bus operating at speeds of 100, 200, or 400 Mb/s.

Merged Module Pair

If you have a pair of modules that are merged in the logic analyzer, you can un-merge them (and use either one). If you want the modules to remain merged, then the probe adapter must connect to the master module.

Connecting to a System Under Test

To connect the logic analyzer to the probe adapter, follow these steps:

CAUTION. *Static discharge can damage the probe adapter, the probes, or the module. To prevent static damage, handle all of these products only in a static-free environment.*

1. Plug the power supply into an appropriate power source.
2. Connect the DC plug to the probe adapter to provide power to the probe adapter.
3. Connect the P6434 probes to the 1394 probe adapter. Align the probe tip with the mating connector and gently connect as shown in Figure 1–2.

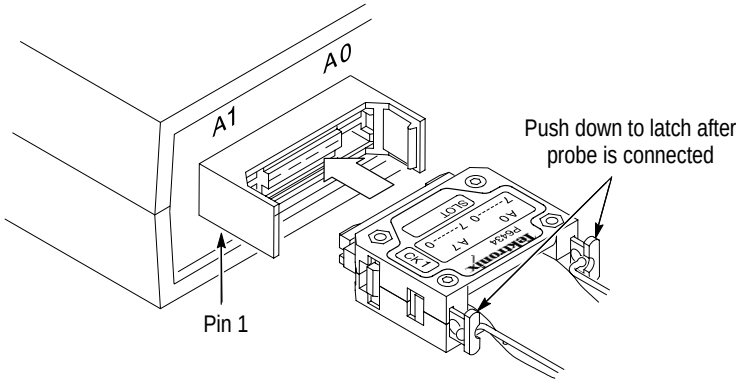

Figure 1–2: Connecting the cables to the probe adapter

CAUTION. *Incorrect handling of the P6434 probe while connecting it to the probe adapter can result in damage to the probe or to the mating connector on the probe adapter. To avoid damaging the probe and probe adapter, always position the probe perpendicular to the mating connector and gently connect the probe.*

4. Connect the module ends of the P6434 probes to the corresponding connectors on the logic analyzer. The probe module ends are keyed.

NOTE. *The right-side P6434 probe (as seen from the rear of the probe adapter) connects to D1–D0 and C3–C2 connectors on the logic analyzer. This may not match the color coding on a pre-labeled P6434 probe.*

5. Connect the 1394 probe adapter to the 1394 system under test using the 6-pin 1394 cable supplied with the probe adapter, or any standard 6-pin 1394 cable. Use any of the three ports on the front of the probe adapter.

6. The complete test setup appears in Figure 1–3 on page 1–5.

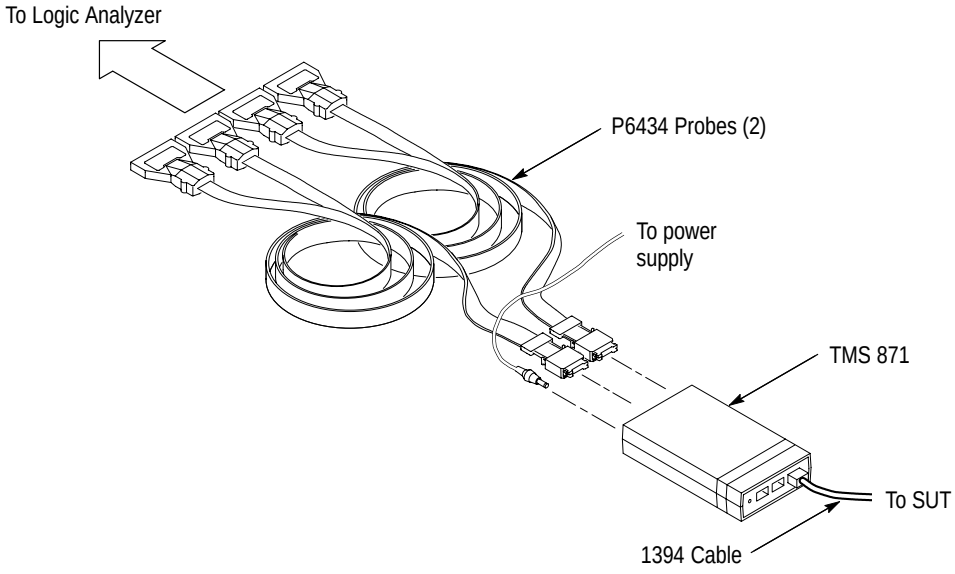

Figure 1–3: Complete test setup

Setting Up the Support

This section describes how to set up the support and includes these topics:

- Channel group definitions
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 871 support package. Information on basic operations describes general tasks and functions.

Before you acquire and display data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support.

Channel Groups

The defined channel groups are Data, Speed, Type, Event, Error, Count, Last_Data, Phy_Data, and Phy_Ctrl.

To see which signal is in which channel group, refer to the channel group assignment tables beginning on page 2–2. Tables 2–2 through 2–6 show the channel assignments for the setup.

Table 2–1: Displayed Channel Groups

Group name	Display radix
Data	HEX
Mnemonic	NONE (disassembly text generated by support)
Speed	SYM
Type	SYM[1]
Event	SYM[1]
Error	SYM[1]
Count	DEC
Last_Data	SYM[1]
Phy_Data	HEX[1]
Phy_Ctrl	SYM[1]
Timestamp	

[1] **These groups are acquired but not displayed in a default listing. They may be added to the listing window by the user.**

Symbols

The TMS 871 support supplies the following seven symbol table files:

- 1394_Error.tsf
- 1394_Event.tsf
- 1394_PCtrl.tsf
- 1394_Speed.tsf
- 1394_Type.tsf
- 1394_Last.tsf
- 1394_Tcode.tsf

Each file replaces specific channel group values with symbolic values when Symbolic is the radix for the channel group.

Error Group

The symbol table file for the Error group is 1394_Error.

The error group represents hardware errors that can occur on the bus. The symbol table shows the error code for the corresponding signal that was set. Multiple errors are not covered by the table.

Table 2–2 shows the 1394_Error symbol table.

Table 2–2: Error group symbol table definitions

Symbol	Error group value Iso_Cycle_Lost Cyc_Too_Long State_Timeout Quad_Align_Err Ack_Err Self_Packet_Err	Description
––	0 0 0 0 0 0	No Error
ISO_LOST	1 0 0 0 0 0	Isochronous cycle did not complete
ISO_LONG	0 1 0 0 0 0	Isochronous cycle exceeds maximum time
TIMEOUT	0 0 1 0 0 0	Phy stayed in one state too long
ALIGN_ERR	0 0 0 1 0 0	Quad data not ending on quadlet boundary
ACK_ERR	0 0 0 0 1 0	2nd nibble of ACK not logical inverse
SLFPKT_ERR	0 0 0 0 0 1	2nd quadlet of self-ID pkt not logical inverse

Event Group

The symbol table file for the Event group is 1394_Event.

The event group collects the validation strobe that, with SysClk, determine the packet is valid. The events are grouped for displaying added information in the listing and for triggering use.

Table 2–3 shows the 1394_Event symbol table.

Table 2–3: Event group symbol table definitions

Symbol	Event group value Arb_Gap Sub_Gap Data_Rdy Ack_Rcvd Reset HW_Error	Description
––	0 0 0 0 0 0	No event
ARB_GAP	1 0 0 0 0 0	Arbitration gap detected
SUB_GAP	0 1 0 0 0 0	Subaction gap detected
DATA_RDY	0 0 1 0 0 0	Quadlet data is valid
ACK_RCVD	0 0 0 1 0 0	Acknowledge data is valid
HW_ERROR	0 0 0 0 1 0	Hardware error has occured
RESET	X X X X X 1	Bus reset detected

PCtrl Group

The symbol table file for the PCtrl group is 1394_PCtrl.

The PCtrl group represents the PHY CTL signals as defined by 1394a. This group is not normally displayed. The information is for those advanced users who wish to look at the signals immediately available at the PHY-Link interface.

Table 2–4 shows the 1394_PCtrl symbol table.

Table 2–4: PCtrl group symbol table definitions

Symbol	PCtrl group value Phy_Ctrl_0 Phy_Ctrl_1	Description
IDLE	0 0	No activity
STATUS	1 0	PHY sending status info to link
RECEIVE	0 1	Packets being received
GRANT	0 0	PHY granting bus to link

Speed Group

The symbol table file for the Speed group is 1394_Speed.

The speed group indicates the bus speed as 100, 200, or 400 Mb/s.

Table 2–5 shows the 1394_Speed symbol table.

Table 2–5: Speed group symbol table definitions

Value	Speed group value Speed_0 Speed_1	Description
100	0 0	Speed is 100 Mb/s
200	1 0	Speed is 200 Mb/s
400	0 1	Speed is 400 Mb/s
–	1 1	Undefined

Type Group

The symbol table file for the Type group is 1394_Type.

The type group represents a collection of special packet identification signals.

Table 2–6 shows the 1394_Type symbol table.

Table 2–6: Type group symbol table definitions

Symbol	Type group value Bcast_Packet Self_Id_Packet Iso_Cyc	Description
––	0 0 0	Other packet type
BCAST	1 X X	Broadcast packet
SLFID	X 1 X	Self-Id packet
ISO	X X 1	Isochronous packet

Last_Data Group

The symbol table file for the Last_Data group is 1394_Last.

The Last_Data symbols label the one bit (last data quadlet in a packet) as true or false to clarify usage in Trigger Setups.

Table 2–7 shows the 1394_Last symbol table.

Table 2–7: Last_Data group symbol table definitions

Value	Last_Rx_Data
True	1
False	0

Tcode Group

The symbol table file for the Tcode group is 1394_Tcode. It is used for trigger setup to identify transaction codes in the Data group on the first quadlet of a packet.

Table 2–8 shows the 1394_Tcode symbol table.

Table 2–8: Tcode group symbol table definitions

	Tcode group value	
Symbol	Tcode	Description
WR_REQ_QUAD	X X X X X X 0 X	Write Request for Data Quadlet
WR_REQ_BLK	X X X X X X 1 X	Write Request for Data Block
WR_RESP	X X X X X X 2 X	Write Response
RD_REQ_QUAD	X X X X X X 4 X	Read Request for Data Quadlet
RD_REQ_BLK	X X X X X X 5 X	Read Request for Data Block
RD_RESP_QUAD	X X X X X X 6 X	Read Request for Data Quadlet
RD_RESP_BLK	X X X X X X 7 X	Read Response for Data Block
CYC_START	X X X X X X 8 X	Cycle Start
LOCK_REQ	X X X X X X 9 X	Lock Request
ISOCH	X X X X X X A X	Isochronous or Streaming Data
LOCK_RESP	X X X X X X B X	Lock Response

Information on basic operations describes how to modify an existing symbol table, create new symbol tables, and use symbolic values for triggering and displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Data

This section describes how to acquire data and view it in a listing window with the following topics and tasks:

- Acquiring data
- Trigger setups
- Clocking options
- Display options
- Displaying data

Acquiring Data

Once you load the 1394 setup, you can specify the trigger, choose a clocking mode, and acquire data.

If you have any problems acquiring data, refer to information on basic operations in your online help.

Trigger Setups

The signals available on the 1394 bus allow for many triggering possibilities. The .tla files include trigger setting examples, which will be similar to the example shown in Figure 2–1 on page 2–8.

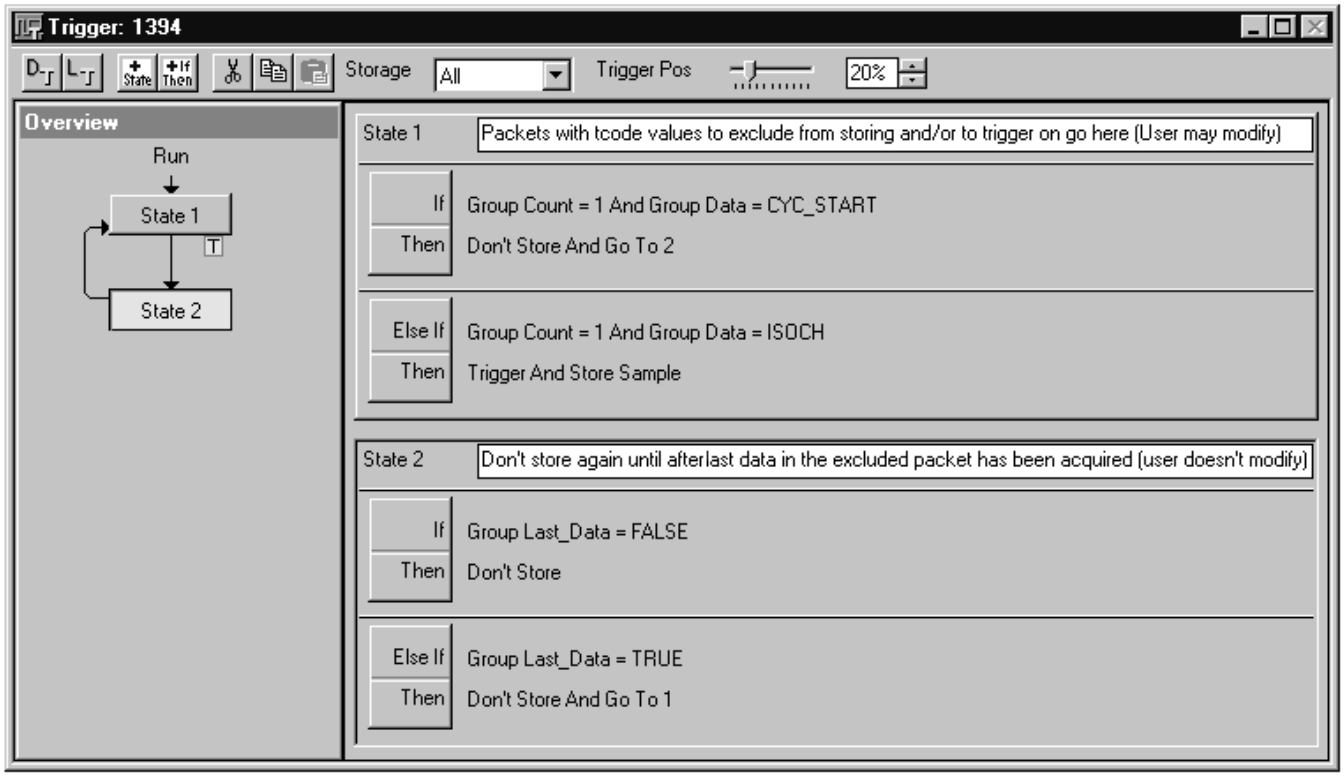

Figure 2–1: Trigger Setup Window

This trigger/capture state machine model can be used for a wide variety of situations. In this example, the default is to store everything with the State 1 being used to identify certain packet types by a specific tcode bit pattern in the first quadlet of the packet. The Last_Data group is TRUE only on the last quadlet which allows State 2 to exclude (not store) the entire packet identified in State 1. In this example, all Cycle Start packets are excluded from being stored and the logic analyzer is triggered on an Isochronous packet.

Note that the custom clocking options also allow the user to not store long packet data, gaps, and errors. As there is a limit to the number of clauses in a trigger state (typically 4), the custom clocking option should be examined for more complex triggering/storage situations.

Using the model shown in Figure 2–1, some variations useful to 1394 might be:

- Group Speed (symbolic). Can exclude packets labeled with a speed code. For example, all 100Mb/s packets can be excluded. State 2 is not needed.
- Group Event (symbolic for event). Singles out specific types of qualifying events. Overlaps custom clocking for gaps and errors. Useful for identifying trigger point, such as triggering on a bus reset.

- Group Count>n. Can be used to store only the first n bytes of the packet. State 2 is not needed. Note that this is covered for a value of 16 by a custom clocking option.
- Type (symbolic for type). Allows broadcast, self-id packets, or iso packets to be excluded. For more information, refer to Tables 3–7 and 3–13 on pages 3–6 and 3–8 for a description of the signals in this group. State 2 is not needed.
- Group Count=1 and Group Data=(symbolic for tcode). Allows various packet types to be excluded from storage. Used with State 2.
- Group Error=(symbolic for error). Singles out a specific type of error to not store or to trigger on. State 2 is not needed.
- Group Count=n and Group Data=HEX. Generic way to specify a packet by information known to be in a certain byte. For example, the destination address which is the first 16 bytes of the first quadlet for several different packet types. Used with State 2 to exclude capture from the identified quadlet through the end of the packet.

Custom Clocking

The TMS 871 will add the selection 1394 to the Load Support Package dialog box, under the File pulldown menu. Once the 1394 support has been loaded, the Custom clocking mode selection in the logic analyzer Setup menu is also enabled. Custom will be the default selection whenever the 1394 support has been loaded.

When Custom is selected, the TMS 871 support will modify the Custom Clocking Options menu to display three options:

- Clocking Mode
- Quadlet Capture
- Packet Truncation

The selections for these three options are defined below.

Clocking Mode

The Clocking Mode option allows the user to select either Normal or Raw Phy modes of clocking. Normal mode is used for disassembly and for all groups except Phy_Data and Phy_Ctrl. In Normal mode, different clock options are available.

Raw Phy mode clocks at twice the rate of Normal mode (the Phy-Link SCLK signal rate) and is used for acquiring the low-level Phy_Ctrl and Phy_Data group signals only. Because of the different clocking, other group values may or may

not be valid when acquired. Raw Phy mode is not useful for disassembly. When this mode is selected, the settings of the other two clocking options have no effect.

Quadlet Capture

There are four quadlet capture selections possible, listed below. These only take effect when the Clocking Mode is set to Normal. The All Valid selection is the default.

- All Valid. The all valid selection qualifies quadlets for acquisition by looking for a Data_Rdy, Arb_Gap, Sub_Gap, Ack_Rcvd, HW_Error, or Reset signal in the Event group (see Table 3–8 on page 3–6). This selection captures all the valid quadlets which include gaps, acks, and errors.
- All Valid, no gaps. Same as All Valid except Arb_Gap and Sub_Gap events are not captured.
- All Valid, no errors. Same as All Valid except errors (HW_errors) are not captured.
- All Valid, no gaps or errors. Same as All Valid except no gaps or errors are captured.

Packet Truncation

There are two selections possible here: None and After 16 quadlets. None is the default. These only take effect when the Clocking Mode is set to Normal.

- None. There is no attempt to truncate packets.
- After 16 quadlets. Only quadlets up to and including the 16th quadlet in each packet will be captured in this mode.

Display Options

The TMS 871 disassembles the fields of the packets specified in 1394-1995 and 1394a standards. The TMS 871 displays various levels of packet detail as selected by choosing one of five disassembly modes as described in *Displaying Data* on page 2–11.

Displaying Data

There are six formats to display 1394 bus cycles:

- Waveform (Timing)
- Listing (State):
  - All Fields
  - Selected Fields
  - Truncated Data
  - Packet Header
  - Packet Type

All Listing modes are available through the Disassembly Properties menu of the Listing display.

All Fields All captured data (packet data, packet header, gaps, errors, and ack data) will be displayed in this mode. Refer to Figure 2–2 on page 2–12.

All numeric values in the 1394 Mnemonics column are in hexadecimal, unless otherwise specified.

Sample	1394 Data	1394 Mnemonics		1394 Speed	1394 Count	Timestamp
219	FFFFFFFF	01E4:	FFFFFFFF	100	31	325.500 ns
220	4DDA5418	data_CRC:	4DDA5418	100	31	326.000 ns
221	--------	Subaction Gap		100	31	7.731,500 us
222	--------	Arbitration Gap		100	31	7.405,000 us
223	FFFF008F	CYCLE START		100	1	67.058,000 us
	FFFF008F	dest_ID:	FFFF(Local Bus, Bdcst Node)	100	1	
	FFFF008F	tl:	0	100	1	
	FFFF008F	rt:	0 (retry_1)	100	1	
	FFFF008F	tcode:	8	100	1	
	FFFF008F	pri:	F	100	1	
224	FFC1FFFF	source_ID:	FFC1(Local Bus, Node 01)	100	2	325.500 ns
225	F0000200	dest_offset:	FFFF F0000200	100	3	326.000 ns
226	6F3D1028	cycle_time:	6F3D1028	100	4	325.500 ns
227	00578D84	header_CRC:	00578D84	100	5	325.500 ns
228	01E87FA0	ISOCH STREAM DATA		100	1	1.139,000 us
	01E87FA0	data_length:	1E8 (488 decimal)	100	1	
	01E87FA0	tag:	1	100	1	
	01E87FA0	channel:	3F (63 decimal)	100	1	
	01E87FA0	tcode:	A	100	1	
	01E87FA0	sy:	0	100	1	
229	762784F4	headerCRC:	762784F4	100	2	326.000 ns
230	0178002F	0000:	0178002F	100	3	325.000 ns
231	8000FFFF	0004:	8000FFFF	100	4	325.500 ns
232	788700FF	0008:	788700FF	100	5	326.000 ns
233	FFFFFFFF	000C:	FFFFFFFF	100	6	325.500 ns
234	00000000	0010:	00000000	100	7	325.500 ns
235	00000000	0014:	00000000	100	8	325.500 ns
236	00000000	0018:	00000000	100	9	325.500 ns
237	00000000	001C:	00000000	100	10	325.500 ns
238	00000000	0020:	00000000	100	11	325.500 ns
239	00000000	0024:	00000000	100	12	325.500 ns
240	00000000	0028:	00000000	100	13	325.500 ns
241	00000000	002C:	00000000	100	14	325.500 ns
242	00000000	0030:	00000000	100	15	326.000 ns
243	00000000	0034:	00000000	100	16	325.000 ns
244	00000000	0038:	00000000	100	17	325.500 ns
245	00000000	003C:	00000000	100	18	326.000 ns
246	00000000	0040:	00000000	100	19	325.000 ns
247	00000000	0044:	00000000	100	20	326.000 ns
248	00000000	0048:	00000000	100	21	325.500 ns
249	00000000	004C:	00000000	100	22	325.500 ns
250	00000000	0050:	00000000	100	23	325.500 ns
251	00000000	0054:	00000000	100	24	325.500 ns
252	94870008	0058:	94870008	100	25	325.500 ns
253	9A130910	005C:	9A130910	100	26	326.000 ns
254	4D24E034	0060:	4D24E034	100	27	325.000 ns

Figure 2–2: All Fields Display

Selected Fields In this mode, only the most significant packet header data fields will be displayed and/or disassembled, along with all data. Gaps will not be displayed, nor will header or data CRC's. Ack data and errors will be displayed. Refer to Figure 2–3.

Sample	1394 Data	1394 Mnemonics		1394 Speed	1394 Count	Timestamp
223	FFFF008F	CYCLE START		100	1	82.520,500 us
	FFFF008F	dest_ID:	FFFF(Local Bus, Bdcst Node)	100	1	
	FFFF008F	tl:	0	100	1	
	FFFF008F	rt:	0 (retry_1)	100	1	
224	FFC1FFFF	source_ID:	FFC1(Local Bus, Node 01)	100	2	325.500 ns
226	6F3D1028	cycle_time:	6F3D1028	100	4	651.500 ns
228	01E87FA0	ISOCH STREAM DATA		100	1	1.464,500 us
	01E87FA0	data_length:	1E8 (488 decimal)	100	1	
	01E87FA0	tag:	1	100	1	
	01E87FA0	channel:	3F (63 decimal)	100	1	
	01E87FA0	sy:	0	100	1	
230	0178002F	0000:	0178002F	100	3	651.000 ns
231	8000FFFF	0004:	8000FFFF	100	4	325.500 ns
232	788700FF	0008:	788700FF	100	5	326.000 ns
233	FFFFFFFF	000C:	FFFFFFFF	100	6	325.500 ns
234	00000000	0010:	00000000	100	7	325.500 ns
235	00000000	0014:	00000000	100	8	325.500 ns
236	00000000	0018:	00000000	100	9	325.500 ns
237	00000000	001C:	00000000	100	10	325.500 ns
238	00000000	0020:	00000000	100	11	325.500 ns
239	00000000	0024:	00000000	100	12	325.500 ns
240	00000000	0028:	00000000	100	13	325.500 ns
241	00000000	002C:	00000000	100	14	325.500 ns
242	00000000	0030:	00000000	100	15	326.000 ns
243	00000000	0034:	00000000	100	16	325.000 ns
244	00000000	0038:	00000000	100	17	325.500 ns
245	00000000	003C:	00000000	100	18	326.000 ns
246	00000000	0040:	00000000	100	19	325.000 ns
247	00000000	0044:	00000000	100	20	326.000 ns
248	00000000	0048:	00000000	100	21	325.500 ns
249	00000000	004C:	00000000	100	22	325.500 ns
250	00000000	0050:	00000000	100	23	325.500 ns
251	00000000	0054:	00000000	100	24	325.500 ns
252	94870008	0058:	94870008	100	25	325.500 ns
253	9A130910	005C:	9A130910	100	26	326.000 ns
254	4D24E034	0060:	4D24E034	100	27	325.000 ns
255	BC711EE0	0064:	BC711EE0	100	28	326.000 ns
256	F6C19B14	0068:	F6C19B14	100	29	325.500 ns
257	B256A6A8	006C:	B256A6A8	100	30	325.500 ns
258	2A1D483C	0070:	2A1D483C	100	31	325.500 ns
259	77E00788	0074:	77E00788	100	31	325.500 ns

Figure 2–3: Selected Fields Display

Truncated Data This mode displays selected fields, but only the first 16 data quadlets of any data field. Refer to Figure 2–4.

Sample	1394 Data	1394 Mnemonics		1394 Speed	1394 Count	Timestamp
223	FFFF008F	CYCLE START		100	1	117.351,000 us
	FFFF008F	dest_ID:	FFFF(Local Bus, Bdcst Node)	100	1	
	FFFF008F	tl:	0	100	1	
	FFFF008F	rt:	0 (retry_1)	100	1	
224	FFC1FFFF	source_ID:	FFC1(Local Bus, Node 01)	100	2	325.500 ns
226	6F3D1028	cycle_time:	6F3D1028	100	4	651.500 ns
228	01E87FA0	ISOCH STREAM DATA		100	1	1.464,500 us
	01E87FA0	data_length:	1E8 (488 decimal)	100	1	
	01E87FA0	tag:	1	100	1	
	01E87FA0	channel:	3F (63 decimal)	100	1	
	01E87FA0	sy:	0	100	1	
230	0178002F	0000:	0178002F	100	3	651.000 ns
231	8000FFFF	0004:	8000FFFF	100	4	325.500 ns
232	788700FF	0008:	788700FF	100	5	326.000 ns
233	FFFFFFFF	000C:	FFFFFFFF	100	6	325.500 ns
234	00000000	0010:	00000000	100	7	325.500 ns
235	00000000	0014:	00000000	100	8	325.500 ns
236	00000000	0018:	00000000	100	9	325.500 ns
237	00000000	001C:	00000000	100	10	325.500 ns
238	00000000	0020:	00000000	100	11	325.500 ns
239	00000000	0024:	00000000	100	12	325.500 ns
240	00000000	0028:	00000000	100	13	325.500 ns
241	00000000	002C:	00000000	100	14	325.500 ns
242	00000000	0030:	00000000	100	15	326.000 ns
243	00000000	0034:	00000000	100	16	325.000 ns
244	00000000	0038:	00000000	100	17	325.500 ns
355	FFFF008F	CYCLE START		100	1	117.352,000 us
	FFFF008F	dest_ID:	FFFF(Local Bus, Bdcst Node)	100	1	
	FFFF008F	tl:	0	100	1	
	FFFF008F	rt:	0 (retry_1)	100	1	
356	FFC1FFFF	source_ID:	FFC1(Local Bus, Node 01)	100	2	325.500 ns
358	6F3D2028	cycle_time:	6F3D2028	100	4	651.000 ns
360	01E87FA0	ISOCH STREAM DATA		100	1	1.465,000 us
	01E87FA0	data_length:	1E8 (488 decimal)	100	1	
	01E87FA0	tag:	1	100	1	
	01E87FA0	channel:	3F (63 decimal)	100	1	
	01E87FA0	sy:	0	100	1	

Figure 2–4: Truncated Data in a Selected Field

Packet Header This mode displays the selected header fields, without data quadlets. Refer to Figure 2–5.

Sample	1394 Data	1394 Mnemonics		1394 Speed	1394 Count	Timestamp
223	FFFF008F	CYCLE START		100	1	122.559,000 us
	FFFF008F	dest_ID:	FFFF(Local Bus, Bdcst Node)	100	1	
	FFFF008F	tl:	0	100	1	
	FFFF008F	rt:	0 (retry_1)	100	1	
224	FFC1FFFF	source_ID:	FFC1(Local Bus, Node 01)	100	2	325.500 ns
226	6F3D1028	cycle_time:	6F3D1028	100	4	651.500 ns
228	01E87FA0	ISOCH STREAM DATA		100	1	1.464,500 us
	01E87FA0	data_length:	1E8 (488 decimal)	100	1	
	01E87FA0	tag:	1	100	1	
	01E87FA0	channel:	3F (63 decimal)	100	1	
	01E87FA0	sy:	0	100	1	
355	FFFF008F	CYCLE START		100	1	122.560,500 us
	FFFF008F	dest_ID:	FFFF(Local Bus, Bdcst Node)	100	1	
	FFFF008F	tl:	0	100	1	
	FFFF008F	rt:	0 (retry_1)	100	1	
356	FFC1FFFF	source_ID:	FFC1(Local Bus, Node 01)	100	2	325.500 ns
358	6F3D2028	cycle_time:	6F3D2028	100	4	651.000 ns
360	01E87FA0	ISOCH STREAM DATA		100	1	1.465,000 us
	01E87FA0	data_length:	1E8 (488 decimal)	100	1	
	01E87FA0	tag:	1	100	1	
	01E87FA0	channel:	3F (63 decimal)	100	1	
	01E87FA0	sy:	0	100	1	
487	FFFF008F	CYCLE START		100	1	122.559,500 us
	FFFF008F	dest_ID:	FFFF(Local Bus, Bdcst Node)	100	1	
	FFFF008F	tl:	0	100	1	
	FFFF008F	rt:	0 (retry_1)	100	1	
488	FFC1FFFF	source_ID:	FFC1(Local Bus, Node 01)	100	2	325.500 ns
490	6F3D3028	cycle_time:	6F3D3028	100	4	651.000 ns
492	01E87FA0	ISOCH STREAM DATA		100	1	1.465,000 us
	01E87FA0	data_length:	1E8 (488 decimal)	100	1	
	01E87FA0	tag:	1	100	1	
	01E87FA0	channel:	3F (63 decimal)	100	1	

Figure 2–5: Packet Header Display

Packet Type This mode displays errors and Ack data, but only one line for each packet (packet type) is displayed . Refer to Figure 2–6.

Sample	1394 Data	1394 Mnemonics	1394 Speed	1394 Count	Timestamp
91	FFFF008F	CYCLE START	100	1	0 ps
96	01E87FA0	ISOCH STREAM DATA	100	1	2.441,500 us
223	FFFF008F	CYCLE START	100	1	122.559,000 us
228	01E87FA0	ISOCH STREAM DATA	100	1	2.441,500 us
355	FFFF008F	CYCLE START	100	1	122.560,500 us
360	01E87FA0	ISOCH STREAM DATA	100	1	2.441,500 us
487	FFFF008F	CYCLE START	100	1	122.559,500 us
492	01E87FA0	ISOCH STREAM DATA	100	1	2.441,500 us

Figure 2–6: Packet Type Display

1394 Bus Packets

Refer to the *IEEE 1394_1995 Standard and the IEEE 1394a supplement* for complete information on packet types and field descriptions.

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Channel assignment tables
- Signal descriptions

Probe Adapter Description

The probe adapter consists of an enclosed unit with three 6-pin connectors for 1394 Bus connections, and two 34-pin connectors for the LA interconnect (via P6434 probes). Power is provided by an external power supply that plugs into the back of the probe adapter. Signals from the 1394 Bus cable flow into the probe adapter and through the P6434 probes to the logic analyzer.

All probe adapter circuitry is powered from an external power supply which must supply 5-15 volts DC, at 350 milliamps maximum. The adapter has an internal fuse and circuitry which protects against damage from reversed-polarity power supply connections.

The probe adapter contains 3-port, 1394a-compliant PHY circuitry. The probe adapter, following 1394 protocols, causes a bus reset when connected, when it arbitrates for a node on the bus. Once connected, the probe adapter does not generate any traffic from the Link layer, and does not expect any traffic to be addressed to it.

After connecting, the probe adapter monitors all PHY-link data and conditions the data with an on-board FPGA to generate signals for acquisition and triggering by the logic analyzer.

The signals presented by the probe adapter to the logic analyzer are TTL level with a clocking speed of 50 MHz or less. The probe adapter does not cause excessive loading on critical signals.

Probe Adapter Functions

The probe adapter captures the following types of bus packets and events.

- Asynch Quadlet
- Isoch Quadlet
- Self ID Quadlet
- Phy Config Quadlet
- Ack Byte
- Arb Gap
- Sub-Action Gap
- Bus Reset

The following Hardware Errors are detected:

- Isochronous cycle lost
- Isochronous cycle too long
- State timeout
- Quadlet alignment error
- Acknowledge packet error
- Self ID packet error

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a 1394-1995 or 1394a-compliant device. The system must be connected in a legal 1394 topology and running at S100, S200, or S400 speeds. Table 3–1 shows the electrical requirements of the probe adapter in order for the support to acquire correct data.

Table 3–1: Electrical specifications

Characteristics	Requirements
Probe Adapter DC power requirements	
5 V Vcc Voltage	4.75–5.25 VDC
5 V Vcc Current	I max (calculated) 350 mA

Table 3–2 shows the environmental specifications.

Table 3–2: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)
Minimum operating	10° C (+50° F)
Non-operating	–50° C to +75° C (–67° to +167° F)

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

Table 3–3 shows the compliances that apply to the probe adapter.

Table 3–3: Certifications and compliances

EMC Compliance	Meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility when it is used with the product(s) stated in the specifications table. Refer to the EMC specification published for the stated products. May not meet the intent of the directive if used with other products.
FCC Compliance	Emissions comply with FCC Code of Federal Regulations 47, Part 15, Subpart B, Class A Limits.

Figure 3–1 shows the dimensions of the probe adapter.

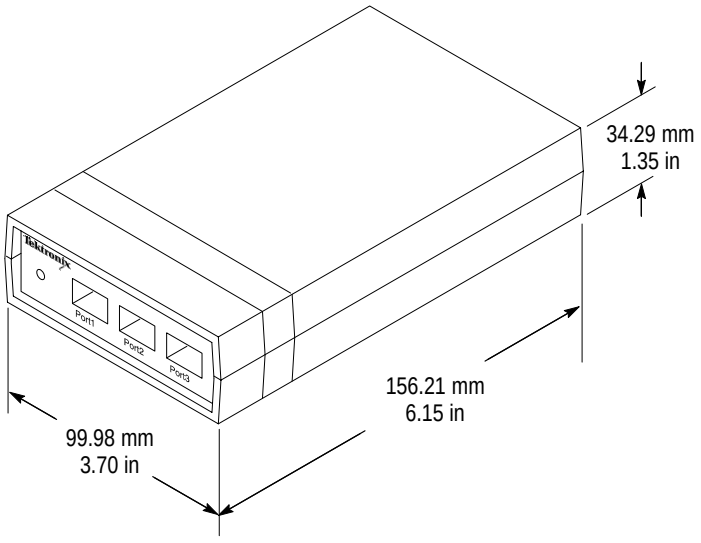

Figure 3–1: Dimensions of the probe adapter

Channel Assignments

Channel assignments shown in Table 3–5 through Table 3–14 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB). Note that 1394 convention labels the most significant bit as zero.
- Section:channel refers to the module channel number.

The group assignment tables indicate whether the signal is required for custom clocking and/or the disassembly. Required signals must be connected to properly strobe and login bus data into acquisition memory, and to disassemble the acquired bus data.

Channel groups will be displayed in the order shown in Table 3–4.

Table 3–4: Channel group display order

Group name	Display radix
Data	HEX
Mnemonic	None (disassembly text generated by support package software)
Speed	SYM
Type	SYM (default not displayed)
Event	SYM (default not displayed)
Error	SYM (default not displayed)
Count	DEC
Last_Data	SYM (default not displayed)
Phy_Data	HEX (default not displayed)
Phy_Ctrl	SYM (default not displayed)
Timestamp	

Table 3–5 shows the probe section and channel assignments for the Quad group and the signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: Quad_Data group assignments

Bit order	Section:channel	Signal name	Required for clocking or disassembly
31	A3:7	Data_0	Disassembly
30	A3:6	Data_1	Disassembly
29	A3:5	Data_2	Disassembly
28	A3:4	Data_3	Disassembly
27	A3:3	Data_4	Disassembly
26	A3:2	Data_5	Disassembly
25	A3:1	Data_6	Disassembly
24	A3:0	Data_7	Disassembly
23	A2:7	Data_8	Disassembly
22	A2:6	Data_9	Disassembly
21	A2:5	Data_10	Disassembly
20	A2:4	Data_11	Disassembly
19	A2:3	Data_12	Disassembly
18	A2:2	Data_13	Disassembly
17	A2:1	Data_14	Disassembly
16	A2:0	Data_15	Disassembly
15	A1:7	Data_16	Disassembly
14	A1:6	Data_17	Disassembly
13	A1:5	Data_18	Disassembly
12	A1:4	Data_19	Disassembly
11	A1:3	Data_20	Disassembly
10	A1:2	Data_21	Disassembly
9	A1:1	Data_22	Disassembly
8	A1:0	Data_23	Disassembly
7	A0:7	Data_24	Disassembly
6	A0:6	Data_25	Disassembly
5	A0:5	Data_26	Disassembly
4	A0:4	Data_27	Disassembly
3	A0:3	Data_28	Disassembly
2	A0:2	Data_29	Disassembly
1	A0:1	Data_30	Disassembly
0	A0:0	Data_31	Disassembly

Table 3–6 shows the Speed group assignments. The default radix of the Speed group is SYMBOLIC. The symbol table filename is 1394_Speed.

Table 3–6: Speed group assignments

Section:channel	Signal name	Required for clocking or disassembly
C3:1	Speed_0	No
C3:0	Speed_1	No

Table 3–7 shows the Type group assignments. The default radix of the Type group is SYMBOLIC. The symbol table filename is 1394_Type.

Table 3–7: Type group assignments

Section:channel	Signal name	Required for clocking or disassembly
C2:7	Bcast_Packet	No
C2:6	Self-Id_Packet	No
C2:5	Iso_Cyc	No

Table 3–8 lists the Event group assignments. The default radix of the event group is SYMBOLIC. The symbol table filename is 1394_Event.

Table 3–8: Event group assignments

Section:channel	Signal name	Required for clocking or disassembly
C2:3	Arb_Gap	Both
C2:2	Sub_Gap	Both
C2:1	Data_Rdy	Both
C2:0	ACK_Rcvd	Both
CLK:1	HW_Error	Both
CLK:3	Reset	Both

Table 3–9 lists the Error group assignments. The default radix of the Error group is SYMBOLIC. The symbol table filename is 1394_Error.

Table 3–9: Error group assignments

Section:channel	Signal name	Required for clocking or disassembly
C3:7	Iso_Cycle_Lost	No
C3:6	Cyc_Too_Long	No
C3:5	State_Timeout	No
C3:4	Quad_Align_Err	No
C3:3	Ack_Err	No
C3:2	Self_Packet_Err	No

Table 3–10 shows the Count group assignments. The default radix of the Count group is DECIMAL.

Table 3–10: Count group assignments

Section:channel	Signal name	Required for clocking or disassembly
CLK:2	Count_0	Disassembly
D1:3	Count_1	Disassembly
D1:2	Count_2	Disassembly
D1:1	Count_3	Disassembly
D1:0	Count_4	Disassembly

Table 3–11 shows the Last_Data group assignments. The default radix of the Last_Data group is SYMBOLIC. The symbol table filename is 1394_Last.

Table 3–11: Last_Data group assignments

Section:channel	Signal name	Required for clocking or disassembly
D1:5	Last_Rx_Data	No

Table 3–12 shows the Phy_Data group assignments. The default radix of the Phy_Data group is HEX.

Table 3–12: Phy_Data group assignments

Section:channel	Signal name	Required for clocking or disassembly
D0:7	Phy_Data_0	No
D0:6	Phy_Data_1	No
D0:5	Phy_Data_2	No
D0:4	Phy_Data_3	No
D0:3	Phy_Data_4	No
D0:2	Phy_Data_5	No
D0:1	Phy_Data_6	No
D0:0	Phy_Data_7	No

Table 3–13 shows the Phy_Ctrl group assignments. The default radix of the Phy_Ctrl group is SYMBOLIC. The symbol table filename is 1394_PCtrl.

Table 3–13: Phy_Ctrl group assignments

Section:channel	Signal name	Required for clocking or disassembly
D1:7	Phy_Ctrl_0	No
D1:6	Phy_Ctrl_1	No

Table 3–14 lists the Clock and Qualifier channel assignments that are used as clocks and/or qualifiers to the Clocking State Machine.

Table 3–14: Clock and qualifier channel assignments

Section:channel	Signal name
CLK:0	Sys Clk
CLK:1	HW_Error
CLK:2	Count_0
CLK:3	Reset
C2:0	Ack_Rcvd
C2:1	Data_Rdy
C2:2	Sub_Gap
C2:3	Arb_Gap

Signal Descriptions

This section includes a table that lists all of the signals generated by the probe adapter with a short description of each. See Table 3–15.

Table 3–15: Signal descriptions

Signal name	Description
SysClk	Master clock at half the rate of the PHY_Link SCLK signal.
Arb_Gap	Indicates an arbitration gap has been detected on the 1394 bus.
Sub_Gap	Indicates a subaction gap has been detected on the 1394 bus.
Data_Rdy	Indicates the data quadlet on the data lines has changed and is valid. This signal is also used to strobe the data quadlet and most control signals into the logic analyzer.
Ack_Rcvd	Indicates an acknowledge packet is being transsmitted on the bus and is present on the 8 least significant bits of quadlet data (Data[24:31]).
Count[0:4]	These bits indicate the count of the current quadlet being transmitted during the packet. Legal values for the count bits are from 1 through 30, inclusive. A count value of 31 is used to indicate a quadlet count value greater than 30.
Speed[0:1]	These bits indicate the speed of the data being transmitted. See Table 2–5.
Bcast_Packet	This signal is asserted during all broadcast packets. A broadcast packet is detected when the destination ID of a packet is 3FF:3F (the 16 bit destination ID is all ones). This signal will remain asserted during the entire packet transfer, including the arbitration and subaction gap periods. This signal will be deasserted only upon the detection of a packet whose destination ID is not 3FF:3F.
Iso_Cyc	This signal will be asserted upon detection of a cycle start packet and will remain asserted during the entire isochronous data transfer cycle.
Self_Id_Packet	Indicates the current quadlet is part of a self-ID packet.
Data[0:31]	Data from the 1394 bus are presented on these data lines in quadlet format. Acknowledge packets are also presented on the 8 least significant bits of the data lines.
Phy_Ctrl[0:1]	The CTL signals from the PHY-Link interface used for low level acquisitions.
Phy_Data[0:7]	The data signals from the PHY-Link interface used for low level acquisitions.
Last_Rx_Data	Indicates the current quadlet is the final quadlet of the packet.
Reset	Indicates that a bus reset state has been detected on the 1394 bus.
HW_Error	Indicates that a hardware error has occurred. This signal is strobed when any of the six specific hardware errors occurs (described below), and is used as the hardware error strobe signal.
Iso_Cycle_Lost	This error signal is asserted with HW_Error when an isochronous cycle did not complete.
Iso_Cycle_Too_Long	This error signal is asserted with HW_Error when an isochronous cycle exceeded the maximum time.

Table 3–15: Signal descriptions (cont.)

Signal name	Description
State_Timeout	This error signal is asserted with HW_Error when the PHY stayed in a particular state too long. This is usually caused by a loop in the cable topology.
Quad_Align_Err	This error signal is asserted with HW_Error when the quadlet data did not end on a quadlet boundary.
Ack_Err	This error signal is asserted with HW_Error when the second nibble of an ack packet is not the logical inverse of the first nibble packet.
Self_Packet_Err	This error signal is asserted with HW_Error when the second quadlet of a self-ID packet is not the logical inverse of the first quadlet of the self-ID packet.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Functional Verification

This chapter contains the following topics:

- Verifying Probe Adapter Clock Activity-verifies internal probe adapter circuitry
- Verifying Probe Adapter Functionality with a TLA System-verifies internal probe adapter circuitry and P6434 interface to the logic analyzer
- Troubleshooting

Probe Adapter Circuit Description

The probe adapter contains a three-port, 1394a-compatible, commercial PHY chip to connect to the 1394 bus system under test and to monitor bus traffic. An on-board FPGA conditions the PHY-Link signals for acquisition and display by the logic analyzer. The probe adapter uses an external power supply to furnish the 5 volts necessary to power the circuitry. An internal, resettable thermal fuse is used for circuit protection. You can monitor the system clock signal (PHY-Link SCLK/2) to verify the circuitry is active when the probe adapter is on.

Equipment Required

Table 4–1 lists the equipment you will need to verify circuit operation. You can use an oscilloscope to check the system clock presence, or view the signal activity if a logic analyzer is available.

Table 4–1: Equipment list

Item description	Recommended example
Screwdriver	Phillips #2
DMM	TX1, TX3
Oscilloscope (25 MHz minimum, TTL level)	TDS210
Logic Analyzer (optional)	TLA 700 with 68-channel module
Two Logic Analyzer Probes (optional)	P6434

Verifying Clock Activity Using an Oscilloscope

For verifying the probe adapter functionality, there is a diagnostic test point connected to the SysClk signal which may be used with an oscilloscope to determine basic operation of the PHY and link chips.

Use the following procedure to verify clock activity in the probe adapter:

1. Plug in the power supply and connect the power jack to the circuit board.
2. Verify the green LED on the front of the probe adapter is lit. If it is not lit, either power is not being supplied correctly to the probe adapter or the probe adapter is defective. See *Troubleshooting* on page 4–4.
3. To access the interal test point, remove the two philips screws accessible from the bottom of the probe adapter case.
4. Remove the top half of the probe adapter case, exposing the top of the circuit board.
5. Connect an oscilloscope probe to the SCLK/2 test point. See Figure 4–1.

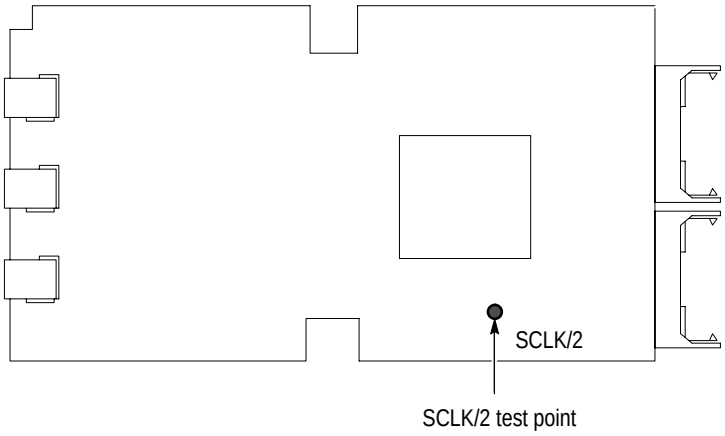

Figure 4–1: SCLK/2 (system clock) signal test point

6. Verify that a TTL-level square wave signal at about 25 MHz is present. Absence of this signal indicates the circuit is not operating correctly. See *Troubleshooting* on page 4–4.

Note that SCLK/2 is the system clock, and it must be active for the custom clocking feature to acquire any data at all.

Verifying Probe Adapter Functionality with the TLA System Activity Monitor

If you have a logic analyzer, module, and probes are available, use the following procedure to verify the probe adapter functionality:

1. Plug in the power supply and connect the power jack to the probe adapter.
2. Verify the green LED on the front of the probe adapter is lit. If it is not lit, either power is not being supplied correctly to the probe adapter or the probe adapter is defective. See *Troubleshooting* on page 4–4.
3. Power on the system and load the 1394 support from the logic analyzer application. The probe adapter should not be connected to a 1394 bus system for this test.
4. Connect the logic analyzer module to the 1394 probe adapter with two P6434 probes. Note that one P6434 connects to A3–A2 and A1–A0 and the other P6434 connector connects to C3–C2 and D1–D0 as indicated on the probe adapter rear panel.
5. Using the supplied 1394 cable, connect any two of the three 1394 ports together to form a 1394 bus loop.
6. Wait for 1 or 2 seconds and then disconnect the cable from both ports.
7. View the activity window in the setup window of the TLA 700 application.

Look for an activity pattern as shown in Figure 4–2. Deviations from this pattern indicate the probe adapter circuitry is not operating correctly or there may be a problem with the logic analyzer probe hookup. Note that CK0 is the system clock and must be active for the support's custom clocking to acquire any data at all.

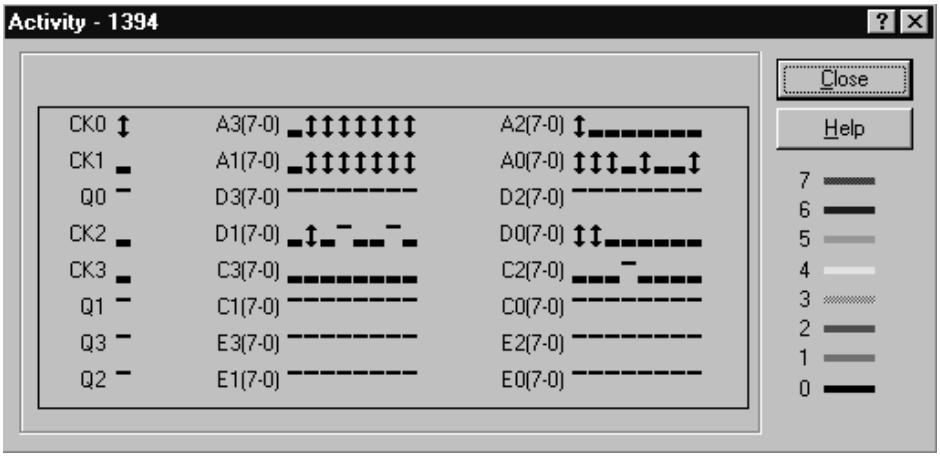

Figure 4–2: Activity pattern

Troubleshooting

If the probe adapter does not appear to function, and the cable and probe connections appear good, you may have a power supply problem. Perform the following steps to verify the power supply is working:

1. Disconnect the power supply from the back of the probe adapter.
2. Check the output with a DMM-it should measure 5 volts.

If the power supply does not measure 5 volts, replace it and verify the probe adapter functions correctly.

If the power supply is not the problem, the fuse inside the probe adapter might be tripped. Do the following steps to reset the fuse:

1. Disconnect the power to the probe adapter.
2. Wait 3 or 4 seconds.
3. Reconnect the power to the probe adapter.
4. If the green LED is lit, retest the probe adapter, using either the *Oscilloscope* or the *Activity Monitor* checks. If the probe adapter still does not work, the probe adapter unit might be defective. Contact your local Tektronix service center.
5. If the green LED is not lit, and the power supply is not the problem, the probe adapter unit might be defective. Contact your local Tektronix service center.

If the square-wave signal is absent when performing the oscilloscope check, the probe adapter unit might be defective. Contact your local Tektronix service center.

If the *Activity Monitor* check fails, the probe adapter unit might be defective. Contact your local Tektronix service center.

Replaceable Parts

This chapter contains a list of the replaceable components for the TMS 871 1394 Bus support.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Parts List

The tabular information in the Replaceable Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1-1972.

Chassis Parts Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Parts List.

Mfr. Code to Manufacturer Cross Index The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077-0001
14310	AULT INC	7105 NORTHLAND TERRACE	MINNEAPOLIS, MN 55428–1534
22526	FCI/BERG ELECTRONICS INC	825 OLD TRAIL ROAD	ETTERS, PA 17319–9769
S3109	FELLER U.S. CORPORATION	72 VERONICA AVE UNIT #5	SOMERSET, NJ 08873
TK1373	PATELEC–CEM	10156 TORINO VAICENTALLO 62/456	ITALY,
TK2541	AMERICOR ELECTRONICS LTD	UNIT–H 2682 W COYLE AVE	ELK GROVE VILLAGE, IL 60007
TK2548	XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON, OR 97005
TK6318	DATA TRANSIT	612 MINDY WAY	SAN JOSE, CA 95123

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
5–1	119-6253-00			1	ADAPTER,PROBE:1394 ASSEMBLY,TMS871 OPT 01	TK6318	119-6253-00
					STANDARD ACCESSORIES		
–2	119-5061-01			1	POWER SUPPLY:25W,5V 5A,CONCENTRIC 2MM,90-265V, 47-63 HZ IEC,15X8.6X5 CM, UL,CSA, TUV,IEC,SELF	14310	SW108KA0002F01
–3	161-0104-00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,RTANG,IEC320, RCPT X STR,NEMA 15-5P,W/CORD GRIP	S3109	ORDER BY DESCRIPTION
–4	012–1567–00			1	CA ASSY:IEEE 1394, 48 L,STANDARD FIREWIRE CABLE	22526	84865–122D
	071-0637-00			1	MANUAL,TECH:INSTRUCTION,TMS871	TK2548	071-0637-00
					OPTIONS AND OPTIONAL ACCESSORIES		
5–2–1	P6434			2	P6434 MASS TERMINATION PROBE, OPT 21 *	80009	ORDER BY DESCRIPTION
	161-0104-06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG, IEC320,RCPT,EUROPEAN,SAFETY CONTROLLED, OPT A1	TK1373	ORDER BY DESCRIPTION
	161-0104-07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10A,2.5 METER,RTANG, IEC320,RCPT X 13A,UNITED KINGDOM,SAFETY CON-TROLLED, OPT A2	TK2541	ORDER BY DESCRIPTION
	161-0104-05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG, IEC320,RCPT,AUSTRALIA,SAFETY CONTROLLED, OPT A3	TK1373	161-0104-05
	161-0167-00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10A,2.5 METER,RTANG, IEC320,RCPT,SWISS,NO CORD GRIP,SAFETY CONTROLLED, OPT A5	S3109	ORDER BY DESCRIPTION

*** Check the P6434 manual for detailed replaceable part information.**

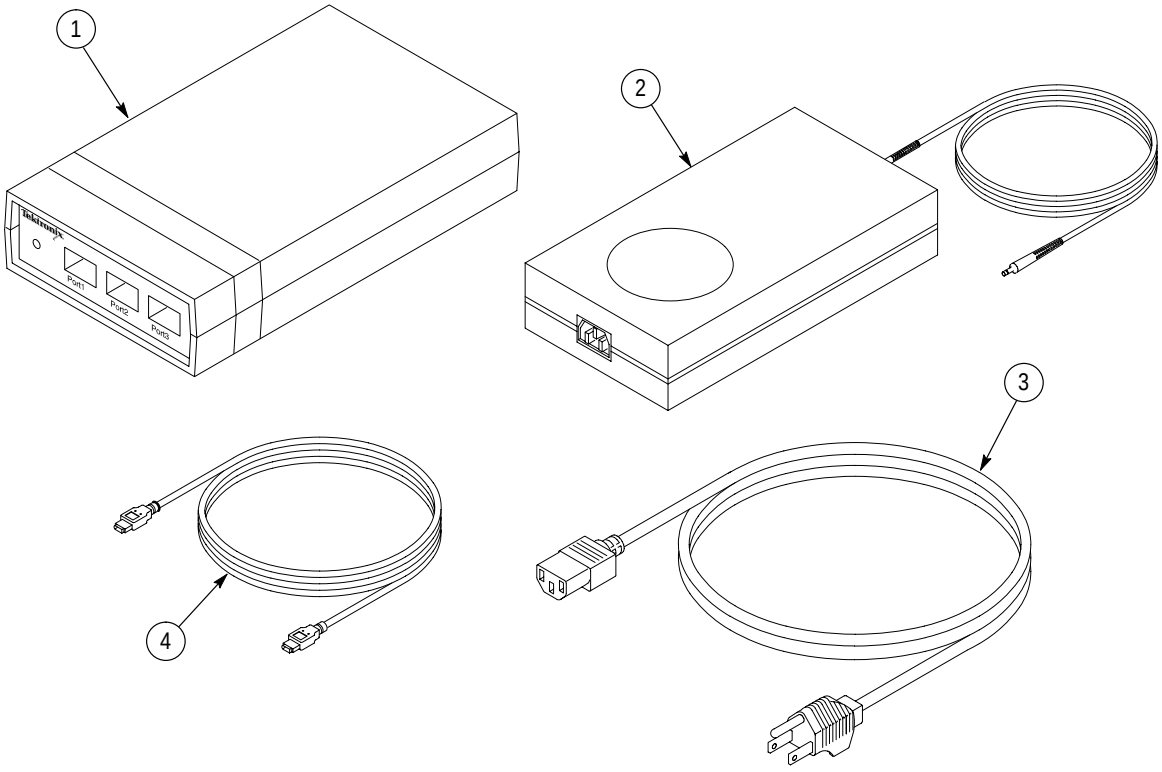

Figure 5–1: TMS 871 replaceable parts

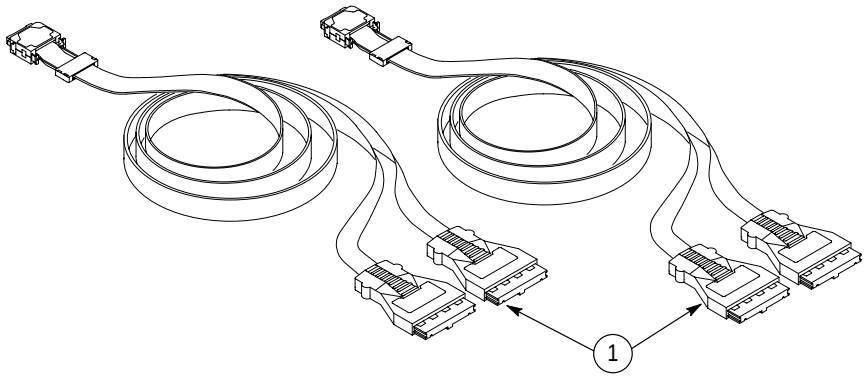

Figure 5–2: TMS 871 options/optional accessories