

Instruction Manual



TMS 545A PPC7400ITR Microprocessor Support 071-0797-00

Warning

The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:



WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*



CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Preface

This instruction manual contains specific information about the TMS 545A PPC7400ITR microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating TMS 545A PPC7400ITR microprocessor support package on the logic analyzer for which the TMS 545A PPC7400ITR support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations in your online help to set up and run the support.

Information on basic operations of PPC7400ITR microprocessor support package is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a user manual covering the basic operations of PPC7400ITR microprocessor support.
- In the information on basic operations, the term “XXX” or “P54C” appearing in field selections and file names must be replaced with PPC7400ITR. This term is the name of the PPC7400ITR microprocessor in field selections and file names you must use to operate the PPC7400ITR support.
- The term SUT (system under test) refers to the PPC7400ITR microprocessor-based system from which data will be acquired.

- The term “HI module” refers to the module in the higher-numbered slot and the term “LO module” refers to the module in the lower-numbered slot.
- PPC7400ITR refers to all supported variations of the PPC750 or PPC740 PPC7400 microprocessors unless otherwise noted.
- An underscore (_) following a signal name indicates an active low signal.

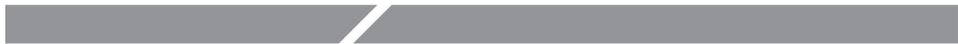
Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the user manual of the corresponding module. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Phone	1-800-833-9200*
Address	Tektronix, Inc. Department or name (if known) 14200 SW Karl Braun Drive P.O. Box 500 Beaverton, OR 97077 USA
Web site	www.tektronix.com
Sales support	1-800-833-9200, select option 1*
Service support	1-800-833-9200, select option 2*
Technical support	Email: support@tektronix.com 1-800-833-9200, select option 3* 1-503-627-2400 6:00 a.m. – 5:00 p.m. Pacific time

* This phone number is toll free in North America. After office hours, please leave a voice mail message.
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.



Getting Started

Getting Started

This chapter contains information on the TMS 545A PPC7400ITR microprocessor support and information on connecting your logic analyzer to your system under test.

Support Package Description

The TMS 545A PPC7400ITR microprocessor support package disassembled data from systems based on the PPC7400ITR microprocessor.

The TMS 545A Support is comprised of the following:

- TMS 545A PPC7400ITR Support SW Disk
- *TMS 545A PPC7400ITR microprocessor Support Instruction Manual*

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 545A PPC7400ITR microprocessor support.

To use this support efficiently, you need the items listed in the information on basic operations as well as:

- MPC 750 RISC Microprocessor User's Manual, 1997
- PowerPC Max Microprocessor Implementation Definition Book 1V Version 2.0, Motorola, 1998.

Options

The following options are available when ordering the TMS 545A Support:

- Option 21 (adds 4 P6434 Probes)

Logic Analyzer Software Compatibility

The label on the PPC7400ITR microprocessor support floppy disk states with which version of logic analyzer software the support is compatible.

Logic Analyzer Configuration

For use with a logic analyzer, the TMS 545A support requires a minimum of one 136-channel module.

Requirements and Restrictions

Review electrical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other PPC7400ITR support requirements and restrictions.

Hardware Reset. If a hardware reset occurs in your PPC7400ITR microprocessor system during an acquisition, the disassembler might acquire an invalid sample.

System Clock Rate. The PPC7400ITR microprocessor support can acquire data from the PPC7400ITR microprocessor operating at speeds of up to 133 MHz. The PPC7400ITR microprocessor support has been tested to 100 MHz.

Channel Groups. The channel groups required for clocking and disassembly are the Address Group, Hi_Data Group, Lo_Data Group, Control Group, Transfer Group, and Tsiz Group.

The channel group not required for clocking and disassembly is the Misc Group.

Disabling the Instruction Cache. To disassemble acquired data, you must disable the internal instruction cache. Disabling the cache makes all instruction prefetches visible on the bus so that they can be acquired and disassembled. To see acquired data with the cache enabled, see *Instruction Trace Reconstruction* on page 2–23.

Disabling the Data Cache. To display acquired data, you must disable the data cache. Disabling the data cache makes visible on the bus all of the loads and stores to memory, including data reads and writes, so that the software can acquire and display them.

Timing Display Format

A Timing Display Format file is provided. It sets up the display to show the following waveforms:

CLK, BR_, Address, TS_, ABB_, BG_, AACK_, ARTRY_, TBST_,
Hi_Data, Lo_Data, TA_, DBB_, DBG_, TEA_, DTI[1]/DRTRY_, Control,
Tsiz, Transfer.

NOTE. *Address, Hi_Data, Lo_Data, Control, Tsiz, and Transfer are displayed in bus form.*

The method of selecting or restoring the Timing Display Format file is different for each platform and will be ignored in this document.

Functionality Not Supported

Interrupt Signals. Not all of the interrupt signals are acquired by the TMS 545A support software. The interrupts that are acquired can be identified by the TMS 545A support software by looking at the address that is displayed for the interrupt service.

Microprocessor. The TMS 545A support acquires all the address and data cycles on the bus and does not differentiate between potential master and alternate master.

L2 cache. L2 cache transactions are not supported for the PPC7400ITR support.

Extra Acquisition Channels. Extra Acquisition Channels are not available on the logic analyzer.

Alternate Bus Master. Alternate bus master transactions are not processed in the disassembly.

Address Pipelining. If address pipelining continues for several sequences (those longer than approximately 1 K), performance might be degraded when you scroll data by entering a sequence number in the cursor field.

If address pipelining continues for additional sequences of 1 K or greater, erroneous address and data association might occur. You can use the Mark Cycles function to correct the interpretation of erroneous address and data association. See *Marking Cycles* on page 2–16 for information on how to correct improper address and data association.

Channel Assignments

Channel assignments shown in Table 1–1 through Table 1–8 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- An underscore (_) following a signal name indicates an active low signal.

Table 1–1 shows the probe section and channel assignments for the Tektronix logic analyzer (TLA) Address group and the PPC7400ITR microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 1–1: TLA Address group channel assignments

Bit order	Section:channel	PPC7400ITR signal name
31	A3:7	A0
30	A3:6	A1
29	A3:5	A2
28	A3:4	A3
27	A3:3	A4
26	A3:2	A5
25	A3:1	A6
24	A3:0	A7
23	A2:7	A8
22	A2:6	A9
21	A2:5	A10
20	A2:4	A11
19	A2:3	A12
18	A2:2	A13
17	A2:1	A14
16	A2:0	A15
15	A1:7	A16
14	A1:6	A17
13	A1:5	A18
12	A1:4	A19
11	A1:3	A20

Table 1-1: TLA Address group channel assignments (cont.)

Bit order	Section:channel	PPC7400ITR signal name
10	A1:2	A21
9	A1:1	A22
8	A1:0	A23
7	A0:7	A24
6	A0:6	A25
5	A0:5	A26
4	A0:4	A27
3	A0:3	A28
2	A0:2	A29
1	A0:1	A30
0	A0:0	A31

Table 1-2 shows the probe section and channel assignments for the TLA Hi_Data group and the PPC7400ITR microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 1-2: TLA Hi_Data group channel assignments

Bit order	Section:channel	PPC7400ITR signal name
31	E3:7	D0
30	E3:6	D1
29	E3:5	D2
28	E3:4	D3
27	E3:3	D4
26	E3:2	D5
25	E3:1	D6
24	E3:0	D7
23	E2:7	D8
22	E2:6	D9
21	E2:5	D10
20	E2:4	D11
19	E2:3	D12
18	E2:2	D13
17	E2:1	D14
16	E2:0	D15
15	E1:7	D16
14	E1:6	D17

Table 1–2: TLA Hi_Data group channel assignments (cont.)

Bit order	Section:channel	PPC7400ITR signal name
13	E1:5	D18
12	E1:4	D19
11	E1:3	D20
10	E1:2	D21
9	E1:1	D22
8	E1:0	D23
7	E0:7	D24
6	E0:6	D25
5	E0:5	D26
4	E0:4	D27
3	E0:3	D28
2	E0:2	D29
1	E0:1	D30
0	E0:0	D31

Table 1–3 shows the probe section and channel assignments for the TLA Lo_Data group and the PPC7400ITR microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 1–3: TLA Lo_Data group channel assignments

Bit order	Section:channel	PPC7400ITR signal name
31	D3:7	D32
30	D3:6	D33
29	D3:5	D34
28	D3:4	D35
27	D3:3	D36
26	D3:2	D37
25	D3:1	D38
24	D3:0	D39
23	D2:7	D40
22	D2:6	D41
21	D2:5	D42
20	D2:4	D43
19	D2:3	D44
18	D2:2	D45
17	D2:1	D46

Table 1-3: TLA Lo_Data group channel assignments (cont.)

Bit order	Section:channel	PPC7400ITR signal name
16	D2:0	D47
15	D1:7	D48
14	D1:6	D49
13	D1:5	D50
12	D1:4	D51
11	D1:3	D52
10	D1:2	D53
9	D1:1	D54
8	D1:0	D55
7	D0:7	D56
6	D0:6	D57
5	D0:5	D58
4	D0:4	D59
3	D0:3	D60
2	D0:2	D61
1	D0:1	D62
0	D0:0	D63

Table 1-4 shows the probe section and channel assignments for the TLA Control group and the PPC7400ITR microprocessor signal to which each channel connects. By default, this channel group is displayed as symbols.

Table 1-4: TLA Control group channel assignments

Bit order	Section:channel	PPC7400ITR signal name
10	C2:2	TS_
9	C3:4	BG_
8	C1:4	DBG_
7	C2:0	ARTRY_
5	C2:1	AACK_
4	Clock:1	TA_
3	Clock:0	TEA_
2	C2:4	ABB_
1	C0:4	DTI[O]
0	Clock:2	DBB_

Table 1–5 shows the probe section and channel assignments for the TLA Transfer group and the PPC7400ITR microprocessor signal to which each channel connects. By default, this channel group is displayed as symbols.

Table 1–5: TLA Transfer group channel assignments

Bit order	Section:channel	PPC7400ITR signal name
5	C3:1	TT0
4	C0:7	TT1
3	C3:6	TT2
2	C3:7	TT3
1	C1:2	TT4
0	C1:7	WT_

Table 1–6 shows the probe section and channel assignments for the TLA Tsiz group and the PPC7400ITR microprocessor signal to which each channel connects. By default, this channel group is displayed in symbols.

Table 1–6: TLA Tsiz group channel assignments

Bit order	Section:channel	PPC7400ITR signal name
3	C3:3	TSIZ2
2	C2:7	TSIZ1
1	C2:6	TSIZ0
0	C3:2	TBST_

Table 1–7 shows the probe section and channel assignments for the TLA Misc group and the PPC7400ITR microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 1–7: TLA Misc group channel assignments

Bit order	Section:channel	PPC7400ITR signal name
2	Clock:3	CLK
1	C1:5	BR_
0	C0:5	GBL_

Logic Analyzer. Extra channels that are not connected in the PPC7400ITR support:

C1:3
C1:5
C0:5

NonIntrusive Acquisition. Acquiring microprocessor bus cycles will be nonintrusive to the system under test. That is, the PPC7400ITR support will not intercept, modify, or present back signals to the system under test.

Acquisition Setup. The PPC7400ITR support will affect the logic analyzer setup menus (and submenus) by modifying existing fields and adding micro-specific fields.

On the logic analyzer, the PPC7400ITR support will add the selection “PPC7400ITR” to the Load Support Package dialog box, under the File pulldown menu. Once that “PPC7400ITR support” has been loaded, the “Custom” clocking mode selection in the logic analyzer module Setup menu is also enabled.

Table 1–8 shows the probe section and channel assignments for the clock probes (not part of any group), and the PPC7400ITR signal to which each channel connects.

Table 1–8: Clock channel assignments

TLA section & probe	PPC7400ITR signal name	Description
CLK:3	CLK	Clock
CLK:2	DBB_	Used as qualifier
CLK:1	TA_	Used as qualifier
CLK:0	TEA_	Used as qualifier
C2:0	ARTRY_	Used as qualifier
C2:1	AACK_	Used as qualifier
C2:2	TS_	Used as qualifier
C2:3	DTI[1]/DRTRY_*	Used as qualifier

* This signal occurs as DTI[1] in 7400 and as DRTRY_ in 750

CPU To Mictor Connections

To probe the microprocessor you will need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the P6434 Mass Termination Probe manual, Tektronix part number 070-9793-xx, for more information on mechanical specifications. Table 1–9 through Table 1–11 show the CPU pin to Mictor pin connections.

Tektronix uses a counter clockwise pin assignment. Pin 1 is located at the top left, and pin 2 is located directly below it. Pin 20 is located on the bottom right, and pin 21 is located directly above it.

AMP uses an odd side-even side pin assignment. Pin 1 is located at the top left, and pin-3 is located directly below it. Pin 2 is located on the top right, and pin 4 is located directly below it.

NOTE. When designing Mictor connectors into your SUT, always follow the Tektronix pin assignment.

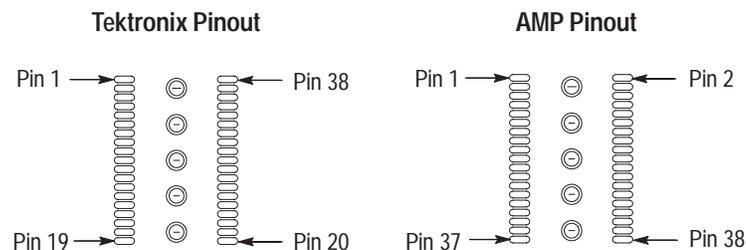


Figure 1-1: Pin assignments for a Mictor connector (component side)

Please pay close attention to the caution below.



CAUTION. To protect the CPU and the inputs of the module, it is recommended that a 180 Ω resistor is connected in series between each ball pad of the CPU and each pin of the Mictor connector. The resistor must be no farther away from the ball pad of the CPU than 1/2-inch.

Table 1-9: TLA CPU to Mictor connections for Mictor A pins

Tektronix Mictor A pin number	AMP Mictor A pin number	PPC7400ITR signal name	PPC 7400/750 socket	PPC 740 socket
1	1	NC	NC	NC
2	3	NC	NC	NC
3	5	TEA_	J1	H13
4	7	A0	A13	C16
5	9	A1	D2	E4
6	11	A2	H11	D13
7	13	A3	C1	F2
8	15	A4	B13	D14
9	17	A5	F2	G1
10	19	A6	C13	D15
11	21	A7	E5	E2
12	23	A8	D13	D16
13	25	A9	G7	D4
14	27	A10	F12	E13
15	29	A11	G3	G2
16	31	A12	G6	E15
17	33	A13	H2	H1
18	35	A14	E2	E16
19	37	A15	L3	H2
20	38	A31	L2	P1
21	36	A30	K2	J15
22	34	A29	K3	M1
23	32	A28	J6	H16
24	30	A27	J2	K2
25	28	A26	H3	G15
26	26	A25	M3	K1
27	24	A24	J7	G13
28	22	A23	F3	F4
29	20	A22	G2	F16
30	18	A21	E1	H3
31	16	A20	H7	F15
32	14	A19	J4	J2
33	12	A18	G4	F14
34	10	A17	L4	J1
35	8	A16	G5	F13

Table 1-9: TLA CPU to Mictor connections for Mictor A pins (cont.)

Tektronix Mictor A pin number	AMP Mictor A pin number	PPC7400ITR signal name	PPC 7400/750 socket	PPC 740 socket
36	6	TA_	F1	H14
37	4	NC	NC	NC
38	2	NC	NC	NC
39	39	GND	NC	NC
40	40	GND	NC	NC
41	41	GND	NC	NC
42	42	GND	NC	NC
43	43	GND	NC	NC

Table 1-10: TLA CPU to Mictor connections for Mictor C pins

Tektronix Mictor C pin number	AMP Mictor C pin number	PPC7400ITR signal name	PPC 7400/750	PPC 740
1	1	NC	NC	NC
2	3	NC	NC	NC
3	5	CLK	H9	C9
4	7	TT3	C12	C14
5	9	TT2	B12	B16
6	11	TEA_	J1	H13
7	13	BG_	H1	L1
8	15	TSIZ2	C9	B12
9	17	TBST_	A11	A14
10	19	TT0	C10	B13
11	21	NC	NC	NC
12	23	TSIZ1	B9	D10
13	25	TSIZ0	A9	A13
14	27	DBB_	K5	J14
15	29	ABB_	L7	K4
16	31	DTI[1]/DRTRY_*	H6	G16
17	33	TS_	K7	J13
18	35	AACK_	N3	L2
19	37	ARTRY_	L6	J4
20	38	ARTRY_DATA_	L6	J4

Table 1–10: TLA CPU to Mictor connections for Mictor C pins (cont.)

Tektronix Mictor C pin number	AMP Mictor C pin number	PPC7400ITR signal name	PPC 7400/750	PPC 740
21	36	AACK_	N3	L2
22	34	TS_	K7	J13
23	32	DTI[1]/DRTRY_*	H6	G16
24	30	DTI[0]	D1	G4
25	28	GBL_	B1	F1
26	26	TA_	F1	H14
27	24	TT1	D11	A15
28	22	NC	NC	NC
29	20	HRESET_	B6	A7
30	18	TT4	F11	C15
31	16	SYSCLK	H9	C9
32	14	DBG_	K1	N1
33	12	BR_	E7	B6
34	10	ARTRY_	L6	J4
35	8	WT	C3	D2
36	6	NC	NC	NC
37	4	NC	NC	NC
38	2	NC	NC	NC
39	39	GND	NC	NC
40	40	GND	NC	NC
41	41	GND	NC	NC
42	42	GND	NC	NC
43	43	GND	NC	NC

* This signal occurs as DTI[1] in 7400 and as DRTRY_ in 750

Table 1–11: CPU to Mictor connections for Mictor D pins

Tektronix Mictor D pin number	AMP Mictor D pin number	PPC7400ITR signal name	PPC 7400/750	PPC 740
1	1	NC	NC	NC
2	3	NC	NC	NC
3	5	NC	NC	NC

Table 1-11: CPU to Mictor connections for Mictor D pins (cont.)

Tektronix Mictor D pin number	AMP Mictor D pin number	PPC7400ITR signal name	PPC 7400/750	PPC 740
4	7	DL0	M6	K13
5	9	DL1	P3	K15
6	11	DL2	N4	K16
7	13	DL3	N5	L16
8	15	DL4	R3	L15
9	17	DL5	M7	L13
10	19	DL6	T2	L14
11	21	DL7	N6	M16
12	23	DL8	U2	M15
13	25	DL9	N7	M13
14	27	DL10	P11	N16
15	29	DL11	V13	N15
16	31	DL12	U12	N13
17	33	DL13	P12	N14
18	35	DL14	T13	P16
19	37	DL15	W13	P15
20	38	DL31	W2	R4
21	36	DL30	U3	T3
22	34	DL29	V3	P4
23	32	DL28	R2	T2
24	30	DL27	N1	T1
25	28	DL26	U1	R3
26	26	DL25	V1	N4
27	24	DL24	P1	N3
28	22	DL23	T1	P3
29	20	DL22	V8	T13
30	18	DL21	V12	N12
31	16	DL20	U11	P13
32	14	DL19	T11	N10
33	12	DL18	W8	T14
34	10	DL17	V10	R14
35	8	DL16	U13	R16
36	6	DL15	K5	J14
37	4	DL14	NC	NC
38	2	DL13	NC	NC

Table 1–11: CPU to Mictor connections for Mictor D pins (cont.)

Tektronix Mictor D pin number	AMP Mictor D pin number	PPC7400ITR signal name	PPC 7400/750	PPC 740
39	39	GND	NC	NC
40	40	GND	NC	NC
41	41	GND	NC	NC
42	42	GND	NC	NC
43	43	GND	NC	NC

Table 1–12: TLA CPU to Mictor connections for Mictor E pins

Tektronix Mictor E pin number	AMP Mictor E pin number	PPC7400ITR signal name	PPC 7400/750	PPC 740
1	1	NC	NA	NA
2	3	NC	NA	NA
3	5	NC	NC	NC
4	7	DH0	W12	P14
5	9	DH1	W11	Y16
6	11	DH2	V11	R15
7	13	DH3	T9	T15
8	15	DH4	W10	R13
9	17	DH5	U9	R12
10	19	DH6	U10	P11
11	21	DH7	M11	N11
12	23	DH8	M9	R11
13	25	DH9	P8	T12
14	27	DH10	W7	T11
15	29	DH11	P9	R10
16	31	DH12	W9	P9
17	33	DH13	R10	N9
18	35	DH14	W6	T10
19	37	DH15	V7	V7
20	38	DH31	R5	T4
21	36	DH30	U4	T5
22	34	DH29	W3	N5

Table 1-12: TLA CPU to Mictor connections for Mictor E pins (cont.)

Tektronix Mictor E pin number	AMP Mictor E pin number	PPC7400ITR signal name	PPC 7400/750	PPC 740
23	32	DH28	V4	R5
24	30	DH27	V5	T6
25	28	DH26	P7	R6
26	26	DH25	W4	N6
27	24	DH24	U5	P6
28	22	DH23	W5	T7
29	20	DH22	U6	R7
30	18	DH21	R7	N7
31	16	DH20	U7	T8
32	14	DH19	T7	R8
33	12	DH18	V9	N8
34	10	DH17	U8	P8
35	8	DH16	V6	T9
36	6	NC	NC	NC
37	4	NC	NC	NC
38	2	NC	NC	NC
39	39	GND	NC	NC
40	40	GND	NC	NC
41	41	GND	NC	NC
42	42	GND	NC	NC
43	43	GND	NC	NC

Channel Charts

Tables 1–13 through 1–19 identify the signal names assigned to the acquisition channel numbers on the logic analyzer.

Table 1–13: Clock channels

TLA clock channel	CLK or Qual	Active CLK edge	Login strobe	PPC7400ITR signal name
CLK:3	CLK	Rising	M	CLK
CLK:2			M	DBB_
CLK:1	Qual		M	TA_
CLK:0	Qual		M	TEA_

Table 1–14 identifies the QUAL channel numbers on the logic analyzer.

Table 1–14: Qualifier channels

TLA qualifier channel	Qual only	Login strobe	PPC7400ITR signal name
QUAL:3		M	
QUAL:2		M	
QUAL:1		M	
QUAL:0		M	

Table 1-15: Address channels

TLA acquisition channel	Login group	Login strobe	PPC7400ITR signal name
A3:7	LOGA7	M	A0
A3:6	LOGA7	M	A1
A3:5	LOGA7	M	A2
A3:4	LOGA7	M	A3
A3:3	LOGA6	M	A4
A3:2	LOGA6	M	A5
A3:1	LOGA6	M	A6
A3:0	LOGA6	M	A7
A2:7	LOGA5	M	A8
A2:6	LOGA5	M	A9
A2:5	LOGA5	M	A10
A2:4	LOGA5	M	A11
A2:3	LOGA4	M	A12
A2:2	LOGA4	M	A13
A2:1	LOGA4	M	A14
A2:0	LOGA4	M	A15
A1:7	LOGA3	M	A16
A1:6	LOGA3	M	A17
A1:5	LOGA3	M	A18
A1:4	LOGA3	M	A19
A1:3	LOGA2	M	A20
A1:2	LOGA2	M	A21
A1:1	LOGA2	M	A22
A1:0	LOGA2	M	A23
A0:7	LOGA1	M	A24
A0:6	LOGA1	M	A25
A0:5	LOGA1	M	A26
A0:4	LOGA1	M	A27
A0:3	LOGA0	M	A28
A0:2	LOGA0	M	A29
A0:1	LOGA0	M	A30
A0:0	LOGA0	M	A31

Table 1–16: Data channels

TLA acquisition channel	Login group	Login strobe	PPC7400ITR signal name
D3:7	LOGD7	M	D32
D3:6	LOGD7	M	D33
D3:5	LOGD7	M	D34
D3:4	LOGD7	M	D35
D3:3	LOGD6	M	D36
D3:2	LOGD6	M	D37
D3:1	LOGD6	M	D38
D3:0	LOGD6	M	D39
D2:7	LOGD5	M	D40
D2:6	LOGD5	M	D41
D2:5	LOGD5	M	D42
D2:4	LOGD5	M	D43
D2:3	LOGD4	M	D44
D2:2	LOGD4	M	D45
D2:1	LOGD4	M	D46
D2:0	LOGD4	M	D47
D1:7	LOGD3	M	D48
D1:6	LOGD3	M	D49
D1:5	LOGD3	M	D50
D1:4	LOGD3	M	D51
D1:3	LOGD2	M	D52
D1:2	LOGD2	M	D53
D1:1	LOGD2	M	D54
D1:0	LOGD2	M	D55
D0:7	LOGD1	M	D56
D0:6	LOGD1	M	D57
D0:5	LOGD1	M	D58
D0:4	LOGD1	M	D59
D0:3	LOGD0	M	D60
D0:2	LOGD0	M	D61
D0:1	LOGD0	M	D62
D0:0	LOGD0	M	D63

Table 1-17: Control channels

TLA acquisition channel	Login group	Login strobe	PPC7400ITR signal name
C3:7	LOGC7	M	TT3
C3:6	LOGC6	M	TT2
C3:5	LOGC5	M	
C3:4	LOGC4	M	BG_
C3:3	LOGC7	M	TSIZ2
C3:2	LOGC6	M	TBST_
C3:1	LOGC5	M	TT0
C3:0	LOGC4	M	
C2:7	LOGC7	M	TSIZ1
C2:6	LOGC6	M	TSIZ0
C2:5	LOGC5	M	
C2:4	LOGC4	M	ABB_
C2:3	LOGC7	M	DTI[1]/DRTRY_*
C2:2	LOGC6	M	TS_
C2:1	LOGC5	M	AACK_
C2:0	LOGC4	M	ARTRY_
C1:7	LOGC3	M	WT_
C1:6	LOGC2	M	ARTRY_1
C1:5	LOGC1	M	BR_
C1:4	LOGC0	M	DBG_
C1:3	LOGC3	M	SYSCLK
C1:2	LOGC2	M	TT4
C1:1	LOGC1	M	HRESET_
C1:0	LOGC0	M	
C0:7	LOGC3	M	TT1
C0:6	LOGC2	M	
C0:5	LOGC1	M	GBL_
C0:4	LOGC0	M	DTI[0]
C0:3	LOGC3	M	
C0:2	LOGC2	M	
C0:1	LOGC1	M	
C0:0	LOGC0	M	ARTRY_DATA_

* This signal occurs as DTI[1] in 7400 and as DRTRY_ in 750

Table 1–18: Control channels

TLA acquisition channel	Login group	Login strobe	PPC7400ITR signal name
C3:7	LOGC7	M	TT3
C3:3	LOGC7	M	TSIZ2
C2:7	LOGC7	M	TSIZ1
C2:3	LOGC7	M	DTI[1]/DRTRY_*
C3:6	LOGC6	M	TT2
C3:2	LOGC6	M	TBST_
C2:6	LOGC6	M	TSIZ0
C2:2	LOGC6	M	TS_
C3:5	LOGC5	M	
C3:1	LOGC5	M	TT0
C2:5	LOGC5	M	
C2:1	LOGC5	M	AACK_
C3:4	LOGC4	M	BG_
C3:0	LOGC4	M	
C2:4	LOGC4	M	ABB_
C2:0	LOGC4	M	ARTRY_
C1:7	LOGC3	M	WT_
C1:3	LOGC3	M	SYSCLK
C0:7	LOGC3	M	TT1
C0:3	LOGC3	M	
C1:6	LOGC2	M	ARTRY_
C1:2	LOGC2	M	TT4
C0:6	LOGC2	M	
C0:2	LOGC2	M	
C1:5	LOGC1	M	BR_
C1:1	LOGC1	M	HRESET_
C0:5	LOGC1	M	GBL_
C0:1	LOGC1	M	
C1:4	LOGC0	M	DBG_
C1:0	LOGC0	M	
C0:4	LOGC0	M	DTI[0]
C0:0	LOGC0	M	ARTRY_DATA_

* This signal occurs as DTI[1] in 7400 and as DRTRY_ in 750

Table 1–19: Extended channels

TLA acquisition channel	Login group	Login strobe	PPC7400ITR signal name
E3:7	LOGE7	M	D0
E3:6	LOGE7	M	D1
E3:5	LOGE7	M	D2
E3:4	LOGE7	M	D3
E3:3	LOGE6	M	D4
E3:2	LOGE6	M	D5
E3:1	LOGE6	M	D6
E3:0	LOGE6	M	D7
E2:7	LOGE5	M	D8
E2:6	LOGE5	M	D9
E2:5	LOGE5	M	D10
E2:4	LOGE5	M	D11
E2:3	LOGE4	M	D12
E2:2	LOGE4	M	D13
E2:1	LOGE4	M	D14
E2:0	LOGE4	M	D15
E1:7	LOGE3	M	D16
E1:6	LOGE3	M	D17
E1:5	LOGE3	M	D18
E1:4	LOGE3	M	D19
E1:3	LOGE2	M	D20
E1:2	LOGE2	M	D21
E1:1	LOGE2	M	D22
E1:0	LOGE2	M	D23
E0:7	LOGE1	M	D24
E0:6	LOGE1	M	D25
E0:5	LOGE1	M	D26
E0:4	LOGE1	M	D27
E0:3	LOGE0	M	D28
E0:2	LOGE0	M	D29
E0:1	LOGE0	M	D30
E0:0	LOGE0	M	D31



Operating Basics

Setting Up the Support

This section provides information on how to set up the support. The information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

The information in this section is specific to the operations and functions of the TMS 545A PPC7400ITR microprocessor support on any Tektronix logic analyzer for which the support can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify the setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the PPC7400ITR support are Address, Hi_Data, Lo_Data, Control, Transfer (Tran), Tsiz, and Misc. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 1–4.

Clocking

Clocking Options

The PPC7400ITR support offers a PPC7400ITR microprocessor-specific clocking mode for the PPC7400ITR microprocessor. This clocking mode is the default selection whenever you load the PPC7400ITR support.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

Custom Clocking

A special clocking program is loaded to the module every time you load the PPC7400ITR support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple channel groups at different times when the signals are valid on the PPC7400ITR bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each PPC7400ITR microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

When Custom is selected, the Custom Clocking Options menu will have the subtitle “PPC7400ITR microprocessor Clocking Support” added, and the clocking options will also be displayed.

The following clocking options are provided:

Select Processor. This clocking option allows the user to select the processor for which disassembly is required. The processors provided in the options are:

- PPC7400ITR microprocessor: This is the default option. This option can be selected when the processor for which support is required is PPC7400ITR.
- PPC 740/750 microprocessor: This option enables the user to acquire and use the disassembly support for PPC 750/740 processors.

Pipeline Depth. This clocking option is provided so as to enable the user to select the depth of address pipelining carried out by the microprocessor.

Two options are provided:

- One: This option can be selected when Address pipelining is occurring on the bus. This is the default option.
- Zero: This can be selected by the user when there is no address pipelining is carried out by the microprocessor.

NOTE. *Pipeline Zero Option should be selected only when the Address and Data cycle of a transaction are completed before the next Address-Data Transaction. This holds true when the number of processors being used in a multiprocessor environment is more than 1.*

For Multiprocessor environments it is always preferable to use the Pipeline One Option.

Bus timing diagram. All the data signals D[0–63] are logged in during “D” strobe and DBG_ and DBWO_ are logged in during “DBB” strobe. All the address signals A[0–31] and the remaining signals are strobed in during “A” strobe. See Figure 2–1.

NOTE. *BG_ logged in by the “A” strobe is the state during the previous cycle.*

An “M” strobe is done if one or more of the following conditions are met:

TA_ is asserted

TS_ is asserted

ARTRY_ is asserted on the second clock after the assertion of AACK_

DRTRY_ is asserted (if the processor selected is PPC 740/750) OR

TEA_ is asserted

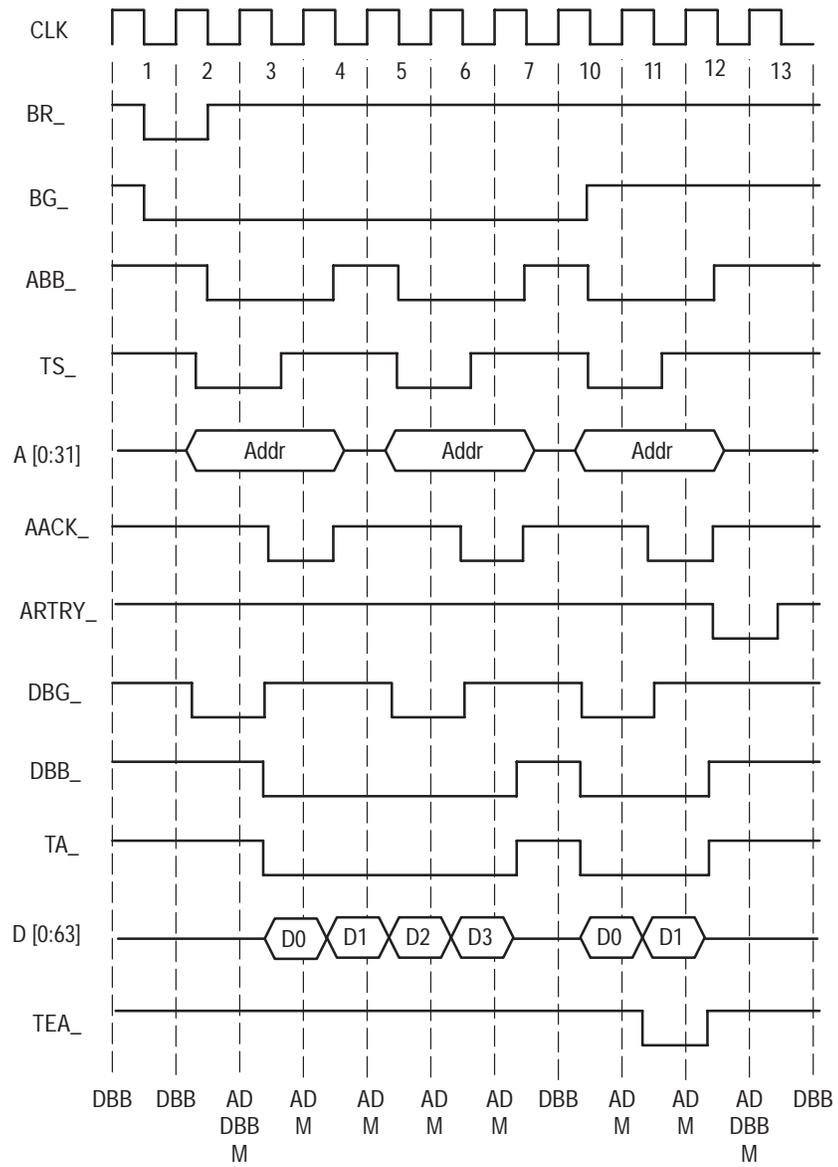


Figure 2-1: PPC 7400/PPC 740/750 support bus timing diagram

Symbols

The TMS 545A support supplies three symbol-table files: PPC7400ITR_Transfer, PPC7400ITR_Tsiz, and PPC7400ITR_Ctrl. The PPC7400ITR_Ctrl file replaces specific Control-channel group values with symbolic values when Symbolic is the radix for the channel group.

Symbol tables are generally not for use in timing or PPC7400ITR_T support disassembly.

Table 2–1 shows the definitions for name, bit pattern, and meaning of the Transfer group symbols in file PPC7400ITR_Transfer.

Table 2–1: PPC7400ITR_Transfer group symbol table definitions

Symbol	Control group value				Description
	TT0 TT1	TT2 TT3	TT4 WT		
FETCH	0 1	0 1 0 1			Instruction fetch cycle
DATA_READ	X 1	X 1 X 1			Read cycle
DATA_WRT	X 0	X 1 X X			Write cycle
ADDR_ONLY	X X	X 0 X X			Address only cycle
UNKNOWN	X X	X X X X			Unknown transfer cycle

Table 2–2 shows the definitions for name, bit pattern, and meaning of the Tsiz group symbols in file PPC7400ITR_Tsiz.

Table 2–2: PPC7400ITR_Tsiz group symbol table definitions

Symbol	Control group value				Description
	TSIZ0 TSIZ1 TSIZ2 TBST_				
BURST	0 1 0 0				Burst transaction
8_BYTE	0 0 0 1				Single beat 8-Byte transaction
1_BYTE	0 0 1 1				Single beat 1-Byte transaction
2_BYTE	0 1 0 1				Single beat 2-Byte transaction
3_BYTE	0 1 1 1				Single beat 3-Byte transaction
4_BYTE	1 0 0 1				Single beat 4-Byte transaction
5_BYTE	1 0 1 1				Single beat 5-Byte transaction
6_BYTE	1 1 0 1				Single beat 6-Byte transaction

Table 2–2: PPC7400ITR_Tsiz group symbol table definitions (cont.)

Symbol	Control group value				Description
	TSIZ0	TSIZ1	TSIZ2	TBST_	
7_BYTE	1	1	1	1	Single beat 7-Byte transaction
UNKNOWN	X	X	X	X	Unknown tsiz cycle

Table 2–3 shows the definitions for name, bit pattern, and meaning of the Control group symbols in file PPC7400ITR_Ctrl.

Table 2–3: PPC7400ITR_Ctrl Control group symbol table definitions

Symbol	Control group value						Description					
	TS_	BG_	DBG_	ARTRY_	DTI[1]/DRTRY_* AACK_	TA_		TEA_	ABB_	DBWO_	DBB_	
ARTRY_POE	X	X	0	0	X	X	X	0	X	X	X	ARTRY Cycle and Data Error
ARTRY_P1E	X	X	X	0	X	X	X	0	X	X	X	ARTRY Cycle and Alternate Master Data Error
ARTRY_DRTRY	X	X	X	0	0	X	X	X	X	X	X	ARTRY Cycle
ARTRY_P0D	X	X	0	0	X	X	0	X	X	X	X	ARTRY Cycle and Data
ARTRY_P1D	X	X	X	0	X	X	0	X	X	X	X	ARTRY Cycle and Alternate Master Data
P0A_POE	0	0	0	1	X	X	X	0	X	X	X	PPC0 Address and PPC0's Data Error
P0A_P1E	0	0	X	1	X	X	X	0	X	X	X	PPC0 Address and PPC1's Data Error
P1A_POE	0	X	0	1	X	X	X	0	X	X	X	PPC1 Address and PPC0's Data Error
P1A_P1E	0	X	X	1	X	X	X	0	X	X	X	PPC1 Address and PPC1's Data Error
P0A_P0D	0	0	0	1	X	X	0	X	X	X	X	Address and Data
P0A_P1D	0	0	X	1	X	X	0	X	X	X	X	Current Master Address and Alternate Master Data
P1A_P0D	0	X	0	1	X	X	0	X	X	X	X	Alternate Master Address and Current Master Data
P1A_P1D	0	X	X	1	X	X	0	X	X	X	X	Alternate Master Address and Data
P0_A	0	0	X	1	X	X	X	X	X	X	X	Address Cycle
P1_A	0	X	X	1	X	X	X	X	X	X	X	Alternate Master Address Cycle
P0_E	X	X	0	X	X	X	X	0	X	X	X	Data Error
P1_E	X	X	X	X	X	X	X	0	X	X	X	Alternate Master Data Error
P0_D	X	X	0	X	X	X	0	X	X	X	X	Data Cycle
P1_D	X	X	X	X	X	X	0	X	X	X	X	Alternate Master Data Cycle
ARTRY	X	X	X	0	X	X	X	X	X	X	X	ARTRY Cycle
P0A_DRTRY	X	X	0	X	0	X	X	X	X	X	X	DRTRY Cycle

Table 2-3: PPC7400ITR_Ctrl Control group symbol table definitions (cont.)

Symbol	Control group value									Description		
	TS_	BG_	DBG_	ARTRY_	DTI[1]/DRTRY_*	AACK_	TA_	TEA_	ABB_		DBWO_	DBB_
P1A_DRTRY	X	X	X	X	0	X	X	X	X	X	X	Alternate Master DRTRY Cycle
UNKNOWN	X	X	X	X	X	X	X	X	X	X	X	Unknown Cycle

* This signal occurs as DTI[1] in 7400 and as DRTRY_ in 750

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as for the Address channel group.

Range Symbols

The TMS 545A design supports range symbols in a manner similar to pattern symbols. Both types of symbols are accessed in the same manner (by the user).

Range symbols associate a range of data values with a symbol “name”. When a range symbol table is selected for the radix of the Address group, all address values (both in the Address column and in the disassembly Mnemonics column) will be replaced with their corresponding symbol name plus an offset, if the value falls within one of the defined ranges. If no symbol is defined, the address value will be displayed in HEX or OCT, depending upon the output radix selection for that symbol table. If the output radix selection is anything but HEX or OCT, addresses will be displayed in HEX. The offset (the difference between the value and the lower bound of the range) will also be displayed in that radix (HEX or OCT).

NOTE. The various ranges must not overlap.

For example, given the following disassembled code fragment:

Address	Mnemonic
.	.
00009700	ba 0000A00F
.	.
.	.
0000A00F	.

and given the Address group range symbol:

```
mysub      0000A000    0000AFFF
```

then displaying disassembly in Hardware mode and selecting symbolic radix for the Address group will cause the following disassembled code fragment to be displayed:

Address	Mnemonic
.	.
00009700	ba mysub+f
.	.
.	.
mysub+f	.

If the output radix of the symbol table is changed to OCTAL then the code fragment will look like:

Address	Mnemonic
.	.
00000113400	ba mysub+17
.	.
.	.
mysub+17	.

Users can also load their own user-defined range symbols if the file follows the conventions of the logic analyzer symbol table file format.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- Changing the way data is displayed
- Changing disassembled cycles with the mark cycles function

Acquiring Data

Once you load the PPC7400ITR support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to Changing How Data is Displayed on page 2–14.*

The default display format shows the Address, HI_Data, LO_Data, Control, Transfer and Tsiz channel group values for each sample of acquired data.

If a channel group is not visible, you must use the Disassembly property page to make the group visible.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–4 shows these special characters and strings, and gives a definition of what they represent.

Table 2-4: Description of special characters in the display

Character or string displayed	Description
>> On the TLA.	The instruction was manually marked
#	Indicates an immediate value
-----	In the Address channel group, this indicates that the sequence did not have information that could be disassembled
-----	In the HI_Data and LO_Data groups, this indicates that the sequence does not contain valid data
-----	In the LO_Data group, this indicates that the bus configuration is 32-Bits
--	In the invalidate byte lanes, this indicates a Data Read or Data Write transaction
-----	Indicates a flushed instruction when only one of the instructions fetched is executed
<Hex value>	In whole bytes that are not valid, this indicates invalidated data; the value for invalidated data is hexadecimal

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses.

If a single sequence has both an Address/Direct Store Access cycle and a Data cycle, then a combination of cycle type labels described in Tables 2-5, 2-6, and 2-7 is displayed. For example, if Alternate Master Address and Alternate Master Data are acquired in one sample, the disassembler would display the cycle type label (ALT ADDR AND ALT DATA).

Table 2-5: Cycle type labels for Address sequences and definitions

Cycle type label	Definition
(7400 ADDRESS)	Address cycle with selected processor mastership
(7400 ARTRY ADDRESS)	Selected processor Address retried
(740/750 ADDRESS)	Address cycle for the selected 740/750 processor mastership
(740/750 ARTRY ADDRESS)	Selected 740/750 processor Address retried
(7400 ADDRESS) & (ALTERNATE MASTER)	Address cycle when the processor selected is PPC 7400 and the option selected under "Processors Used" is <i>less than 3</i> . This is relevant when simultaneous disassembly is done for a max of 2 processors.
(740/750 ADDRESS) & (ALTERNATE MASTER)	Address cycle when the processor selected is PPC 740/750 and the option selected under "Processors Used" is <i>less than 3</i> . This is relevant when simultaneous disassembly is done for a max of 2 processors.

Table 2-5: Cycle type labels for Address sequences and definitions (cont.)

Cycle type label	Definition
(ALTERNATE MASTER ADDRESS)	Alternate master address. This is relevant when the option selected under "Processors used" is <i>greater than 2</i> . This implies that simultaneous disassembly would not be done when the number of processors in a multiprocessing environment is <i>more than 2</i> .
(INVALID ADDRESS)	Invalid selected processor Address which cannot associate with any data

Table 2-6: Cycle type labels for Data sequences and definitions

Cycle type label	Definition
(7400 DATA)	Data cycle with selected processor mastership
(740/750 DATA)	Data cycle with selected processor mastership
(ALTERNATE MASTER DATA)	Alternate Master Data. This is applicable when the option selected under "Processors Used" is <i>greater than 2</i> .
(INVALID DATA)	Invalid selected processor Data does not associate with address.

Table 2-7: Cycle type labels for ARTRY, DRTRY, and Data Error cycles

Cycle type label	Definition
(7400 DATA ERROR)	Data error in selected processor data – Assertion of TEA. This is applicable only in the case where the option selected under "Processors Used" is <i>less than 3</i> and the processor being used is PPC7400.
(740/750 DATA ERROR)	Data error in selected processor data – Assertion of TEA. This is applicable only in the case where the option selected under "Processors Used" is <i>less than 3</i> and the processor being used is PPC 740/750.
(ALTERNATE DATA ERROR)	Data error in Alternate Master Data
(ARTRY_CYCLE)	Sequence having ARTRY* asserted
(UNKNOWN)	Cycle does not carry valid information

If a sequence contains both Address and Data, then a combination of labels described above can be expected. For example, Alternate Masters address and data if acquired in a single sequence, that sequence would be labeled as (ALTERNATE ADDRESS AND ALTERNATE DATA).

The processor performing a transaction on the bus in a multiprocessor environment would be treated as an Alternate master only when the option selected under “Processors Used” is greater than 2. Hence, even if the number of processors in the multiprocessor environment is 2 and if the above mentioned option is selected, then all the transactions of the second processor would still be treated as Alternate Master Transactions.

A sequence containing data may also be labeled as shown in Table 2–8.

Table 2–8: General cycle type labels definitions

Cycle type label	Definition
(FLUSH)	An instruction is fetched but not executed; it is labeled as FLUSH
(FLUSH: PREDICTION FAIL)	An instruction was fetched based on the prediction bit, but the prediction was incorrect
(CACHE FILL)	Burst read transfer that occurs after wrap around of the end of the cache line
(CLEAN BLOCK)	Clean Block transaction
(FLUSH BLOCK)	Flush Block transaction
(SYNC)	Address Only transaction due to the execution of Sync instruction
(KILL BLOCK)	Kill Block transaction
(EIEIO)	Enforce In-Order Execution of I/O cycle
(LARX RSRV SET)	Reservation Set
TLBSYNC	Translation Lookaside Buffer Synchronization
ICBI	Instruction Cache Block Invalidate
(GRAPHICS WRITE)	External Control Word Write transaction
(GRAPHICS READ)	External Control Word Read transaction
(WRT WITH FLUSH)	Write-with-Flush operation issued by the processor
(WRT WITH KILL)	Write with Kill operation
(DATA READ)	Single Beat Read or Burst Read operation
(RWITM)	Read-With-Intent-To-Modify transaction
(WWF-ATOMIC)	Write-With-Flush-Atomic operations issued by the processor
(READ-ATOMIC)	Read-Atomic operation
(RWITM-ATOMIC)	Read-With-Intent-To-Modify-Atomic transaction
(RWNITC)	Read With No Intent To Cache
(RCLAIM)	Read Claim (Applicable only in the MaxBus mode which is not supported)
(RESERVED)	Reserved Transaction type match any of the defined patterns

Sample	PPC7400ITR Address	PPC7400ITR TraceAddr	PPC7400ITR Hi_Data	PPC7400ITR Lo_Data	PPC7400ITR Mnemonics
534	00000D00	00000D00	-----	-----	(TRACE EXCEPTION)
	00000D00	00000D00	7C5A02A6	-----	mfspr r2,26
	00000D04	00000D04	-----	7C842278	xor r4,r4,r4
535	00000D08	-----	-----	-----	(7400 ADDRESS)
536	00000D08	00000D08	38840400	-----	addi r4,r4,#400
	00000D0C	00000D0C	-----	90440000	stw r2,#0(r4)
537	00000D10	-----	-----	-----	(7400 ADDRESS)
538	00000400	-----	-----	-----	(7400 ADDRESS)
539	00000D10	00000D10	4C000064	-----	rfi crb0,crb0,crb0
540	00000D18	-----	-----	-----	(7400 ADDRESS)
541	00000400	00000400	0006002C	-----	(WRT WITH FLUSH)
542	00000D18	00000D18	-----	-----	(FLUSH)
543	00060028	-----	-----	-----	(7400 ADDRESS)
544	00060028	00060028	41800018	-----	bc 12,0,00060040
545	00060030	-----	-----	-----	(7400 ADDRESS)
546	00060030	00060030	-----	-----	(FLUSH:PREDICTION FAIL)
547	00060038	-----	-----	-----	(7400 ADDRESS)
548	00060038	00060038	-----	-----	(FLUSH:PREDICTION FAIL)
549	00060040	-----	-----	-----	(7400 ADDRESS)
550	00060040	00060040	7D2A5A14	-----	add r9,r10,r11
	00060044	00060044	-----	7D4B6214	add r10,r11,r12
551	00060048	-----	-----	-----	(7400 ADDRESS)
552	00060048	00060048	7D6C6A14	-----	add r11,r12,r13
	0006004C	0006004C	-----	7D8D7214	add r12,r13,r14
553	00060050	-----	-----	-----	(7400 ADDRESS)
554	00060050	00060050	7DAE7A14	-----	add r13,r14,r15
	00060054	00060054	-----	48060002	ba 00060000
555	00060058	-----	-----	-----	(7400 ADDRESS)
556	00060058	00060058	-----	-----	(FLUSH)
557	00000D00	-----	-----	-----	(7400 ADDRESS)
558	00000D00	00000D00	-----	-----	(TRACE EXCEPTION)
	00000D04	00000D04	7C5A02A6	-----	mfspr r2,26
	00000D08	00000D08	-----	7C842278	xor r4,r4,r4
559	00000D08	-----	-----	-----	(7400 ADDRESS)
560	00000D08	00000D08	38840400	-----	addi r4,r4,#400
	00000D0C	00000D0C	-----	90440000	stw r2,#0(r4)

Figure 2–2: Example of the hardware display format

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the PPC7400ITR microprocessor are as follows:

b	bl	sc
ba	bla	rfi

Instructions that might generate a change in the flow of control in the PPC7400ITR microprocessor are as follows:

bc	bcla	bcctr	tdi
bca	bclr	bcctrl	tw
bcl	bclrl	td	twi

The disassembler displays some instructions that cause traps or interrupts, as well as exception vector reads that are taken and "the message" (****BAD CYCLE TYPE****). Mnemonics misinterpreted by the disassembler are also displayed.

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the PPC7400ITR microprocessor are as follows:

sc rfi

Instructions that might generate a subroutine call or a return in the PPC7400ITR microprocessor are as follows:

td tdi tw twi

The disassembler displays some instructions that cause traps or interrupts, as well as exception vector reads that are taken and "the message" (****BAD CYCLE TYPE****). Mnemonics misinterpreted by the disassembler are also displayed.

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the PPC7400ITR support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception cycles

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

- Select the prefetch byte order
- Select the alternate byte order low and high bounds
- Select the exception byte order
- Specify the exception prefix

The PPC7400ITR support product has five additional fields: Prefetch Byte Ord, Alt-Byte Ord-Lo Bound, Alt-Byte Ord-Hi Bound, Exception Byte Ord, and Exception Prefix. These fields appear in the area indicated in the basic operations user manual.

Prefetch Byte Order. You can select the byte ordering for the predominant instruction fetches as Big- or Little-Endian.

Alt Byte Ord - Lo Bound and Alt Byte Ord - Hi Bound. You can enter the low and high bounds for the alternate byte ordering range. The default is 00000000.

You should enter alternate values on double-word boundaries. If the value is not on a double-word boundary, the disassembler assumes the value to be the nearest double-word.

If you do not enter a value in the field, the data is acquired and disassembled according to the selection in the Prefetch Byte Ord field.

***NOTE.** The alternate high bound value must be greater than the alternate low bound value or disassembly will be incorrect.*

Exception Byte Order. You can select the byte ordering for exception processing as Big- or Little-Endian.

Exception Prefix. You can enter the prefix value of the exception table as 000 to FFF. The default prefix value is 000. The exception table must reside in external memory for interrupt and exception cycles to be visible to the disassembler.

***NOTE.** If an address is in the Exception processing region and in the range selected for the alternate byte ordering, the disassembler uses the byte ordering selected for the Exception processing.*

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it.

Marks are placed by using the Mark Opcode button. The Mark Opcode button will always be available. If the sample being marked is not an Address cycle or Data cycle of the potential bus master, the Mark Opcode selections will be replaced by a note indicating that “An Opcode Mark cannot be placed at the selected data sample.”

When a cycle is marked, the character “>>” is displayed immediately to the left of the Mnemonics column. Cycles can be unmarked by using the “Undo Mark” selection, which will remove the character “>>”.

The list of selections varies depending on the selection in the Bus Processor Select field in the Disassembly property page (Disassembly Format Definition overlay).

Mark selections available on data sequences without an address and data cycle associated with a fetch cycle when the PPC7400ITR microprocessor is operating in 64-bit mode are as follows:

- Opcode - Opcode
- Opcode - Flush
- Flush - Opcode
- Flush - Flush
- Invalid_Data
- Undo Mark

Mark selections available on sequences with only an Address cycle are as follows:

- Invalid_Address
- Undo Mark

The following two extra marking options are provided when the Heuristic Method is chosen for Instruction Fetch and Data Read differentiation.

- Not an Instruction Fetch
- Instruction Fetch

Mark selections available on sequences with both data and address cycles (if the data cycle is associated with a fetch cycle) and the PPC7400ITR microprocessor is operating in 64-bit mode are as follows:

- Opcode - Opcode
- Opcode - Flush
- Flush - Opcode
- Flush - Flush
- Invalid_Data

Invalid_Address
 Opcode - Opcode Invalid_Address
 Opcode - Flush Invalid_Address
 Flush - Opcode Invalid_Address
 Flush - Flush Invalid_Address
 Invalid_Address Invalid_Data
 Undo Mark

Mark selections available on sequences with data that is not associated with a Fetch cycle are as follows:

Invalid_Data
 Undo Mark

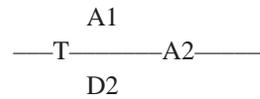
Table 2–9 describes the various combinations of mark selections.

Table 2–9: Mark selections and definitions

Mark selection or combination *	Definition
Opcode - Opcode	HI_Data and LO_Data are disassembled
Opcode - Flush	Only HI_Data is disassembled in Big-Endian mode or only LO_Data is disassembled in Little-Endian mode
Flush - Opcode	Only LO_Data is disassembled in Big-Endian mode or only HI_Data is disassembled in Little-Endian mode
Flush - Flush	Instructions not disassembled and labeled as (FLUSH)
Invalid_Address	Valid PPC 7400 address is invalidated and labeled as (Incom_Addrs)
Instruction Fetch	The data corresponding to the address is decoded as an instruction fetch
Not an Instruction Fetch	The data corresponding to the address is decoded as a data read
Opcode - Opcode Invalid_Address	Use to mark a sequence with PPC7400ITR address and data from different transactions; HI_Data and LO_Data are disassembled; the address is invalidated
Opcode - Flush Invalid_Address	HI_Data is disassembled only in Big-Endian mode or LO_Data is disassembled only in Little-Endian mode; the address is invalidated
Flush - Opcode Invalid_Address	LO_Data is disassembled only in Big-Endian mode or HI_Data is disassembled only in Little-Endian mode; the address is invalidated
Flush - Flush Invalid_Address	Instructions not disassembled and labeled as (FLUSH); the address is invalidated
Invalid_Address	Address is invalidated
Invalid_Data	HI_Data and LO_Data are invalidated
Invalid_Address Invalid_Data	Address, HI_Data, and LO_Data are invalidated
Undo Mark	Removes all marks on the selected sample

* Mark selections intended to be used on sequences with data are not available for noninstructions.

The Invalid_Address mark invalidates the address from being associated with the wrong data. You can use this mark if you determine that the data for the address was not acquired. For example:



Here, data for the address A1 was not acquired. But the disassembler will associate the address A1 with the data D2. Hence, A1 has to be marked as Invalid_Address to invalidate A1.

The Invalid_Data mark invalidates the data from being associated with the wrong address. You can use this mark if you determine that the address for the data was not acquired. For example:



Here, Address for Data D0 was not acquired or the disassembler has failed to associate Data D0 with Address A0 for some reason. The resulting display associates Data D0 with Address A1 and Data D1 with Address A2 which is wrong. To correct the disassembly, data D0 may have to be marked as Invalid_Data so that Address A1 will associate with Data D1.

Not an Instruction Fetch. This marking option primarily allows the user to correct any data that has wrongly been decoded as an instruction fetch. Such a wrong decoding is possible sometimes in the Heuristic Method since the TT encodings along with WT_pin does not provide a clear distinction between Instruction Fetches and Data Reads as in PPC 740/750. Hence the Heuristic Algorithm is used to perform the necessary distinction, which is again approximate.

This marking option has to be used on the address of the data that has been wrongly decoded as instruction fetch.

The same explanation, though in the reverse context, is true for the marking option Instruction Fetch.

Information on basic operations contains more details on marking cycles.

Displaying Exception Labels

The disassembler can display PPC7400ITR exception labels. The exception table must reside in external memory for interrupt and exception cycles to be visible to the disassembler.

You can enter the table prefix in the Exception Prefix field. The Exception Prefix field provides the disassembler with the offset address; enter a three-digit hexadecimal value corresponding to the prefix of the exception table.

These fields are located in the Disassembly property page (Disassembly Format Definition overlay).

Table 2–10 lists the PPC7400ITR interrupt and exception labels.

Table 2–10: Interrupt and exception labels

Offset	Displayed interrupt or exception name
0x00000	(RESERVED)
0x00100	(SYSTEM RESET)
0x00200	(MACHINE CHECK EXPN)
0x00300	(DSI EXPN)
0x00400	(ISI EXPN)
0x00500	(EXTERNAL INTRPT)
0x00600	(ALIGNMENT EXPN)
0x00700	(PROGRAM EXPN)
0x00800	(FLOATING-POINT UNAVLBL EXPN)
0x00900	(DECREMETER EXPN)
0x00A00 to 0x00BFF	(RESERVED)
0x00C00	(SYSTEM CALL)
0x00D00	(TRACE EXPN)
0x00E00	(RESERVED)
0x00F00	(PERFORMANCE MONITOR EXPN)
0x01000	(RESERVED)
0x01100	(RESERVED)
0x01200	(RESERVED)
0x01300	(INST ADDRESS BREAKPOINT EXPN)
0x01400	(SYS MGMT INTERRUPT EXPN)
0x1500	(RESERVED)
0x1600	(VMX ASSIST INTERRUPT)
0x01700	(THERMAL MGMT INTRPT)
0xF200	(ALTIVEC UNAVAILABLE EXPN)
0x01800 to 0x02FFF	(RESERVED)

Disassembly Display Options

Table 2–11: TLA disassembly display options

Description	Option
Show:	Hardware (Default) Software Control Flow Subroutine
Highlight:	Software (Default) Control Flow Subroutine None
Disasm Across Gaps:	Yes (Default) No

Micro Specific Fields

This submenu will have the title:“PPC7400ITR Controls”.

Select Processor. The processor for which disassembly is to be done has to be selected through this option. This consists of the following two options:

- **PPC 7400:** This option has to be selected when the processor for which disassembly has to be carried out is PPC 7400.
- **PPC 740/750:** This option has to be selected when the processor for which the disassembly has to be done is PPC 740 or PPC 750.

Processors Used. The TMS 545A support provides simultaneous disassembly for a maximum of 2 processors. If there are more than two processors used, then the transaction by the processors other than the one that is being probed are labeled as Alternate Master Transactions. This consists of the following two options:

- **Less Than 3:** This option should be selected when the number of processors being used in a mutiprocessor environment is less than 3. The usage of this option causes simultaneous disassembly to be carried out for a maximum of two processors.
- **Greater Than 2:** This option should be selected when the number of processors being used is greater than 2. The selection of this option causes all the transactions caused by the other processors to be labeled as Alternate Master Transactions.

NOTE. *If an address happens to be in both the Exception processing region of the processor and in the range selected for the alternate byte ordering, then the byte ordering selected for the Exception processing will be assumed for that address.*

Instruction Fetch Indicator Provides two options to the user:

- Transfer Group
- By Heuristic Method

The Transfer Group option should be selected by the user only when TT[0–4] signals distinguish between Instruction Fetches and Data reads. This is possible only when the IFTT bit in the HID0 register is set.

The By Heuristic Method option should be chosen only when the TT[0–4] signals do not differentiate between Instruction Fetches and Data Reads. Now a Heuristic algorithm is used to differentiate between the two types of transactions. Note that this algorithm provides only an approximate differentiation between the two types of transactions. In cases where the differentiation is incorrect marking, options have to be used to do the necessary correction.

Disassemble based on. This option lets the user select the basis for disassembly.

Fetch Stream (Default)

Memory Image

When the option Fetch Stream is selected normal disassembly occurs. But when the Memory Image option is selected disassembly is based on the image file, for example, S-record file.

Address for Trace Writes. This field contains the address to which the Branch Trace Exception handler needs to write the branch target address (SRR0 value).

0x00000000 (default)

Maximum Instructions. Here the user needs to enter the number of instructions to be displayed (from the image file each time a BTE is encountered) in the property for Maximum Instructions.

40 (default)

The user needs to enter the number of instructions to be displayed (from the image file each time a BTE is encountered). This number is the maximum number of instructions that will be taken from the image file to show each time a control flow change occurs.

Image file path. The user needs to enter the complete path to the S-record file in the property for Image file path. The Browse button can be used for this.

C:\Program Files\TLA 700\Supports\PPC7400ITR\Demo.src (Default)

Address Offset in Hex. This is the address offset (in hex) from the starting address (as indicated by the S-record) where the user program will be loaded in memory.

0x00000000 (default)

Suppose the linker output and the corresponding S-record file have a starting address of 0x0, but the user loads at a different address. For example, 0x50, then the user will need to specify the offset 0x50 in this field.

Instruction Trace Reconstruction (ITR)

The logic Analyzer acquires data, which appears on the external bus of the microprocessor. When the internal instruction cache is enabled, most of the instruction fetches happen from the cache for which no external bus activity occurs. This severely limits the information that a logic analyzer can display for the user. To address this problem, some indirect methods are used to logically track the program flow even though instruction fetches are happening from internal cache. Following is brief explanation with examples showing ways you can use the ITR method with this support.

It is possible to reconstruct the program execution. That is, the portions of the program which get executed inside the cache can be read from the Image File and shown on the display. This can occur if both a program image (or Image File) that is being executed is available externally (in S-record format for example), and if the processor provides information about the control flow instructions being executed and they can be acquired.

Memory Image (S-record)

The memory image is a hexadecimal form of the program being executed by the processor; therefore, it is the output of the Compiler/Assembler and Linker. Linker output is normally available in one of the industry standard formats like Intel Hex format, S-record format, or a proprietary format used by the software development system. This support requires the external Image file to be in the Motorola S-record format. Usually, tools are available to convert proprietary output formats into Motorola S-record. The usage of one particular tool to convert a source file into a S-record file (Image file) is also explained in a later section.

Image Reader

The Motorola MPC7400 processor provides a Branch Trace Exception (BTE), which can generate an exception on change of control flow, whenever a branch instruction is encountered. Branch Trace Exception is a feature available in the

processor used for collecting information about the program flow inside the cache. The BTE is used to provide information about the target address, whenever a change in control flow takes place. This in conjunction with the external image file is used to display cache activity. TMS 545A supports only the S-record format so it requires that the image file be available in Motorola S-record format.

Basically, whenever a gap occurs in the acquisition because fetches take place from internal cache, instructions are taken from the external image file and displayed.

Viewing Cache Activity

This section on *Viewing Cache Activity* on the Tektronix logic analyzer consists of a three-part procedure and a section showing the limits to using this procedure when using self-modifying code (see page 2–29).

This procedure uses Green Hills software and SDS (Software Development Solutions) Compiler for Embedded PCs. If you do not have this software, you will need to find an alternative. Contact your Tektronix sales representative if you need support.

Three-part procedure:

- Retrieving Control Flow Information
- Converting an Image file to S-record format
- Configuring the Tektronix logic analyzer

Retrieving Control Flow Information. Follow this procedure to retrieve information about the Control flow from the Processor:

1. Enable the Branch Trace Exception bit of the Processor.

The Branch Trace enable bit is part of the register MSR. Once this bit is enabled whenever a branch occurs in the program, a BTE is generated. This exception is used to discover that a branch instruction has occurred and to make target address available.

2. Write the exception handler routine.

Whenever a branch is encountered, the program flows to the exception handling routine, which for MPC7400 is at D00. You have to write your exception handler routine here. A sample is shown below.

```

mfsrr0 r2    // r2 and r4 are assumed not to be modified by the user's
              program. The user is advised to use registers which are not
              used in their main program.

xor r4,r4,r4

addi r4,r4,Non-cacheable address //The user has to enter the required
                                  noncacheable address.

stw r2,0(r4)

rfi

```

The exception handler routine for the PPC7400ITR support needs the starting address to look into the code in the image file. This address will be available as the “return address from a BTE / branch target address” in the register SRR0. The value of SRR0 must be written onto a noncacheable region of memory so that it appears on the external bus. The Image reader reads this value and the cache activity is filled in. In the above code, the value of SRR0 is moved to a register (R2) and this value is written onto a noncacheable region of the memory so that it is available on the external bus.

Converting an Image File to S-Record Format. The source code must be converted to S-record format. For example:

FileName.s (the source file with the mnemonics) to FileName.src

Follow these steps to convert an image file into S-record format using Green Hills software:

- a. Open the Green Hills command line
- b. Change the working directory to the directory with FileName.s, which for this example is c:\test
- c. Type `cd c:\test`
- d. Type `asppc -o FileName.o FileName.s`
This command will generate a FileName.o file
- e. Type `lx -o FileName.out FileName.o`
This command will generate a FileName.out file

Execute step f at an MS Windows command prompt, not a Green Hills command prompt. You can either go to the directory `c:\sds73\hcppc\bin` and type the following:

f. `elf2hex -o c:\test\FileName.src -m c:\test\FileName.out`

Or you can go to the directory where `FileName.s` is present for example, `c:\test` and type the following:

g. `c:\sds73\hcppc\bin\elf2hex -o FileName.src -m FileName.out`

The `elf2hex` utility used in this example is part of SDS (Software Development Solutions) Compiler for Embedded PCs.

This will generate a `FileName.src` file in the same directory as the `FileName.s` file, which for this example is `c:\test`.

Configuring the TLA. Follow these steps to configure your Tektronix logic analyzer.

1. In the TLA software, load the support package.
2. Click on Setup, and then, on Trigger. Set the trigger for the address D00, which is the Exception handler routine address.
3. Modify the TLA listing window properties as shown in Figure 2–3.

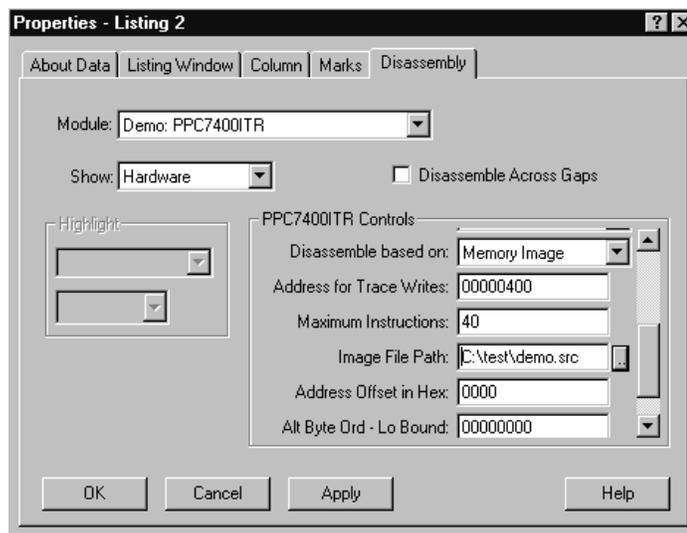


Figure 2–3: Listing window

- a. Change the Disassemble based on property to Memory Image.
- b. Enter the noncacheable address used in the exception routine in the property for Address for Trace Writes.
- c. Enter the number of instructions to be displayed (from the image file each time a BTE is encountered) in the property for Maximum Instructions. The default value is 40. This number is the maximum number of instructions that will be taken from the image file to show each time a control flow change occurs.

The number of instructions displayed is limited by two conditions:

- Number of instructions entered by the user.
- Another branch instruction encountered in the Image file will stop the display.

The Image reader displays instructions from the cache until the number of instructions entered by the user is completed or another branch instruction is encountered.

- d. Enter the complete path to the S-record file in the property for Image file path. Either type in the path name or select the path name by pressing the menu button to the right of the property for Image file path.
- e. Enter the address offset in the field corresponding to Address Offset in Hex. This is the address offset (in hex) from the starting address (as indicated by the S-record) where the user program will be loaded in memory.

Suppose the linker output and the corresponding S-record file have a starting address of 0x0, but the user loads at a different address, for example, 0x50, then the user needs to specify the offset 0x50 in this field.

When all three sections of the procedure are completed, press ok/apply to view the cache data on the display. To revert back to the original Fetch Stream data, change the property for “Disassemble based on” back to Fetch Stream. Figures 2–4 and 2–5 show the effect of changing the property for “Disassemble based on” from Fetch Stream data to Memory Image.

Figure 2–4 shows that the property for Fetch Stream is enabled. The exception handler was written to make the value of SRR0 appear on the bus thus enabling the Image reader to access the Image file. Figure 2–5 shows that the property for Memory Image is enabled. In this case, the fetch stream is not disassembled and is shown as “Instruction from fetch”.

Sample	PPC7400ITR Address	PPC7400ITR TraceAddr	PPC7400ITR Hi_Data	PPC7400ITR Lo_Data	PPC7400ITR Mnemonics
510	00060000	00060000	7C000278	-----	xor r0,r0,r0
511	00060004	00060004	-----	7C210A78	xor r1,r1,r1
512	00060008	00060008	7DF08A14	-----	(7400 ADDRESS)
513	00060010	00060010	-----	7E119214	add r15,r16,r17
514	00060014	00060014	7C200800	-----	add r16,r17,r18
515	00060018	00060018	-----	4080000C	(7400 ADDRESS)
516	00060018	00060018	-----	-----	bc 4,0,00060020
517	00000000	00000000	-----	-----	(7400 ADDRESS)
518	00000000	00000000	-----	-----	(FLUSH)
519	00000004	00000004	7C5A02A6	-----	(TRACE EXCEPTION)
520	00000008	00000008	38840400	-----	mf spr r2,26
521	0000000C	0000000C	-----	7C842278	xor r4,r4,r4
522	00000400	00000400	-----	-----	(7400 ADDRESS)
523	00000010	00000010	4C000064	-----	addi r4,r4,#400
524	00000018	00000018	-----	90440000	stw r2,#0(r4)
525	00000400	00000400	-----	-----	(7400 ADDRESS)
526	00000018	00000018	-----	-----	(7400 ADDRESS)
527	00060020	00060020	7D2A5A14	-----	rfi crb0,crb0,crb0
528	00060024	00060024	-----	7D4B6214	(7400 ADDRESS)
529	00060028	00060028	41800018	-----	(WRT WITH FLUSH)
530	00060030	00060030	-----	-----	(FLUSH)
531	00000000	00000000	-----	-----	(7400 ADDRESS)
532	00000004	00000004	7C5A02A6	-----	(TRACE EXCEPTION)
533	00000008	00000008	-----	7C842278	mf spr r2,26
534	0000000C	0000000C	-----	-----	xor r4,r4,r4
535	00000010	00000010	38840400	-----	(7400 ADDRESS)
536	00000018	00000018	-----	-----	addi r4,r4,#400

Figure 2-4: Display showing Fetch Stream

Sample	PPC7400ITR Address	PPC7400ITR TraceAddr	PPC7400ITR Hi_Data	PPC7400ITR Lo_Data	PPC7400ITR Mnemonics
524	00000018	-----	-----	-----	(7400 ADDRESS)
525	00000018	-----	00060020	00060020	-- Instn From Fetch --
526	00060020	00060020	7D2A5A14	-----	add r9,r10,r11
527	00060024	00060024	-----	7D4B6214	add r10,r11,r12
528	00060028	00060028	4180000C	-----	bc 12,0,00060034
529	FFFFFFFF	-----	7C60212E	7C7A02A6	-- Instn From Fetch --
530	00060020	-----	-----	-----	(7400 ADDRESS)
531	FFFFFFFF	-----	7D2A5A14	7D4B6214	-- Instn From Fetch --
532	FFFFFFFF	-----	-----	-----	(7400 ADDRESS)
533	FFFFFFFF	-----	4180000C	7EB61A14	-- Instn From Fetch --
534	00000000	-----	-----	-----	(7400 ADDRESS)
535	FFFFFFFF	-----	7ED7C214	7EF8CA14	-- Instn From Fetch --
536	FFFFFFFF	-----	7C5A02A6	7C842278	(7400 ADDRESS)
537	FFFFFFFF	-----	-----	-----	-- Instn From Fetch --
538	00000008	-----	38840400	90440000	(7400 ADDRESS)
539	00000010	-----	-----	-----	-- Instn From Fetch --
540	00000018	-----	-----	-----	(7400 ADDRESS)
541	00000018	-----	0006002C	0006002C	-- Instn From Fetch --
542	0006002C	0006002C	7EB61A14	-----	add r21,r22,r3
543	00060030	00060030	7ED7C214	-----	add r22,r23,r24
544	00060034	00060034	-----	7EF8CA14	add r23,r24,r25
545	00060034	00060034	-----	7EF8CA14	*** More Instructions (Change MA
546	FFFFFFFF	-----	7C60212E	7C7A02A6	-- Instn From Fetch --
547	FFFFFFFF	-----	-----	-----	(7400 ADDRESS)
548	FFFFFFFF	-----	4180000C	7EB61A14	-- Instn From Fetch --
549	00060030	-----	-----	-----	(7400 ADDRESS)

Figure 2-5: Display showing Memory Image

The limitation of this procedure is that it will not work correctly with self-modifying code.

Error Messages Specific to the ITR support. The following are error messages which are relevant to the ITR support.

1. **Could Not Open File** — This error message is displayed if the system is unable to open the specified file.
2. **Specified File is Not a Valid S-Record File** — This message is displayed if the file is not a valid S-record file. This might occur if:
 - The file is corrupted.
 - The format is not in the Motorola S-record format.
3. **Insufficient Memory** — This error occurs if problems are encountered with allocating memory for the different buffers.
4. **Error in Processing File** — Unspecified error occurred while processing the file.
5. **Invalid Address: No Associated Data** — This error implies that the data is not corresponding to the address passed to the Image reader. This might occur when the wrong .src file has been given as input to the Image reader or when there is an error in the flow of code.

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so that you can see an example of how your PPC7400ITR microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use, and you can view it without connecting the logic analyzer to your system under test.

Information on basic operations describes how to view the file.



Specifications

Specifications

This chapter contains information regarding the specifications of the support.

Specification Tables

Table 3–1 lists the electrical requirements the system under test must produce for the support to acquire correct data.

Table 3–1: Electrical specifications

Characteristics	Requirements
SUT clock rate	
PPC7X0 specified clock rate	Max 133 MHz
PPC7X0 tested clock rate	Max 100 MHz
Minimum setup time required	
TLA 700	2.5 ns
Minimum hold time required	
TLA 700	0 ns



Replaceable Parts List

Replaceable Parts List

This section contains a list of the replaceable parts for the TMS 545A PPC7400ITR microprocessor support product.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1–1972.

**Mfr. Code to Manufacturer
Cross Index** The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Replaceable Parts Lists

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077-0001

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discount'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
---	071-0797-00			1	MANUAL,TECH INSTRUCTIONS,PPC 7400_ITR;TMS 545A	80009	071-0797-00



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