Instruction Manual

Tektronix

TMS562A
MPC8260ITR Microprocessor
Software Support

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www.tektronix.com

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Preface

This instruction manual contains specific information about the TMS562A MPC8260ITR microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS562A MPC8260ITR support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to logic analyzer online help, an installation manual, or a user manual covering the basic operations of microprocessor support.

Contacting Tektronix

Phone	1-800-833-9200*
Address	Tektronix, Inc. Department or name (if known) 14200 SW Karl Braun Drive P.O. Box 500 Beaverton, OR 97077 USA
Web site	www.tektronix.com
Sales support	1-800-833-9200, select option 1*
Service support	1-800-833-9200, select option 2*
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 1-503-627-2400 6:00 a.m. – 5:00 p.m. Pacific time

*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This section contains information on the TMS562A MPC8260ITR microprocessor support and information on connecting your logic analyzer to your system under test.

Support Package Description

The TMS562A MPC8260ITR microprocessor support package displays disassembled data from systems based on the Motorola MPC8260 microprocessor.

The TMS562A support includes the 8260ITR_60X software support for the 60x Compatible Bus Mode (SDRAM, GPCM) and the 8260ITR_SNG software support for the Single 8260 Mode (SDRAM, GPCM).

To use this support efficiently, refer to your logic analyzer online help and the *PowerQUICC II User's Manual Rev. 1.0.*

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states the version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

The TMS562A support requires a minimum of one 136 module configuration when using either the 8260ITR_60X support or the 8260ITR_SNG support.

Requirements and Restrictions

Review the electrical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other MPC8260ITR support requirements and restrictions. The following information applies to both the 8260ITR_SNG and the 8260ITR_60X supports unless specified otherwise.

Reset. If a hardware reset occurs in your MPC8260ITR system during an acquisition, the application disassembler might acquire an invalid sample and display the disassembled data incorrectly.

System Clock Rate. The operating speeds that the TMS562A support can acquire data from the MPC8260ITR microprocessor are listed on page 3–1. These specifications were valid at the time this manual was printed. Please contact your Tektronix Sales Representative for current information on the fastest devices supported.

Disabling the Instruction Cache. To display disassembled acquired data, you must disable the internal instruction cache. Disabling the cache makes all instruction prefetches visible on the bus so that they can be acquired and displayed disassembled.

Disabling the Data Cache. To display acquired data, you must disable the data cache. Disabling the data cache makes visible all loads and stores to memory on the bus, including data reads and writes, so the software can acquire and display them.

Viewing Instruction Cache Activity. To see the Instruction cache activity, set the disassembly option "Disassemble based on" to Memory Image. For further details see the section *Viewing Cache Activity* on page 2–25.

Address Translation. The address translation must be turned off for proper disassembly. The TMS562A support does not handle address translation.

NonIntrusive Acquisition. Acquiring microprocessor bus cycles is nonintrusive to the system under test. That is, the MPC8260ITR support does not intercept, modify, or present signals back to the system under test.

Memory Region. If the memory region of a PortWidth overlaps with another PortWidth the disassembly may be incorrect.

Symbolic Display for Control group. The listed cycle types may be frequently wrong for the Control group when using noncustom clocked data. This problem occurs in waveform because the Control group is symbolic by default. To overcome this problem, you must expand the group and look at the individual lines.

Endian Mode for the Memory Image Option. The disassembly from the Memory Image occurs correctly only for Big endian mode. Therefore, the Memory image must be in Big Endian format.

8260ITR_SNG Support

EAV Bit. The EAV bit of the Bus Configuration Register (BCR) is required to be set to 1 for correct disassembly. In this case, the Bank select signals are not driven on the address bus. During READ and WRITE commands to SDRAM devices, the full address is driven on bus address lines. Therefore, when the EAV bit is set to 1, the full address is valid at PSDCAS~ asserted with PSDRAS~ deasserted for SDRAM accesses.

Memory Image Mode. In Memory Image Mode, NonMemory Image Cycles are shown:

Fetches/Reads as	(READ)
Writes as	(WRITE)

SDRAM Address Multiplexing. The SDRAM address Multiplexing is not supported, for correct disassembly the Full address is required on the bus along with the above requirement for the EAV bit.

Opcode Fetch/Opcode Read. The MPC8260 single mode microprocessor does not provide a signal to distinguish between Data Read and Opcode Fetch. The MPC8260ITR support adopts a heuristic approach and makes a reasonable estimate when looking at the address values of a few sequences around the current sequence. Yet, in some instances the support may fail, and then you need to use the Marking Cycles option (see page 2–21).

Internal Cycles. Internal Cycles are detected, but not disassembled. These cycles are shown as INTERNAL MEMORY CYCLE. Your input fields for entering the start address of Internal Memory must be appropriate.

Branch Instructions. When the Trace Exception is enabled for branch instructions the control goes to the Exception Handler. In that case the conditional branches are not shown as taken (even if taken) and flushing is not done. You must use Marking Cycles option for Flushing (see page 2–21).

Burst Cycles. There are no external signals available to indicate a burst transaction. The 8260ITR_SNG support adopts a heuristic approach and makes a reasonable estimate by looking at the address values of a few sequences around the current sequence to decide the burst. Yet, in some instances the support may fail in doing so, and then you need to use the Marking Cycles option (see page 2-18).

Data for Memory Read and Write. There are no external signals to indicate the size of the data in single 8260 mode. For memory reads and writes, all the data bytes

(on the data bus) starting from the address (indicated by Address group) are shown as valid irrespective of the size of the data.

8260ITR_60X Support

Pipeline. If the following behavior is observed, the association of ADDRESS1 to DATA 1 is handled correctly:

TRANSFER START
ADDRESS1
TRANSFER START
ADDRESS2
DATA 1

This behavior is basically a pipelined transaction. However, if ADDRESS1 is for a READ cycle, then ADDRESS1 is associated with DATA 1 which is not recommended. Such cycles are not observed normally and you may be requested to mark DATA 1 again as Opcode (see Marking Cycles option on page 2–21).

Memory Image Mode. In Memory Image Mode, NonMemory Image Cycles are shown in the following list when you set the Disassembly option Instruction Fetch Indicator to TC[0:2] Bits:

Fetch as	"——Fetch Stream——"
Reads as	(READ)
Writes as	(WRITE)

When a heuristic approach is chosen the 60x mode labels a NonMemory Image cycles as "——fetch Stream——".

TC[2:0] Encoding. When you set the disassembly option Instruction Fetch Indicator to TC[2:0] Bits Fetches, Reads and Writes are distinguished by encoding the TC[2:0] signals. The assumption is that each bus transaction has the corresponding TC bits valid throughout the transaction.

Opcode Fetch/Opcode Read. Fetch is based on TC encoding or a Heuristic approach. When a heuristic approach is selected, the MPC8260ITR support makes a reasonable estimate for the address values of a few sequences around the current sequence. Yet, in some instances the support may fail, and then you need to use the Marking Cycles option on page 2–21.

Alternate Master Cycles. Alternative bus master transactions are acquired by the MPC8260ITR support. The disassembler can distinguish between the MPC8260ITR cycle and the alternate master cycle by looking at a qualified Bus Grant. Alternate Cycles are not disassembled but shown as ALTERNATE MASTER CYCLE.

The Alternate Master operates under the following assumptions:

- The data and address buses can only have one master. If a master owns the address bus then the same master also owns the data bus. However, the period the buses are granted may differ due to split bus transactions or pipelining. In another words, if the BG~ and DBG~ signals are for the same alternate master and not a different alternate master then the buses must be granted to the requesting device.
- The arbiter type (external or internal) is determined at the time of system reset and will not change dynamically during program execution. This means that if the arbiter is configured as internal then BG~ and DBG~ signals are the output signals from the 8260 microprocessor throughout the execution. The signals BG~ and DBG~ are the inputs if the arbiter is external.
- If an alternate device asks for the bus (data / address) ownership and the current master grants it, the alternate device becomes the bus master in the next cycle. The alternate device continues to be the owner but for only one bus transaction. If the alternate device wants to be the master again then it must get bus grants from the original master again.
- If the BG~ is asserted before TS~ the address bus must be granted. This means that alternate master cycles must be BG~ (qualified) for the TS~ to grant the address bus to the requesting device. If there is a TS~ signal without a BG~ signal (qualified) assertion then the following cycle belongs to the original master. In the latter case when the address bus is not granted, the data bus is also assumed to belong to the original master.

Internal Cycles. Internal Cycles are detected but not disassembled. Those cycles are shown as INTERNAL MEMORY CYCLE. You must enter the appropriate input in the field for the start address of Internal Memory.

Write Cycles Data. ITR operates with the assumption that Write cycles Data is valid with ALE true, therefore, the corresponding address is valid.

Functionality Not Supported

Interrupt Signals Not all interrupt signals are acquired by the TMS562A support software. The interrupt signals that are acquired can be identified by the TMS562A support software by looking at the address that is displayed for the interrupt service.

CPM Cycles The communication processor module (CPM) is not supported.

DMA Cycles SDMA/IDMA cycles are not supported. DMA cycles are shown as ALTERNATE MASTER CYCLE.

UPM Cycles UPM cycles are not supported.

Local Bus Only the 60x Compatible bus mode is supported. The local bus of the processor is not supported.

Address Retry Cycles Address Retry cycles are not supported.

Transfer Error Cycles Transfer Error cycles are not supported. However, some specific errors can be detected based on available information: Bus Monitor Timeout error (using the Time Stamp information), and Write protect error (by locating the address falling in the memory region defined as read-only) etc.

Features Not Tested

Exceptions All exceptions not tested (for both 8260ITR_60X and 8260ITR_SNG).

Symbol Table The symbol table was checked for correct display only. Evaluation of the ability to trigger using the symbols was not performed (for both 8260ITR_60X and 8260ITR_SNG).

8260ITR_60X Setup

Memory. Memory with 8, 16, 32 PortWidths

Little Endian Mode. PPC Little Endian Mode

ITR. Internal Trace Reconstruction (ITR)

8260ITR_SNG Setup

Memory. Memory with 8, 16, 32 PortWidths (tested only through reference memory editing)

Little Endian Mode. PPC Little Endian Mode (tested only through reference memory editing)

ITR. Internal Trace Reconstruction (ITR) has been tested with only Assembly Level Language source code and not with High Level Language.

Memory Type. Only SDRAM and SRAM have been tested. DRAM is not tested.

Standard Accessories

The TMS562A Support is shipped with the following standard accessories:

- TMS562A Support SW Disk includes:

  8260ITR_60X for the 60x Compatible Bus support
  8260ITR_SNG for the Single 8260 support

- *TMS562A Support Instruction Manual*

Options

The following option is available when ordering the TMS562A Support:

- Option 21–Add P6434 Mass-Termination Probes

Connecting the Logic Analyzer to a System Under Test

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your system under test.

To connect the probes to MPC8260ITR signals in the system under test using a test clip, follow these steps:

1. Power off your system under test. It is not necessary to power off the logic analyzer.

CAUTION. *To prevent static damage, handle the microprocessor, the probes, and the logic analyzer module only in a static-free environment. Static discharge can damage these components.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from the test clip.

CAUTION. *To prevent permanent damage to the pins on the microprocessor place the system under test on a horizontal surface before connecting the test clip.*

3. Place the system under test on a horizontal, static-free surface.
4. Use Table 5–5 through Table 5–20 starting on page 5–5 to connect the channel probes to MPC8260ITR signal pins on the test clip or in the system under test.
5. Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. The information gives an overview of channel groups definitions, support package setups, and clocking options.

The information in this section is specific to the operations and functions of the TMS562A MPC8260ITR support on any Tektronix logic analyzer for which it can be purchased.

Before you acquire and display disassembled data, you need to load the support and specify the setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Installing the Support Software

NOTE. *Before you install any software, it is recommended that you verify that the microprocessor support software is compatible with the logic analyzer software.*

To install the TMS562A software on your Tektronix logic analyzer, follow these steps:

1. Insert the floppy disk in the disk drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the floppy disk.

To remove or uninstall software, close all windows, and then follow the above instructions and select Uninstall.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the TMS562A support is listed in the following tables and displayed in this order:

8260ITR_SNG support	Default display radix
Address	Hexadecimal
High_Data	Hexadecimal
Low_Data	Hexadecimal
TraceAddr	Hexadecimal (Synthesized Group)
Mnemonics	None (Disassembly text generated by PDL)
Control	Symbol
PortWidth	Hexadecimal (Synthesized Group)
Misc	OFF

8260ITR_60X support	Default display radix
Address	Hexadecimal
High_Data	Hexadecimal
Low_Data	Hexadecimal
Trace Address	Hexadecimal (Synthesized group)
Mnemonics	None (Disassembly text generated by PDL)
Control	Symbolic
Tsize	Symbolic
TransferType	Hexadecimal
TC	Hexadecimal
Misc	OFF

The channel group tables begin on page 5–1.

Support Package Setups

The TMS562A software installs MPC8260ITR support package setup file.

8260ITR_60X Setup This setup provides disassembly support for an alternate master, for example, an L2 cache, an ASIC DMA, a high-end PowerPC processor, or an MPC8260ITR microprocessor. Signals are displayed as they appear electrically on the front side bus.

8260ITR_SNG Setup This setup provides disassembly support for a single MPC8260ITR bus mode. Signals are displayed as they appear electrically on the front side bus.

Clocking

This section provides information on clocking options for the MPC8260ITR support.

Custom Clocking

A special clocking program is loaded to the module every time you load the MPC8260ITR support. This special clocking is called Custom.

When Custom is selected, the Custom Clocking Options menu has the following subtitles added:

- 8260ITR_60X Microprocessor Clocking Support
- 8260ITR_SNG Microprocessor Clocking Support

Clocking Options

The TMS562A support offers a microprocessor-specific clocking mode for the MPC8260ITR microprocessor. This clocking mode is the default selection whenever you load the MPC8260ITR support.

Disassembly is not correct when using the Internal or External clocking modes. Information in your logic analyzer online help describes how to use these clock selections for general-purpose analysis.

Setup and Hold Time. You can change the Setup and Hold time window of all the signal groups. The default Setup time is 2.5 ns and the Hold time is 0 ns. The user defined Setup and Hold has precedence over default Setup and Hold times.

Signal Acquisition

The following section shows timing diagrams and tables that list details about how you acquire the relevant address, data, and control signals from various memory types.

Figures 2–1 shows bus timing for the 8260ITR_60X mode.

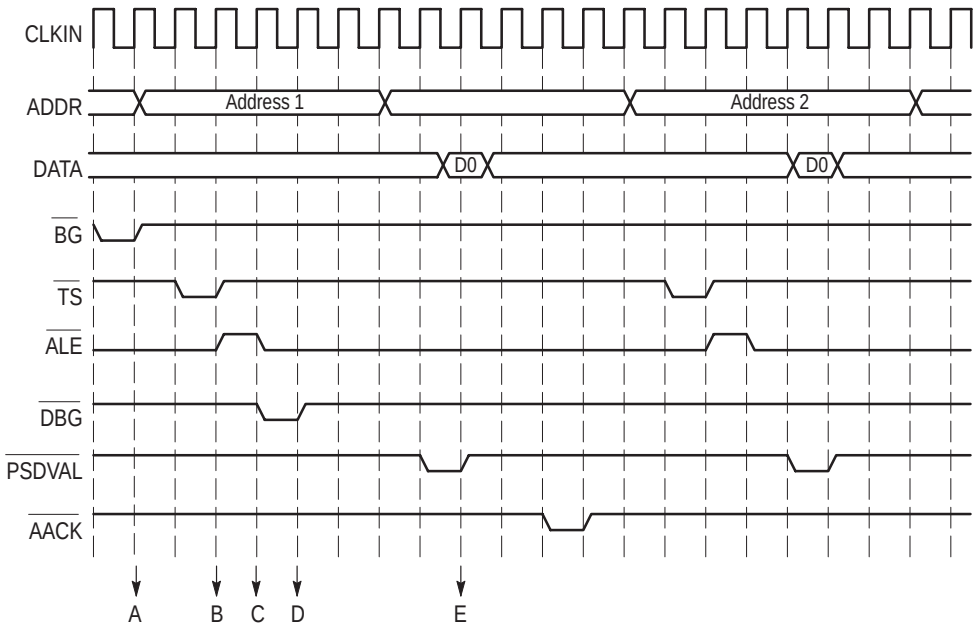


Figure 2–1: Bus timing for 8260ITR_60X mode

8260ITR_60X Mode. The Custom Clock is the rising edge of CLKIN Clock. Table 2–1 lists the acquisition of signals for 8260ITR_60X mode.

- Sample points:

  BUS_GRANT =
  {”BG~”,”DBG~”,”ABB~/IRQ2~”,”DBB~/IRQ3~”,”ARTRY~”};

  TS_ATRIB = {”TS~”, ”TBST~”, ”TSIZ0”, ”TSIZ1”, ”TSIZ2”,”TSIZ3”,
  BNKSEL0/TC0/AP1/MODCK1~”,
  ”BNKSEL1/TC1/AP2/MODCK2~”,
  “BNKSEL2/TC2/AP3/MODCK3~”, ”TT0”, ”TT1”, ”TT2”,
  ”TT3”, ”TT4”, ,}

- Master sample points:

  Master sample_pt M = {”PSDA10/PGPL0”, ”HRESET~”, ”SRESET~”, ”PSDAMUX/PGPL5”, ”L2_HIT~/IRQ4~”, ”CS3~”, ”CS1~”, ”CS0~”, LOGA7, LOGA6, LOGA5, LOGA4, LOGA3, LOGA2, LOGA1, LOGA0, LOGE7, LOGE6, LOGE5, LOGE4, LOGE3, LOGE2, LOGE1, LOGE0, LOGD7, LOGD6, LOGD5, LOGD4, LOGD3, LOGD2, LOGD1, LOGD0, ”PSDVAL~”, ”TA~”, ”BCTL0~”, ”AACK~”, ”BR~”}

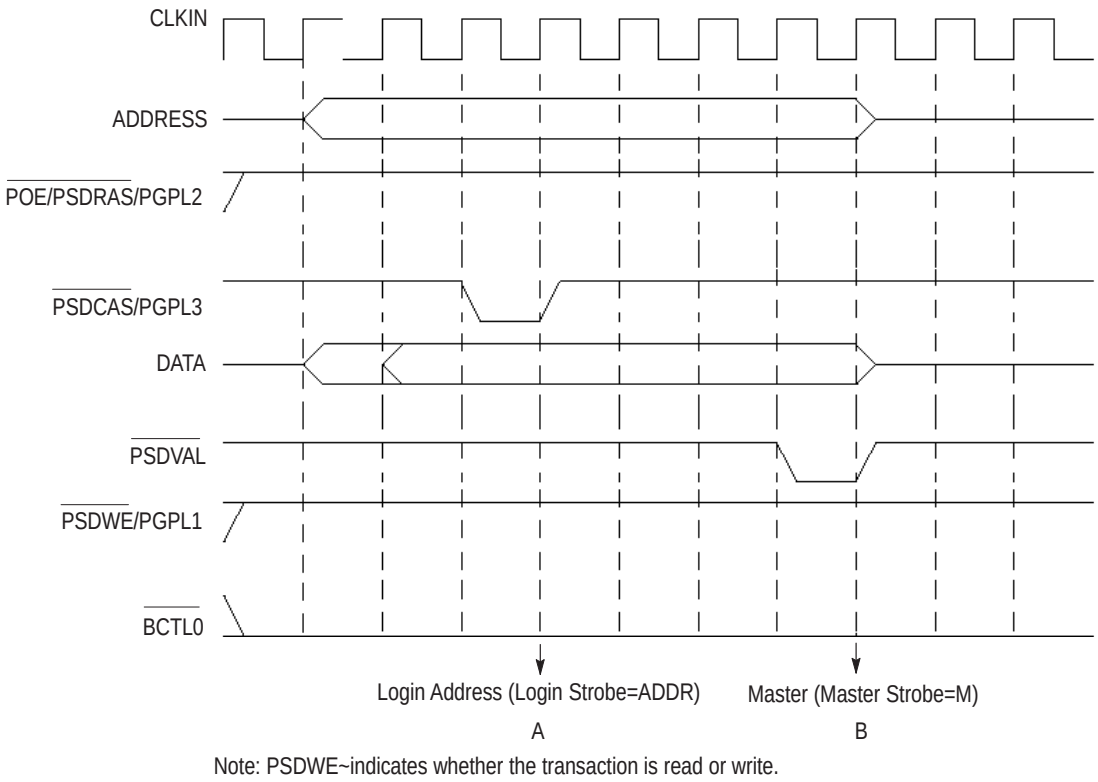
Table 2–1: Signal acquisition for 8260ITR_60X mode

Qualifiers		Operation	Signals	Position
BG~	= Low	Sample BUS_GRANT and Master	BG~, DBG~, ABB~/IRQ2~, DBB~/IRQ3~, ARTRY~ PSDA10/PGPL0, HRESET~, SRESET~, PSDAMUX/PGPL5, L2_HIT~/IRQ4~, CS3~, CS1~, CS0~, A[0–26], D[0–31], D[32–63], BADDR[27–31], PSDVAL~, TA~, BCTL0~, AACK~, BR~	Position A
TS~	= Low	Sample TS_ATRIB and Master	TS~, TBST~, TSIZ0, TSIZ1, TSIZ2, TISZ3, BNKSEL0/TC0/AP1/MODCK1~, BNKSEL1/TC1/AP2/MODCK2~, BNKSEL2/TC2/AP3/MODCK3~, TT0, TT1, TT2, TT3, TT4PSDA10/PGPL0, HRESET~, SRESET~, PSDAMUX/PGPL5, L2_HIT~/IRQ4~, CS3~, CS1~, CS0~, A[0–26], D[0–31], D[32–63], BADDR[27–31], PSDVAL~, TA~, BCTL0~, AACK~, BR~	Position B
ALE	= High	Master	PSDA10/PGPL0, HRESET~, SRESET~, PSDAMUX/PGPL5, L2_HIT~/IRQ4~, CS3~, CS1~, CS0~, A[0–26], D[0–31], D[32–63], BADDR[27–31], PSDVAL~, TA~, BCTL0~, AACK~, BR~	Position C

Table 2–1: Signal acquisition for 8260ITR_60X mode (Cont.)

Qualifiers	Operation	Signals	Position
DBG~ = Low	Sample TS_ATRIB and BUS_GRANT	TS~, TBST~, TSIZ0, TSIZ1, TSIZ2, TISZ3, BNKSEL0/TC0/AP1/MODCK1~, BNKSEL1/TC1/AP2/MODCK2~, BNKSEL2/TC2/AP3/MODCK3~, TT0, TT1, TT2, TT3, TT4BG~, DBG~, ABB~/IRQ2~, DBB~/IRQ3~, ARTRY~	Position D
PSDVAL~ = Low	Master	PSDA10/PGPL0, HRESET~, SRESET~, PSDAMUX/PGPL5, L2_HIT~/IRQ4~, CS3~, CS1~, CS0~, A[0–26], D[0–31], D[32–63], BADDR[27–31], PSDVAL~, TA~, BCTL0~, AACK~, BR~	Position E

Figures 2–2 shows that at the raising edge of the clock and on PSDCAS~/PGPL3, asserted and POE~/PSDRAS~/PGPL2 deasserted, ADDR is logged in. Finally at the raising edge of the clock and on PSDVAL~ assertion the data is sampled and master strobed.



Note: PSDWE~indicates whether the transaction is read or write.

Figure 2–2: Bus timing for 8260 single mode of SDRAM memory type

8260ITR_SNG Mode (SDRAM Acquisition). The Custom Clock is the rising edge of CLKIN Clock. Table 2–2 lists the acquisition of signals from SDRAM.

- Sample points:

  ADDR = {PSDCAS~/PGPL3, POE~/PSDRAS~/PGPL2, A3:7–0, A2:7–0, A1:7–0, A0:7–0}

- Master sample points:

  Master sample_pt M = {Master sample points include all other signals except those in ADDR sample point}

Table 2–2: Signal acquisition from SDRAM

Qualifiers	Operation	Signal	Position
PSDCAS~ = Low & PSDRAS~ = High	Sample ADDR	PSDCAS~/PGPL3, POE~/PSDRAS~/PGPL2, A3:7–0, A2:7–0, A1:7–0, A0:7–0	Position A
PSDVAL~ = Low	Master	PSDCAS~/PGPL3, POE~/PSDRAS~/PGPL2, A3:7–0, A2:7–0, A1:7–0, A0:7–0CLKIN, PSDA10/PGPL0, HRESET~, SRESET~, PSDAMUX/PGPL5, L2_HIT~/IRQ4~, CS3~, CS1~, CS0~, BR~, BNKSEL0/TC0/AP1/MODCK1~, BNKSEL1/TC1/AP2/MODCK2~, BNKSEL2/TC2/AP3/MODCK3~, TT0, TT1, TT2, TT3, TT4, TBST~, TSIZ0, TSIZ1, TSIZ2,TSIZ3TS~, ALE, PSDVAL~, AACK~, ARTRY~, DBB~/IRQ3~, BCTL0~, TA~, PSDWE~/PGPL1, TEA~A[0–31], D[0–31], D[32–63]	Position B

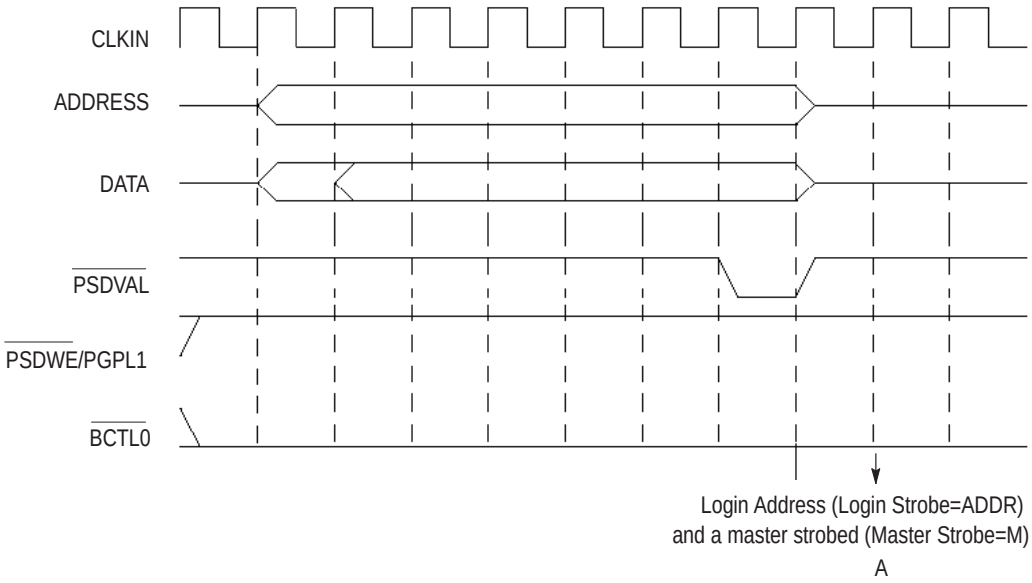
NON-SDRAM Acquisition. The Custom Clock is the rising edge of the CLKIN Clock. Table 2–3 lists signal acquisition from nonSDRAM.

Figure 2–3 timing waveforms show when the address, data and other signals are logged in.

The login strobe:
ADDR = {”PSDCAS~/PGPL3”, ”POE~/PSDRAS~/PGPL2”, A3: 7–0,A2: 7–0,A1: 7–0,A0: 7–0};

The Master strobe M includes all other signals except the one in ADDR.

In this case at the rising edge of the clock and on PSDVAL~ assertion, all the signals are sampled and master strobed.



Note: BCTL0~ indicates whether the transaction is read or write.

Figure 2–3: Bus timing for 8260 single mode of nonSDRAM access

Table 2–3: Signal acquisition from nonSDRAM

Qualifiers	Operation	Signal	Position
PSDVAL~ = Low	Sample ADDR and Master	PSDCAS~/PGPL3, POE~/PSDRAS~/PGPL2, A3:7–0, A2:7–0, A1:7–0, A0:7–0CLKIN, PSDA10/PGPL0, HRESET~, SRESET~, PSDAMUX/PGPL5, L2_HIT~/IRQ4~, CS3~, CS1~, CS0~, BR~, BNKSEL0/TC0/AP1/MODCK1~ BNKSEL1/TC1/AP2/MODCK2~ BNKSEL2/TC2/AP3/MODCK3~ TT0, TT1, TT2, TT3, TT4, TBST~, TSIZ0, TSIZ1, TSIZ2,TSIZ3TS~, ALE, PSDVAL~, AACK~, ABB~/IRQ2~, ARTRY~, DBB~/IRQ3~, BCTL0~, TA~, PSDWE~/PGPL1, TEA~A[0–31], D[0–31], D[32–63]	Position A

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. The information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Labeling Cycle type
- Changing the way data is displayed
- Changing disassembled cycles with the mark cycles function

Acquiring Data

Once you load the MPC8260ITR support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the *Basic Operations User Manual*.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–16.*

The default display format displays the Address, Data, Tsize, Control, and Misc, channel group values for each sample of acquired data.

If a channel group is not visible, you must use the Disassembly property page to make the group visible.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–4 lists these special characters and strings and gives a definition of what they represent.

Table 2–4: Description of special characters in the display

Character or string displayed	Definition
>	Indicates there is insufficient room on the screen to show all available data.
»	The instruction was manually marked by the user using the Mark Cycle function.

Hardware Display Format

In the hardware display format, all valid opcode fetch bus cycles are disassembled and displayed. Noninstruction bus cycles are displayed with the appropriate Cycle Type label, as defined in Sections. There is no attempt to link operand reads and writes with the instructions which cause them. This is the default format for disassembly.

Sample	Address	High_Data	Low_Data	Mnemonic
.	.	.	.	.
100	00004000	. . . .	. . . .	b 0xA000
101	00004002	A000	. . . .	(EXTENSION)
102	00004004	. . . .	. . . .	(FLUSH)
103	0000A000	. . . .	. . . .	xor r0, r1, r2
104	0000A000	. . . .	. . . .	(EXTENSION)
105	. . . . .	. . . .	. . . .	(SDRAM ADDRESS)

In the hardware display format, the disassembler displays certain cycle-type labels in parentheses, see Table 2–5.

Table 2–5: Support cycle-type labels for sequences and definitions (for 8260ITR_60X).

Cycle type	Definition
(ADDRESS)	This indicates an Address cycle.
(UNASSOCIATED DATA)	This indicates that none of the pattern matches.
(FLUSH)*	This cycle was fetched but not executed.
(CACHE FILL)*	The processor only fetches to fill the cache line but is not executed.
(ADDRESS ONLY)*	This indicates that the transfer does not have any data sequences associated with it.
(EXTENSION)*	This cycle is an extension to a preceding instruction opcode.
(UNASSOCIATED ADDRESS)*	This indicates that the corresponding TS~ asserted sequence is not found in the acquisition.
(TRANSFER START)	This indicates that the corresponding TS~ is an asserted sequence.
(ALTERNATE MASTER CYCLE)	This indicates alternate Master Transactions.
(INTERNAL MEMORY CYCLE)	This indicates the Internal Memory Cycles.
(QUALIFIED BUS GRANT)	This indicates a Qualified Bus Grant has occurred.
(DIS-QUALIFIED BUS GRANT)	This indicates that the Bus Grant is not qualified.

* **Computed cycles types**

Table 2–6: Cycle-type labels for sequences and definitions for 8260ITR_SNG

Cycle type	Definition
(FLUSH)*	This indicates the cycle was fetched but not executed.
(CACHE FILL)*	The indicates the processor only fetches to fill the cache line but is not executed.
(EXTENSION)*	This indicates the cycle is an extension to a preceding instruction opcode.
(INTERNAL MEMORY CYCLE)	This indicates the Internal Memory Cycles.
(READ)	This indicates memory read cycles.
(WRITE)	This indicates memory write cycles.

Table 2–6: Cycle-type labels for sequences and definitions for 8260ITR_SNG (cont.)

Cycle type	Definition
(UNASSOCIATED DATA)	This indicates that the corresponding to this cycle is not associated to any address or cycle type.

* **Computed cycles types**

Figure 2–4 illustrates an example of the Hardware display.

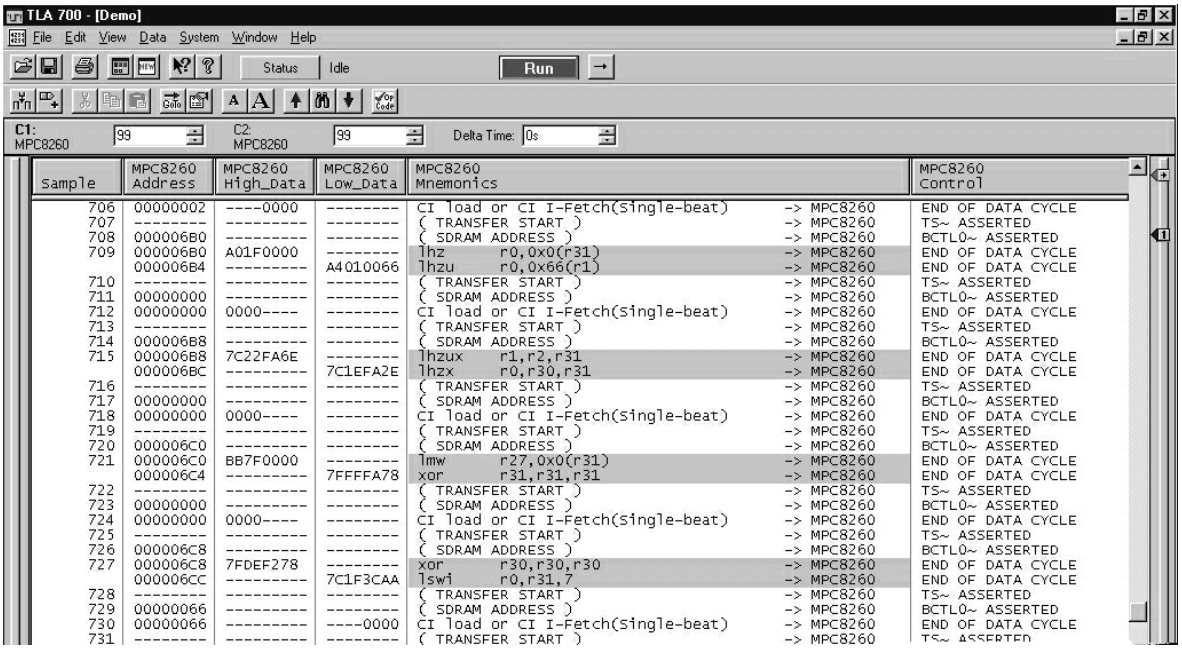


Figure 2–4: Example of the hardware display format

Software Display Format

In Software display format only the first opcode fetch of executed instruction cycles are displayed (read extensions are used to disassemble the instruction but are not displayed as separate cycles in Software mode). Non instruction bus cycles are not displayed in Software mode.

Note that any ”special” cycles that are described as appearing in Control Flow or Subroutine display formats also show up here.

Sample	Address	High_Data	Low_Data	Mnemonic
.	.	.	.	.
100	00009700	. . . .		add r0, r0, r1
104	0000A000	. . . .		xor r0, r1, r2
.	.	.	.	.

Control Flow Display Format

In Control Flow display format only the first opcode fetch of instructions which cause a branch in the addressing are displayed. Thus, branches not taken are not displayed.

If a conditional branch branches to an address that is reached sequentially, it may be impossible to determine if the branch was taken or not. In this instance, the branch is not displayed in the Control Flow display, and no flushing is done. Unconditional branches are always displayed whether or not the destination address is seen on the bus (although no flushing is done in that case).

The following MPC8260 microprocessor instructions unconditionally affect control flow and is always displayed:

b ba bl bla rfi sc

The following MPC8260 microprocessor instructions conditionally affect control flow and is always displayed:

bc bca bcl bcla bcctr
bcctrl bclr bclrl tw twi

Subroutine Display Format

The Subroutine display format displays only the first fetch of subroutine call and return instructions. It displays conditional subroutine calls if they are considered to be taken.

The following MPC8260ITR microprocessor instructions unconditionally affect subroutine display:

sc rfi

The following MPC8260ITR microprocessor instructions conditionally affect subroutine display:

tw twi

Changing How Data is Displayed

Common fields and features allow you to modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page.

You can make selections unique to the MPC8260ITR support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception cycles

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

Show:	Hardware	(default)
	Software	
	Control Flow	
	Subroutine	
Highlight:	Software	(default)
	Control Flow	
	Subroutine	
	None	
Disasm Across Gaps:	Yes	
	No	(default)

Micro Specific Fields

The Micro Specific Fields are for both the 8260ITR_60X and the 8260ITR_SNG supports unless specified otherwise.

Byte Order. Byte ordering is selected from one of the two available options.

Big Endian	(default)
PPC Little	

***NOTE**. When PPC Little is selected as the Byte Order, the Address column displays the physical address, whereas the TraceAddr column displays the Effective address.*

Bus Arbiter (8260ITR_60X Only). The bus arbiter has two selections available. Internal Arbiter is selected if the internal on-chip arbiter is used and External Arbiter is selected if an external bus arbiter is used.

Internal (default)
External

Exception Prefix. The valid exception prefix has two selections available. Choose one of the following options depending on the system being used.

000 (default)
FFF

Instruction Fetch Indicator. The instruction fetch indicator defaults to TC [0–2] bits, indicating that those bits are used for Fetch/Read identification. Otherwise, you can select the heuristic method to differentiate between the fetches and reads.

TC [0–2] bits (default)
By Heuristic Method

Trace Writes Address. This field contains the Trace Writes address in use. You need to enter the noncacheable address, and then the exception handler writes the target address.

First 64 Bit Area Low. This field is the lower address of the Memory map for the 64 bit port size.

0x00000000 (default)

First 64 Bit Area High. This field is the higher address of the memory map for the 64 bit port size.

0x00000000 (default)

Second 64 Bit Area Low. This field is the lower address of the Memory map for the 64 bit port size.

0x00000000 (default)

Second 64 Bit Area High. This field is the higher address of the memory map for the 64 bit port size.

0x00000000 (default)

Third 64 Bit Area Low. This field is the lower address of the Memory map for the 64 bit port size.

0x00000000 (default)

Third 64 Bit Area High. This field is the higher address of the memory map for the 64 bit port size.

0x00000000 (default)

Fourth 64 Bit Area Low. This field is the lower address of the Memory map for the 64 bit port size.

0x00000000 (default)

Fourth 64 Bit Area High. This field is the higher address of the memory map for the 64 bit port size.

0x00000000 (default)

***NOTE**. Four options are provided for the 64 bit region. These options are provided for boards having multiple memory ranges that are not joined for a single portwidth. If the board has two unjoined 64 bit regions, you must enter the lower and upper address for both regions for correct disassembly.*

First 32 Bit Area Low. This field is the lower address of the memory map for the 32 bit port size.

0x00000000 (default)

First 32 Bit Area High. The 32 Bit Area High is the higher address of the memory map of 32 bit port size.

0x00000000 (default)

Second 32 Bit Area Low. This field is the lower address of the memory map for the 32 bit port size.

0x00000000 (default)

Second 32 Bit Area High. The 32 Bit Area High is the higher address of the memory map of 32 bit port size.

0x00000000 (default)

***NOTE**. Two options are provided for the 32 bit region. These options are provided for boards with multiple memory ranges that are not joined for a single port width. If a board has two unjoined 32 bit regions, you must enter the lower and upper address for both regions for correct disassembly.*

16 Bit Area Low. The 16 Bit Area Low is the lower address of the memory map of 16 bit port size.

0x00000000 (default)

16 Bit Area High. The 16 Bit area High is the higher address of the memory map of 16 bit port size.

0x00000000 (default)

8 Bit Area Low. The 8 Bit Area Low is the lower address of the memory map of 8 bit port size.

0x00000000 (default)

8 Bit Area High. The 8 Bit area High is the higher address of the memory map of 8 bit port size.

0x00000000 (default)

Internal Memory Map Low. This field is the lower address of the reserved Internal Memory Space.

0x00000000 (default)

Internal Memory Map High. This field is the higher address of the reserved Internal Memory Space.

0x00000000 (default)

Memory Image Status. When you choose the Enabled option you can not edit or modify the S-Record (Image File currently in use). You must choose the Disabled option to edit or modify the S-record.

Enabled (Default)
Disabled

Disassemble Based On. This option allows you select the basis for disassembly. If you choose the option Fetch Stream, normal disassembly occurs. But when you select the Memory Image option disassembly is based on the image file. For example, S-record file.

Fetch Stream (default)
Memory Image

Image File Path. Enter the complete path to the S-record file in the property field for Image File Path (use the Browse button).

This is blank by default

Address Offset in Hex. This is the address offset (in hexadecimal) from the starting address (as indicated by the S-record) where the your program is loaded in memory.

0x00000000 (default)

For example, the linker output and the corresponding S-record file has a starting address of 0x0, but you loaded at a different address (0x50), and then you specified the offset –0x50 (0xFFFFFFB0) in this field.

- When the S-record address is less than the Processor_Address, then the Address_Offset is negative.
- When the S-record address is greater than the Processor_Address, then the Address_Offset is positive.

The outcome is: Processor_Address + Address_Offset == S_Record_Address

Maximum Instructions. Enter the number of instructions to be displayed (from the image file each time a BTE is encountered) in the property field for Maximum Instructions.

40 (default)

BCTL0~ Used As (8260ITR_SNG only). This disassembly option reflects the polarity of the signal BCTL0~. When the option W/R~ is chosen BCTL0~ indicates memory write when active high and memory read when active low. When the option R/W~ is chosen BCTL0~ indicates memory read when active high and memory write when active low.

W/R~ (Default)
R/W~

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it.

NOTE. *The* TMS562A *support only allows marking of instruction fetch cycles that also includes read extensions and flush cycles.*

The Mark Opcode function is not effective in Memory Image Mode.

Marks are placed by using the Mark Opcode button. The Mark Opcode button is always be available. If the sample being marked is not an address cycle or data cycle of the potential bus master, the Mark Opcode selections are replaced by a note indicating that an Opcode Mark cannot be placed at the selected data sample.

When a cycle is marked, the character, >>, is displayed immediately to the left of the Mnemonics column. Cycles can be unmarked using the Undo Mark selection, which removes the character >>.

Table 2–7 describes the mark selections available for instruction fetch cycles.

Table 2–7: Mark selections and definitions

Mark selection or combination	Definition
Opcode-Opcode	Marks the current cycle and the next cycle as an instruction opcode
Opcode-Flush	Marks the current cycle as an instruction opcode and flushes the next cycle
Flush-Opcode	Marks the current cycle as a flushed cycle and the next cycle as an instruction opcode
Flush-Flush	Marks the current and the next cycle as a flushed cycle
Opcode	Marks cycle as an instruction opcode
Flush	Marks cycle as a flushed cycle
Invalid Data	Marks the data as invalid
Undo Mark	Removes all marks from the current sequence

The Marks Opcode-Opcode, Opcode-Flush, Flush-Opcode, and Flush-Flush are available only to 64-bit data sequences.

The Mark Opcode is available only to 32/16/8-bit data sequences.

The Marks Invalid Data and Undo Mark are available to all data sequences.

Table 2–8 describes the mark selections available on a sequence which has the TS~ signal asserted..

Table 2–8: Marks available with TS~ asserted (for 8260ITR_60X only)

Mark selection or combination	Definition
Invalid TS~	Marks the current TS~ sequence as invalid
Instruction Fetch[1]	Treat the data associated with the TS~ sequence as fetches
Not an Instruction Fetch[1]	Treat the data associated with the TS~ sequence as non-fetch
Undo Mark	Removes all marks from the current sequence

[1] **Indicates that these cycle marks are available only when the Instruction Fetch Indicator is set to "By Heuristic Method" in the disassembly field selection.**

Displaying Exception Labels

The disassembler can display MPC8260ITR exception labels. The exception table must reside in external memory for interrupt and exception cycles to be visible to the disassembler.

Select the table prefix in the Exception Prefix field. The Exception Prefix field provides the disassembler with the prefix value. Select a three-digit hexadecimal value from the two values provided, corresponding to the prefix of the exception table. These fields are located in the Disassembly property page.

Table 2–9 lists the MPC8260ITR interrupt and exception labels.

Table 2–9: Interrupt and exception labels

Cycle type label	Definition
(SYSTEM RESET EXCEPTION)	Caused due to the assertion of SRESET~ or HRESET~.
(MACHINE CHECK EXCEPTION)	Caused by the assertion of TEA~ signal during a data bus transaction,assertion of MCP~ or an address or data parity error.
(DATA ACCESS EXCEPTION)	Generated when data translation is active and the desired access to the effective address is not permitted.
(INSTRUCTION ACCESS EXCEPTION)	Generated when instruction fetch cannot be performed due to: ■ effective address cannot be translated. (For example, there is a page fault.) ■ fetch access to a direct store segment. ■ fetch access violates memory protection.

Table 2–9: Interrupt and exception labels (cont.)

Cycle type label	Definition
(EXTERNAL INTERRUPT)	Generated when MSR[EE]=1 and the INT~ signal is asserted.
(ALIGNMENT EXCEPTION)	Caused when processor core cannot perform a memory access.
(PROGRAM EXCEPTION)	Attempted execution of illegal instructions, TRAP Instructions, privileged instruction in problem state.
(FLOATING-POINT UNAVAILABLE EXCEPTION)	This is not implemented in MPC8260.
(DECREMENTER EXCEPTION)	Occurs when the most significant bit of the decrementer (DEC) register transitions from 0 to 1.
(SYSTEM CALL EXCEPTION)	Occurs when a System call (SC) instruction is executed.
(TRACE EXCEPTION)	Occurs when MSR[SE]=1 or when the currently completing instruction is a branch and MSR[BE]=1.
(FLOATING-POINT ASSIST EXCEPTION)	Occurs when attempting to execute a floating-point arithmetic instruction.
(INSTRUCTION TRANSLATION MISS EXCEPTION)	Occurs when the effective address for an instruction fetch cannot be translated by the ITLB.
(DATA LOAD TRANSLATION MISS EXCEPTION)	Caused when the effective address for a data load operation cannot be translated by the DTLB.
(DATA STORE TRANSLATION MISS EXCEPTION)	Caused when the effective address for a data store operation cannot be translated by the DTLB or when DTLB hit occurs.
(INSTRUCTION ADDRESS BREAKPOINT EXCEPTION)	Occurs when the address (bits 0–29) in the IABR matches the next instruction to complete in the completion unit and the IABR bit 30 is set.
(SYSTEM MANAGEMENT INTERRUPT)	Occurs when MSR[EE]=1 and the SMI~ input signal is asserted.

These exception types are displayed in parentheses in the disassembly. The exception vector table must reside in external memory for the exception cycle to be visible to the disassembler.

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided on your MPC8260ITR software support disk so you can see an example of how your MPC8260ITR microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing

the module for use. You can view the system file without connecting the logic analyzer to your system under test.

Internal Trace Reconstruction (ITR)

The logic analyzer acquires data, which appears on the external bus of the microprocessor. When internal instruction cache is enabled, most of the instruction fetches happen from the cache for which no external bus activity occurs. This severely limits the information that a logic analyzer can display for the user. To address this problem, some indirect methods are used to logically track the program flow even though instruction fetches are happening from internal cache. A brief explanation follows with examples showing ways you can use the ITR method with this support.

It is possible to reconstruct the program execution. That is, the portions of the program, which get executed inside the cache, can be read from the Image file and shown on the display. This can occur if both an Image File of the program that is being executed is available externally (in S-record format for example), and if the processor provides information about the control flow instructions being executed and they can be acquired.

Memory Image (S-record)

The memory image is a hexadecimal form of the program being executed by the processor. It is the output of the Compiler/Assembler and Linker. Linker output is normally available in one of the industry standard formats like Intel Hex format, S-record format or a proprietary format used by the software development system. This support requires the external image file to be in the Motorola S-record format. Usually tools are available to convert proprietary output formats into Motorola S-record. You can use Green Hills software and SDS (Software Development Solutions) compiler for Embedded PCs to convert a source file into an S-record file (Image file). See *Viewing Cache Activity* in the following paragraph.

Image Reader

The Motorola MPC8260 processor provides a Branch Trace Exception (BTE). This particular exception is generated whenever change of control flow occurs, for example, whenever a branch instruction is encountered. The BTE feature is available in the processor and is used for collecting information about the program flow inside the cache. Whenever a change in control flow occurs, this BTE occurs, and this BTE provides the branch target address information. This BTE in conjunction with the external image file is used to display the cache activity. The TMS562A supports only the S-record format so it requires that the Image File be available in Motorola S-record format.

Viewing Cache Activity

This procedure (for converting a source file into an S-record file) uses Green Hills software and the SDS (Software Development Solutions) compiler for Embedded PCs. If you do not have this software, you need to find an alternative. Contact your Tektronix sales representative if you need support.

This section on viewing the cache activity on the Tektronix logic analyzer consists of a three-step procedure.

- Retrieving Control Flow information
- Generating an S-record file (Image file)
- Configuring the TLA (Tektronix Logic Analyzer)

Retrieving Control Flow Information. Follow this procedure to retrieve information about the Control Flow from the processor.

1. Enable the Branch Trace Exception bit of the Processor.

The “Branch Trace Enable (BTE)” bit is part of the Machine Status Register (MSR). On enabling this bit, we ensure that whenever a branch occurs in the program, a “Branch Trace Exception” is generated. This exception is used to discover that a branch instruction is executed and to make the target address available.

2. Write the exception handler routine.

Whenever a branch is encountered, the program flows to the exception handling routine, which for MPC8260ITR support is at 0xnnnn_nD00, where nnnn_n and 0xFFFFF or 0x00000 is based on the Exception Prefix (EP) bit setting of the MSR. You have to write your exception handler routine here. Following is an example code.

```
mfsrr0 r2    // r2 and r4 are assumed not to be modified by the
                          user's program. The user is advised to
                          use registers which are not used in
                          their main program.
xor r4,r4,r4
ori r4,Non-cacheable address // The user has to enter
                          the required non-cacheable
                          address.
stw r2,0x0(r4)rfi
```

The BTE handler for the MPC8260ITR support needs to provide the starting address to look at the code in the image file. This address is available as the “return address for the BTE / branch target address” in the register SRR0. The value of SRR0 is written onto a “Noncacheable region” of memory so that it appears on the external bus. The Image reader reads this value and uses this value to fill in the cache activity in display. In the above example code, the value of

SRR0 is moved to a register (R2) and this value is written onto a noncacheable region of the memory so that it is available on the external bus.

Generating an S-record file (Image file). The source code must be converted into an S-record format. Following are the steps to produce an S-record file from a source file using Green Hills software:

NOTE*. The file naming conventions that the Green Hills software follows are:*

- A source file has an extension '.s'
- An object file has an extension '.o'
- An elf file, for example the output of the linker, has the extension '.out'
- The Motorola S-records have an extension '.src'

1. Open the Green Hills Command Line
2. Create the object file (.o) using the following command:

   ```
   asppc -o objfile.o source.s
   ```

3. Create the elf file, for example an executable and linker file, using the linker command:

   ```
   lx –sec @sectionfile –o <outfile.out> <objfile.o>
   ```

4. To get an S-record file using this .out file, execute the following command at the prompt:

   ```
   elf2sr outfile.out –o srecord.src
   ```

This S-record file is used as the Image file in this support.

NOTE*. If you are using the Green Hills documentation for this compiler, refer to their documentation for further details about the commands.*

Configure the TLA. Follow these steps to configure your logic analyzer.

1. In the logic analyzer software, load the support package.
2. Click on Setup, then on Trigger. Set the trigger for the address xxxxxD00, which is the Exception handler routine address.
3. Modify the properties in the listing window of the logic analyzer as shown in Figure 2–5.

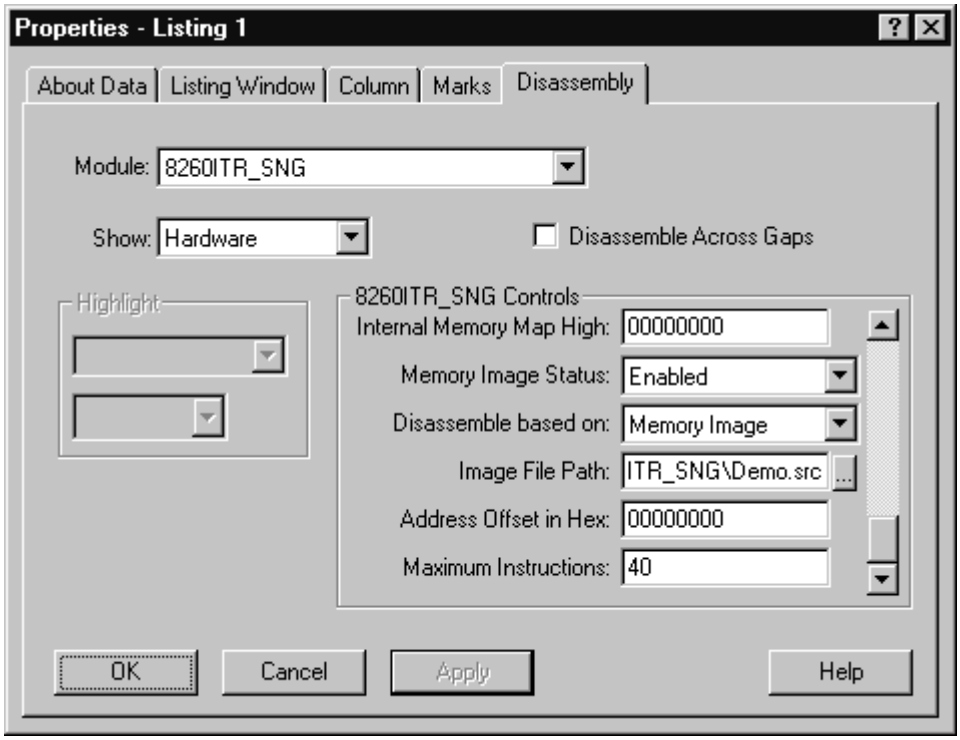


Figure 2–5: Listing window

a. Change the “Disassemble based on” property to “show Memory Image”.

b. Enter the noncacheable address used in the exception routine in the property Address for Trace Writes.

c. Enter the number of instructions displayed in the Maximum Instructions property. The default value is 40. This number is the maximum number of instructions that are taken from the image file to show each time a control flow change occurs.

The number of instructions displayed is limited by two conditions:

- Maximum instructions you entered.
- If another branch instruction is encountered in the Image file, the display is stopped.

That is, the Image reader displays instructions from the cache until the Maximum instructions entered by you are over or another branch instruction is encountered.

d. Enter the complete path to the S-record file / Image file in the property Image file path. This can be done either manually or by pressing the menu button to the right of the property for Image file path which opens up a “browse” window.

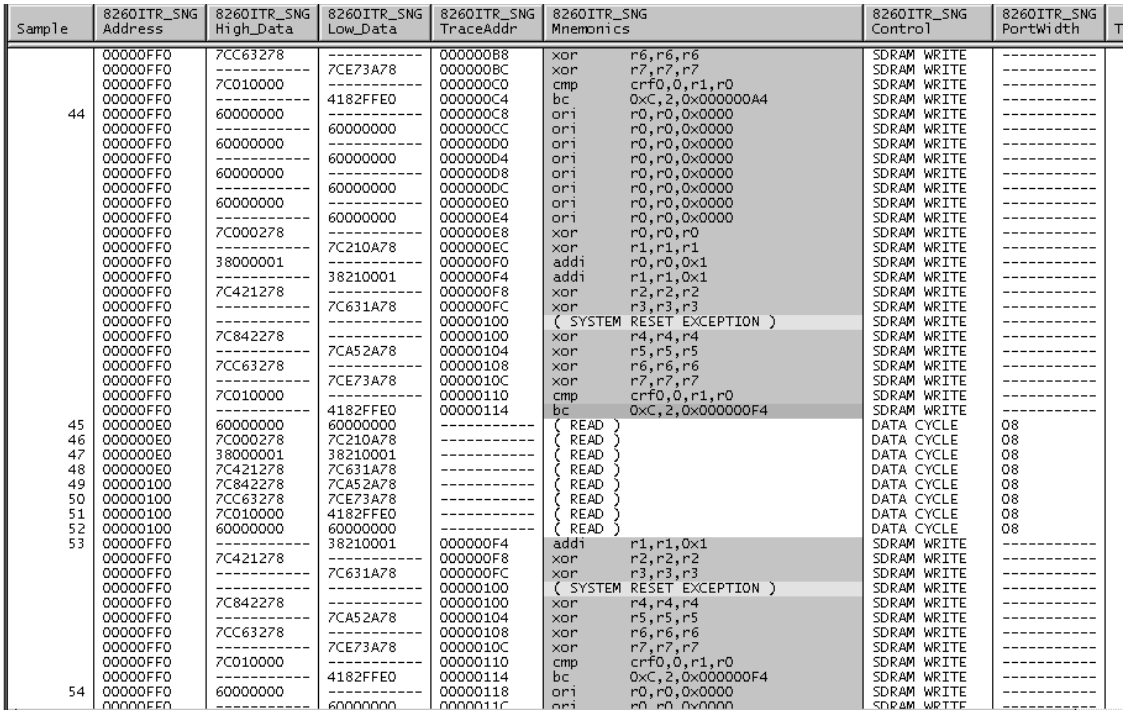
Once the above settings are done, select ok/apply to view the cache data on the display. To revert back to the original Fetch Stream data, change the value of the property “Disassemble based on” to “show Fetch Stream”. Following are sample screen shots for both options.

Figure 2–6 shows where the display is according to the normal fetch stream. The exception handler written makes the value of SRR0 appear on the bus thus enabling the Image reader to access the Image file.

Sample	8260ITR_SNG Address	8260ITR_SNG High_Data	8260ITR_SNG Low_Data	8260ITR_SNG TraceAddr	8260ITR_SNG Mnemonics	8260ITR_SNG Control	8260ITR_SNG PortWidth
1	00000008	7C421278	----------	00000008	xor r2,r2,r2	DATA CYCLE	08
	0000000C	----------	7C631A78	0000000C	xor r3,r3,r3	DATA CYCLE	08
2	00000010	7C842278	----------	00000010	xor r4,r4,r4	DATA CYCLE	08
	00000014	----------	60630800	00000014	ori r3,r3,0x0800	DATA CYCLE	08
3	00000018	80230003	----------	00000018	lwz r1,0x3(r3)	DATA CYCLE	08
	0000001C	----------	60420900	0000001C	ori r2,r2,0x0900	DATA CYCLE	08
4	00000803	------00	00000000	----------	(READ)	DATA CYCLE	08
5	00000020	80220001	----------	00000020	lwz r1,0x1(r2)	DATA CYCLE	08
	00000024	----------	60000000	00000024	ori r0,r0,0x0000	DATA CYCLE	08
6	00000028	90230005	----------	00000028	stw r1,0x5(r3)	DATA CYCLE	08
	0000002C	----------	48000052	0000002C	ba 0x00000050	DATA CYCLE	08
7	00000030	60000000	----------	00000030	(FLUSH)	DATA CYCLE	08
	00000034	----------	60000000	00000034	(FLUSH)	DATA CYCLE	08
8	00000038	00000000	----------	00000038	(FLUSH)	DATA CYCLE	08
	0000003C	----------	00000000	0000003C	(FLUSH)	DATA CYCLE	08
9	00000804	----------	00000000	----------	(READ)	DATA CYCLE	08
10	00000901	--000000	00000000	----------	(READ)	DATA CYCLE	08
11	00000904	----------	00000000	----------	(READ)	DATA CYCLE	08
12	00000805	----------	--000000	----------	(WRITE)	SDRAM WRITE	08
13	00000808	007FA062	60000000	----------	(WRITE)	SDRAM WRITE	08
14	00000050	7C000278	----------	00000050	xor r0,r0,r0	DATA CYCLE	08
	00000054	----------	7C210A78	00000054	xor r1,r1,r1	DATA CYCLE	08
15	00000058	7C421278	----------	00000058	xor r2,r2,r2	DATA CYCLE	08
	0000005C	----------	7C631A78	0000005C	xor r3,r3,r3	DATA CYCLE	08
16	00000040	----------	----------	00000040	(CACHE FILL)	DATA CYCLE	08
	00000044	----------	----------	00000044	(CACHE FILL)	DATA CYCLE	08
17	00000048	----------	----------	00000048	(CACHE FILL)	DATA CYCLE	08
	0000004C	----------	----------	0000004C	(CACHE FILL)	DATA CYCLE	08
18	00000D00	----------	----------	----------	(TRACE EXCEPTION)	DATA CYCLE	08
	00000D00	7FFA02A6	----------	00000D00	mfspr r31,SRR0	DATA CYCLE	08
	00000D04	----------	7D084278	00000D04	xor r8,r8,r8	DATA CYCLE	08
19	00000D08	7D294A78	----------	00000D08	xor r9,r9,r9	DATA CYCLE	08
	00000D0C	----------	93E80FF0	00000D0C	stw r31,0xFF0(r8)	DATA CYCLE	08
20	00000D10	60000000	----------	00000D10	ori r0,r0,0x0000	DATA CYCLE	08
	00000D14	----------	4C000064	00000D14	rfi	DATA CYCLE	08
21	00000D18	60000000	----------	00000D18	(FLUSH)	DATA CYCLE	08
	00000D1C	----------	60000000	00000D1C	(FLUSH)	DATA CYCLE	08
22	00000FF0	00000050	60000000	----------	(WRITE)	SDRAM WRITE	08
23	00000D20	60000000	----------	00000D20	(FLUSH)	DATA CYCLE	08
	00000D24	----------	60000000	00000D24	(FLUSH)	DATA CYCLE	08
24	00000D28	60000000	----------	00000D28	(FLUSH)	DATA CYCLE	08
	00000D2C	----------	60000000	00000D2C	(FLUSH)	DATA CYCLE	08
25	00000D30	60000000	----------	00000D30	(FLUSH)	DATA CYCLE	08
	00000D34	----------	60000000	00000D34	(FLUSH)	DATA CYCLE	08
26	00000D38	60000000	----------	00000D38	(FLUSH)	DATA CYCLE	08

Figure 2–6: Display showing Fetch Stream

Figure 2–7 shows where the Memory Image property is enabled. In this case, the fetch stream is not disassembled and is shown as “Instruction from fetch”.



Sample	8260ITR_SNG Address	8260ITR_SNG High_Data	8260ITR_SNG Low_Data	8260ITR_SNG TraceAddr	8260ITR_SNG Mnemonics	8260ITR_SNG Control	8260ITR_SNG PortWidth
	00000FF0	7CC63278	----------	000000B8	xor r6,r6,r6	SDRAM WRITE	----------
	00000FF0	----------	7CE73A78	000000BC	xor r7,r7,r7	SDRAM WRITE	----------
	00000FF0	7C010000	----------	000000C0	cmp crf0,0,r1,r0	SDRAM WRITE	----------
	00000FF0	----------	4182FFE0	000000C4	bc 0xC,2,0x000000A4	SDRAM WRITE	----------
44	00000FF0	60000000	----------	000000C8	ori r0,r0,0x0000	SDRAM WRITE	----------
	00000FF0	----------	60000000	000000CC	ori r0,r0,0x0000	SDRAM WRITE	----------
	00000FF0	60000000	----------	000000D0	ori r0,r0,0x0000	SDRAM WRITE	----------
	00000FF0	----------	60000000	000000D4	ori r0,r0,0x0000	SDRAM WRITE	----------
	00000FF0	60000000	----------	000000D8	ori r0,r0,0x0000	SDRAM WRITE	----------
	00000FF0	----------	60000000	000000DC	ori r0,r0,0x0000	SDRAM WRITE	----------
	00000FF0	60000000	----------	000000E0	ori r0,r0,0x0000	SDRAM WRITE	----------
	00000FF0	----------	60000000	000000E4	ori r0,r0,0x0000	SDRAM WRITE	----------
	00000FF0	7C000278	----------	000000E8	xor r0,r0,r0	SDRAM WRITE	----------
	00000FF0	----------	7C210A78	000000EC	xor r1,r1,r1	SDRAM WRITE	----------
	00000FF0	38000001	----------	000000F0	addi r0,r0,0x1	SDRAM WRITE	----------
	00000FF0	----------	38210001	000000F4	addi r1,r1,0x1	SDRAM WRITE	----------
	00000FF0	7C421278	----------	000000F8	xor r2,r2,r2	SDRAM WRITE	----------
	00000FF0	----------	7C631A78	000000FC	xor r3,r3,r3	SDRAM WRITE	----------
	00000FF0	----------	----------	00000100	(SYSTEM RESET EXCEPTION)	SDRAM WRITE	----------
	00000FF0	7C842278	----------	00000100	xor r4,r4,r4	SDRAM WRITE	----------
	00000FF0	----------	7CA52A78	00000104	xor r5,r5,r5	SDRAM WRITE	----------
	00000FF0	7CC63278	----------	00000108	xor r6,r6,r6	SDRAM WRITE	----------
	00000FF0	----------	7CE73A78	0000010C	xor r7,r7,r7	SDRAM WRITE	----------
	00000FF0	7C010000	----------	00000110	cmp crf0,0,r1,r0	SDRAM WRITE	----------
	00000FF0	----------	4182FFE0	00000114	bc 0xC,2,0x000000F4	SDRAM WRITE	----------
45	000000E0	60000000	60000000	----------	(READ)	DATA CYCLE	08
46	000000E0	7C000278	7C210A78	----------	(READ)	DATA CYCLE	08
47	000000E0	38000001	38210001	----------	(READ)	DATA CYCLE	08
48	000000E0	7C421278	7C631A78	----------	(READ)	DATA CYCLE	08
49	00000100	7C842278	7CA52A78	----------	(READ)	DATA CYCLE	08
50	00000100	7CC63278	7CE73A78	----------	(READ)	DATA CYCLE	08
51	00000100	7C010000	4182FFE0	----------	(READ)	DATA CYCLE	08
52	00000100	60000000	60000000	----------	(READ)	DATA CYCLE	08
53	00000FF0	----------	38210001	000000F4	addi r1,r1,0x1	SDRAM WRITE	----------
	00000FF0	7C421278	----------	000000F8	xor r2,r2,r2	SDRAM WRITE	----------
	00000FF0	----------	7C631A78	000000FC	xor r3,r3,r3	SDRAM WRITE	----------
	00000FF0	----------	----------	00000100	(SYSTEM RESET EXCEPTION)	SDRAM WRITE	----------
	00000FF0	7C842278	----------	00000100	xor r4,r4,r4	SDRAM WRITE	----------
	00000FF0	----------	7CA52A78	00000104	xor r5,r5,r5	SDRAM WRITE	----------
	00000FF0	7CC63278	----------	00000108	xor r6,r6,r6	SDRAM WRITE	----------
	00000FF0	----------	7CE73A78	0000010C	xor r7,r7,r7	SDRAM WRITE	----------
	00000FF0	7C010000	----------	00000110	cmp crf0,0,r1,r0	SDRAM WRITE	----------
	00000FF0	----------	4182FFE0	00000114	bc 0xC,2,0x000000F4	SDRAM WRITE	----------
54	00000FF0	60000000	----------	00000118	ori r0,r0,0x0000	SDRAM WRITE	----------
	00000FF0	----------	60000000	0000011C	ori r0,r0,0x0000	SDRAM WRITE	----------

Figure 2–7: Display showing Memory Image

Error messages specific to the ITR support. The following are the error messages, which are relevant to the ITR support.

1. *** S–Record: File path too long ***
2. *** S–Record: Not a valid file ***
3. *** S–Record: File open failed (bad path?) ***
4. *** S–Record: Non–hexadecimal digit ***
5. *** S–Record: File operation failure(s) ***
6. *** S–Record: No or incomplete associated image bytes ***
7. *** S–Record: Null character in file ***
8. *** S–Record: Line too long ***
9. *** S–Record: Start of line is bad ***
10. *** S–Record: Length field is too small ***
11. *** S–Record: Non–digit type character ***
12. *** S–Record: Address space wrapping not supported ***
13. *** S–Record: Internal problem, mixed endian layouts not supported ***
14. *** S–Record: Unable to allocate sufficient memory ***

15. *** S–Record: Internal problem, too many bytes requested at once ***
16. *** S–Record: Internal problem, region vs. content mismatch ***
17. *** S–Record: Internal problem, invalid cache entry accessed ***
18. *** S–Record: Internal problem, bad start region ***
19. *** Memory Image Disabled ***

NOTE. *Error message 19 is displayed when the option Disabled is selected for the Memory Image Status field.*

Specifications

Specifications

This section contains information regarding the specifications of the TMS562A support.

Specification Tables

Table 3–1 lists the electrical requirements the system under test must produce for the support to acquire correct data.

Table 3–1: Electrical specifications

Characteristics	Requirements
SUT clock rate	
MPC8260ITR specified clock rate	Max 66 MHz
MPC8260ITR tested clock rate	Max 66 MHz
Minimum setup time required	
TLA 700	2.5 ns
Minimum hold time required	
TLA 700	0 ns

Replaceable Parts List

Replaceable Parts List

This section contains a list of the replaceable components for the TMS562A hardware support product.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Using the Replaceable Parts List

The tabular information in the Replaceable Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2548	XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON, OR 97005

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
	071-0798-00			1	MANUAL,TECH:INSTRUCTION,MPC8260_ITR SUPPORT,TMS562A, DP	TK2548	071-0798-00

Reference

Reference: Tables

This section lists the Symbol tables and the Channel group tables for disassembly and timing.

Symbol Tables

Table 5–1 lists the name, bit pattern, and meaning for the symbols in the file 8260ITR_60X_Ctrl, the Control channel group symbol table.

Table 5–1: 8260ITR_60X _Ctrl group symbol table definitions

Symbol	Control group value				Meaning
	TS~	ALE PSDVAL~ BG~ AACK~ DBG~	ABB~/IRQ2~ ARTRY~ DBB~/IRQ3~	BCTL0~ TA~ PSDWE TEA~	
TRANSFER START	0	XXXXX	XXX	XXXX	#TS~ signal asserted
BUS GRANT	X	XX0XX	XXX	XXXX	#BG~ signal asserted
DATA CYCLE	X	00XXX	XXX	XXXX	#PSDVAL~ signal asserted
END OF DATA CYCLE	X	XXXXX	XXX	X0XX	#TA~ signal asserted
ADDRESS ACKNOWLEDGE	X	XXX0X	XXX	XXXX	#AACK~ signal asserted
ADDRESS RETRY	X	XXXXX	X0X	XXXX	#ARTRY~ signal asserted
DATA BUS GRANT	X	XXXX0	XXX	XXXX	#DBG~ signal asserted
ADDRESS BUS BUSY	X	XXXXX	0XX	XXXX	#ABB~/IRQ2~ asserted
DATA BUS BUSY	X	XXXXX	XX0	XXXX	#DBB~/IRQ3~ asserted

Table 5–2 lists the name, bit pattern, and meaning for the symbols in the file 8260ITR_SNG _Ctrl, the Control channel group symbol table.

Table 5–2: 8260ITR_SNG Ctrl group symbol table definitions

Symbol	Control group value PSDVAL~ POE~/PSDRAS~/PGPL2 PSDCAS~/PGPL3 BCTL0~ PSDWE~/PGPL1	Meaning
SDRAM WRITE	X X X X 0	PSDWE~/PGPL1 signal asserted
DATA CYCLE	0 X X X X	PSDVAL~ signal asserted

Table 5–3 lists the name, bit pattern, and meaning for the symbols in the file 8260ITR_60X _Tsiz, the Tsize channel group symbol table.

Table 5–3: 8260ITR_60X _Tsiz group symbol table definitions

Symbol	Tsize group value TSIZ0 TSIZ1 TSIZ2 TBST~ TSIZ3	Meaning
BYTE	1 0 0 0 1	Byte
HALF WORD	1 0 0 1 0	Half Word
THREE BYTES	1 0 0 1 1	Three Bytes
WORD	1 0 1 0 0	Word
EXTENDED 5 BYTES	1 0 1 0 1	Extended 5 Bytes
EXTENDED 6 BYTES	1 0 1 1 0	Extended 6 Bytes
EXTENDED 7 BYTES	1 0 1 1 1	Extended 7 Bytes
DOUBLE WORD	1 0 0 0 0	Double Word
EXTENDED DOUBLE DOUBLE WORD	1 1 0 0 1	Extended Double Double Word
EXTENDED TRIPLE DOUBLE WORD	1 1 0 1 0	Extended Triple Double Word
QUAD DOUBLE WORD	0 0 0 1 0	Quad Double Word
UNKNOWN	X X X X X	Unknown

Table 5–4 lists the name, bit pattern, and meaning for the symbols in the file 8260ITR_60X _Tc, the TC channel group symbol table.

Table 5–4: 8260ITR_60X _Tc group symbol table definitions

Symbol	TC group value BNKSEL0/TC0/AP1/MODCK1~ BNKSEL1/TC1/AP2/MODCK2~ BNKSEL2/TC2/AP3/MODCK3~	Meaning
CORE DATA TRANSACTION / WRITE	0 0 0	Core Data Transaction / Write
CORE TOUCH LOAD	0 0 1	Core Touch Load
CORE INSTRUCTION FETCH	0 1 0	Core Instruction Fetch
RESERVED	0 1 1	Reserved
RESERVED	1 0 0	Reserved
RESERVED	1 0 1	Reserved
DMA FUNCTION CODE 0	1 1 0	Dma Function Code 0
DMA FUNCTION CODE 1	1 1 1	Dma Function Code 1

Channel Assignments

Channel assignments listed in Tables 5–5 through 5–20 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are listed starting with the most significant bit (MSB), descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde symbol (~) following a signal name indicates an active low signal.
- An equals symbol (=) following a signal name indicates that it is double probed.
- The module in the lower-numbered slot is referred to as the Master module and the module in the higher-numbered slot is referred to as the Slave module.

  The portable logic analyzer has the lower-numbered slots on the top, and the benchtop logic analyzer has the lower-numbered slots on the left.

The channel assignment groups are displayed in the following order:

8260ITR_SNG support	**Default display radix**
Address	Hexadecimal
High_Data	Hexadecimal
Low_Data	Hexadecimal
TraceAddr	Hexadecimal (Synthesized Group)
Mnemonics	None (Disassembly text generated by PDL)
Control	Symbol
PortWidth	Hexadecimal (Synthesized Group)
Misc	OFF

See page 5–15 for 8260ITR_SNG Channel Group Assignment tables.

8260ITR_60X support	**Default display radix**
Address	Hexadecimal
High_Data	Hexadecimal
Low_Data	Hexadecimal
Trace Address	Hexadecimal (Synthesized group)
Mnemonic	None (Disassembly text generated by PDL)
Control	Symbolic
Tsize	Symbolic
TransferType	Hexadecimal
TC	Hexadecimal
Misc	OFF

8260ITR_60X Channel Group Assignments

Table 5–5 lists the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, the Data channel group assignments are displayed in hexadecimal.

Table 5–5: Address channel group assignments for 8260ITR_60X

Bit order	LA channel	8260ITR_60X signal name
31	A3:7	A0
30	A3:6	A1
29	A3:5	A2
28	A3:4	A3
27	A3:3	A4
26	A3:2	A5
25	A3:1	A6
24	A3:0	A7
23	A2:7	A8
22	A2:6	A9
21	A2:5	A10
20	A2:4	A11
19	A2:3	A12
18	A2:2	A13
17	A2:1	A14
16	A2:0	A15
15	A1:7	A16
14	A1:6	A17
13	A1:5	A18
12	A1:4	A19
11	A1:3	A20
10	A1:2	A21
9	A1:1	A22
8	A1:0	A23
7	A0:7	A24
6	A0:6	A25
5	A0:5	A26
4	A0:4	BADDR27
3	A0:3	BADDR28

Table 5–5: Address channel group assignments for 8260ITR_60X (cont.)

Bit order	LA channel	8260ITR_60X signal name
2	A0:2	BADDR29
1	A0:1	BADDR30
0	A0:0	BADDR31

TraceAddr group Assignments. The TraceAddr group is used for tracking the program flow when the cache is enabled. The default radix for this group is OFF.

The TraceAddr group is a synthesized group. The TraceAddr group uses the "Trace Write Address" values in the disassembly option to trace the writes to noncacheable regions which are used for reading Memory Image.

1. Enter the "Trace Write Address" value in the disassembly option field.
2. Enable the Branch Trace Exception by setting the BE field in the MSR of the MPC8260 support.

   When the Branch Trace Exception subroutine is encountered, the SRR0 register contains the target address of the branch that was just executed.
3. In the Trace Exception subroutine, you need to write the value stored in the SRR0 register into the noncacheable region of the "Trace Write Address" field. The SRR0 value needs to be a 32 bit write since the address is 32 bits.

Once you have entered the SRR0 value, the TraceAddr field then contains the value of the written data that points to the target of the branch instruction. When reading from the Memory Image starts, the TraceAddr field then contains the address to be traced from the Memory Image.

NOTE. The Trace Write Address must be word aligned.

Table 5–6 lists the probe section and channel assignments for the High_Data group and the microprocessor signal to which each channel connects. By default, the High_Data channel group assignments are displayed in hexadecimal.

Table 5–6: High_Data channel group assignments for 8260ITR_60X

Bit order	LA channel	8260ITR_60X signal name
31	E3:7	D0
30	E3:6	D1
29	E3:5	D2
28	E3:4	D3

Table 5–6: High_Data channel group assignments for 8260ITR_60X (cont.)

Bit order	LA channel	8260ITR_60X signal name
27	E3:3	D4
26	E3:2	D5
25	E3:1	D6
24	E3:0	D7
23	E2:7	D8
22	E2:6	D9
21	E2:5	D10
20	E2:4	D11
19	E2:3	D12
18	E2:2	D13
17	E2:1	D14
16	E2:0	D15
15	E1:7	D16
14	E1:6	D17
13	E1:5	D18
12	E1:4	D19
11	E1:3	D20
10	E1:2	D21
9	E1:1	D22
8	E1:0	D23
7	E0:7	D24
6	E0:6	D25
5	E0:5	D26
4	E0:4	D27
3	E0:3	D28
2	E0:2	D29
1	E0:1	D30
0	E0:0	D31

Table 5–7 lists the probe section and channel assignments for the Low_Data group and the microprocessor signal to which each channel connects. By default, the Low_Data channel group assignments are displayed in hexadecimal.

Table 5–7: Low_Data channel group assignments for 8260ITR_60X

Bit order	LA channel	8260ITR_60X signal name
31	D3:7	D32
30	D3:6	D33
29	D3:5	D34
28	D3:4	D35
27	D3:3	D36
26	D3:2	D37
25	D3:1	D38
24	D3:0	D39
23	D2:7	D40
22	D2:6	D41
21	D2:5	D42
20	D2:4	D43
19	D2:3	D44
18	D2:2	D45
17	D2:1	D46
16	D2:0	D47
15	D1:7	D48
14	D1:6	D49
13	D1:5	D50
12	D1:4	D51
11	D1:3	D52
10	D1:2	D53
9	D1:1	D54
8	D1:0	D55
7	D0:7	D56
6	D0:6	D57
5	D0:5	D58
4	D0:4	D59
3	D0:3	D60

Table 5–7: Low_Data channel group assignments for 8260ITR_60X (cont.)

Bit order	LA channel	8260ITR_60X signal name
2	D0:2	D61
1	D0:1	D62
0	D0:0	D63

Table 5–8 lists the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. The default radix of the Control group is SYMBOLIC on the logic analyzer. The symbol table file name is 8260ITR_60X_Ctrl on the logic analyzer.

Table 5–8: Control channel group assignments for 8260ITR_60X

Bit order	LA channel	8260ITR_60X signal name
12	CLK:3	TS~
11	C2:3	ALE
10	CLK:0	PSDVAL~
9	C2:1	BG~
8	C2:0	AACK~
7	C2:2	DBG~
6	C3:6	ABB~/IRQ2~
5	C1:6	ARTRY~
4	C2:7	DBB~/IRQ3~
3	C3:7	BCTL0~
2	C0:3	TA~
1	C3:5	PSDWE~/PGPL1
0	C0:2	TEA~

Table 5–9 lists the probe section and channel assignments for the Tsize group and the microprocessor signal to which each channel connects. The default radix of the Control group is SYMBOLIC on the logic analyzer. The symbol table file name is 8260ITR_60X_Tsiz on the logic analyzer.

Table 5–9: Tsize channel group assignments for 8260ITR_60X

Bit order	LA channel	8260ITR_60X signal name
4	C1:7	TBST~
3	C1:4	TSIZ0
2	C1:3	TSIZ1
1	C1:2	TSIZ2
0	C1:1	TSIZ3

Table 5–10 lists the probe section and channel assignments for the TransferType group and the microprocessor signal to which each channel connects. By default, the TransferType channel group assignments are displayed in hexadecimal.

Table 5–10: TransferType channel group assignments for 8260ITR_60X

Bit order	LA channel	8260ITR_60X signal name
4	C1:0	TT0
3	C0:7	TT1
2	C0:6	TT2
1	C0:5	TT3
0	C0:4	TT4

Table 5–11 lists the probe section and channel assignments for the TC group and the microprocessor signal to which each channel connects. By default, the TC channel group assignments are displayed in hexadecimal.

Table 5–11: TC channel group assignments for 8260ITR_60X

Bit order	LA channel	8260ITR_60X signal name
2	C0:1	BNKSEL0/TC0/AP1/MODCK1~
1	C0:0	BNKSEL1/TC1/AP2/MODCK2~
0	C2:6	BNKSEL2/TC2/AP3/MODCK3~

Table 5–12 lists the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, the Misc channel group assignments are not displayed.

Table 5–12: Misc channel group assignments for 8260ITR_60X

Bit order	LA channel	8260ITR_60X signal name
9	CLK:1	CLKIN
8	C3:1	PSDA10/PGPL0
7	C3:3	HRESET~
6	C3:0	SRESET~
5	C2:5	PSDAMUX/PGPL5
4	C2:4	L2_HIT~/IRQ4~
3	CLK:2	CS3~
2	QUAL_2	CS1~
1	QUAL_3	CS0~
0	C3:2	BR~

Table 5–13 lists the probe section and clock and qualifier channel assignments. The clock probes are not part of any group.

Table 5–13: Clock and Qualifier channel assignments for 8260ITR_60X

LA channel	8260ITR_60X signal name
CLK:0	PSDVAL~
CLK:1	CLKIN as clock
CLK:2	CS3~
CLK:3	TS~
C2:0	AACK~
C2:1	BG~
C2:2	DBG~
C2:3	ALE
QUAL:0	CS2~
QUAL:1	Not connected
QUAL:2	CS1~
QUAL:3	CS0~

Acquisition Setup. The TMS562A support affects the logic analyzer setup menus (and submenus) by modifying existing fields and adding micro-specific fields.

The TMS562A support adds the selection 8260ITR_60X and 8260ITR_SNG to the Load Support Package dialog box, under the File pulldown menu. Once the 8260ITR_60X and 8260ITR_SNG supports are loaded, the Custom clocking mode selection in the module Setup menu is also enabled.

Table 5–14 lists the 8260ITR_60X signals required for clocking and disassembly.

Table 5–14: Signals required for clocking and disassembly for 8260ITR_60X

MPC8260ITR signal name	Channel name
A0 – A26, BADDR27 – BADDR31	A0:0–7
(Address Group)	A1:0–7
–	A2:0–7
–	A3:0–7
–	–
D0–D63	E0:0–7
(High_Data & Low_Data Groups)	E1:0–7
–	E2:0–7
–	E3:0–7
–	D0:0–7
–	D1:0–7
–	D2:0–7
–	D3:0–7
CLKIN	CLK:1
TS~	CLK:3
ALE	C2:3
PSDVAL~	CLK:0
BG~	C2:1
BR~	C3:2
DBG~	C2:2
ARTRY~	C1:6
AACK~	C2:0
TBST~	C1:7
TSIZ0	C1:4
TSIZ1	C1:3
TSIZ2	C1:2
TSIZ3	C1:1
TT0	C1:0

Table 5–14: Signals required for clocking and disassembly for 8260ITR_60X (cont.)

MPC8260ITR signal name	Channel name
TT1	C0:7
TT2	C0:6
TT3	C0:5
TT4	C0:4
DBB~/IRQ3~	C2:7
ABB~/IRQ2~	C3:6
TEA~	C0:2
TA~	C0:3
BNKSEL0/TC0/AP1/MODCK1~	C0:1
BNKSEL1/TC1/AP2/MODCK2~	C0:0
BNKSEL2/TC2/AP3/MODCK3~	C2:6

Table 5–15 lists the signals not required for clocking and disassembly.

Table 5–15: Signals not required for clocking and disassembly for 8260ITR_60X

Signal name	Channel name
CS3~	CLOCK:2
CS2~	QUAL:0
No Connection	QUAL:1
CS1~	QUAL:2
CS0~	QUAL:3
BCTL0~	C3:7
HRESET~	C3:3
SRESET~	C3:0
PSDA10/PGPL0	C3:1
PSDWE~/PGPL1	C3:5
PSDAMUX/PGPL5	C2:5
L2_HIT~/IRQ4~	C2:4

8260ITR_SNG Channel Group Assignments

Table 5–16 lists the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, the Address channel group assignments are displayed in hexadecimal.

Table 5–16: Address channel group assignments for 8260ITR_SNG

Bit order	LA channel	8260ITR_SNG signal name
31	A3:7	A0
30	A3:6	A1
29	A3:5	A2
28	A3:4	A3
27	A3:3	A4
26	A3:2	A5
25	A3:1	A6
24	A3:0	A7
23	A2:7	A8
22	A2:6	A9
21	A2:5	A10
20	A2:4	A11
19	A2:3	A12
18	A2:2	A13
17	A2:1	A14
16	A2:0	A15
15	A1:7	A16
14	A1:6	A17
13	A1:5	A18
12	A1:4	A19
11	A1:3	A20
10	A1:2	A21
9	A1:1	A22
8	A1:0	A23
7	A0:7	A24
6	A0:6	A25
5	A0:5	A26
4	A0:4	A27

Table 5–16: Address channel group assignments for 8260ITR_SNG (cont.)

Bit order	LA channel	8260ITR_SNG signal name
3	A0:3	A28
2	A0:2	A29
1	A0:1	A30
0	A0:0	A31

TraceAddr Group Assignments. The TraceAddr group is used for tracking the program flow when the cache is enabled. The default radix for this group is OFF. The TraceAddr group is a synthesized group. The TraceAddr group uses the "Trace Write Address" values in the disassembly option to trace the writes to noncacheable regions that are used for reading Memory Image.

1. Enter the "Trace Write Address" value in the disassembly option field.
2. Enable the Branch Trace Exception by setting the BE field in the MSR of the MPC8260 support. When the Branch Trace Exception subroutine is encountered, the SRR0 register contains the target address of the branch that was just executed.
3. In the Trace Exception subroutine, you need to write the value stored in the SRR0 register into the noncacheable region of the "Trace Write Address" field. The SRR0 value needs to be a 32 bit write since the address is 32 bits. Once you have entered the SRR0 value, the TraceAddr field then contains the value of the written data that points to the target of the branch instruction. When reading from the Memory Image starts, the TraceAddr field then contains the address to be traced from the Memory Image.

Table 5–17 lists the probe section and channel assignments for the High_Data group and the microprocessor signal to which each channel connects. By default, the High_Data channel group assignments are displayed in hexadecimal.

NOTE. The Trace Write Address must be word aligned.

Table 5–17: High_Data channel group assignments for 8260ITR_SNG

Bit order	LA channel	8260ITR_SNG signal name
31	E3:7	D0
30	E3:6	D1

Table 5–17: High_Data channel group assignments for 8260ITR_SNG (cont.)

Bit order	LA channel	8260ITR_SNG signal name
29	E3:5	D2
28	E3:4	D3
27	E3:3	D4
26	E3:2	D5
25	E3:1	D6
24	E3:0	D7
23	E2:7	D8
22	E2:6	D9
21	E2:5	D10
20	E2:4	D11
19	E2:3	D12
18	E2:2	D13
17	E2:1	D14
16	E2:0	D15
15	E1:7	D16
14	E1:6	D17
13	E1:5	D18
12	E1:4	D19
11	E1:3	D20
10	E1:2	D21
9	E1:1	D22
8	E1:0	D23
7	E0:7	D24
6	E0:6	D25
5	E0:5	D26
4	E0:4	D27
3	E0:3	D28
2	E0:2	D29
1	E0:1	D30
0	E0:0	D31

Table 5–18 lists the probe section and channel assignments for the Low_Data group and the microprocessor signal to which each channel connects. By default, the Low_Data channel group assignments are displayed in hexadecimal.

Table 5–18: Low_Data channel group assignments for 8260ITR_SNG

Bit order	LA channel	8260ITR_SNG signal name
31	D3:7	D32
30	D3:6	D33
29	D3:5	D34
28	D3:4	D35
27	D3:3	D36
26	D3:2	D37
25	D3:1	D38
24	D3:0	D39
23	D2:7	D40
22	D2:6	D41
21	D2:5	D42
20	D2:4	D43
19	D2:3	D44
18	D2:2	D45
17	D2:1	D46
16	D2:0	D47
15	D1:7	D48
14	D1:6	D49
13	D1:5	D50
12	D1:4	D51
11	D1:3	D52
10	D1:2	D53
9	D1:1	D54
8	D1:0	D55
7	D0:7	D56
6	D0:6	D57
5	D0:5	D58
4	D0:4	D59

Table 5–18: Low_Data channel group assignments for 8260ITR_SNG (cont.)

Bit order	LA channel	8260ITR_SNG signal name
3	D0:3	D60
2	D0:2	D61
1	D0:1	D62
0	D0:0	D63

Table 5–19 lists the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. The default radix of the Control group is SYMBOLIC on the logic analyzer. The symbol table file name is 8260ITR_SNG_Ctrl on the logic analyzer.

Table 5–19: Control channel group assignments for 8260ITR_SNG

Bit order	LA channel	8260ITR_SNG signal name
4	CLK:0	PSDVAL~
3	C2:1	POE~/PSDRAS~/PGPL2
2	C2:2	PSDCAS~/PGPL3
1	C3:7	BCTL0~
0	C3:5	PSDWE~/PGPL1

***NOTE**. The signals POE~/PSDRAS~/PGPL2 and PSDCAS~/PGPL3 are used as PSDCAS~ and PSDCAS~ respectively in 8260ITR_SNG.*

PortWidth Group Assignments. This group displays the PortWidth (in number of bytes) corresponding to the current sample. In Memory Image mode this displays the PortWidth only for the samples belonging to fetch stream and not for the ones read from the memory image.

Table 5–20 lists the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, the Misc channel group assignments are not displayed.

Table 5–20: Misc channel group assignments for 8260ITR_SNG

Bit order	LA channel	8260ITR_SNG signal name
30	Clock:1	CLKIN
29	C3:1	PSDA10/PGPL0
28	C3:3	HRESET~
27	C3:0	SRESET~
26	C2:5	PSDAMUX/PGPL5
25	C2:4	L2_HIT~/IRQ4~
24	Clock:2	CS3~
23	Qual_2	CS1~
22	Qual_1	CS0~
21	C3:2	BR~
20	C0:1	BNKSEL0/TC0/AP1/MODCK1~
19	C0:0	BNKSEL1/TC1/AP2/MODCK2~
18	C2:6	BNKSEL2/TC2/AP3/MODCK3~
17	C1:0	TT0
16	C0:7	TT1
15	C0:6	TT2
14	C0:5	TT3
13	C0:4	TT4
12	C1:7	TBST~
11	C1:4	TSIZ0
10	C1:3	TSIZ1
9	C1:2	TSIZ2
8	C1:1	TSIZ3
7	Clock:3	TS~
6	C2:3	ALE
5	C2:0	AACK~
4	C3:6	ABB~/IRQ2~
3	C1:6	ARTRY~

Table 5–20: Misc channel group assignments for 8260ITR_SNG (cont.)

Bit order	LA channel	8260ITR_SNG signal name
2	C2:7	DBB~/IRQ3~
1	C0:3	TA~
0	C0:2	TEA~

Table 5–21 lists the probe section and clock and qualifier channel assignments. The clock probes are not part of any group.

Table 5–21: Clock and Qualifier channel assignments for 8260ITR_SNG

8260ITR_SNG signal name	Channel name
CLK:0	PSDVAL~
CLK:1	CLKIN as clock
CLK:2	CS3~
CLK:3	TS~
C2:0	AACK~
C2:1	POE~/PSDRAS~/PGPL2
C2:2	PSDCAS~/PGPL3
C2:3	ALE
QUAL:0	CS2~
QUAL:1	Not connected
QUAL:2	CS1~
QUAL:3	CS0~

Table 5–22 Signals required for clocking and disassembly for the 8260ITR_SNG interface.

Table 5–22: Signals required for clocking and disassembly for 8260ITR_SNG

8260ITR_SNG signal name	Channel name
A0 – A31	A0:0–7
(Address Group)	A1:0–7
–	A2:0–7
–	A3:0–7
–	–
D0–D63	E0:0–7
(High_Data & Low_Data Groups)	E1:0–7
–	E2:0–7
–	E3:0–7
–	D0:0–7
–	D1:0–7
–	D2:0–7
–	D3:0–7
CLKIN	CLK:1
PSDVAL~	CLK:0
POE~/PSDRAS~/PGPL2	C2:1
PSDCAS~/PGPL3	C2:2
BCTL0~	C3:7
PSDWE~/PGPL1	C3:5

Table 5–23 Signals not required for clocking and disassembly for the 8260ITR_SNG interface.

Table 5–23: Signals not required for clocking and disassembly for 8260ITR_SNG

8260ITR_SNG signal name	Channel name
PSDA10/PGPL0	C3:1
HRESET~	C3:3
SRESET~	C3:0

Table 5–23: Signals not required for clocking and disassembly for 8260ITR_SNG (cont.)

8260ITR_SNG signal name	Channel name
PSDAMUX/PGPL5	C2:5
L2_HIT~/IRQ4~	C2:4
CS3~	Clock:2
CS1~	Qual_2
CS0~	Qual_1
BR~	C3:2
BNKSEL0/TC0/AP1/MODCK1~	C0:1
BNKSEL1/TC1/AP2/MODCK2~	C0:0
BNKSEL2/TC2/AP3/MODCK3~	C2:6
TT0	C1:0
TT1	C0:7
TT2	C0:6
TT3	C0:5
TT4	C0:4
TBST~	C1:7
TSIZ0	C1:4
TSIZ1	C1:3
TSIZ2	C1:2
TSIZ3	C1:1
TS~	Clock:3
ALE	C2:3
AACK~	C2:0
ABB~/IRQ2~	C3:6
ARTRY~	C1:6
DBB~/IRQ3~	C2:7
TA~	C0:3
TEA~	C0:2

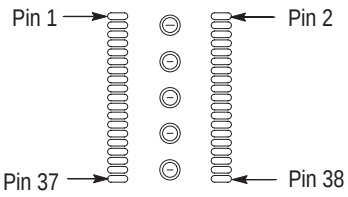
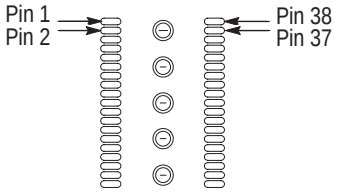
CPU To Mictor Connections

For design purposes, you may need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the *P6434 Mass Termination Probe* manual, Tektronix part number 070-9793-XX, for more information on mechanical specifications.

CAUTION. *To protect the CPU and the inputs of the module, it is recommended that a 180 Ω resistor is connected in series between each ball pad of the CPU and each pin of the Mictor connector. The resistor must be within 1/2 inch of the ball pad of the CPU.*

The recommended pin assignment is the Amp pin assignment, because the AMP circuit board layout model and other commercial CAD packages use the Amp numbering scheme. In order to use the Tektronix numbering scheme a custom model must be created for your circuit board layout CAD application. See Figure 5–24.

Table 5–24: Recommended pin assignments for a Mictor connector (component side)

Type of pin assignment	Comments
Recommended  **Amp Pin Assignment**	Recommended. This pin assignment is the industry standard and is what we recommend that you use.
Not Recommended  **Non Standard Pin Assignment**	Not recommended. This pin assignment was previously used by Tektronix but is no longer recommended due to incompatibility with other commercial CAD packages.

8260ITR_60X Mictor Connections

Tables 5–25 through 5–27 list the microprocessor signals visible at the mictor connectors.

Table 5–25: CPU to Mictor connections for Mictor A pins for 8260ITR_60X

AMP Mictor A pin number (recommended)	Tektronix Mictor A pin number	Logic analyzer channel	8260ITR_60X signal name	Comments
1	1	GND	GND	GND
3	2	GND	GND	GND
5	3	CLK:0	PSDVAL~	Data signal
7	4	A3:7	A0	Address
9	5	A3:6	A1	Address
11	6	A3:5	A2	Address
13	7	A3:4	A3	Address
15	8	A3:3	A4	Address
17	9	A3:2	A5	Address
19	10	A3:1	A6	Address
21	11	A3:0	A7	Address
23	12	A2:7	A8	Address
25	13	A2:6	A9	Address
27	14	A2:5	A10	Address
29	15	A2:4	A11	Address
31	16	A2:3	A12	Address
33	17	A2:2	A13	Address
35	18	A2:1	A14	Address
37	19	A2:0	A15	Address
38	20	A0:0	BADDR31	Address
36	21	A0:1	BADDR30	Address
34	22	A0:2	BADDR29	Address
32	23	A0:3	BADDR28	Address
30	24	A0:4	BADDR27	Address
28	25	A0:5	A26	Address
26	26	A0:6	A25	Address
24	27	A0:7	A24	Address
22	28	A1:0	A23	Address

Table 5–25: CPU to Mictor connections for Mictor A pins for 8260ITR_60X (cont.)

AMP Mictor A pin number (recommended)	Tektronix Mictor A pin number	Logic analyzer channel	8260ITR_60X signal name	Comments
20	29	A1:1	A22	Address
18	30	A1:2	A21	Address
16	31	A1:3	A20	Address
14	32	A1:4	A19	Address
12	33	A1:5	A18	Address
10	34	A1:6	A17	Address
8	35	A1:7	A16	Address
6	36	CLK:1	CLKIN	Clock

Table 5–26: CPU to Mictor connections for Mictor C pins for 8260ITR_60X

AMP Mictor C pin number (recommended)	Tektronix Mictor C pin number	Logic analyzer channel	8260ITR_60X signal name	Comments
01	01	–	–	Not Connected
03	02	–	–	Not Connected
05	03	CLK:3	TS~	Transfer Start
07	04	C3:7	BCTL0~	Buffer Control 0
09	05	C3:6	ABB~/IRQ2~	Address Bus Busy
11	06	C3:5	PSDWE~/PGPL 1	60x BUS SDRAM write enable
13	07	C3:4	–	–
15	08	C3:3	HRESET~	Hard Reset
17	09	C3:2	BR~	Bus Request
19	10	C3:1	PSDA10/PGPL0	
21	11	C3:0	SRESET~	Soft Reset
23	12	C2:7	DBB~/IRQ3~	Data Bus Busy
25	13	C2:6	BNKSEL2/TC2/ AP3/MODCK3~	Transfer Code 2
27	14	C2:5	PSDAMUX/ PGPL5	60x bus SDRAM Address Multiplexer

Table 5–26: CPU to Mictor connections for Mictor C pins for 8260ITR_60X (cont.)

AMP Mictor C pin number (recommended)	Tektronix Mictor C pin number	Logic analyzer channel	8260ITR_60X signal name	Comments
29	15	C2:4	L2_HIT~/IRQ4~	L2 Cache Signal
31	16	C2:3	ALE	Address Latch Enable
33	17	C2:2	DBG~	Data Bus Grant
35	18	C2:1	BG~	Bus Grant
37	19	C2:0	AACK~	Address Acknowledge
38	20	C0:0	BNKSEL1/TC1/ AP2/MODCK2~	Transfer Code 1
36	21	C0:1	BNKSEL0/TC0/ AP1/MODCK1~	Transfer Code 0
34	22	C0:2	TEA~	Transfer Error Acknowledge
32	23	C0:3	TA~	Transfer Acknowledge
30	24	C0:4	TT4	Transfer Type
28	25	C0:5	TT3	Transfer Type
26	26	C0:6	TT2	Transfer Type
24	27	C0:7	TT1	Transfer Type
22	28	C1:0	TT0	Transfer Type
20	29	C1:1	TSIZ3	Transfer Size
18	30	C1:2	TSIZ2	Transfer Size
16	31	C1:3	TSIZ1	Transfer Size
14	32	C1:4	TSIZ0	Transfer Size
12	33	C1:5	–	–
10	34	C1:6	ARTRY~	Address Retry
08	35	C1:7	TBST~	Transfer Burst
06	36	QUAL_1	Not connected	–
04	37	–	–	–
02	38	–	–	–

Table 5–27: CPU to Mictor connections for Mictor E pins for 8260ITR_60X

AMP Mictor E pin number (recommended)	Tektronix Mictor E pin number	Logic analyzer channel	8260ITR_60X signal name	Comments
1	1	–	–	Not Connected
3	2	–	–	Not Connected
5	3	Qual_3	CS0~	–
7	4	E3:7	D0	High_Data
9	5	E3:6	D1	High_Data
11	6	E3:5	D2	High_Data
13	7	E3:4	D3	High_Data
15	8	E3:3	D4	High_Data
17	9	E3:2	D5	High_Data
19	10	E3:1	D6	High_Data
21	11	E3:0	D7	High_Data
23	12	E2:7	D8	High_Data
25	13	E2:6	D9	High_Data
27	14	E2:5	D10	High_Data
29	15	E2:4	D11	High_Data
31	16	E2:3	D12	High_Data
33	17	E2:2	D13	High_Data
35	18	E2:1	D14	High_Data
37	19	E2:0	D15	High_Data
38	20	E0:0	D31	High_Data
36	21	E0:1	D30	High_Data
34	22	E0:2	D29	High_Data
32	23	E0:3	D28	High_Data
30	24	E0:4	D27	High_Data
28	25	E0:5	D26	High_Data
26	26	E0:6	D25	High_Data
24	27	E0:7	D24	High_Data
22	28	E1:0	D23	High_Data
20	29	E1:1	D22	High_Data
18	30	E1:2	D21	High_Data

Table 5–27: CPU to Mictor connections for Mictor E pins for 8260ITR_60X (cont.)

AMP Mictor E pin number (recommended)	Tektronix Mictor E pin number	Logic analyzer channel	8260ITR_60X signal name	Comments
16	31	E1:3	D20	High_Data
14	32	E1:4	D19	High_Data
12	33	E1:5	D18	High_Data
10	34	E1:6	D17	High_Data
8	35	E1:7	D16	High_Data
6	36	Qual_2	CS1~	–
4	37	–	–	–
2	38	–	–	–

Table 5–28: CPU to Mictor connections for Mictor D pins for 8260ITR_60X

AMP Mictor D pin number (recommended)	Tektronix Mictor D pin number	Logic analyzer channel	8260ITR_60X signal name	Comments
1	1	–	–	Not Connected
3	2	–	–	Not Connected
5	3	–	–	Not Connected
7	4	D3:7	D32	Low_Data
9	5	D3:6	D33	Low_Data
11	6	D3:5	D34	Low_Data
13	7	D3:4	D35	Low_Data
15	8	D3:3	D36	Low_Data
17	9	D3:2	D37	Low_Data
19	10	D3:1	D38	Low_Data
21	11	D3:0	D39	Low_Data
23	12	D2:7	D40	Low_Data
25	13	D2:6	D41	Low_Data
27	14	D2:5	D42	Low_Data
29	15	D2:4	D43	Low_Data
31	16	D2:3	D44	Low_Data

Table 5–28: CPU to Mictor connections for Mictor D pins for 8260ITR_60X (cont.)

AMP Mictor D pin number (recommended)	Tektronix Mictor D pin number	Logic analyzer channel	8260ITR_60X signal name	Comments
33	17	D2:2	D45	Low_Data
35	18	D2:1	D46	Low_Data
37	19	D2:0	D47	Low_Data
38	20	D0:0	D63	Low_Data
36	21	D0:1	D62	Low_Data
34	22	D0:2	D61	Low_Data
32	23	D0:3	D60	Low_Data
30	24	D0:4	D59	Low_Data
28	25	D0:5	D58	Low_Data
26	26	D0:6	D57	Low_Data
24	27	D0:7	D56	Low_Data
22	28	D1:0	D55	Low_Data
20	29	D1:1	D54	Low_Data
18	30	D1:2	D53	Low_Data
16	31	D1:3	D52	Low_Data
14	32	D1:4	D51	Low_Data
12	33	D1:5	D50	Low_Data
10	34	D1:6	D49	Low_Data
8	35	D1:7	D48	Low_Data
6	36	–	–	–
4	37	–	–	–
2	38	–	–	–

8260ITR_SNG Mictor Connections

Tables 5–29 and 5–31 list the microprocessor signals visible at the mictor connectors.

Table 5–29: CPU to Mictor connections for Mictor A pins for 8260ITR_SNG

AMP Mictor A pin number (recommended)	Tektronix Mictor A pin number	Logic analyzer channel	8260ITR_SNG signal name	Comments
1	1	–	–	Not Connected
3	2	–	–	Not Connected
5	3	CLK:0	PSDVAL~	Data signal
7	4	A3:7	A0	Address
9	5	A3:6	A1	Address
11	6	A3:5	A2	Address
13	7	A3:4	A3	Address
15	8	A3:3	A4	Address
17	9	A3:2	A5	Address
19	10	A3:1	A6	Address
21	11	A3:0	A7	Address
23	12	A2:7	A8	Address
25	13	A2:6	A9	Address
27	14	A2:5	A10	Address
29	15	A2:4	A11	Address
31	16	A2:3	A12	Address
33	17	A2:2	A13	Address
35	18	A2:1	A14	Address
37	19	A2:0	A15	Address
38	20	A0:0	A31	Address
36	21	A0:1	A30	Address
34	22	A0:2	A29	Address
32	23	A0:3	A28	Address
30	24	A0:4	A27	Address
28	25	A0:5	A26	Address
26	26	A0:6	A25	Address
24	27	A0:7	A24	Address
22	28	A1:0	A23	Address

Table 5–29: CPU to Mictor connections for Mictor A pins for 8260ITR_SNG (cont.)

AMP Mictor A pin number (recommended)	Tektronix Mictor A pin number	Logic analyzer channel	8260ITR_SNG signal name	Comments
20	29	A1:1	A22	Address
18	30	A1:2	A21	Address
16	31	A1:3	A20	Address
14	32	A1:4	A19	Address
12	33	A1:5	A18	Address
10	34	A1:6	A17	Address
8	35	A1:7	A16	Address
6	36	CLK:1	CLKIN	Clock

Table 5–30: CPU to Mictor connections for Mictor C pins for 8260ITR_SNG

AMP Mictor C pin number (recommended)	Tektronix Mictor C pin number	Logic analyzer channel	8260ITR_SNG signal name	Comments
1	1	–	–	Not Connected
3	2	–	–	Not Connected
5	3	CLK:3	TS~	Transfer Start
7	4	C3:7	BCTL0~	Buffer Control 0
9	5	C3:6	ABB~/IRQ2~	Address Bus Busy
11	6	C3:5	PSDWE~/PGPL1	60x Bus SDRAM Write Enable
13	7	C3:4	–	–
15	8	C3:3	HRESET~	Hard Reset
17	9	C3:2	BR~	Bus Request
19	10	C3:1	PSDA10/PGPL0	60x bus SDRAM A10
21	11	C3:0	SRESET~	Soft Reset
23	12	C2:7	DBB~/IRQ3~	Data Bus Busy
25	13	C2:6	BNKSEL2/TC2/AP3/MODCK3~	Transfer Code 2
27	14	C2:5	PSDAMUX/PGPL5	60x bus SDRAM Address Multiplexer

Table 5–30: CPU to Mictor connections for Mictor C pins for 8260ITR_SNG (cont.)

AMP Mictor C pin number (recommended)	Tektronix Mictor C pin number	Logic analyzer channel	8260ITR_SNG signal name	Comments
29	15	C2:4	L2_HIT~/IRQ4~	L2 Cache Signal
31	16	C2:3	ALE	Address Latch enable
33	17	C2:2	PSDCAS~/PGPL3	60x BUS SDRAM CAS
35	18	C2:1	POE~/PSDRAS~/ PGPL2	60X Bus SDRAM RAS
37	19	C2:0	AACK~	Address Acknowledge
38	20	C0:0	BNKSEL1/TC1/A P2/MODCK2~	Transfer code 1
36	21	C0:1	BNKSEL0/TC0/A P1/MODCK1~	Transfer Code 0
34	22	C0:2	TEA~	Transfer Error Acknowledge
32	23	C0:3	TA~	Transfer Acknowledge
30	24	C0:4	TT4	Transfer Type
28	25	C0:5	TT3	Transfer Type
26	26	C0:6	TT2	Transfer Type
24	27	C0:7	TT1	Transfer Type
22	28	C1:0	TT0	Transfer Type
20	29	C1:1	TSIZ3	Transfer Size
18	30	C1:2	TSIZ2	Transfer Size
16	31	C1:3	TSIZ1	Transfer Size
14	32	C1:4	TSIZ0	Transfer Size
12	33	C1:5		
10	34	C1:6	ARTRY~	Address Retry
8	35	C1:7	TBST~	Transfer Burst
6	36	Qual_1	Not connected	–
4	37	–	–	–
2	38	–	–	–

Table 5–31: CPU to Mictor connections for Mictor E pins for 8260ITR_SNG

AMP Mictor E pin number (recommended)	Tektronix Mictor E pin number	Logic analyzer channel	8260ITR_SNG signal name	Comments
1	1	–	–	Not Connected
3	2	Qual_3	CS0~	Not Connected
5	3	–	–	SystemReset
7	4	E3:7	D0	High_Data
9	5	E3:6	D1	High_Data
11	6	E3:5	D2	High_Data
13	7	E3:4	D3	High_Data
15	8	E3:3	D4	High_Data
17	9	E3:2	D5	High_Data
19	10	E3:1	D6	High_Data
21	11	E3:0	D7	High_Data
23	12	E2:7	D8	High_Data
25	13	E2:6	D9	High_Data
27	14	E2:5	D10	High_Data
29	15	E2:4	D11	High_Data
31	16	E2:3	D12	High_Data
33	17	E2:2	D13	High_Data
35	18	E2:1	D14	High_Data
37	19	E2:0	D15	High_Data
38	20	E0:0	D31	High_Data
36	21	E0:1	D30	High_Data
34	22	E0:2	D29	High_Data
32	23t	E0:3	D28	High_Data
30	24	E0:4	D27	High_Data
28	25	E0:5	D26	High_Data
26	26	E0:6	D25	High_Data
24	27	E0:7	D24	High_Data
22	28	E1:0	D23	High_Data
20	29	E1:1	D22	High_Data
18	30	E1:2	D21	High_Data

Table 5–31: CPU to Mictor connections for Mictor E pins for 8260ITR_SNG (cont.)

AMP Mictor E pin number (recommended)	Tektronix Mictor E pin number	Logic analyzer channel	8260ITR_SNG signal name	Comments
16	31	E1:3	D20	High_Data
14	32	E1:4	D19	High_Data
12	33	E1:5	D18	High_Data
10	34	E1:6	D17	High_Data
8	35	E1:7	D16	High_Data
6	36	Qual_2	CS1~	–
4	37	–	–	–
2	38	–	–	–

Table 5–32: CPU to Mictor connections for Mictor D pins for 8260ITR_SNG

AMP Mictor D pin number (recommended)	Tektronix Mictor D pin number	Logic analyzer channel	8260ITR_SNG signal name	Comments
1	1	–	–	Not Connected
3	2	Qual_0	CS2~	Not Connected
5	3	CLK	–	System Reset
7	4	D3:7	D32	Low_Data
9	5	D3:6	D33	Low_Data
11	6	D3:5	D34	Low_Data
13	7	D3:4	D35	Low_Data
15	8	D3:3	D36	Low_Data
17	9	D3:2	D37	Low_Data
19	10	D3:1	D38	Low_Data
21	11	D3:0	D39	Low_Data
23	12	D2:7	D40	Low_Data
25	13	D2:6	D41	Low_Data
27	14	D2:5	D42	Low_Data
29	15	D2:4	D43	Low_Data
31	16	D2:3	D44	Low_Data

Table 5–32: CPU to Mictor connections for Mictor D pins for 8260ITR_SNG (cont.)

AMP Mictor D pin number (recommended)	Tektronix Mictor D pin number	Logic analyzer channel	8260ITR_SNG signal name	Comments
33	17	D2:2	D45	Low_Data
35	18	D2:1	D46	Low_Data
37	19	D2:0	D47	Low_Data
38	20	D0:0	D63	Low_Data
36	21	D0:1	D62	Low_Data
34	22	D0:2	D61	Low_Data
32	23	D0:3	D60	Low_Data
30	24	D0:4	D59	Low_Data
28	25	D0:5	D58	Low_Data
26	26	D0:6	D57	Low_Data
24	27	D0:7	D56	Low_Data
22	28	D1:0	D55	Low_Data
20	29	D1:1	D54	Low_Data
18	30	D1:2	D53	Low_Data
16	31	D1:3	D52	Low_Data
14	32	D1:4	D51	Low_Data
12	33	D1:5	D50	Low_Data
10	34	D1:6	D49	Low_Data
8	35	D1:7	D48	Low_Data
6	36	Clock:2	CS3~	–
4	37	–	–	–
2	38	–	–	–

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