Instruction Manual

Tektronix

TMS833
UTOPIA3 Software Support

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www.tektronix.com

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Preface

This instruction manual contains specific information about the TMS833 UTOPIA3 software support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating bus support packages on the logic analyzer for which the TMS833 UTOPIA3 support was purchased, you will probably only need this instruction manual to set up and run the support package.

If you are not familiar with operating bus support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support package.

Information on basic operations of bus support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of logic analyzer online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the target system
- Setting up the logic analyzer to acquire data from the target system
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into header and payload information.
- The phrase “information on basic operations” refers to logic analyzer online help or a user manual, covering the basic operations of the bus support.
- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.

Contacting Tektronix

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*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
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Getting Started

Getting Started

This section contains information on the TMS833 UTOPIA3 bus support, and information on connecting your logic analyzer to your target system.

Support Package Description

The TMS833 bus support package displays disassembled data from systems based on the Utopia Level 3 bus in the Transmit or Receive mode.

The highlights of Utopia Level 3 specification are as follows:

- Allows 32 bit, 16 bit or 8 bit data paths
- Supports data rates of 3.2 Gb/s for 32 bit data path, 1.6 Gb/s for 16 bit data path, and 800 Mb/s for 8 bit data path
- Provides Single Physical and Multi-Physical operations

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS833 support package.

To use this support efficiently, you need the items listed in the information on basic operations in your logic analyzer online help and the following user manuals.

- Utopia level 3-ATM-PHY Interface Specification AF-PHY-0136.000 November, 1999
- ITU-T Recommendations I.361, I.363, I.363.1, I.363.2, I.363.3 and I.363.5
- ITU-T recommendation I.361 for the interpretation of the ATM cell header information

Logic Analyzer Software Compatibility

The label on the bus support floppy disk states which version of logic analyzer software this support is compatible with.

Logic Analyzer Configuration

The TMS833 support allows a choice of required minimum module configurations.

The Utopia Level 3 support package is divided into two support packages:

- UTOPIA3RX: UTOPIA3RX requires at least one 68-channel module to acquire data from the receive interface.
- UTOPIA3TX: UTOPIA3TX requires at least one 68-channel module to acquire data from the transmit interface.

To monitor both interfaces simultaneously the support package requires two 68-channel modules. You must load the Transmit support package in one of the 68-channel modules and the Receive support package in the other. By double probing the common clock, the support acquires the Transmit and Receive data information coming on the Utopia interface simultaneously.

To use only one support at a time, you must select the correct module and specify the support.

Requirements and Restrictions

Review the electrical specifications in the *Specifications* section in this manual as they pertain to your target system, as well as the following descriptions of other TMS833 UTOPIA3 support requirements and restrictions.

Hardware Reset. If a hardware reset occurs in your TMS833 UTOPIA3 system during an acquisition, the application disassembler might acquire invalid samples.

Clock Rate. The TMS833 UTOPIA3 bus support can acquire data from the UTOPIA3 bus operating at speeds of up to 104 MHz[1].

Setup and Hold Time Adjustments. You cannot change the setup and hold time for any signal group.

Nonintrusive Acquisition. Acquiring Utopia3 bus cycles is nonintrusive to the target system. That is, the TMS833 UTOPIA3 does not intercept, modify, or present signals back to the target system.

[1] **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

Channel Groups. Channel groups required for clocking and disassembly for TMS833 UTOPIA3 bus support are as follows:

Receive bus:
Address Group, Data Group, Control Group, and RXCLAV Group.

Transmit bus:
Address Group, Data Group, Control Group, and TXCLAV Group.

Address Display. The address of the PHY port from which the cell is transmitted or received is correct only when the custom clocking option is Header and Payload or Header Only. The support displays the address only when more than one physical port is involved. In a Single PHY operation, the Address column is dashed out. The software supports a maximum of seven address lines.

The disassembly shows correct information only when the appropriate disassembly and custom clocking options are chosen.

Table 1–1 shows the invalid combinations of disassembly and clocking option.

Table 1–1: Invalid disassembly and clocking combinations

Clocking option	Disassembly option
Header and Payload	All Cycles
Header Only	All Cycles, Header and Payload

AAL Decoding. This information covers the features that are supported in each of the AAL layers and their limitations.

***NOTE**. You can see AAL decoding only when the disassembly SHOW option is set to Header and Payload. All field values that are decoded are in binary or in hexadecimal. The support does not decode AAL when all the 48 payload bytes of the ATM cell are not available.*

AAL 1: In this layer, the TMS833 UTOPIA3 support decodes up to the SAR-PDU level: SAR-PDU header and payload information.

Refer to the ITU-T I.363.1 B-ISDN ATM adaptation layer specification for details about the PDU format.

Limitation: The TMS833 UTOPIA3 does not support the Structured Data Transfer format of SAR-PDU payload.

AAL 2: In this layer, the TMS833 UTOPIA3 support decodes information up to the CPS-PACKET level. The support identifies the CPS-PACKET header and Packet payloads.

Refer to the ITU-T I.363.2 B-ISDN ATM adaptation layer specification for details about the PDU format.

Limitation: The TMS833 UTOPIA3 does not support multiplexing and packing of CPS-PACKETs into CPS-PDUs.

AAL 3/4: The TMS833 UTOPIA3 support decodes information up to the SAR-PDU and to a certain extent the CPCS-PDU. The support decodes the SAR-PDU to show details of the SAR-PDU header and trailer information and identifies the SAR-PDU whether it is BOM, COM, EOM, or SSM.

The support identifies the two types of SAR-PDUs: Data-SAR-PDU and Abort-SAR-PDU. The SAR-PDUs are further decoded to show the CPCS-PDU header and trailer information based on whether it is BOM, EOM, COM, or SSM.

Refer to the ITU-T I.363.3 B-ISDN ATM adaptation layer specification for details about the PDU format.

AAL 5: The support decodes the information up to the SAR-PDU and identifies the last SAR-PDU payload based on the AUU parameter. The support decodes the CPCS trailer information (the CPCS trailer is in the last eight octets of the last SAR-PDU.)

Refer to the ITU-T I.363.5 B-ISDN ATM adaptation layer specification for details about the PDU format.

Timing Display Format

A Timing Display Format file is also provided for this support. It sets up the display to show the following waveforms for the TMS833 bus support.

For UTOPIA3TX Support:

TxClk
TxSOC
TxEnb*
Address
Data
Control

For UTOPIA3RX Support:

RxClk
RxSOC
RxEnb*
Address
Data
Control

***NOTE**. An asterisk (*) following a signal name indicates an active low signal.*

Address, Data, and Control groups are displayed in bus form.

Functionality Not Supported

The TMS833 UTOPIA3 package does not support the following functionality:

- The payload is not analyzed to decode higher layer protocols other than AAL information.

Connecting the Logic Analyzer to a Target System

You can use the channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make the connections between the logic analyzer and your target system.

To connect the probes to TMS833 UTOPIA3 signals in the target system using a test clip, follow the steps:

1. Power off your target system. It is not necessary to power off the logic analyzer.

***CAUTION.** To prevent static damage, handle the target systems, probes, and the logic analyzer module in a static-free environment. Static discharge can damage these components.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the target system.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored electricity from the test clip.
3. Place the target system on a horizontal, static-free surface.
4. Use Tables 3–3 through 3–14 starting on page 3–2 to connect the channel probes to TMS833 UTOPIA3 signal pins on the test clip or in the target system.
5. Use leadsets to connect at least one ground lead from each channel and the ground lead from each clock probe to the ground pins on your test clip.

Labeling P6434 Probes

The TMS833 bus support package relies on the channel mapping and labeling scheme for the P6434 Probes. Apply labels using the instructions described in the *P6434 Probe Instructions* manual.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support and covers the following topics:

- Channel group definitions
- Clocking options

The information in this section is specific to the operations and functions of the TMS833 UTOPIA3 support on a Tektronix logic analyzer for which the support is compatible. Information on basic operations describes general tasks and functions.

Before you acquire and display disassembled data, you need to load the support and specify the setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change the setups as needed.

Installing the Support Software

***NOTE**. Before you install any software, it is recommended you verify that the bus support software is compatible with the logic analyzer software.*

To install the TMS833 UTOPIA3 software on your Tektronix logic analyzer, follow these steps:

1. Insert the floppy disk in the disk drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the floppy disk.

To remove or uninstall software, follow the above instructions and select Uninstall. You need to close all windows before you uninstall any software.

Support Package Setups

The software installs two support packages. Each support package offers different clocking and display options.

Acquisition Setup. The support package consists of two different supports, one for the Transmit Interface and the other for the Receive Interface. You must make connections and load the appropriate package for the desired support. The TMS833 support will affect the logic analyzer setup menus (and submenus) by modifying existing fields, and adding UTOPIA3 bus-specific fields. The TMS833 adds the selection "UTOPIA3RX" and "UTOPIA3TX" to the "Load Support Package" dialog box, under the File pulldown menu.

Once the corresponding support has been loaded, the "Custom" clocking mode selection in the logic analyzer setup menu is also enabled. "Custom" is the default selection whenever the UTOPIA3RX or UTOPIA3TX support loads.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the TMS833 UTOPIA3 support for the Receive bus are Address, Data, Control, and RXCLAV. Table 2–1 gives the Receive bus group names and the display radix for each.

Table 2–1: Receive bus group names

Group name	Display radix
Address	HEX
Data	HEX
Cell Details	NONE - Disassembly generated text
Control	SYM
RXCLAV	BIN

The channel groups for the TMS833 UTOPIA3 support for the Transmit bus are Address, Data, Control, and TXCLAV. Table 2–2 gives the Transmit bus group names and the display radix for each.

Table 2–2: Transmit bus group names

Group name	Display radix
Address	HEX
Data	HEX
Cell Details	NONE - Disassembly generated text
Control	SYM
TXCLAV	BIN

If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–2.

Clocking

Clocking Options

The TMS833 support offers a bus-specific clocking mode for the TMS833 UTOPIA3 bus interface. This clocking mode is the default selection whenever you load the UTOPIA3 support.

Disassembly is not correct when using the Internal or External clocking modes. Information on basic operations in the logic analyzer online help describes how to use these clock selections for general purpose analysis.

Custom Clocking

A special clocking program is loaded on the module every time you load the UTOPIA3 support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple channel groups at different times when the signals are valid on the Utopia3 bus. The module then sends all the logged in signals to the trigger machine and to the acquisition memory of the module for storage.

In the custom mode, the support uses a TxClk as the clock for the transmit interface and a RxClk as the clock for the receive interface. After loading the UTOPIA3TX or UTOPIA3RX support, the sample points and master points are defined based on the selections of each of the clocking options.

The TMS833 modifies the Custom Clocking Options menu of the logic analyzer. The following options are available to acquire Utopia3 Receive (in UTOPIA3RX) and Utopia3 Transmit (in UTOPIA3TX) bus signals:

Capture. Select one of the three options for Capture.

- All Cycles (default)

Use the All Cycles option to acquire the information on the bus at every rising edge of the clock. The All Cycles option describes the conditions that exist on the bus, in addition to acquiring the header and payload information.

- Header and Payload

If you choose the Header and Payload option when the Utopia Level 3 interface is connected, the acquisition will consist of ATM cells only. The support does not acquire samples corresponding to cycles when valid data is not available on the interface.

- Header Only

Select the Header Only option if only ATM cell headers must be acquired. In this mode, the Header option must be set appropriately for correct disassembly.

Data_Width. Use the Data_Width option to distinguish the width of the data path. The data path width information is important when the custom clocking option is set to Header Only. The data path width can be any one of the following.

32 bit (default)
16 bit
8 bit

Header. Use the Header option depending on the type of ATM Cells used. Select one of the following options:

Does not contain HEC (default)
Contains HEC

Table 2–3 shows the options that can be selected for the ATM Cell types.

Table 2–3: Options for ATM Cell types

Data width	Type of ATM cell	Select option
8 bits	52 byte	Does not contain HEC
16 bits	52 byte	Does not contain HEC
32 bits	52 byte	Does not contain HEC
8 bits	53 byte	Contains HEC
16 bits	54 byte	Contains HEC
32 bits	56 byte	Contains HEC

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. The following information covers these topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Viewing cycle type labels
- Changing the way data is displayed

Acquiring Data

The TMS833 UTOPIA3 software package installs two different supports, one for the Transmit Interface, and the other for the Receive Interface.

Once you load either the Transmit or Receive Interface, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your logic analyzer online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations manual.

Signal Acquisition in Transmit Mode

This section shows a timing diagram and tables that list details on how to acquire the relevant address, data, and control signals in the Transmit mode.

Figure 2-1 shows a Tx bus mode timing diagram.

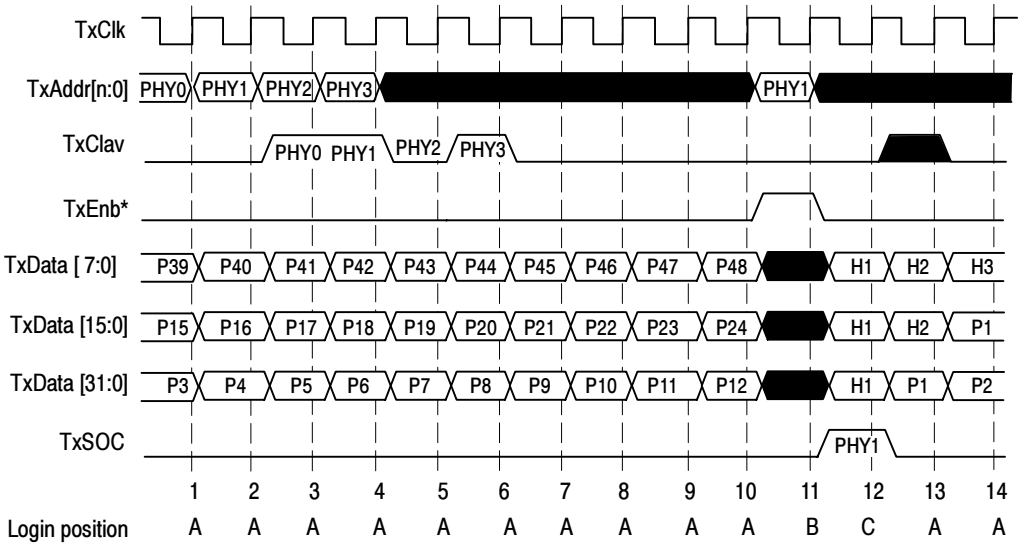


Figure 2-1: Tx bus mode timing diagram

The custom Clock uses the rising edge of the TxClk signal. An asterisk (*) indicates an active low signal. The support provides the following options to acquire the Utopia3 Transmit bus signals.

Capture. Select one of the three options for Capture.

- All Cycles

Use the All Cycles option to acquire the information on the bus at every rising edge of the clock. The All Cycles option describes the conditions that exist on the bus, in addition to acquiring the header and payload information. The support logs in the control, address, data, and masters all signals with every rising edge of the clock.

- Header and Payload

If you choose the Header and Payload option when the Utopia Level 3 interface is connected, the acquisition consists of ATM cells only. The support does not acquire samples corresponding to cycles when valid data is not available on the interface.

Table 2–4 shows the signals that are acquired in the Header and Payload option with reference to Figure 2–1. An asterisk (*) indicates an active low signal.

Table 2–4: Signals in the Header and Payload option

Qualifiers	Signals	Login position
TxEnb* High and TxSOC Low	These address signals are logged: TxAddr6, TxAddr5, TxAddr4, TxAddr3, TxAddr2, TxAddr1, TxAddr0	B
TxEnb* Low and TxSOC High	All signals are mastered	C
TxEnb* Low and TxSOC Low	All signals are mastered	A

- Header Only

Select the Header Only option if only ATM cell headers must be acquired. In this mode, the Header option must be set appropriately for correct disassembly.

Signal Acquisition in Receive Mode

This section contains the timing diagram and the tables that show details on acquiring the relevant address, data, and control signals in the Receive mode.

Figure 2–2 shows the bus timing diagram in the Receive mode. An asterisk (*) indicates an active low signal. The custom clock uses the rising edge of RxClk.

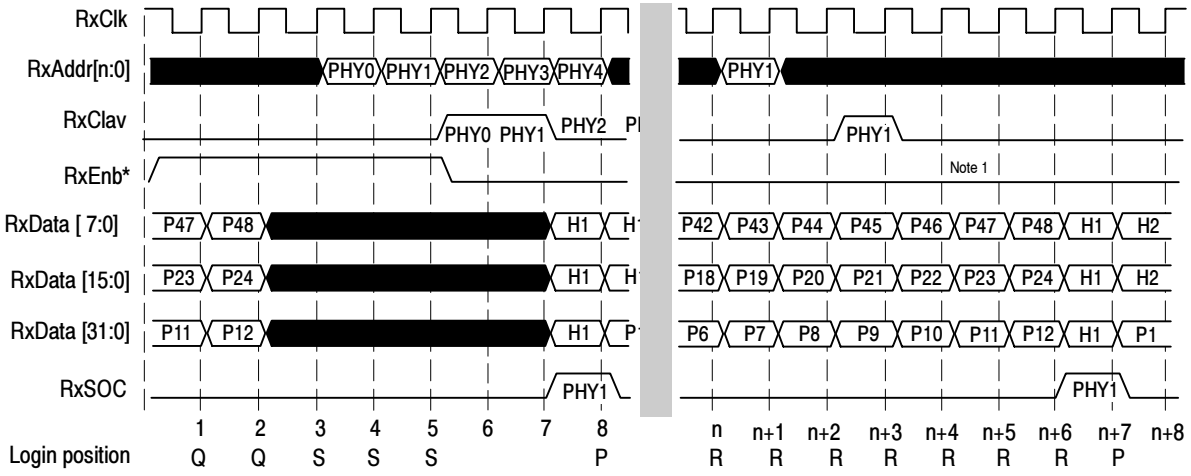


Figure 2–2: Rx bus mode timing diagram

The support provides the following options to acquire the Utopia3 Receive bus signals.

Capture. Select one of the three options for Capture.

- All Cycles

Use the All Cycles option to acquire the information on the bus at every rising edge of the clock. The All Cycles option describes the conditions that exist on the bus, in addition to acquiring the header and payload information. The support logs in the control, address, data and masters all signals with every rising edge of the clock.

- Header and Payload

If you choose the Header and Payload option when the Utopia Level 3 interface is connected, the acquisition will consist of ATM cells only. The support does not acquire samples corresponding to cycles when valid data is not available on the interface. Table 2–5 shows how signals are acquired in the receive mode with reference to Figure 2–2. An asterisk (*) indicates an active low signal.

Table 2–5: Signals in Header and Payload option

Qualifiers	Signals	Login position
RxEnb* Low and RxSOC High	All signals are mastered	P
RxEnb* High and RxSOC Low	These address signals are logged: RxAddr6, RxAddr5, RxAddr4, RxAddr3, RxAddr2, RxAddr1, RxAddr0	S
RxEnb* Low and RxSOC Low	All signals are mastered	R
RxEnb* High and RxSOC Low	All signals are mastered	Q

- Header Only

Select the Header Only option if only ATM cell headers must be acquired. In this mode, the Header option must be set appropriately for correct disassembly.

Viewing Disassembled Data

You can view disassembled data in three display formats:

All Cycles (Disassembly)
Header and Payload (Disassembly)
Header Only (Disassembly)

The information on basic operations describes how to select the disassembly display formats.

***NOTE**. You must set the selections in the Disassembly property page (the Disassembly Format Definition overlay) correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2-15.*

For the UTOPIA3 support, the default display format shows the Address and Data channel group values for each sample of acquired data.

If a channel group is not visible, you must use Add Column or Ctrl+L to make the group visible.

The disassembler displays special characters and strings in the Cell Details column to indicate significant events. Table 2-6 shows these special characters and strings and describes what they represent.

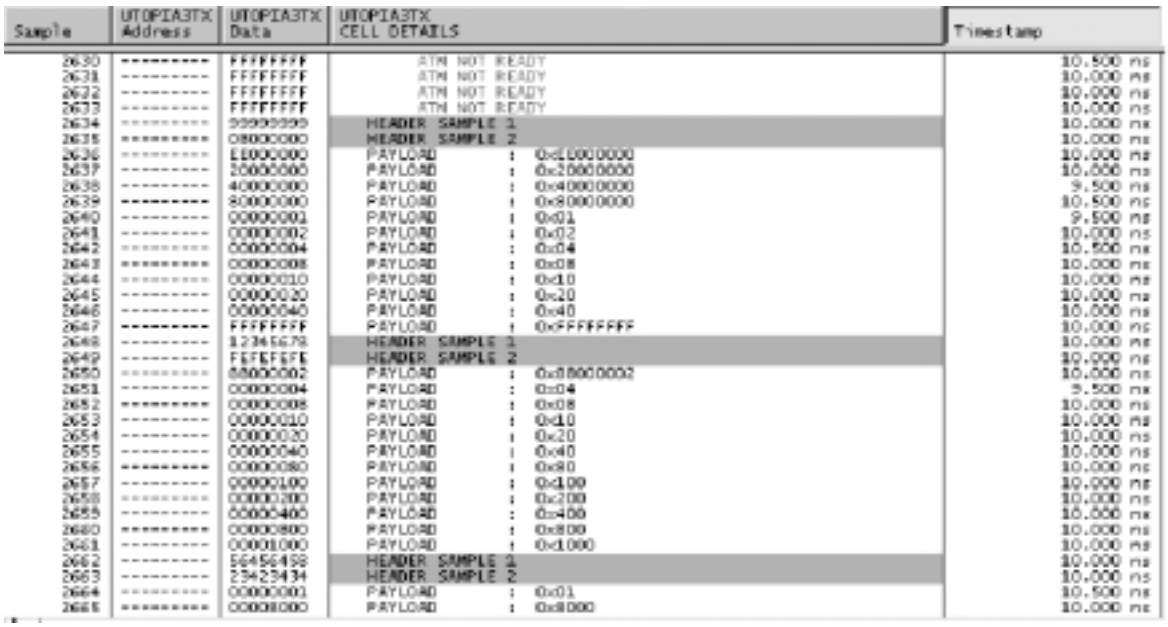
Table 2-6: Description of special characters in the display

Character or string displayed	Description
0x	Indicates that the given number is in hexadecimal.
>	Insufficient room on the screen to show all available data.
t	Indicates that the given number is in decimal.
0b	Indicates that the given number is in binary.

All Cycles Display Format

Along with the All Cycles option in custom clocking, the All Cycles Display Format provides disassembly of all the cycles including those where valid data transfers are not available. The All Cycles Display Format displays all the valid ATM cell headers and their payloads, any Invalid cycles, and Polling cycles that occur.

Figure 2-3 shows an example of the All Cycles display format with a 32 bit SIGPHY interface.



Sample	UTOPIA3TX Address	UTOPIA3TX Data	UTOPIA3TX CELL DETAILS	Timestamp
2630	----------	FFFFFFFF	ATM NOT READY	10.500 ns
2631	----------	FFFFFFFF	ATM NOT READY	10.000 ns
2632	----------	FFFFFFFF	ATM NOT READY	10.000 ns
2633	----------	FFFFFFFF	ATM NOT READY	10.000 ns
2634	----------	99999999	HEADER SAMPLE 1	10.000 ns
2635	----------	08000000	HEADER SAMPLE 2	10.000 ns
2636	----------	E0000000	PAYLOAD : 0xE0000000	10.000 ns
2637	----------	20000000	PAYLOAD : 0x20000000	10.000 ns
2638	----------	40000000	PAYLOAD : 0x40000000	9.500 ns
2639	----------	80000000	PAYLOAD : 0x80000000	10.500 ns
2640	----------	00000001	PAYLOAD : 0x01	9.500 ns
2641	----------	00000002	PAYLOAD : 0x02	10.000 ns
2642	----------	00000004	PAYLOAD : 0x04	10.500 ns
2643	----------	00000008	PAYLOAD : 0x08	10.000 ns
2644	----------	00000010	PAYLOAD : 0x10	10.000 ns
2645	----------	00000020	PAYLOAD : 0x20	10.000 ns
2646	----------	00000040	PAYLOAD : 0x40	10.000 ns
2647	----------	FFFFFFFF	PAYLOAD : 0xFFFFFFFF	10.000 ns
2648	----------	12345678	HEADER SAMPLE 1	10.000 ns
2649	----------	FEFEFEFE	HEADER SAMPLE 2	10.000 ns
2650	----------	80000002	PAYLOAD : 0x80000002	10.000 ns
2651	----------	00000004	PAYLOAD : 0x04	9.500 ns
2652	----------	00000008	PAYLOAD : 0x08	10.000 ns
2653	----------	00000010	PAYLOAD : 0x10	10.000 ns
2654	----------	00000020	PAYLOAD : 0x20	10.000 ns
2655	----------	00000040	PAYLOAD : 0x40	10.000 ns
2656	----------	00000080	PAYLOAD : 0x80	10.000 ns
2657	----------	00000100	PAYLOAD : 0x100	10.000 ns
2658	----------	00000200	PAYLOAD : 0x200	10.000 ns
2659	----------	00000400	PAYLOAD : 0x400	10.000 ns
2660	----------	00000800	PAYLOAD : 0x800	10.000 ns
2661	----------	00001000	PAYLOAD : 0x1000	10.000 ns
2662	----------	56456458	HEADER SAMPLE 1	10.000 ns
2663	----------	23423434	HEADER SAMPLE 2	10.000 ns
2664	----------	00000001	PAYLOAD : 0x01	10.500 ns
2665	----------	00008000	PAYLOAD : 0x8000	10.000 ns

Figure 2-3: Example of All Cycles display format

Header and Payload Display Format

Along with the “All Cycles” or “Header and Payload” option in custom clocking, the Header and Payload Display Format provides disassembly of the header details and payload information. If you select AAL type in disassembly, the payload is analyzed to display details of AAL SAR-PDU. If you select Header Only option in custom clocking, the display shows the ATM cell header details.

Figure 2-4 shows an example of the Header and Payload display format with a 32 bit SIGPHY interface with the AAL option set to AAL3/4.

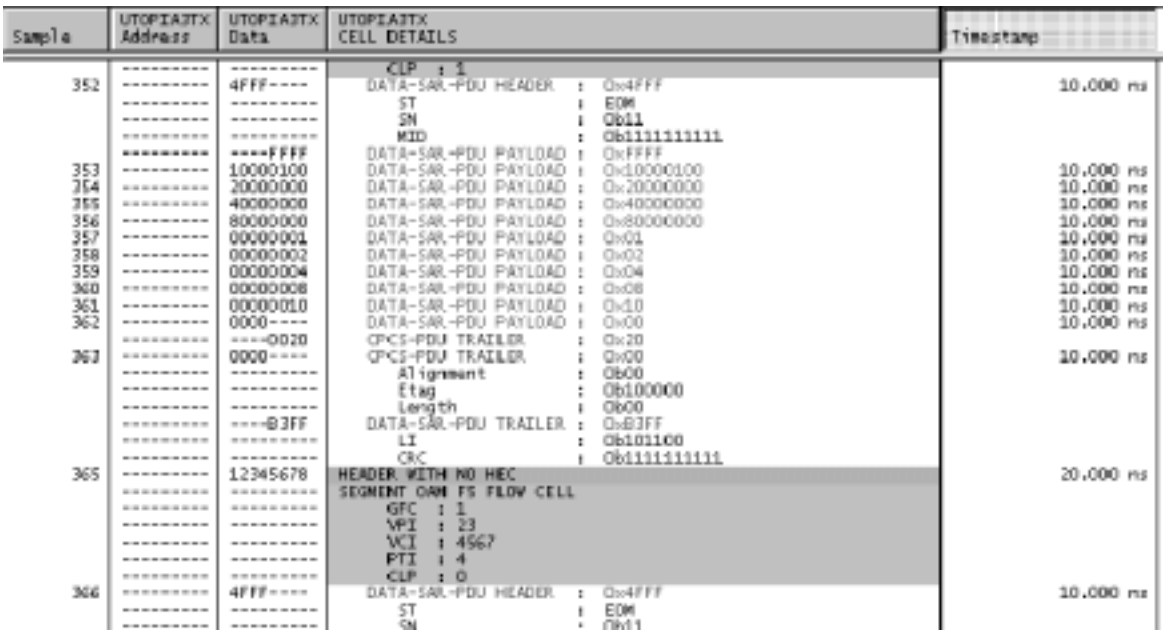


Figure 2-4: Example of Header and Payload display format

Header Only Display Format

The Header Only Display Format shows the header details irrespective of the Capture option in custom clocking. For correct disassembly, set the appropriate Header option both in acquisition and disassembly.

Figure 2–5 shows an example of the Header Only display format with a 32 bit SIGPHY interface.

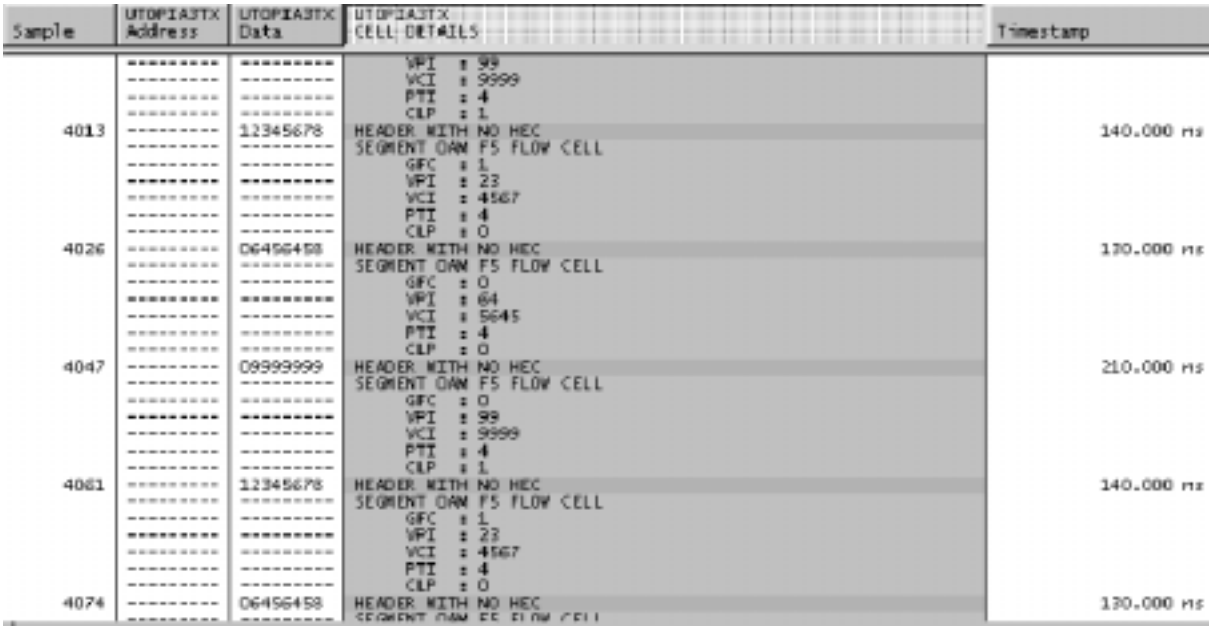


Figure 2–5: Example of Header Only display format

UTOPIA3 Specific Labels

This section gives information about the labels used in TMS833 UTOPIA3 support. Table 2–7 gives the Utopia3 specific labels and the definition of each.

Table 2–7: UTOPIA3 specific labels

UTOPIA3 specific label (Mnemonics)	Definition
HEADER WITH HEC	Refers to the Header type which contains HEC field according to the user selected option
HEADER WITH NO HEC	Refers to the Header type which does not contain HEC field according to the user selected option
PAYLOAD	Refers to the ATM cell payload
*** UNKNOWN ***	Displayed when an unknown combination of control bits occurs
HEADER SAMPLE Byte Number	Header byte of the Atm Cell. Byte number refers to the corresponding header byte. For example: HEADER SAMPLE 1 refers to the first header byte of the cell

Table 2-7: UTOPIA3 specific labels (Cont.)

UTOPIA3 specific label (Mnemonics)	Definition
*** HEADER TRUNCATED ***	Displayed when all the header bytes are not available for disassembly
*** PAYLOAD TRUNCATED ***	Displayed when all the 48 bytes of payload are not available for disassembly
*** CELL TRUNCATED ***	Displayed when all bytes of ATM cell are not available for disassembly. This happens at the start and end of acquisition
*** INVALID DATA ***	Displayed when an invalid cycle occurs
ATM NOT READY	Displayed when the acquisition is done in single physical mode. This label is displayed for those cycles where the ATM layer device is not ready for the transaction.
PHY NOT READY	Displayed when the acquisition is done in single physical mode. This label is displayed for those cycles where the physical layer device is not ready for the transaction.
POLLING CYCLES	Displayed when polling cycles are acquired from multi-physical interface

For the following labels, refer to B-ISDN ATM layer specification ITU-T I.361.

ATM cell header details:

GFC
VPI
VCI
PTI
CLP
HEC
UDF2
UDF3
UDF4

The following strings are displayed corresponding to the preassigned header fields:

UNASSIGNED CELL
INVALID
META-SIGNALLING
GENERAL BROADCAST SIGNALLING
POINT-TO-POINT SIGNALLING
RESERVED FOR FUTURE FUNCTIONS
RESERVED FOR FUTURE VP FUNCTIONS
RESERVED FOR PRIVATE NETWORK USE

SEGMENT OAM F4 FLOW CELL
END-TO-END OAM F4 FLOW CELL
VP RESOURCE MANAGEMENT CELL
SEGMENT OAM F5 FLOW CELL
END TO END OAM F5 FLOW CELL
VC RESOURCE MANAGEMENT CELL
RESERVED FOR FUTURE VC FUNCTIONS
RESERVED FOR FUTURE FUNCTIONS
NNI SIGNALLING
NOT PRE_ASSIGNED

For the following labels, refer to B-ISDN ATM Adaptation Layer Specification ITU-T I.363.1.

AAL1:

SAR-PDU HEADER
SN
SN-CSI Bit
SN-Sequence Count Field
SNP Field
SNP-CRC Field Bit
SNP-Even Parity Bit
SAR-PDU PAYLOAD

For the following labels, refer to B-ISDN ATM Adaptation Layer Specification ITU-T I.363.2.

AAL 2:

CPS-PDU Start Field
CPS-PDU Offset Field
CPS-PDU Sequence Number
CPS-PDU Parity
CPS-PDU PAYLOAD
CPS-PDU PACKET HEADER
CPS-PDU Channel Identifier
CPS-PDU PACKET PAYLOAD
CPS-PDU Length Indicator
CPS-PDU HEC
CPS-PDU UUI

For the following labels refer to B-ISDN ATM Adaptation Layer Specification ITU-T I.363.3.

AAL3/4:

DATA-SAR-PDU HEADER
ABORT-SAR-PDU HEADER
BOM

COM
EOM
SSM
ST
SN
MID
ABORT-SAR-PDU TRAILER
DATA-SAR-PDU TRAILER
LI
CRC
CPCS-PDU HEADER
CPI
Btag
Basize
ABORT-SAR-PDU PAYLOAD
DATA-SAR-PDU PAYLOAD
CPCS-PDU TRAILER
Alignment
Etag
Length
UNUSED DATA

For the following labels refer to B-ISDN ATM Adaptation Layer Specification ITU-T I.363.5.

AAL 5:

SAR-PDU PAYLOAD
CPCS-UU
CPCS-CPI
CPCS SDU Length
CPCS-CRC

Changing How Data is Displayed

The TMS833 UTOPIA3 support package allows you to further modify display data to suit your needs. You can make optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the TMS833 UTOPIA3 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles

Optional Display Selections

Table 2–8 shows the logic analyzer disassembly display options.

Table 2–8: Logic analyzer disassembly display options

Description	Option
Show:	All Cycles (Default) Header and Payload Header Only
Highlight:	Disabled
Disassemble Across Gaps:	Yes No (Default)

All Cycles. Along with the "All Cycles" option in custom clocking, the All Cycles provides disassembly of all the cycles including those where valid data transfers are not available. The All Cycles option displays all the valid ATM cell headers and their payloads, any Invalid cycles, and Polling cycles that occur.

Header and Payload. Along with the "All Cycles" or "Header and Payload" option in custom clocking, if you select the "Header and Payload" option in the disassembly properties, the disassembly shows header details and payload information. In addition, if AAL type is chosen in disassembly, the payload is analyzed to show details of AAL SAR-PDU. If acquisition uses the "Header Only" option, the display shows only the ATM cell header details.

Header Only. With this option, the disassembly consists of only the header details irrespective of the acquisition mode "Capture". If an incorrect "Header" option is chosen during acquisition, the disassembly is incorrect. For correct disassembly, set the same "Header" option in both acquisition and disassembly.

The header is segregated and displayed as different fields and the meaning (for example, the kind of cell) is interpreted according to the ITU-T recommendation I.361 and displayed.

Bus Specific Fields

Along with the optional selections described in the logic analyzer online help, you can change displayed data in the following ways.

Data_Width. Use the Data_Width option to distinguish the width of the data path. The data width can be any one of the following.

32 bit (default)
16 bit
8 bit

Header. Use the Header option depending on the type of ATM Cells used. Select one of the following options:

Does not contain HEC (default)
Contains HEC

Table 2–9 shows the options that can be selected for the ATM Cell types.

Table 2–9: Options for ATM Cell types

Data width	Type of ATM cell	Select option
8 bits	52 byte	Does not contain HEC
16 bits	52 byte	Does not contain HEC
32 bits	52 byte	Does not contain HEC
8 bits	53 byte	Contains HEC
16 bits	54 byte	Contains HEC
32 bits	56 byte	Contains HEC

Number of PHY Ports. The Utopia Level 3 interface has three interface modes: SIGPHY, MULPHY-DSI, and MULPHY-POLLING. Select one of the following options.

- SIGPHY (default) (Single PHY interface)

If you select the SIGPHY option, one ATM layer port and one PHY layer port are connected. No address information is available and a single TxClav and RxClav signal exists. SIGPHY is the default selection.

- MULPHY-DSI (Multiple PHY interface Direct status indication)

If you select the MULPHY-DSI option, one ATM layer port and Multiple physical layer ports are connected. The transaction on the bus includes the address information and the additional TxClav[3:1] signals. In this mode, you can connect a maximum of four physical ports to the ATM device. Each port uses a dedicated Tx/RxClav line for handshaking. For this option, the Number of Addr Lines should be set to 4.

- MULPHY-POLLING (Multiple PHY interface under polling)

In the MULPHY-POLLING mode, only one Tx/RxClav signal exists. The physical port to which the ATM device transmits or receives is decided by polling the single Tx/RxClav signal and presenting device addresses on the address bus.

Number of Addr Lines. You can edit this option and enter the number of address lines used in Multi-Physical mode. For correct disassembly, connect the address lines with channel D0(0) as the LSB (least significant bit). Connect the address lines such that all lower order lines are used before connecting the higher order address lines. The support recognizes up to 128 ports which means that you can connect at most seven address lines. Depending on the number of address lines entered, the other address entries are dashed out in the display. The default value in this field is 0 signifying the default selection of Single Physical interface under the Number of PHY devices menu.

Type of Interface. You can select the type of interface by selecting one of the two available options.

- UNI (default)

Select the UNI option to display the header fields including the Generic Flow Control (GFC). The VPI field width is 8 bits, the VCI field width is 16 bits, PTI field width is 3 bits, and CLP field width is 1 bit.

- NNI

Select the NNI option to display the header fields (does not include GFC). The subsequent field, VPI, is 12 bits in length instead of 8 bits as in UNI.

Type of AAL. Select the Type of AAL option to indicate how the payload information must be interpreted. The format of the SAR-PDUs displayed depends on this option. Select the AAL type from the available options.

AAL 0 (default)
AAL 1
AAL 2
AAL 3/4
AAL 5

Trigger Programs

This section describes how to install and load trigger programs. A trigger library containing programs that can trigger on preassigned header field combinations is provided on your disk. The preassigned header field combinations are restricted to the combinations mentioned in the ITU-T recommendation I.361 (February 1999).

Installing Trigger Programs

The trigger programs are installed along with the TMS833 UTOPIA3 support package:

- Trigger Programs for the Transmit Interface are in C:\Program Files\TLA 700\ Supports\UTOPIA3TX folder.
- Trigger Programs for the Receive Interface are in C:\Program Files\TLA 700\ Supports\UTOPIA3RX folder.

Loading Trigger Programs

To load a trigger program from UTOPIA3TX or UTOPIA3RX folders, follow these steps:

1. Load the support package.
2. From the system window, click the 

Trigger button.
3. From the Trigger window, click the  Load Trigger Toolbar button.

4. From the Load LA Trigger dialog box, click the Browse button. Figure 2-6 shows the Load LA Trigger screen.

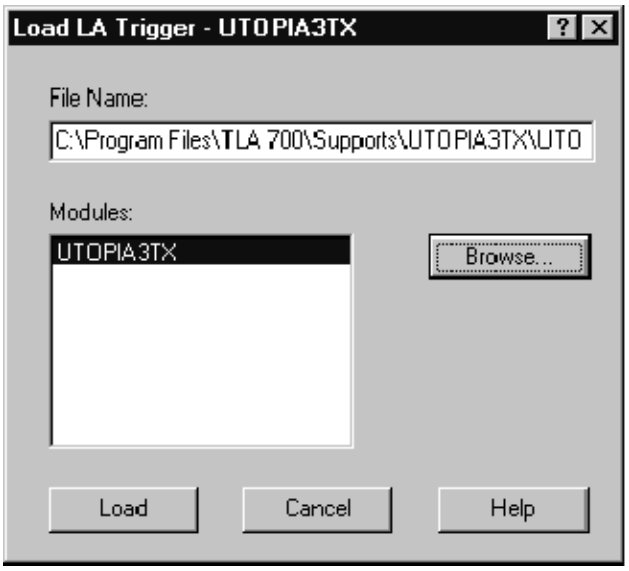


Figure 2-6: Loading trigger programs

Select the Transmit Trigger Programs from the path C:\Program Files\TLA 700\ Supports\UTOPIA3TX.

Select the Receive Trigger Programs from the path C:\Program Files\TLA 700\ Supports\UTOPIA3RX.

5. Select a trigger program from the list.
6. Click Open to apply the selection.
7. Click Load to load the trigger program into the module.

For more information, refer to the logic analyzer online help and the logic analyzer user manual.

The trigger programs follow these conventions:

Bits with the lowest numbers are treated as LSB bits and bits with the highest numbers are treated as MSB bits.

For example: D15.....D0
(MSB) (LSB)

File Name Conventions for the Transmit Interface. Trigger programs have the following file naming conventions.

UTOPIA3TX (For Transmit Interface): UTOPIA3TX_TrigOn_DataWidth_InterfaceType_Preassigned Cell Type.tla,

where,

- DataWidth

32 bit: Logic analyzer file names with the 32-bit suffix are the trigger programs to be used when the data path width is 32 bit.

16 bit: Logic analyzer file names with the 16-bit suffix are the trigger programs to be used when the data path width is 16 bit.

8 bit: Logic analyzer file names with the 8-bit suffix are the trigger programs to be used when the data path width is 8 bit.

- InterfaceType

UNI: Logic analyzer file names with the UNI suffix are the trigger programs to be used when the interface is “User Network Interface”.

NNI: Logic analyzer file names with the NNI suffix are the trigger programs to be used when the interface is “Network Node Interface”.

- Preassigned Cell Type

These are the various cell types based on the preassigned header field combinations as mentioned in the ITU-T Recommendation I.361 (February 1999). The cell types have preassigned combinations of VPI, VCI, PTI, and CLP values at UNI (User Network Interface) and NNI (Network Node Interface).

File Name Conventions for the Receive Interface. Trigger programs have the following file naming conventions.

UTOPIA3RX_TrigOn_DataWidth_InterfaceType_Preassigned Cell Type.tla

where,

- DataWidth

32 bit: Logic analyzer file names with the 32-bit suffix are the trigger programs to be used when the data path width is 32 bit.

16 bit: Logic analyzer file names with the 16-bit suffix are the trigger programs to be used when the data path width is 16 bit.

8 bit: Logic analyzer file names with the 8-bit suffix are the trigger programs to be used when the data path width is 8 bit.

- Interface Type

UNI: Logic analyzer file names with the UNI suffix are the trigger programs to be used when the interface is “User Network Interface”.

NNI: Logic analyzer file names with the NNI suffix are the trigger programs to be used when the interface is “Network Node Interface”’.

- Preassigned Cell Type

These are the various cell types based on the preassigned header field combinations as mentioned in the ITU-T Recommendation I.361 (February 1999). The cell types have preassigned combinations of VPI, VCI, PTI, and CLP values at UNI (User Network Interface) and NNI (Network Node Interface).

NOTE*. Trigger programs can trigger only on the preassigned header combination. You cannot trigger on various other combinations with the trigger library provided. You can write your own trigger programs based on your requirement.*

Trigger Programs for UTOPIA3 Support

The various preassigned cells for which the trigger programs have been provided for the UNI (User Network Interface) are:

Meta-signalling cell
General broadcast signalling cell
Point-to-point signalling cell
Segment OAM F4 flow cell
End-to-end OAM F4 flow cell
VP resource management cell
Segment OAM F5 flow cell
End-to-end OAM F5 flow cell

The various preassigned cells for which the trigger programs have been provided for the NNI (Network Node Interface) are:

NNI-signalling cell
Segment OAM F4 flow cell
End-to-end OAM F4 flow cell
VP resource management cell
Segment OAM F5 flow cell
End-to-end OAM F5 flow cell

Reference

Symbol and Channel Assignment Tables

This section lists the symbol tables and channel assignment tables for disassembly and timing.

Symbol Tables

The TMS833 support package supplies two symbol table files for the UTOPIA3, the Transmit and Receive Interfaces.

The UTOPIA3RX_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group in UTOPIA3 Receive support. The UTOPIA3TX_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group in UTOPIA3 Transmit support. This also applies to other symbol tables.

Symbol tables are generally not for use in timing or UTOPIA3 support disassembly.

Tables 3–1 through 3–2 show the definitions for name, bit pattern, and meaning of the group symbols in Control file for Utopia Level 3 Transmit and Receive interface support.

Table 3-1: UTOPIA3RX_Ctrl group symbol table definitions

Symbol	Control group value RxPrty RxSOC RxEnb*	Description
Rx_in_progress	X 0 0	Reception in progress
Start_of_Cell	X 1 0	Start of Header
ATM/PHY_NotRdy	X 0 1	ATM or PHY is not ready

Table 3-2: UTOPIA3TX_Ctrl group symbol table definitions

Symbol	Control group value TxPrty TxSOC TxEnb*	Description
Tx_in_progress	X 0 0	Transmission in progress
Start_of_Cell	X 1 0	Start of Cell
ATM/PHY_NotRdy	X 0 1	ATM or PHY is not ready

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as for the Address channel group.

Channel Assignment Tables

Channel assignments shown in Table 3-3 through Table 3-10 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules, unless otherwise noted.
- An asterisk (*) following a signal name indicates an active low signal.

Channel Assignments for UTOPIA3 Receive Interface

Table 3-3 shows the probe section and channel assignments for the logic analyzer Address group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-3: Address group channel assignments for UTOPIA3RX signals

Section:channel	UTOPIA3RX signal name
D0:6 (MSB)	RxAddr6
D0:5	RxAddr5
D0:4	RxAddr4
D0:3	RxAddr3
D0:2	RxAddr2
D0:1	RxAddr1
D0:0 (LSB)	RxAddr0

Table 3–4 shows the probe section and channel assignments for the Data group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-4: Data group channel assignments for UTOPIA3RX signals

Section:channel	UTOPIA3RX signal name
A3:7 (MSB)	RxData31
A3:6	RxData30
A3:5	RxData29
A3:4	RxData28
A3:3	RxData27
A3:2	RxData26
A3:1	RxData25
A3:0	RxData24
A2:7	RxData23
A2:6	RxData22
A2:5	RxData21
A2:4	RxData20
A2:3	RxData19
A2:2	RxData18
A2:1	RxData17
A2:0	RxData16
A1:7	RxData15
A1:6	RxData14
A1:5	RxData13
A1:4	RxData12
A1:3	RxData11
A1:2	RxData10
A1:1	RxData9
A1:0	RxData8
A0:7	RxData7
A0:6	RxData6
A0:5	RxData5
A0:4	RxData4
A0:3	RxData3
A0:2	RxData2

Table 3-4: Data group channel assignments for UTOPIA3RX signals (cont.)

Section:channel	UTOPIA3RX signal name
A0:1	RxData1
A0:0 (LSB)	RxData0

Table 3–5 shows the probe section and channel assignments for the Control group and the bus signal to which each channel connects. By default, this channel group is displayed in symbols. The symbol table file name is UTOPIA3RX_Ctrl

Table 3-5: Control group channel assignments for UTOPIA3RX signals

Section:channel	UTOPIA3RX signal name
C2:4 (MSB)	RxPrty
C2:1	RxSOC
C2:0 (LSB)	RxEnb*

Table 3–6 shows the probe section and channel assignments for the RXCLAV (Cell Available) group and the bus signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3-6: RXCLAV group channel assignments for UTOPIA3RX signals

Section:channel	UTOPIA3RX signal name
C3:7 (MSB)	RxClav3
C3:6	RxClav2
C3:3	RxClav1
C3:2 (LSB)	RxClav0

Channel Assignments for UTOPIA3 Transmit Interface

Table 3–7 shows the probe section and channel assignments for the Address group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-7: Address group channel assignments for UTOPIA3TX signals

Section:channel	UTOPIA3TX signal name
D0:6 (MSB)	TxAddr6
D0:5	TxAddr5
D0:4	TxAddr4

Table 3-7: Address group channel assignments for UTOPIA3TX signals (cont.)

Section:channel	UTOPIA3TX signal name
D0:3	TxAddr3
D0:2	TxAddr2
D0:1	TxAddr1
D0:0 (LSB)	TxAddr0

Table 3–8 shows the probe section and channel assignments for the Data group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-8: Data group channel assignments for UTOPIA3TX signals

Section:channel	UTOPIA3TX signal name
A3:7 (MSB)	TxData31
A3:6	TxData30
A3:5	TxData29
A3:4	TxData28
A3:3	TxData27
A3:2	TxData26
A3:1	TxData25
A3:0	TxData24
A2:7	TxData23
A2:6	TxData22
A2:5	TxData21
A2:4	TxData20
A2:3	TxData19
A2:2	TxData18
A2:1	TxData17
A2:0	TxData16
A1:7	TxData15
A1:6	TxData14
A1:5	TxData13
A1:4	TxData12
A1:3	TxData11

Table 3-8: Data group channel assignments for UTOPIA3TX signals (cont.)

Section:channel	UTOPIA3TX signal name
A1:2	TxData10
A1:1	TxData9
A1:0	TxData8
A0:7	TxData7
A0:6	TxData6
A0:5	TxData5
A0:4	TxData4
A0:3	TxData3
A0:2	TxData2
A0:1	TxData1
A0:0	TxData0

Table 3–9 shows the probe section and channel assignments for the logic analyzer Control group and the bus signal to which each channel connects. By default, this channel group is displayed in symbols. The symbol table file name is UTOPIA3TX_Ctrl on the logic analyzer.

Table 3-9: Control group channel assignments for UTOPIA3TX signals

Section:channel	UTOPIA3TX signal name
C2:4 (MSB)	TxPrty
C2:1	TxSOC
C2:0 (LSB)	TxEnb*

Table 3–10 shows the probe section and channel assignments for the TXCLAV group and the bus signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3-10: TXCLAV group channel assignments for UTOPIA3TX signals

Section:channel	UTOPIA3TX signal name
C3:7 (MSB)	TxClav3
C3:6	TxClav2
C3:3	TxClav1
C3:2 (LSB)	TxClav0

Logic Analyzer Channels not Connected

Extra channels that are not connected in the TMS833 UTOPIA3 support are:

CLK2:0
C3:5, C3:4, C3:1, C3:0
D0:7, D1:7–0
C2:7, C2:6, C2:5, C2:3, C2:2

Clock and Qualifier Channels

Table 3–11 and Table 3–12 show the probe section and channel assignments for the clock probes (not part of any group), and the TMS833 UTOPIA3 signal to which each channel connects.

Table 3-11: Clock channel assignments for UTOPIA3RX

Logic analyzer section and probe	UTOPIA3RX signal name
CLK:3	RxClk

Table 3-12: Clock channel assignments for UTOPIA3TX

Logic analyzer section and probe	UTOPIA3TX signal name
CLK:3	TxClk

Tables 3–13 through 3–14 list the qualifier channel assignments for the Utopia3 Receive and Transmit interfaces.

Table 3-13: Qualifier channel assignments for UTOPIA3RX

Logic analyzer section and probe	UTOPIA3RX signal name
C2:0	RxEnb*
C2:1	RxSOC

Table 3-14: Qualifier channel assignments for UTOPIA3TX

Logic analyzer section and probe	UTOPIA3TX signal name
C2:0	TxEnb*
C2:1	TxSOC

***NOTE**. An asterisk (*) indicates an active low signal.*

Signals not Required for Disassembly

Tables 3–15 and 3–16 show the signals not required for disassembly of the Utopia3 bus signals.

Table 3-15: Signals not required for UTOPIA3TX support

Section:channel	UTOPIA3TX signal name
C2:4	TxPrty
C3:7	TxClav3
C3:6	TxClav2
C3:3	TxClav1

Table 3-16: Signals not required for UTOPIA3RX support

Section:channel	UTOPIA3RX signal name
C2:4	RxPrty
C3:7	RxClav3
C3:6	RxClav2
C3:3	RxClav1

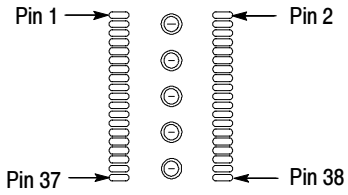
Signal Source To Mictor Connections

For design purposes, you may need to make connections between the Signal Source and the Mictor pins of the P6434 Mass Termination Probe. Refer to the *P6434 Mass Termination Probe* manual, Tektronix part number 070-9793-XX, for more information on mechanical specifications. Tables 3–18 through 3–21 show the Signal Source to Mictor pin connections.

***NOTE**. To preserve signal quality in the target system, it is recommended that a 180 Ω resistor be connected in series between each ball pad of the Signal Source and each pin of the Mictor connector. The resistor must be within 1/2 inch of the ball pad of the Signal Source.*

The recommended pin assignment is the AMP pin assignment, because the AMP circuit board layout model and other commercial CAD packages use the AMP numbering scheme. See Table 3–17.

Table 3-17: Recommended pin assignments for a Mictor connector (component side)

Type of pin assignment	Comments
Recommended  **AMP Pin Assignment**	Recommended. This pin assignment is the industry standard and is what we recommend that you use.

Connections for UTOPIA3 Receive Interface

Tables 3–18 through 3–19 show the mictor pin connections for the UTOPIA3 Receive Interface.

Table 3-18: Signal Source to Mictor connections for Mictor 1 pins for UTOPIA3RX

AMP Mictor pin number	Logic analyzer channel name	UTOPIA3RX signal name	Required/Not required for disassembly
Mictor 1 pin 01	Not Connected	Not Connected	
Mictor 1 pin 03	Not Connected	Not Connected	

Table 3-18: Signal Source to Mictor connections for Mictor 1 pins for UTOPIA3RX (cont.)

AMP Mictor pin number	Logic analyzer channel name	UTOPIA3RX signal name	Required/Not required for disassembly
Mictor 1 pin 05	CLK:0	Not Connected	
Mictor 1 pin 07	A3:7	RxData31	Required
Mictor 1 pin 09	A3:6	RxData30	Required
Mictor 1 pin 11	A3:5	RxData29	Required
Mictor 1 pin 13	A3:4	RxData28	Required
Mictor 1 pin 15	A3:3	RxData27	Required
Mictor 1 pin 17	A3:2	RxData26	Required
Mictor 1 pin 19	A3:1	RxData25	Required
Mictor 1 pin 21	A3:0	RxData24	Required
Mictor 1 pin 23	A2:7	RxData23	Required
Mictor 1 pin 25	A2:6	RxData22	Required
Mictor 1 pin 27	A2:5	RxData21	Required
Mictor 1 pin 29	A2:4	RxData20	Required
Mictor 1 pin 31	A2:3	RxData19	Required
Mictor 1 pin 33	A2:2	RxData18	Required
Mictor 1 pin 35	A2:1	RxData17	Required
Mictor 1 pin 37	A2:0	RxData16	Required
Mictor 1 pin 38	A0:0	RxData0	Required
Mictor 1 pin 36	A0:1	RxData1	Required
Mictor 1 pin 34	A0:2	RxData2	Required
Mictor 1 pin 32	A0:3	RxData3	Required
Mictor 1 pin 30	A0:4	RxData4	Required
Mictor 1 pin 28	A0:5	RxData5	Required
Mictor 1 pin 26	A0:6	RxData6	Required
Mictor 1 pin 24	A0:7	RxData7	Required
Mictor 1 pin 22	A1:0	RxData8	Required
Mictor 1 pin 20	A1:1	RxData9	Required
Mictor 1 pin 18	A1:2	RxData10	Required
Mictor 1 pin 16	A1:3	RxData11	Required
Mictor 1 pin 14	A1:4	RxData12	Required
Mictor 1 pin 12	A1:5	RxData13	Required

Table 3-18: Signal Source to Mictor connections for Mictor 1 pins for UTOPIA3RX (cont.)

AMP Mictor pin number	Logic analyzer channel name	UTOPIA3RX signal name	Required/Not required for disassembly
Mictor 1 pin 10	A1:6	RxData14	Required
Mictor 1 pin 08	A1:7	RxData15	Required
Mictor 1 pin 06	CLK:1	Not Connected	
Mictor 1 pin 04	Not Connected	Not Connected	
Mictor 1 pin 02	Not Connected	Not Connected	

Table 3-19: Signal Source to Mictor connections for Mictor 2 pins for UTOPIA3RX

AMP Mictor pin number	Logic analyzer channel name	UTOPIA3RX signal name	Required/Not required for disassembly
Mictor 2 pin 01	Not Connected	Not Connected	
Mictor 2 pin 03	Not Connected	Not Connected	
Mictor 2 pin 05	CLK:3	RxClk	Required
Mictor 2 pin 07	C3:7	RxClav3	Not required
Mictor 2 pin 09	C3:6	RxClav2	Not required
Mictor 2 pin 11	C3:5	Not Connected	
Mictor 2 pin 13	C3:4	Not Connected	
Mictor 2 pin 15	C3:3	RxClav1	Not required
Mictor 2 pin 17	C3:2	RxClav0	Required
Mictor 2 pin 19	C3:1	Not Connected	
Mictor 2 pin 21	C3:0	Not Connected	
Mictor 2 pin 23	C2:7	Not Connected	
Mictor 2 pin 25	C2:6	Not Connected	
Mictor 2 pin 27	C2:5	Not Connected	
Mictor 2 pin 29	C2:4	RxPrty	Not required
Mictor 2 pin 31	C2:3	Not Connected	
Mictor 2 pin 33	C2:2	Not Connected	
Mictor 2 pin 35	C2:1	RxSOC	Required
Mictor 2 pin 37	C2:0	RxEnb*	Required

Table 3-19: Signal Source to Mictor connections for Mictor 2 pins for UTOPIA3RX (cont.)

AMP Mictor pin number	Logic analyzer channel name	UTOPIA3RX signal name	Required/Not required for disassembly
Mictor 2 pin 38	D0:0	RxAddr0	Required
Mictor 2 pin 36	D0:1	RxAddr1	Required
Mictor 2 pin 34	D0:2	RxAddr2	Required
Mictor 2 pin 32	D0:3	RxAddr3	Required
Mictor 2 pin 30	D0:4	RxAddr4	Required
Mictor 2 pin 28	D0:5	RxAddr5	Required
Mictor 2 pin 26	D0:6	RxAddr6	Required
Mictor 2 pin 24	D0:7	Not Connected	
Mictor 2 pin 22	D1:0	Not Connected	
Mictor 2 pin 20	D1:1	Not Connected	
Mictor 2 pin 18	D1:2	Not Connected	
Mictor 2 pin 16	D1:3	Not Connected	
Mictor 2 pin 14	D1:4	Not Connected	
Mictor 2 pin 12	D1:5	Not Connected	
Mictor 2 pin 10	D1:6	Not Connected	
Mictor 2 pin 08	D1:7	Not Connected	
Mictor 2 pin 06	CLK:2	Not Connected	
Mictor 2 pin 04	Not Connected	Not Connected	
Mictor 2 pin 02	Not Connected	Not Connected	

Connections for UTOPIA3 Transmit Interface

Tables 3-20 through 3-21 show the mictor pin connections for UTOPIA3 Transmit Interface.

Table 3-20: Signal Source to Mictor connections for Mictor 1 pins for UTOPIA3TX

AMP Mictor pin number	Logic analyzer channel name	UTOPIA3TX signal name	Required/Not required for disassembly
Mictor 1 pin 01	Not Connected	Not Connected	
Mictor 1 pin 03	Not Connected	Not Connected	
Mictor 1 pin 05	CLK:0	Not Connected	

Table 3-20: Signal Source to Mictor connections for Mictor 1 pins for UTOPIA3TX (cont.)

AMP Mictor pin number	Logic analyzer channel name	UTOPIA3TX signal name	Required/Not required for disassembly
Mictor 1 pin 07	A3:7	TxData31	Required
Mictor 1 pin 09	A3:6	TxData30	Required
Mictor 1 pin 11	A3:5	TxData29	Required
Mictor 1 pin 13	A3:4	TxData28	Required
Mictor 1 pin 15	A3:3	TxData27	Required
Mictor 1 pin 17	A3:2	TxData26	Required
Mictor 1 pin 19	A3:1	TxData25	Required
Mictor 1 pin 21	A3:0	TxData24	Required
Mictor 1 pin 23	A2:7	TxData23	Required
Mictor 1 pin 25	A2:6	TxData22	Required
Mictor 1 pin 27	A2:5	TxData21	Required
Mictor 1 pin 29	A2:4	TxData20	Required
Mictor 1 pin 31	A2:3	TxData19	Required
Mictor 1 pin 33	A2:2	TxData18	Required
Mictor 1 pin 35	A2:1	TxData17	Required
Mictor 1 pin 37	A2:0	TxData16	Required
Mictor 1 pin 38	A0:0	TxData0	Required
Mictor 1 pin 36	A0:1	TxData1	Required
Mictor 1 pin 34	A0:2	TxData2	Required
Mictor 1 pin 32	A0:3	TxData3	Required
Mictor 1 pin 30	A0:4	TxData4	Required
Mictor 1 pin 28	A0:5	TxData5	Required
Mictor 1 pin 26	A0:6	TxData6	Required
Mictor 1 pin 24	A0:7	TxData7	Required
Mictor 1 pin 22	A1:0	TxData8	Required
Mictor 1 pin 20	A1:1	TxData9	Required
Mictor 1 pin 18	A1:2	TxData10	Required
Mictor 1 pin 16	A1:3	TxData11	Required
Mictor 1 pin 14	A1:4	TxData12	Required
Mictor 1 pin 12	A1:5	TxData13	Required
Mictor 1 pin 10	A1:6	TxData14	Required

Table 3-20: Signal Source to Mictor connections for Mictor 1 pins for UTOPIA3TX (cont.)

AMP Mictor pin number	Logic analyzer channel name	UTOPIA3TX signal name	Required/Not required for disassembly
Mictor 1 pin 08	A1:7	TxData15	Required
Mictor 1 pin 06	CLK:1	Not Connected	
Mictor 1 pin 04	Not Connected	Not Connected	
Mictor 1 pin 02	Not Connected	Not Connected	

Table 3-21: Signal Source to Mictor connections for Mictor 2 pins for UTOPIA3TX

AMP Mictor pin number	Logic analyzer channel name	UTOPIA3TX signal name	Required/Not required for disassembly
Mictor 2 pin 01	Not Connected	Not Connected	
Mictor 2 pin 03	Not Connected	Not Connected	
Mictor 2 pin 05	CLK:3	TxClk	Required
Mictor 2 pin 07	C3:7	TxClav3	Not required
Mictor 2 pin 09	C3:6	TxClav2	Not required
Mictor 2 pin 11	C3:5	Not Connected	
Mictor 2 pin 13	C3:4	Not Connected	
Mictor 2 pin 15	C3:3	TxClav1	Not required
Mictor 2 pin 17	C3:2	TxClav0	Required
Mictor 2 pin 19	C3:1	Not Connected	
Mictor 2 pin 21	C3:0	Not Connected	
Mictor 2 pin 23	C2:7	Not Connected	
Mictor 2 pin 25	C2:6	Not Connected	
Mictor 2 pin 27	C2:5	Not Connected	
Mictor 2 pin 29	C2:4	TxPrty	Not required
Mictor 2 pin 31	C2:3	Not Connected	
Mictor 2 pin 33	C2:2	Not Connected	
Mictor 2 pin 35	C2:1	TxSOC	Required
Mictor 2 pin 37	C2:0	TxEnb*	Required
Mictor 2 pin 38	D0:0	TxAddr0	Required

Table 3-21: Signal Source to Mictor connections for Mictor 2 pins for UTOPIA3TX (cont.)

AMP Mictor pin number	Logic analyzer channel name	UTOPIA3TX signal name	Required/Not required for disassembly
Mictor 2 pin 36	D0:1	TxAddr1	Required
Mictor 2 pin 34	D0:2	TxAddr2	Required
Mictor 2 pin 32	D0:3	TxAddr3	Required
Mictor 2 pin 30	D0:4	TxAddr4	Required
Mictor 2 pin 28	D0:5	TxAddr5	Required
Mictor 2 pin 26	D0:6	TxAddr6	Required
Mictor 2 pin 24	D0:7	Not Connected	
Mictor 2 pin 22	D1:0	Not Connected	
Mictor 2 pin 20	D1:1	Not Connected	
Mictor 2 pin 18	D1:2	Not Connected	
Mictor 2 pin 16	D1:3	Not Connected	
Mictor 2 pin 14	D1:4	Not Connected	
Mictor 2 pin 12	D1:5	Not Connected	
Mictor 2 pin 10	D1:6	Not Connected	
Mictor 2 pin 08	D1:7	Not Connected	
Mictor 2 pin 06	CLK:2	Not Connected	
Mictor 2 pin 04	Not Connected	Not Connected	
Mictor 2 pin 02	Not Connected	Not Connected	

Specifications

Specifications

This section contains the specifications for the support package.

Specification Tables

Table 4–1 lists the electrical requirements that the target system must produce for the support to acquire correct data.

Table 4–1: Electrical specifications

Characteristics	Requirements
Target system clock rate	
TMS833 specified clock rate	Maximum 104 MHz
Minimum setup time required	
Logic analyzer	2.5 ns
Minimum hold time required	
Logic analyzer	0 ns

Replaceable Parts List

Replaceable Parts List

This section contains a list of the replaceable components and modules for the TMS833 UTOPIA3 support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Using the Replaceable Parts List

The tabular information in the Replaceable Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX, INC.	P.O. BOX 500	BEAVERTON, OR, 97077-0001

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
	071-1146-00			1	MANUAL,TECH INSTRUCTION,UTOPIOA3;TMS833	80009	071-1146-00

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