TLA7SA08 & TLA7SA16 Series
Product Specifications & Performance Verification

Technical Reference Manual

This document applies to TLA System Software V5.7 or higher.

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Preface

This document provides the specifications of the TLA7SA16 and TLA7SA08 Logic Protocol Analyzer Modules for the TLA7012 and TLA7016 mainframes and high-level procedures to verify that the products are functioning correctly.

Related Documentation

The following table lists related documentation that is available for your Tektronix logic analyzer family product. The documentation is available on the TLA Documentation CD included with your instrument and on the Tektronix Web site (www.tektronix.com). Refer to the Tektronix Web site for the most current documentation.

To obtain documentation that is not specified in the table, contact your local Tektronix representative.

Related documentation

Item	Purpose
TLA Quick Start User Manuals	High-level operational overview
Online Help	In-depth operation and UI help
Installation Reference Sheets	High-level installation information
Installation Manuals	Detailed first-time installation information
XYZs of Logic Analyzers	Logic analyzer basics
Declassification and Securities instructions	Data security concerns specific to sanitizing or removing memory devices from Tektronix products
Application notes	Collection of logic analyzer application specific notes
Product Specifications & Performance Verification Procedures	TLA Product specifications and performance verification procedures
TPI.NET Documentation	Detailed information for controlling the logic analyzer using .NET
Field upgrade kits	Upgrade information for your logic analyzer
Optional Service Manuals	Self-service documentation for modules and mainframes

Specifications and Characteristics

All specifications in this document are guaranteed unless noted *Typical*. Typical characteristics describe typical or average performance and provide useful reference information.

Specifications that are marked with the ✓ symbol are checked directly (or indirectly) at your nearest Tektronix location.

The performance limits in this specification are valid with these conditions:

- The instrument must be in an environment with temperature, altitude, humidity, and vibration within the operating limits described in these specifications.
- The instrument must have had a warm-up period of at least 30 minutes.

For modules, the performance limits in this specification are valid with these conditions:

- The logic protocol analyzer modules must be installed in a Logic Analyzer Mainframe.
- The module must have been calibrated/adjusted at an ambient temperature between +20 °C and +30 °C.

Atmospheric Characteristics

The following table lists the Atmospheric characteristics of the Tektronix logic protocol analyzers.

Table 1: Atmospheric characteristics

Characteristic	Description
Temperature	*Operating (no media in CD or DVD drive of the mainframe)*
	0 °C to +40 °C, 15 °C/hr maximum gradient, noncondensing, derated 1°C per 300 meters (~1000 ft) above 1500 meters (~5000 ft) altitude
	Nonoperating (no media)
	-20 °C to +60 °C, 15 °C/hr maximum gradient, without disk media installed in disk drives
Relative Humidity	*Operating (no media)*
	5% to 95% relative humidity (%RH), up to +30 °C
	5% to 75% relative humidity above +30 °C up to +40 °C, noncondensing and as limited by a Maximum Wet-bulb Temperature of +29.4 °C
	Nonoperating (no media)
	5% to 95% relative humidity (%RH) up to +30 °C, 75% RH up to 60 °C, noncondensing, and as limited by a Maximum Wet-Bulb Temperature of +40 °C (derates relative humidity to 20% RH at +60 °C)

Table 1: Atmospheric characteristics (cont.)

Characteristic	Description
Altitude	*Operating*
	Up to 3,000 meters (~10,000 ft), derated 1 °C per 300 meters (~1000 ft) above 1500 meters (~5000 ft) altitude
	Nonoperating
	Up to 12,000 meters (~40,000 ft)

TLA7SA08 & TLA7SA16 Logic Protocol Analyzer Modules Specifications

Table 2: Data input for differential probes

Characteristic	Description
Data rate	2.5 Gbps and 5.0 Gbps (modulated from -10% to +10%) 8.0 Gbps (modulated from -10% and +5%)
Number of FTS packets required to resynchronize following the L0s exit *(Typical)*	Gen1: 20 ns EIDLE minimum ÷ 4 FTS Gen2: 20 ns EIDLE minimum ÷ 1 EIEOS + 6 FTS Gen3: 20 ns EIDLE minimum ÷ 1 EIEOS + 4 FTS

Table 3: Width and depth

Characteristic		Description
Number of inputs	TLA7SA08	8 differential inputs, x4 link
	TLA7SA16	16 differential inputs, x8 link
Acquisition memory depth	TLA7SA08	160 mega samples per differential input (4 GB physical memory total)
	TLA7SA16	160 mega samples per differential input (8 GB physical memory total)

Table 4: Clocking

Characteristic	Description
External reference clock	
Minimum peak-to-peak differential input voltage *(Typical)*	150 mV
Absolute differential input voltage limit *(Typical)*	2.5 V
Clock frequency *(Typical)*	100 MHz 90 MHz through 110 MHz when acquiring frequency margined data
Frequency tolerance *(Typical)*	±300 ppm

Table 5: SerDes

Characteristic	Description
Clock encoding standard	Supports 8b/10b encoded serial data Supports 128b/130b encoded serial data

Table 6: Lane processing

Characteristic	Description	
Time required to dynamically change the data rate *(Typical)*	200 ns minimum EIDLE time Detials: ■ Maximum time to change to Gen 1 rate: 2 TS1 ■ Maximum time to change to Gen 2 rate: 1 EIEOS + 3 TS1 ■ Maximum time to change to Gen 3 rate: 1 EIEOS + 6 TS1	
Polarity inversion	Available on all inputs	
Descrambling polynomial used	Gen1/Gen2	$X^{16} + X^5 + X^4 + X^3 + X^1$
	Gen3	$X^{23} + X^{21} + X^{16} + X^8 + X^5 + X^2 + 1$
Autoset lane number	Each lane has a training sequence recognizer that stores the last known lane number assignment. Can only autoset polarity at Gen 1 and Gen 2 rates. The SUT must provide TS1 training sequences for the Autoset to work. Changes are not applied automatically. The software polls the lane number registers and then prompts the user to use Autoset when changes are detected.	
Autoset lane polarity	Each lane has a training sequence recognizer that stores the last known lane polarity. The SUT must provide TS1 training sequences for the Autoset to work. Changes are not applied automatically. The software polls the lane number registers and then prompts the user to use Autoset when changes are detected.	
Auto-track lane rate	When the auto-track feature is enabled, data is acquired at the current data rate. Training sequences must be acquired for the module to change rates. EIOS packets must be acquired to initiate the speed change. The signaling levels (specified above) must be met.	
Force lane rate	When forced, data is acquired at the specified rate of 2.5 Gbps, 5.0 Gbps, or 8.0 Gbps.	
Lane data groups	Reports the 8b/10b symbol information acquired from each lane or internal module status symbols if no data is available.	
	The following information for Gen 1 and Gen2 is available when 8b/10b symbols are acquired: ■ Disparity error indicator ■ Running disparity error indicator ■ K-code/D-code indicator ■ 8-bit code value ■ Full 10b value if an 8b/10b code error is encountered	
	Gen 3: Reports the 8b symbol information acquired from each lane and 2 bit Sync Character bits, or internal module status symbols if no symbol data is available	

Table 7: Link processing

Characteristic	Description	
Cross-point switch	Any-to-any channel mapping	
Lane alignment entrance	If the link is not currently in the aligned state, the hardware will automatically attempt lane-to-lane alignment (deskew) on any of the following conditions: ■ Skip ordered set ■ Electrical idle exit ordered set ■ Entry/exit of a TS2 training sequence ■ Start data stream ordered set (Gen 3 only)	
Lane alignment exit	If the link is currently in the aligned state, the hardware will abandon the current alignment (deskew) settings on any of the following conditions: ■ Electrical idle ordered set ■ Misaligned COM symbol across the active lanes ■ Data rate mismatch occurs on the lanes within the link ■ Any lane wakes up from electrical idle	
Lane alignment exit recovery	32 symbol times	
Maximum skew between lanes of a link	12 symbol times This defines the maximum skew between lanes of a link that the lane alignment module can deskew	
Link support	TLA7SA08	One unidirectional x8, x4, x2, or x1 link One bidirectional x4, x2, or x1 link
	TLA7SA16	One unidirectional x16, x8, x4, x2, or x1 link One bidirectional x8, x4, x2, or x1 link
Auto-track link width	Link-width changes are automatically tracked; this feature is always enabled. Real-time resources that depend on link width (such as packet recognizers) remain unusable through any change in link width.	

Table 8: Event recognizer resources

Characteristic		Description
DLLP packet recognizers		4 per link direction Each recognizer supports full 32-bit mask and match on the DLLP packet excluding the CRC and framing bytes. Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned.
TLP packet recognizers		4 per link direction Each recognizer supports full 32-bit mask and match for the first 4 dwords of the TLP packet excluding the framing and sequence number. Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned.
Symbol sequence recognizers		4 shared between link directions Each recognizer supports full mask and match on each symbol in a sequence up to 16 symbols deep. Any position in the sequence can be marked with a NOT in which case the recognition process will only continue if the current symbol does not satisfy the mask and match logic.
Link event recognizers		4 per link direction Each recognizer is a unique logical OR of the selected link events
Link event:	Disparity error	Asserts when an 8b/10b disparity error is detected on any of the selected lanes. Each lane of the link can be individually included or excluded
	10b Code error	Asserts when an 8b/10b table lookup error is detected on any of the selected lanes. Each lane of the link can be individually included or excluded
	Electrical idle	Asserts when electrical idle is detected on any of the selected lanes. Each lane of the link can be individually included or excluded
	DLLP frame error	Asserts when an SDP start symbol is detected in a non-modulo-4 lane number Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned
	TLP frame error	Asserts when an STP start symbol is detected in a non-modulo-4 lane number Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned
	DLLP CRC error	Asserts when the calculated CRC does not match the CRC value in the packet payload Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned
	Logical idle error	Asserts when packet and ordered set traffic is not active and a non-zero data symbol is detected in any of the active lanes in the link Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned

Table 8: Event recognizer resources (cont.)

Characteristic		Description
	END Bad Packet	Asserts when an End Bad Symbol (Gen 1, Gen 2) or End Bad Token (Gen 3) occurs Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned
	Gen 3 TLP FCRC Error	Asserts when the calculated FCRC does not match the FCRC value in the Gen 3 TLP token Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligning
	Data rate change	Programmed to assert when the link data rate changes: ■ To Gen1 (2.5 Gbps) ■ To Gen2 (5.0 Gbps) ■ To Gen3 (8.0 Gbps) ■ To any rate different than the last known rate Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned
	Link width change	Can be programmed to assert when the link width changes: ■ Downtrain (to any width less than the last known width) ■ Uptrain (to any width more than the last known width) ■ x1, x2, x4, x8, or x16 ■ Not x1, Not x2, Not x4, Not x8, or Not x16 ■ To any width different than the last known width Automatically disqualified when the link status is Rates_Vary, Aligning, or !Aligned

Table 9: Filtering

Characteristic	Description
Bidirectional filtering control	Each direction of a link has independent filter control settings
Idle filtering	Logical idle and electrical idle conditions can be filtered from storage.
Ordered set filtering	The following ordered sets can be selected for filtering from storage: TS1, TS2, SKP, EIOS, FTS, EIEOS SDS (Gen3 only)
DLLP packet filtering	The following DLLP packet types can be selected for filtering from storage: Ack, Nack, PM, FC1, FC2, UpdateFC, Vendor Specific
TLP packet filtering	The following TLP packet types can be selected for filtering from storage: MRd, MRdLk, MWr, IORd, IOWr, CfgRd0, CfgWr0, CfgRd1, CfgWr1, Msg, MsgD, Cpl, CplD, CplLk, CplDLk, FetchAdd, Swap, CAS, LPrfx, EPrfx

Table 10: Trigger state machine

Characteristic	Description
Sequencer states	8
Sequencer rate	The trigger state machine evaluates its logic and can advance states at the symbol rate time. The symbol rate can be Gen 1, Gen 2, or Gen 3.
Event recognizer inputs per state	10 total, eight programmable event recognizer inputs and two dedicated event occurrence counter results.
Event occurrence counters	Two 31-bit event occurrence counters per state. Each counter can be independently programmed to monitor any event recognizer output. The counter actions are automatic. They automatically increment at the rate of the selected event recognizer output. And they automatically reset when their host state is exited.
Global counter-timers	There are four 48-bit signed global counter/timers that are actionable at the rate of the sequencer. Maximum count value = $2^{47} - 1$ Maximum time value = $(2^{47} - 1) \times 3.7$ ns = ~146 hours Counter-timers have a 19 cycle (71.25 ns) latency before the result of any counter-timer action can be tested by the trigger machine event logic.
Backplane trigger	The backplane trigger signal can be recognized as the trigger for the acquisition.
Arm Hold-off	The execution of the trigger state machine can be held off by using the Arm input. The Arm input can be controlled by any other module in the system. If Arm is not explicitly assigned, then the module will automatically arm itself immediately at the beginning of each acquisition.
Backplane signal inputs	Up to four backplane signals can be used as events.
Trigger position	The trigger position is programmable to any data sample.

Table 11: Trigger machine actions

Characteristic	Description
Trigger	Triggers the acquisition memory.
Increment or decrement global counter	Counters can be incremented or decremented. These actions occur at the sequencer rate.
Reset global counter	Counters can be reset.
Start or stop global timer	Timers can be started or stopped. When stopped they hold their present value.
Reset global timer	Timers can be reset. When reset, it continues in the state it was in before the reset action – either running or stopped.
Reset and start or stop global timer	Timer resources can be simultaneously reset and started or reset and stopped in a single action.
Set or clear backplane signal	Any of the four signals can be driven on the backplane to be used by another module. All four backplane signals can be used. If ARM is used then Signal-4 is not available.

Table 11: Trigger machine actions (cont.)

Characteristic	Description
Trigger Out	A Trigger Out signal can be driven to the backplane to trigger other modules.
Goto state	Jump to any state from any state.
Start or stop storage	Turns storage on or off. Once turned off, no samples will be stored until another start storage action is encountered. The data sample containing the condition that stops storage is stored. This ensures that a partial packet is not truncated.

Table 12: Module input/trigger/backplane delay relationships

Characteristic	Description
Real-time signal uncertainty *(Typical)*	Data Rate Offset ±15 ns Gen1 = 98 ns Gen2 = 4 ns Gen3 = 0 ns
External trigger in to probe tip *(Typical)*	690 ns + real-time signal uncertainty
External signal in to probe tip *(Typical)*	715 ns + real-time signal uncertainty
Probe tip to external trigger out *(Typical)*	920 ns + real-time signal uncertainty
Probe tip to external signal out *(Typical)*	900 ns + real-time signal uncertainty
Internal TLA7SAxx to module signal delay *(Typical)*	
TLA7SAxx to TLA7SAxx	144 ns + real-time signal uncertainty
TLA7SAxx to TLA7Axx	114 ns + real-time signal uncertainty
TLA7SAxx to TLA7Bxx	-319 ns + real-time signal uncertainty
TLA7SAxx to TLA7Sxx	-107 ns + real-time signal uncertainty
Internal TLA7SAxx to module trigger delay *(Typical)*	
TLA7SAxx to TLA7SAxx	127 ns + real-time signal uncertainty
TLA7SAxx to TLA7Axx	112 ns + real-time signal uncertainty
TLA7SAxx to TLA7Bxx	-336 ns + real-time signal uncertainty
TLA7SAxx to TLA7Sxx	-153 ns + real-time signal uncertainty
Internal TLA7SAxx to module arm delay *(Typical)*	
TLA7SAxx to TLA7SAxx	136 ns + real-time signal uncertainty
TLA7SAxx to TLA7Axx	104 ns + real-time signal uncertainty
TLA7SAxx to TLA7Bxx	-320 ns + real-time signal uncertainty
TLA7SAxx to TLA7Sxx	-47 ns + real-time signal uncertainty
Internal module to TLA7SAxx signal delay *(Typical)*	
TLA7Axx to TLA7SAxx	154 ns + real-time signal uncertainty
TLA7Bxx to TLA7SAxx	562 ns + real-time signal uncertainty
TLA7Sxx to TLA7SAxx	374 ns + real-time signal uncertainty

Table 12: Module input/trigger/backplane delay relationships (cont.)

Characteristic	Description
Internal module to TLA7SAxx trigger delay *(Typical)*	
TLA7Axx to TLA7SAxx	136 ns + real-time signal uncertainty
TLA7Bxx to TLA7SAxx	545 ns + real-time signal uncertainty
TLA7Sxx to TLA7SAxx	385 ns + real-time signal uncertainty
Internal module to TLA7SAxx arm delay *(Typical)*	
TLA7Axx to TLA7SAxx	130 ns + real-time signal uncertainty
TLA7Bxx to TLA7SAxx	544 ns + real-time signal uncertainty
TLA7SAxx to TLA7SAxx	136 ns + real-time signal uncertainty
TLA7Sxx to TLA7SAxx	363 ns + real-time signal uncertainty

Table 13: Storage control

Characteristic	Description
Initial storage state	The initial storage state can be set to store all or store none at the beginning of each acquisition. The start/stop storage trigger machine actions can be used to change the storage state during the acquisition.

Table 14: Data placement

Characteristic		Description
System time zero placement error *(Typical)*		±3.75 ns + 10 MHz backplane skew
Timestamp accuracy *(Typical)*		±5 ns
Data correlation error *(Typical)*		Timestamp accuracy + System time zero placement error
Timestamp counter		
	Resolution	936 ps
	Duration	292 hours (12 days)
2.4.18 Configuration Memory Characteristics		

Table 15: Configuration memory

Characteristic	Description
Nonvolatile memory retention time *(Typical)*	NVRAM 10 years minimum data retention rate. The length of time that FPGA images and other information stored in FLASH memory is retained in the absence of power to the instrument.

Table 16: Mechanical

Characteristic		Description
Material		Chassis parts are constructed of aluminum alloy. The front panel is constructed of plastic laminated to steel front panel. Circuit boards are constructed of glass laminate.
Weight	TLA7SA08	6 lbs (2.72 kg)
	TLA7SA16	7 lbs (3.18 kg)
Overall dimensions	Height	10.32 in (262 mm)
	Width	2.39 in (61 mm)
	Length	14.7 in (373 mm)

P67SA01SD Probe Specifications

Table 17: Electrical specification for P67SA01SD probe

Characteristic	Description
General	
Number of inputs	1 differential input
Input	
Input impedance *(Typical)*	AC coupled
	174 Ω resistor in series with 1 µf and terminating with 50 Ω
Minimum peak-to-peak differential input amplitude	268 $V_{p\text{-}p\ diff}$
Maximum nondestructive input signal to probe	±6.3 V
Input Common mode range	±6.3 V

Table 18: Cable specifications for P67SA01SD probe

Characteristic	Description
Physical length	6 ft (1.8 m)

Table 19: Atmospheric characteristics for P67SA01SD probe

Characteristic	Description
Temperature	*Operating*
	0 °C to +50 °C, with 15 °C/hour maximum gradient, noncondensing, derated 1 °C per 300 meters (~1000 ft) above 1500 meters (~5000 ft) altitude
	Nonoperating
	-40 °C to +71 °C, with 15 °C/hour maximum gradient
Humidity	*Operating*
	5% to 95% relative humidity (%RH) up to +30 °C
	5% to 75% RH up to +50 °C
	Nonoperating
	5% to 95% RH up to +30 °C
	5% to 60% RH up to +71 °C
Altitude	*Operating*
	Up to 3,000 meters (~10,000 ft), derate maximum operating temperature by 1 °C per 300 meters (~1000 ft) above 1500 meters (~5000 ft) altitude
	Nonoperating
	Up to 12000 meters (~40,000 ft)

P67SAxx Midbus Probe Specifications

Table 20: Electrical specification for P67SAxx midbus probe

Characteristic		Description
General		
Number of inputs	P67SA08	16 differential pairs
	P67SA16	16 differential pairs
Input		
Input impedance *(Typical)*		AC coupled
		450 Ω resistor in series with 1 µf and terminating with 50 Ω
Minimum peak-to-peak differential input amplitude		268 $mV_{p\text{-}p\ diff}$
Maximum nondestructive input signal to probe		±6.3 V
Input common mode range		±6.3 V

Table 21: Atmospheric characteristics for P67SAxx midbus probe

Characteristic	Description
Temperature	*Operating*
	0 °C to +50 °C, with 15 °C/hour maximum gradient, non-condensing, derated 1 °C per 1000 feet above 5000 feet altitude
	Nonoperating
	-40 °C to +71 °C, with 15 °C/hour maximum gradient
Humidity	*Operating*
	5% to 95% relative humidity (%RH) up to +30 °C
	5% to 75% RH up to +50 °C
	Nonoperating
	5% to 95% RH up to +30 °C
	5% to 60% RH up to +71 °C
Altitude	*Operating*
	Up to 3,000 meters (~10,000 ft), derate maximum operating temperature by 1 °C per 300 meters (~1000 ft) above 1500 meters (~5000 ft) altitude
	Nonoperating
	Up to 12000 meters (~40,000 ft)

Table 22: Mechanical characteristics for P67SAxx midbus probe

Characteristic		Description
Weight	P67SA08	1 lb 0 oz (0.45 kg)
	P67SA16	1 lb 14 oz (0.85 kg)

P67SAxxS Slot Interposer Specifications

Table 23: Electrical specification for P67SAxxS slot interposer

Characteristic		Description
General		
Number of Inputs	P67SA16S	32 (16 upstream + 16 downstream) differential pairs
	P67SA08S	16 (8 upstream + 8 downstream) differential pairs
	P67SA04S	8 (4 upstream + 4 downstream) differential pairs
	P67SA01S	2 (1 upstream + 2 downstream) differential pairs
Probe gain		800 $mV_{p\text{-}p\ diff}$ minimum Gain is defined as the differential peak-to-peak out put voltage divided by the differential peak-to-peak voltage at the probe tip. Gain will vary from channel to channel. Some channels may have gains up to approximately 3 dB at 800 $mV_{p\text{-}p\ diff}$.
Output amplitude *(Typical)*		
	Minimum output voltage	800 $mv_{p\text{-}p\ diff}$, with 800 $mv_{p\text{-}p\ diff}$ input
	Maximum output voltage	1400 $mv_{p\text{-}p\ diff}$, with 800 $mv_{p\text{-}p\ diff}$ input
	Maximum output voltage	1600 $mv_{p\text{-}p\ diff}$, with 1200 $mv_{p\text{-}p\ diff}$ input
Channel delay and skew – Through path *(Typical)*		
Delay	P67SA08S, P67SA04S, P67SA01S	650 ps ±100 ps
	P67SA16S	890 ps ±100 ps
Input		
Input impedance *(Typical)*		42.5 Ω, single ended, 85 Ω differential
Minimum peak-to-peak differential input amplitude *(Typical)*		268 $mV_{p\text{-}p\ diff}$
Maximum nondestructive input signal to probe		1.8 $V_{p\text{-}p\ diff}$
Input common mode range		0 V

Table 24: Cable specifications for P67SAxxS slot interposer

Characteristic	Description
Physical length	6 ft (1.8 m)

Table 25: Mechanical characteristics for P67SAxxS slot interposer

Characteristic		Description
Overall dimensions		Refer to the Probe Dimension section in the Tektronix Logic Protocol Analyzer Solutions for PCI Express 3.0 Instruction Manual (Tektronix part number, 077-0400-xx)
Weight	P67SA16S	3 lb 12 oz (1.7 kg)
	P67SA08S	1 lb 15 oz (0.88 kg)
	P67SA04S	1 lb 2 oz (0.51 kg)
	P67SA01S	0 lb 10 oz (0.28 kg)

Table 26: Atmospheric characteristics for P67SAxxS slot interposer

Characteristic	Description
Temperature	*Operating*
	0 °C to +50 °C, with 15 °C/hour maximum gradient, noncondensing, derated 1 °C per 300 meters (~1000 ft) above 1500 meters (~5000 ft) altitude
	Nonoperating
	-40 °C to +71 °C, with 15 °C/hour maximum gradient
Humidity	*Operating*
	5% to 95% relative humidity (%RH) up to +30 °C
	5% to 75% RH up to +50 °C
	Nonoperating
	5% to 95% RH at up to +30 °C
	5% to 60% RH at up to +71 °C
Altitude	*Operating*
	Up to 3,000 meters (10,000 ft), derate maximum operating temperature by 1 °C per 300 meters (~1000 ft) above 1500 meters (~5000 ft) altitude
	Nonoperating
	Up to 12000 meters (~40,000 ft)

P67SA16G2 Midbus Probe Specifications

Table 27: Electrical specification for P67SA16G2 midbus probe

Characteristic	Description
General	
Number of inputs	16 differential pairs
Input	
Input impedance *(Typical)*	AC coupled
	450 Ω resistor in series with 1 µf and terminating with 50 Ω
Minimum peak-to-peak differential input amplitude	268 $mV_{p\text{-}p\ diff}$
Maximum nondestructive input signal to probe	±6.3 V
Input common mode range	±6.3 V
Weight	1 lb 15 oz (0.88 kg)

Table 28: Atmospheric characteristics for P67S16AG2 midbus probe

Characteristic	Description
Temperature	*Operating*
	0 °C to +50 °C, with 15 °C/hour maximum gradient, non-condensing, derated 1 °C per 1000 feet above 5000 feet altitude
	Nonoperating
	-40 °C to +71 °C, with 15 °C/hour maximum gradient
Humidity	*Operating*
	5% to 95% relative humidity (%RH) up to +30 °C
	5% to 75% RH up to +50 °C
	Nonoperating
	5% to 95% RH up to +30 °C
	5% to 60% RH up to +71 °C
Altitude	*Operating*
	Up to 3,000 meters (~10,000 ft), derate maximum operating temperature by 1 °C per 300 meters (~1000 ft) above 1500 meters (~5000 ft) altitude
	Nonoperating
	Up to 12000 meters (~40,000 ft)

P6716G3 Midbus Probe Specifications

Table 29: Electrical specification for P6716G3 midbus probe

Characteristic	Description
General	
Number of inputs	16 differential pairs
Input	
Input impedance *(Typical)*	AC coupled
	450 Ω resistor in series with 1 µf and terminating with 50 Ω
Minimum peak-to-peak differential input amplitude	120 $mV_{p\text{-}p\ diff}$
Maximum nondestructive input signal to probe	±7.5 V
Input common mode range	±7.5 V

Table 30: Atmospheric characteristics for P67S16AG3 midbus probe

Characteristic	Description
Temperature	*Operating*
	0 °C to +50 °C, with 15 °C/hour maximum gradient, non-condensing, derated 1 °C per 1000 feet above 5000 feet altitude
	Nonoperating
	-40 °C to +71 °C, with 15 °C/hour maximum gradient
Humidity	*Operating*
	5% to 95% relative humidity (%RH) up to +30 °C
	5% to 75% RH up to +50 °C
	Nonoperating
	5% to 95% RH up to +30 °C
	5% to 60% RH up to +71 °C
Altitude	*Operating*
	Up to 3,000 meters (~10,000 ft), derate maximum operating temperature by 1 °C per 300 meters (~1000 ft) above 1500 meters (~5000 ft) altitude
	Nonoperating
	Up to 12000 meters (~40,000 ft)

Performance Verification Procedures

There are no customer self-service performance verification procedures for the TLA7SA08 or TLAS7SA16 Logic Protocol Analyzer modules. To verify the performance of your logic protocol analyzer module, you must return the module to your local Tektronix office. However, you can perform a functional check. (See page 20, *Functional Verification*.)

Functional Check Procedures

Functional Verification

Functional verification procedures consist of running the Power-on diagnostics, Extended diagnostics, and acquiring a signal from the SUT.

Power-On and Extended Diagnostics

Do the following steps to run the power-on and extended diagnostics:

NOTE. *Running the extended diagnostics will invalidate any acquired data. To save any of the acquired data, do so before running the extended diagnostics.*

You will need a mainframe with a logic protocol analyzer module installed in the mainframe.

NOTE. *If you control your logic analyzer from a remote location, make sure that you select Run Power-on Diagnostics in the TLA Connection dialog box. Otherwise the instrument will bypass the power-on diagnostics.*

Perform the following tests to complete the functional verification procedure:

1. If you have not already done so, power on the instrument.

   The instrument runs the power-on diagnostics each time that you power-on the instrument. If any failures occur, the diagnostic window will appear.

2. Go to the System menu and select Calibration and Diagnostics.

3. Scroll through the list of tests and verify that all power-on diagnostics pass.

NOTE. *Allow the instrument to warm up for 30 minutes before continuing with the Extended diagnostics.*

4. Click the Extended Diagnostics tab.

5. Select the top-most selection for your module in the list of tests. For example, if your logic protocol analyzer module is installed in Slot 3 of your mainframe, select Slot 3:TLA7SA08 - SA.

6. Select the type of test that you want to run (One Time, Continuous, or Until Fail).

7. Click Run to start the tests.

All tests that displayed an "Unknown" status will change to a Pass or Fail status depending on the outcome of the tests.

8. After the tests have completed, scroll through the list and verify that the instrument passes all tests.

NOTE. *Installing a module in the mainframe provides a means of verifying connectivity and communication between the module and the mainframe. If the instrument fails any test, try using a different module and repeat the tests to isolate the problem to the mainframe or to the module.*