TLA6000 Series Logic Analyzer
Product Specifications & Performance Verification

Technical Reference

Revision A

This document applies to TLA System Software Version 5.7 and above

Warning

These servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries before performing service.

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Tektronix

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Contacting Tektronix

Tektronix, Inc.
14150 SW Karl Braun Drive
P.O. Box 500
Beaverton, OR 97077
USA

For product information, sales, service, and technical support:

- In North America, call 1-800-833-9200.
- Worldwide, visit www.tektronix.com to find contacts in your area.

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General safety summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of a larger system. Read the safety sections of the other component manuals for warnings and cautions related to operating the system.

To avoid fire or personal injury

Use proper power cord. Use only the power cord specified for this product and certified for the country of use.

Connect and disconnect properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe all terminal ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

The inputs are not rated for connection to mains or Category II, III, or IV circuits.

Connect the probe reference lead to earth ground only.

Power disconnect. The power cord disconnects the product from the power source. Do not block the power cord; it must remain accessible to the user at all times.

Do not operate without covers. Do not operate this product with covers or panels removed.

Do not operate with suspected failures. If you suspect that there is damage to this product, have it inspected by qualified service personnel.

Avoid exposed circuitry. Do not touch exposed connections and components when power is present.

Use proper fuse. Use only the fuse type and rating specified for this product.

Do not operate in wet/damp conditions.

Do not operate in an explosive atmosphere.

Keep product surfaces clean and dry.

Provide proper ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Terms in this manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

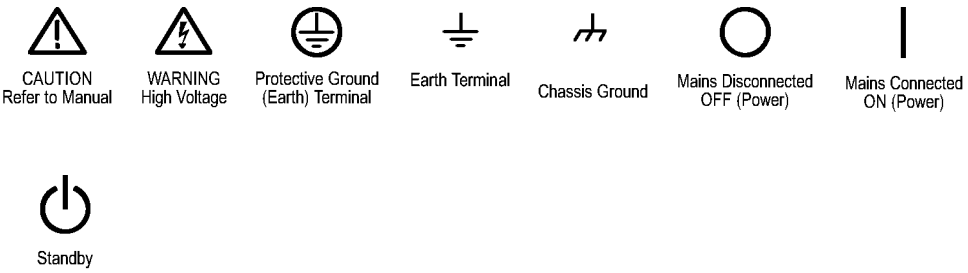
CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Symbols and terms on the product

These terms may appear on the product:

- DANGER indicates an injury hazard immediately accessible as you read the marking.
- WARNING indicates an injury hazard not immediately accessible as you read the marking.
- CAUTION indicates a hazard to property including the product.

The following symbol(s) may appear on the product:



Service safety summary

Only qualified personnel should perform service procedures. Read this *Service safety summary* and the *General safety summary* before performing any service procedures.

Do not service alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use care when servicing with power on. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This document lists the characteristics and specifications of the TLA6000 series logic analyzers. It also includes the performance verification procedures. Microprocessor-related products and individual logic analyzer probes have their own documentation for characteristics and specifications.

To prevent personal injury or damage consider the following requirements before attempting service:

- The procedures in this manual should be performed only by qualified service personnel.
- Read the General Safety Summary and Service Safety Summary found at the beginning of this manual.

Be sure to follow all warnings, cautions, and notes in this manual.

Related Documentation

The following list and table provide information on the related documentation available for your Tektronix product. For additional information, refer to the Tektronix Web site (www.tektronix.com/manuals).

Related documentation

Item	Purpose
TLA Quick Start User Manuals	High-level operational overview
Online Help	In-depth operation and UI help
Installation Reference Sheets	High-level installation information
Installation Manuals	Detailed first-time installation information
XYZs of Logic Analyzers	Logic analyzer basics
Declassification and Securities instructions	Data security concerns specific to sanitizing or removing memory devices from Tektronix products
Application notes	Collection of logic analyzer application specific notes
Product Specifications & Performance Verification Procedures	TLA Product specifications and performance verification procedures
TPI.NET Documentation	Detailed information for controlling the logic analyzer using .NET
Field upgrade kits	Upgrade information for your logic analyzer
Optional Service Manuals	Self-service documentation for modules and mainframes

Specifications

The following tables list the specifications for the TLA6000 series logic analyzers. All specifications are guaranteed unless noted *Typical*. Typical characteristics describe typical or average performance and provide useful reference information.

Specifications that are marked with the ✓ symbol are checked directly (or indirectly) in the *Performance Verification* chapter of this document.

The performance limits in this specification are valid with these conditions:

- The instrument must be in an environment with temperature, altitude, humidity, and vibration within the operating limits described in these specifications.
- The instrument must have had a warm-up period of at least 30 minutes.
- The instrument must have been calibrated/adjusted at an ambient temperature between +20 °C and +30 °C.

For optimum performance using an external oscilloscope, please consult the documentation for any external oscilloscopes used with your Tektronix logic analyzer to determine the warm-up period and signal-path compensation requirements.

Atmospheric Characteristics

The following table lists the Atmospheric characteristics of components in the TLA6000 series logic analyzers.

Table 1: Atmospheric characteristics

Characteristic	Description
Temperature	*Operating (no media in CD or DVD drive)*
	+5 °C to +40 °C (+41 °F to +104 °F), 11 °C/hr (52 °F/hr) maximum gradient, noncondensing (derated 1 °C (34 °F) per 305 m (1000 ft) above 1524 m (5000 ft) altitude)
	Nonoperating (no media in drive)
	-20 °C to +60 °C (-4 °F to +104 °F), 15 °C/hr (59 °F/hr) maximum gradient, noncondensing
Relative Humidity	*Operating (no media in drive)*
	5% to 80% relative humidity, up to +30 °C (+86 °F), 75% from +30 to +40 °C (+86 °F to +104 °F) noncondensing. Maximum wet bulb temperature: +29.4 °C (+85 °F)
	Nonoperating (no media in drive)
	5% to 90% relative humidity, noncondensing. Maximum wet bulb temperature: +40 °C (+104 °F)
Altitude	*Operating*
	To 3000 m (9843 ft), (derated 1 °C (34 °F) per 305 m (1000 ft) above 1524 m (5000 ft) altitude.
	Nonoperating
	12,190 m (40,000 ft)

System Characteristics

Table 2: Backplane interface

Characteristic	Description
Clock10 Frequency (system clock)	10 MHz ±100 ppm

Table 3: System trigger and external signal input latencies *(Typical)*

Logic analyzer source characteristic	Description
External system trigger input to LA probe tip [1]	–626 ns
External Signal In to LA probe tip via Signals 3, 4 (TTLTRG 0,1) [2]	–535 ns + Clk
External Signal In to LA probe tip via Signals 1, 2 (ECLTRG 0,1) [2] [3]	–627 ns + Clk

1 In the Waveform window, triggers are always marked immediately except when delayed to the first sample. In the Listing window, triggers are always marked on the next sample period following their occurrence.

2 Clk represents the time to the next master clock at the destination logic analyzer module. With asynchronous clocking this represents the delta time to the next sample clock. With synchronous sampling this represents the time to the next master clock generated by the setup of the clocking state machine and the supplied SUT clocks and qualification data.

3 Signals 1 and 2 (ECLTRG0, 1) are limited to a broadcast mode where only one source can drive the signal node at any one time. The signal source can be used to drive any combination of destinations.

Table 4: System trigger and external signal output latencies*(Typical)*

Logic analyzer source characteristic [1]	Deacripton
LA probe tip to external system trigger out (skid) [2]	794 ns + Smpl
LA probe tip to External Signal Out via Signal 3, 4 (TTLTRG 0,1) [3]	
OR function	793 ns + Smpl
AND function	803 ns + Smpl
LA probe tip to External Signal Out via Signals 1, 2 (ECLTRG0,1) [3] [4]	793 ns + Smpl

1 SMPL represents the time from the event to the next valid data sample at the probe tip of the LA module. With asynchronous sampling, this represents the delta time to the next sample clock. With MagniVu asynchronous sampling, this represents 500 ps or less. With synchronous sampling, this represents the time to the next master clock generated by the setup of the clocking state machine, the system-under-test supplied clocks, and the qualification data.

2 Skid is commonly referred to as the system level system trigger and signaling output latency. This is the absolute time from when the event first appears at the input probe tips of a module to when the corresponding event that it generates appears at the system trigger or external signal outputs.

3 All signal output latencies are validated to the rising edge of an active (true) high output.

4 Signals 1 and 2 (ECLTRG0, 1) are limited to a broadcast mode where only one source can drive the signal node at any one time. The signal source can be used to drive any combination of destinations.

Table 5: External signal interface

Characteristic		Description	
System Trigger Input		TTL compatible input via rear panel mounted BNC connectors	
	Input levels	0 V to 3.0 V	
	Minimum input voltage swing	300 mV	
	Threshold range	0.5 V to 1.5 V	
	Threshold step size	50 mV	
	Input destination	System trigger	
	Input Mode	Falling edge sensitive, latched (active low)	
	Minimum Pulse Width	12 ns	
	Active Period	Accepts system triggers during valid acquisition periods via real-time gating, resets system trigger input latch between valid acquisition periods	
	Maximum Input Voltage	0 to + 5 V peak	
External Signal Input		TTL compatible input via rear panel mounted BNC connectors	
	Input Destination	Signal 1, 2, 3, 4	
	Input levels	0 V to 3.0 V	
	Minimum input voltage swing	300 mV	
	Threshold range	0.5 V to 1.5 V	
	Threshold step size	50 mV	
	Input Mode	Active (true) low, level sensitive	
	Input Bandwidth [1]	*Signal 1, 2*	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum
	Active Period	Accepts signals during valid acquisition periods via real-time gating	
	Maximum Input Voltage	0 V to 5 V peak	

Table 5: External signal interface (cont.)

Characteristic		Description	
System Trigger Output		TTL compatible output via rear panel mounted BNC connectors	
	Source selection	System trigger	
	Source Mode	Active (true) low, falling edge latched	
	Active Period	Outputs system trigger state during valid acquisition period, resets system trigger output to false state between valid acquisitions	
	Output Levels V_{OH} V_{OL}	50 Ω back terminated TTL-compatible output ≥4 V into open circuit, ≥2 V into 50 Ω to ground ≤0.7 V sinking 10 mA	
	Output Protection	Short-circuit protected (to ground)	
External Signal Output		TTL compatible outputs via rear panel mounted BNC connectors	
	Source Selection	Signal 1, 2 Signal 3, 4 10 MHz clock	
	Output Modes Level Sensitive	User definable Active (true) low or active (true) high	
	Output Levels V_{OH} V_{OL}	50 Ω back terminated TTL output ≥4 V into open circuit, ≥2 V into 50 Ω to ground ≤0.7 V sinking 10 mA	
	Output Bandwidth [2]	*Signal 1, 2*	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum
	Active Period	Outputs signals during valid acquisition periods, resets signals to false state between valid acquisitions Outputs 10 MHz clock continuously	
	Output Protection	Short-circuit protected (to ground)	
Intermodule Signal Line Bandwidth		Minimum bandwidth up to which the intermodule signals are specified to operate correctly	
		Signal 1, 2	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum

1 The Input Bandwidth specification only applies to signals to the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

2 The Output Bandwidth specification only applies to signals from the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

Table 6: Display system

Characteristic		Description		
Display selection		The motherboard can drive 3 video displays. One VGA and one DVI connector are provided for external monitors. The connectors provide the same video information The third display connector is available only as an internal connection. This connection is via LVDS. This port drives the internal 15-inch display. One of the external connectors and the internal connection are connected to the same video information.		
External display drive		One VGA, SVGA, or XGA-compatible output on two connectors (VGA & DVI)		
		Resolution (Pixels)	*Colors*	*Refresh Rates*
	Minimum	800 x 600	16-bit	60
	Maximum	2048 x 1536	32-bit	85
Internal display	Classification	Color LCD (NEC TFT NL10276BC30-24D) Color LCD module NL10276BC30-24D is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight. This LCD display will be driven directly by the motherboard via LVDS signaling.		
	Resolution/Refresh rate and area	1024 pixels horizontal by 768 pixels vertical (1024X768) at 60 Hz refresh rate Area of 304 mm (11.7 in) by 228 mm (9 in) of viewing area.		
	Color scale	262, 144 colors (6-bit RGB) with a color gamut of 42% at center to NTSC		

Table 7: Front-panel interface

Characteristic		Description
Keypad		18 buttons allow user to perform the most common tasks required to operate theTLA
Special function knobs	Multi-function Knob	Various increment, decrement functions dependent on screen/window selected.
	Vertical position	Scrolling and positioning dependent on display type.
	Vertical scale	Scales waveform displays only.
	Horizontal position	Scrolling and positioning dependent on display type.
	Horizontal scale	Scales waveform displays only.
USB Port		Three USB 2.0 connectors at lower right of front panel

Table 8: Rear-panel interface

Characteristic		Description
TekLink interface bus		Connector supports Reference Clock (10 MHz), Power On Signaling, Run event, System Trigger, General purpose events
	Input signal characteristics	LVDS compatible inputs via rear-panel 40-pin connector
	Output signal characteristics	LVDS compatible outputs via rear-panel 40-pin connector
	Reference clock characteristics	LVDS compatible inputs via rear-panel 40-pin connector
SVGA output ports		One DVI and one 15-pin D-sub VGA connector
External Trigger input		Trigger input routed to the system trigger line
External Signal input		Signal input routed to one of four internal signals
System Trigger output		Internal system trigger routed as TTL-compatible output
External Signal output		One of four internal signals routed to the signal output connector. The internal 10 MHz reference clock can be routed to this output.
USB 2.0 ports		Four USB 2.0 connections
GBit LAN port		Two RJ-45 LAN ports
Serial interface port		Two 9-pin male D-sub connectors to support RS-232
Mouse port		PS/2 compatible mouse port
Keyboard port		PS/2 compatible keyboard port

Table 9: AC power source

Characteristic	Description
Source voltage and frequency	100 V_{RMS} to 240 V_{RMS} ±10%, 50 Hz to 60 Hz 115 V_{RMS} ±10%, 400 Hz
Maximum power consumption	750 W
Steady-state input current	6 A_{RMS} maximum at 90 VAC_{RMS}, 60 Hz or 100 VAC_{RMS}, 400 Hz
Inrush surge current	70 A maximum
Power factor correction	Yes
On/Sleep indicator	Green/yellow front panel LED located left of the On/Standby switch provides visual feedback when the switch is actuated. When the LED is green, the instrument is powered and the processor is not sleeping. When the LED is yellow, the instrument is powered, but the processor is sleeping.
On/Standby switch and indicator	Front panel On/Standby switch allows users to turn the instrument on. A soft power down is implemented so that users can turn the instrument off without going through the Windows shutdown process; the instrument powers down normally. The power cord provides main power disconnect

Table 10: Transportation and storage

Characteristic	Description
Transportation package material	Transportation Package material meets recycling criteria as described in Environmental Guidelines for Package Design (Tektronix part number 063-1290-00) and Environmentally Responsible Packaging Handbook (Tektronix part number 063-1302-00).

Table 11: Cooling

Characteristic	Description
Cooling system	Forced air circulation system with no removable filters using eight fans operating in parallel
Pressurization	Negative pressurization system in all chambers including modules
Air intake	Front sides and bottom
Air exhaust	Back rear
Cooling clearance	6 inches (152 mm) front, sides, top, and rear. Prevent blockage of airflow to bottom of instrument by placing on a solid, noncompressable surface; can be operated on rear feet.
Fan speed and operation	All fans operational at half their rated potential and speed (12 VDC)

Table 12: Input parameters (with probes)

Characteristic		Description	
✓ Threshold accuracy (Certifiable parameter)		±(35 mV + 1% of the threshold voltage setting)	
Threshold range and step size		Settable from +4.5 V to -2.0 V in 5 mV steps	
Threshold channel selection		16 threshold groups assigned to channels. Each probe has four threshold settings, one for each of the clock/qualifier channels and one per group of 16 data channels.	
✓ Channel to channel skew		≤400 ps maximum	
Channel-to-channel skew *(Typical)*		≤300 ps	
Sample uncertainty		*Asynchronous*	*Synchronous*
		Sample period	125 ps
Minimum slew rate *(Typical)*		0.2 V/ns	
Input voltage range		-2.5 V to +5 V	
Maximum operating voltage swing		6.0 V peak-to-peak	
Probe overdrive	Single ended probes	±150 mV or ±25% of signal swing minimum required beyond threshold, whichever one is greater	
	Differential probes	V_{pos}-V_{neg} is ≥150 mV_{p-p}	
Maximum nondestructive input signal to probe		±15V	
Minimum input pulse width (single channel) *(Typical)*		P6860, P6880, P6960, and P6980 probes	500 ps
		P6810 probes	750 ps

Table 12: Input parameters (with probes) (cont.)

Characteristic	Description	
Delay time from probe tip to input probe connector *(Typical)*	P6860, P6960, and P6980 probes	7.7 ns ±60ps
	P6810 and P6880 probes	7.7 ns ±80ps

Table 13: Analog output

Characteristic	Description
Number of outputs	Four analog outputs regardless of the channel width. Any four of the channels can be mapped to the four analog outputs.
Attenuation	10X mode for normal operation 5X mode for small signals (-1.5 V to +2.5 V)
Bandwidth *(Typical)*	2 GHz
Accuracy (gain and offset) *(Typical)*	±(50 mV + 2% of signal amplitude)

Table 14: Channel width and depth

Characteristic		Description
Number of channels	TLA6204	128 data, 8 clock/qualifier
	TLA6203	96 data, 6 clock/qualifier
	TLA6202	64 data, 4 clock/qualifier
Acquisition memory depth		128 M per channel, maximum

Table 15: Clocking

Characteristic	Description	
Asynchronous sampling		
✓ Sampling period	500 ps to 50 ms in a 1-2-5 sequence. Storage control can be used to only store data when it has changed (transitional storage) 2 ns minimum for all channels 1 ns minimum for half channels (using 2:1 Demultiplex mode) 0.5 ns minimum for quarter channels (using 4:1 Demultiplex mode)	
✓ Minimum recognizable word [1] (across all channels)	Channel-to-channel skew + sample uncertainty Example for a P6860 high-density probe and a 2 ns sample period: 400 ps + 2 ns = 2.4 ns	
Synchronous sampling		
Master clock channels [2]	4	
Qualifier channels Note: Qualifier channels are stored.	*Product*	*Qualifier channels*
	TLA6202	0
	TLA6203	2
	TLA6204	4
Single channel setup and hold window size *(Typical)*	500 ps	
✓ Setup and hold window size (data and qualifiers)	Maximum window size = Maximum channel-to-channel skew + (2 x sample uncertainty) + 100 ps Maximum setup time = User interface setup time + 75 ps Maximum hold time = User interface hold time + 50 ps Example using a P6800 series probe and user interface setup and hold of 625/0 typical: Maximum window size = 400 ps + 250 ps + 100 ps = 750 ps Maximum setup time = 625 ps + 75 ps = 700 ps Maximum hold time = 0.0 ps + 50 ps = 50 ps	

Table 15: Clocking (cont.)

Characteristic	Description
Setup and hold window size (data and qualifiers) *(Typical)*	Typical window size = Typical channel-to-channel skew + (2 x sample uncertainty) + 75 ps Example using P6860 probe: 300 ps + 250 ps + 75 ps = 625 ps
Setup and hold window range	For each channel, the setup and hold window can be moved from +8.0 ns (T_s typical) to -8.0 ns (T_s typical) in 0.125 ns steps (setup time). The setup and hold window can be shifted toward the setup region by 0 ns, 4 ns, or 8 ns. With a 0 ns shift, the range is +8 ns to -8 ns; with a 4 ns shift, the range is +12 ns to -4 ns; with an 8 ns shift, the range is +16 ns to 0 ns. The sample point selection region is the same setup and hold window. Setup times are specified as typical figures. Hold time follows the setup time by the setup and hold window size.
Demultiplex clocking	
Demultiplex channels (2:1) TLA6203, TLA6204	Any individual channel can be demultiplexed with its partner channel. If multiplexing is enabled, all of the A and D channels are multiplexed; there is no individual selection. Channels demultiplex as follows:
	A3(7:0) to/from D3(7:0) A2(7:0) to/from D2(7:0) A1(7:0) to/from D1(7:0) A0(7:0) to/from D0(7:0) E3(7:0) to/from E1(7:0) TLA6204 only E2(7:0) to/from E0(7:0) TLA6204 only CK3 to/from Q2 TLA6204 only CK2 to/from Q3 TLA6204 only CK1 to/from Q0 CK0 to/from Q1
TLA6202	Any individual channel can be demultiplexed with its partner channel. If multiplexing is enabled, all of the A and D channels are multiplexed; there is no individual selection. Channels demultiplex as follows:
	A3(7:0) to/from C3(7:0) A2(7:0) to/from C2(7:0) A1(7:0) to/from D1(7:0) TLA6202 only A0(7:0) to/from D0(7:0) TLA6202 only
Demultiplex channels (4:1) TLA6203, TLA6204	Unlike the 2:1 Demultiplex, the channels within a group of four cannot arbitrarily drive the others.
	E3(7:0) to E2(7:0), E1(7:0), E0(7:0) TLA6204 only A3(7:0) to A2(7:0), D3(7:0), D2(7:0) A1(7:0) to A0(7:0), D1(7:0), D0(7:0) C3(7:0) to C2(7:0), C1(7:0), C0(7:0) CK3 to CK2, Q3, Q2 TLA6204 only CK1 to CK0, Q1, Q0

Table 15: Clocking (cont.)

Demultiplex clocking	
TLA6202	Unlike the 2:1 Demultiplex, the channels within a group of four cannot arbitrarily drive the others.
	A1(7:0) to A0(7:0), D1(7:0), D0(7:0)
	C3(7:0) to C2(7:0), A3(7:0), A2(7:0)
Time between Demultiplex clock edges *(Typical)*	Same limitations as normal synchronous acquisition
Source synchronous sampling	
Clocks per module	Four
Clock groups	Four
Size of clock group valid FIFO	Four stages when operated at 235 MHz or below (three stages when operated above 235 MHz); this allows four (source synchronous or other) clocks to occur before the clock that completes the Clock Group Valid signal for that group.
Source synchronous clock alignment window	Channel-to-channel skew only
Source synchronous clock reset	The Clock Group Valid FIFO can be reset in one of two ways: **1.** By the overflow of a presettable (0-255) 8-bit counter that counts one of the following clocks: 2 ns Clock or the master heartbeat clock (synchronous or asynchronous). An active edge places the reset count to its preset value. An active clock edge will clear the Clock Group Valid reset before the clock gets to the FIFO so that no data is lost. **2.** Any one of the clocks can be selected. A polarity selection is available. This mode affects all Clock Group Complete circuits. Neither one of the above modes can be intermixed; one or the other must be selected.
Clocking state machine	
Pipeline delays	Channel groups can be programmed with a pipeline delay of 0 through 7 active clock changes.

1 Specification only applies with asynchronous clocking. With synchronous sampling, the setup and hold window size applies.

2 Any clock channel can be enabled. For enabled clock channels, either the rising, falling, or both edges can be selected as active clock edges; clock channels are stored.

3 This is a special mode and has some limitations such as the clocking state machine and trigger state machine only running at 500 MHz.

Table 16: Trigger system

Characteristic	Description
Trigger resources	
Word recognizers and range recognizers	16 word recognizers can be combined to form full-width, double-bounded range recognizers. The following selections are available:
	16 word recognizers — 0 range recognizers
	13 word recognizers — 1 range recognizer
	10 word recognizers — 2 range recognizers
	7 word recognizers — 3 range recognizers
	4 word recognizers — 4 range recognizers
Range recognizer channel order	From most-significant probe group to least-significant probe group:
	C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0
	Missing channels for instruments with fewer than 136 channels are omitted.
Glitch detector (normal asynchronous clock mode)	Channel groups can be enabled to detect glitches.
	Glitches are subject to pulse width variations of up to ±125ps
Minimum detectable glitch pulse width *(Typical)*	Minimum input pulse width (single channel)
	P6860, P6960 high-density probe: 500 ps
	P6880, P6980 differential probe: 500 ps
	P6810 general purpose probe: 750 ps
Setup and hold violation detector (normal synchronous clock mode)	Any channel can be enabled to detect a setup or hold violation. The range is from 8.0 ns before the clock edge to 8.0 ns after the clock edge in 0.125 ns steps. The channel setup and hold violation size can be individually programmed.
	The range can be shifted toward the positive region by 0 ns, 4 ns, or 8 ns. With a 0 ns shift, the range is +8 ns to -8 ns; with a 4 ns shift, the range is +12 ns to -4 ns; with an 8 ns shift, the range is +16 ns to 0 ns. The sample point selection region is the same as the setup and hold window.
	Any setup value is subject to variation of up to the channel skew specification. Any hold value is subject to variation of up to the channel skew specification.
Transition detector	16 transition detectors.
	Any channel group can be enabled or disabled to detect a rising transition, a falling transition, or both rising and falling transitions between the current valid data sample and the previous valid data sample.
Counter/timers	2 counter/timers, 51 bits wide, can be clocked up to 500 MHz
	Maximum count is 2^50-1 (excluding sign bit)
	Maximum time is 4.5 X 10^6 seconds or 52 days
	Counters can be used as Settable, resettable, and testable flags. Counters can be reset, do nothing, increased, or decreased. Timers can be reset, started, stopped, or not changed. Counters and timers have zero reset latency and one clock terminal count latency.
Signal In 1	A backplane input signal
Signal In 2	A backplane input signal

Table 16: Trigger system (cont.)

Characteristic	Description
Trigger In	A backplane input signal that causes the main acquisition and the MagniVu acquisition to trigger if they are not already triggered.
Active trigger resources	16 maximum (excluding counter/timers) Word recognizers are traded off one-for-one as Signal In 1, Signal In 2, glitch detection, setup and hold detection, or transition detection resources are added.
Trigger states	16
✓ Trigger state machine (TSM) sequence rate	DC to 500 MHz (2.00 ns) For data rates of 500 Mb/s or less, the TSM evaluates one data sample per TSM clock. For data rates greater than 500 Mb/s, the TSM evaluates multiple data samples per TSM clock up to the maximum acquired data rate.
Trigger machine actions	
Main acquisition trigger	Triggers the main acquisition memory
Main trigger position	Programmable to any data sample (2 ns boundaries)
MagniVu trigger	Main acquisition machine controls the triggering of the MagniVu memory
MagniVu trigger position	Programmable within 2 ns boundaries and separate from the main acquisition memory trigger position
Increment/decrement counter	Counter/timers used as counters can be increased or decreased.
Start/stop timer	Either of the two counter/timers used as timers can be started or stopped.
Reset counter/timer	Either of the two counter/timers can be reset. When a counter/timer used as a timer is reset, the timer continues in the started or stopped state that it was before the reset.
Reloadable word recognizer (snapshot)	Loads the current acquired data sample into the reference value of the word recognizer via a trigger machine action. All data channels are loaded into their respective word recognizer reference register on a one-to-one manner.
Reloadable word recognizer latency	378 ns
Signal Out	A signal sent to the backplane to be used by other instruments
Trigger Out	A signal sent to the backplane to trigger other instruments
Storage control	
Storage	Storage is allowed only if a specific condition is met. The condition can use any of the trigger resources except for counter/timers. Storage commands defined in the current trigger state will override the global storage control. Storage can be used to start the acquisition with storage initially turned on (default setting) or off.
By event	Storage can be turned on or off; only the current sample can be stored. Event storage control overrides any global storage commands.
Block storage (store stretch)	When enabled, 31 samples are stored before and after the valid sample. This allows the storage of a group of samples around a valid data sample when storage control is being used. This only has meaning when storage control is used. Block storage is disallowed when glitch storage or setup and hold violation storage is enabled.

Table 16: Trigger system (cont.)

Characteristic	Description
Glitch violation storage	Glitch violation information can be stored to acquisition memory with each data sample when asynchronous sampling is used. The acquisition data storage size is reduced by half when this mode is enabled (the other half holds violation information). The fastest asynchronous clock rate is reduced to 4 ns.
Setup and hold violation storage	Setup and hold violation information can be stored to acquisition memory with each data sample when synchronous sampling is used. The acquisition data storage size is reduced by half when this mode is enabled (the other half holds violation information). The maximum synchronous clock rate in this mode is 235 MHz.

Table 17: MagniVu acquisition

Characteristic	Description
MagniVu sampling period	Data is asynchronously sampled and stored every 125 ps in a separate MagniVu (high-resolution) memory. The storage speed can be changed by software to 250 ps, 500 ps, or 1000 ps with no loss in memory depth so that the high resolution memory covers more time at a lower resolution.
MagniVu memory depth	Approximately 16 K per channel. The MagniVu memory is separate from the main acquisition memory.

Table 18: Data placement

Characteristic	Description
Timestamp counter resolution and duration	125 ps resolution 3.25 days duration

Table 19: NVRAM

Characteristic	Description
Nonvolatile memory retention time (*Typical*)	The battery life is integral to the NVRAM; battery life is >10 years.

Table 20: Mechanical

Characteristic		Description
Classification		The instrument is intended for design and development bench and lab-based applications.
Overall dimensions		Dimensions are without front feet extended, front cover attached, pouch attached, nor power cord attached.
	Height (with feet)	11.6 in (294.64 mm)
	Width	17.75 in (450.85 mm)
	Depth	18.1 in (459.74 mm)
Weight		Includes instrument with front cover and empty accessory pouch
	TLA6202	20.73 kg (46 lbs 1 oz)
	TLA6203	20.83 kg (45 lbs 6 oz)
	TLA6204	20.89 kg (45 lbs 12.8 oz)
Acoustic noise level *(Typical)*		43 dBA weighted (operator) 41 dBA weighted (bystander)
Construction materials		Chassis parts are constructed of aluminum alloy; front panel and trim peaces are constructed of plastic; circuit boards are constructed of glass.
Finish type		Tektronix blue body and Tektronix silver-gray trim and front with black pouch, FDD feet, handle, and miscellaneous trim pieces

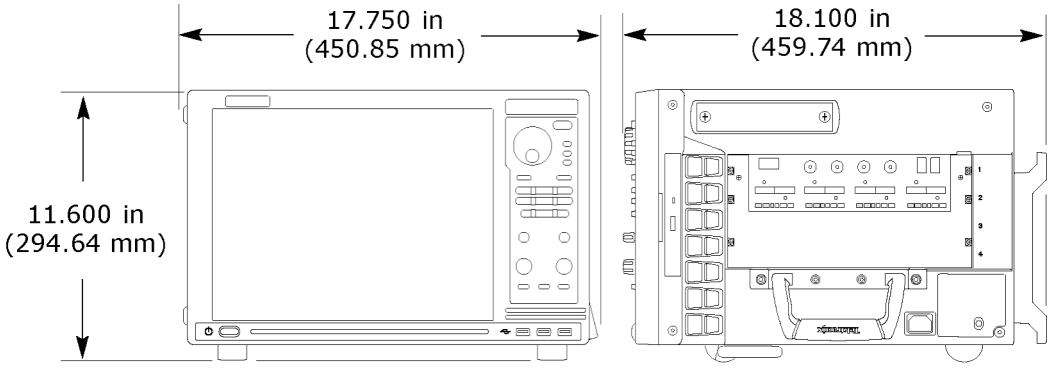


Figure 1: Dimensions of the TLA6000 series logic analyzer

Performance Verification Procedures

This chapter contains procedures for functional verification, certification, and performance verification procedures for the TLA6000 series logic analyzers. Generally, you should perform these procedures once per year or following repairs that affect certification.

Summary Verification

Functional verification procedures verify the basic functionality of the instrument inputs, outputs, and basic instrument actions. These procedures include power-on diagnostics, extended diagnostics, and manual check procedures. These procedures can be used for incoming inspection purposes.

Performance verification procedures confirm that a product meets or exceeds the performance requirements for the published specifications documented in the *Specifications* chapter of this manual. The performance verification procedures certify the accuracy of an instrument and provide a traceability path to national standards.

Certification procedures certify the accuracy of an instrument and provide a traceability path to national standards. Certification data is recorded on calibration data reports provided with this manual. The calibration data reports are intended to be copied and used for calibration/certification procedures.

As you complete the performance verification procedures, fill out a calibration data report to keep on file with your instrument. A blank copy of the calibration data report is provided with this manual. The calibration data report is intended to be copied and used to record the results of the calibration/certification procedures.

Test Equipment

These procedures use external, traceable signal sources to directly test characteristics that are designated as checked ✓ in the *Specifications* chapter of this manual. Always warm up the equipment for 30 minutes before beginning the procedures.

Table 21: Test equipment

Item number and description	Minimum requirements	Example
Logic analyzer	TLA6202, TLA6203, or TLA6204	-
Logic analyzer probe	One required	P6810
Precision voltage reference or a DC signal generator and precision digital voltmeter	(accurate to within ±5 mV)	-
Data Timing Generator	Tektronix DTG 524 with a DTGM30 Output Module	-
Frequency counter	Frequency accuracy: <0.0025% Frequency range: 1 kHz to 100 MHz	Hewlett Packard 5314A
Test fixture, Threshold Accuracy	One required	Refer to Threshold Accuracy Test Fixture. (See page 29.)
Test fixture, Setup and Hold	Minimum of two test fixtures required	Refer to Setup and Hold Test Fixture. (See page 30.)
Cable, precision 50 Ω coaxial	50 Ω , 36 in, male-to-male BNC connectors	Tektronix part number 012-0482-XX

Functional Verification

The following list describes the functional verification procedures for the TLA6000 series logic analyzer.

- Power-on and fan operation
- Power-on diagnostics
- Extended diagnostics
- TLA Mainframe diagnostics
- CheckIt Utilities diagnostics

Power-On and Fan Operation

Complete the following steps to check the power-on and fan operation of the logic analyzer:

1. Power on the instrument and observe that the On/Standby switch illuminates.
2. Check that the fans spin without undue noise.

3. If everything is properly connected and operational, you should see the modules in the System window of the logic analyzer application.
4. If there are no failures indicated in the System window, the power-on diagnostics pass when you power on the insturment.

Extended Diagnostics

Do the following steps to run the extended diagnostics:

NOTE. *Running the extended diagnostics will invalidate any acquired data. If you want to save any of the acquired data, do so before running the extended diagnostics.*

Prerequisites Warm-up time: 30 minutes

Perform the following tests to complete the functional verification procedure:

1. If you have not already done so, power on the instrument and start the logic analyzer application if it did not start by itself.
2. Go to the System menu and select Calibration and Diagnostics.
3. Verify that all power-on diagnostics pass.
4. Click the Extended Diagnostics tab.
5. Select All Modules, All Tests, and then click the Run button on the property sheet.

   All tests that displayed an "Unknown" status will change to a Pass or Fail status depending on the outcome of the tests.
6. Scroll through the tests and verify that all tests pass.

TLA Mainframe Diagnostics

The TLA Mainframe Diagnostics are a comprehensive software test that checks the functionality of the instruments. To run these diagnostics, do the following steps:

1. Quit the logic analyzer application.
2. Click the Windows Start button.
3. Select All Programs > Tektronix Logic Analyzer > TLA Mainframe Diagnostics.
4. Select your instrument from the Connection dialog box (in most cases this will be the **[Local]** selection).
5. Run the mainframe diagnostics.

CheckIt Utilities

CheckIt Utilities is a comprehensive software application used to check and verify the operation of the PC hardware in the instrument. To run the software, you must have either a keyboard, mouse, or other pointing device.

NOTE. *To check the DVD drive, you must have a test CD installed before starting the CheckIt Utilities. The test CD must have a file with a size between 5 MB and 15 MB.*

To run CheckIt Utilities, follow these instructions:

1. Quit the logic analyzer application.
2. Click the Windows Start button.
3. Select All Programs > CheckIt Utilities.
4. Run the tests. If necessary, refer to the CheckIt Utilities online help for information on running the software and the individual tests.

Certification

The system clock is checked for accuracy, and the input probe channels are checked for threshold accuracy and setup and hold accuracy. The instrument is certifiable if these parameters meet specifications. Complete the performance verification procedures and record the certifiable parameters in a copy of the Calibration Data Report at the end of this chapter.

Performance Verification Procedures

This section contains procedures to verify that the instrument performs as warranted. Verify instrument performance whenever the accuracy or function of your instrument is in question.

Tests Performed

Do the following tests to verify the performance of the instrument. You will need test equipment to complete the performance verification procedures. (See Table 21 on page 18.) If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Table 22: Parameters checked by verification procedures

Parameter	Verification method
System clock (CLK10) accuracy [1]	Verified by the 10 MHz system clock test
Threshold accuracy [1]	Verified by the threshold accuracy test. Certified by running the certification procedure.

Table 22: Parameters checked by verification procedures (cont.)

Parameter	Verification method
Setup and hold window size (data and qualifiers)	Verified directly by setup and hold procedure
Channel-to-channel skew	Verified indirectly by the setup and hold procedure
Internal sampling period	Verified indirectly by the 10 MHz system clock test
Minimum recognizable word (across all channels)	Verified indirectly by the setup and hold procedure and by the Internal Sampling Period
Maximum synchronous clock rate	Diagnostics verify the clock detection/sampling circuitry. Bandwidth is verified indirectly by the at-speed diagnostics, the setup and hold test, and the clock test.
Counters and timers	Verified by diagnostics
Trigger state machine (TSM) sequence rate	Verified indirectly by at-speed diagnostics

1 Certifiable parameter

Checking the 10 MHz System Clock (CLK10)

The following procedure checks the accuracy of the 10 MHz system clock:

Equipment required	Frequency counter Precision BNC cable
Prerequisites	Warm-up time: 30 minutes

1. Verify that all of the prerequisites above are met for the procedure.
2. Connect the frequency counter to the External Signal Out BNC connector on the instrument.
3. Go to the System window and select System Configuration from the System menu.
4. In the System Configuration dialog box, select 10 MHz Clock from the list of routable signals in the External Signal Out selection box and click OK.
5. Verify that the output frequency at the External Signal Out connector is 10 MHz ±1 kHz. Record the measurement on a copy of the calibration data report and disconnect the frequency counter.
6. In the System Configuration dialog box, reset the External Signal Out signal to None.

Threshold Accuracy Test

This procedure verifies the threshold voltage accuracy of the logic analyzer.

Equipment required	Precision voltage reference or a DC signal generator and precision digital voltmeter (accurate to within ±5 mV) Threshold Accuracy test fixture P6810 Logic analyzer probe
Prerequisites	Warm-up time: 30 minutes

Test Equipment Setup

Connect a P6810 probe from the logic analyzer to the voltage source, using the Threshold Accuracy test fixture. If the voltage source does not have the required output accuracy, use a multimeter with the required accuracy to verify the voltage output levels specified in the procedure.

TLA6000 Setup

To set up the logic analyzer for this test, you must define the characteristics of the channel that you are testing, and then set the trigger parameters:

1. Open the Setup window.
   a. In the Group column, enter a name for the probe group that you are testing ("Test" in the example).
   b. Define the signals for the group that you are testing.
   c. Set the sampling to Asynchronous, 2.0 ns.
   d. Set the Acquisition Length to 128K or less.
   e. Set Acquire to Samples.
2. Go to the Trigger window and select the Power Trigger tab. Create a trigger program that triggers the logic analyzer when it does not see all highs or all lows:
   a. Click the If Then button.
   b. Set the channel definition to match the figure shown. (See Figure 2.)
   c. After you set the channel definitions, click OK.

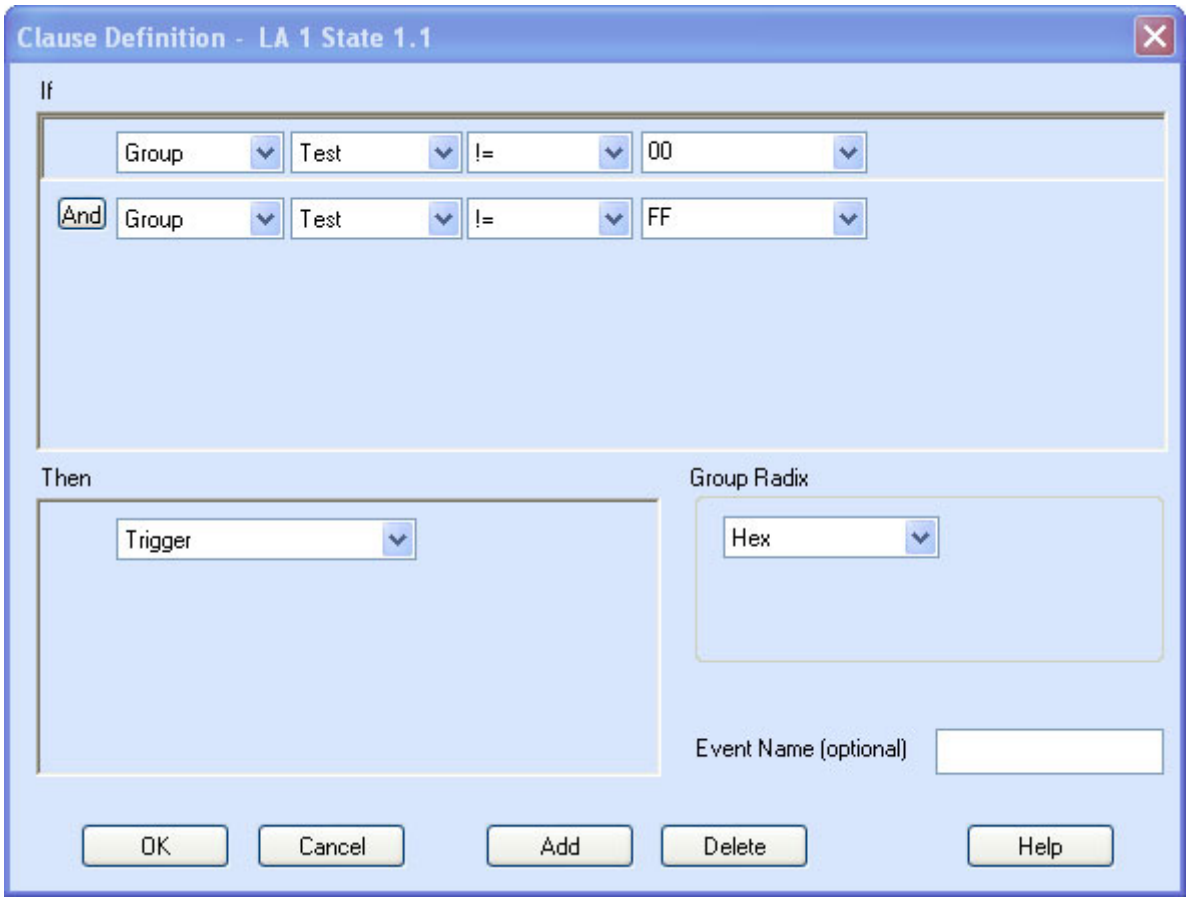


Figure 2: Setting trigger parameters

Verification Procedure

Complete the following steps to complete this procedure. Record the results on the copy of the Calibration Data Sheet.

1. Go to the Setup window of the logic analyzer and set the probe threshold voltages to 4 V.
2. Set the voltage source to 3.850 V.
3. Start the logic analyzer and verify that it does not trigger.
4. Increase the voltage in 10 mV steps, waiting at least 3 seconds between steps to make sure that the logic analyzer continues to run without triggering. Continue until the logic analyzer triggers and then record the voltage.
5. Set the voltage source to 4.150 V.
6. Start the logic analyzer and verify that it does not trigger.
7. Decrease the voltage in 10 mV steps, waiting at least 3 seconds between steps to make sure that the logic analyzer continues to run without triggering. Continue until the logic analyzer triggers and then record the voltage.
8. Add the two voltage values and divide by two. Verify that the result is 4.00 V ±75 mV. Record the voltage on the Calibration Data Sheet.
9. Go to the Setup window and set the logic analyzer threshold voltages to –2.0 V.
10. Repeat steps 3 through 8 for –2.130 V and –1.870 V.
11. Add the two voltage values and divide by two. Verify that the result is –2.00 V ±55 mV. Record the voltage on the Calibration Data Sheet.
12. Repeat the procedure for each probe channel group that you want to verify.

Setup and Hold

This procedure verifies the setup and hold specifications of the logic analyzer.

Equipment required	Tektronix DTG 524 Data Timing Generator with a DTGM30 Output Module Precision BNC cable Setup and Hold test fixture
Prerequisites	Warm-up time: 30 minutes

Digital Timing Generator Setup

1. Verify that the digital timing generator (DTG) has been calibrated so that the channel-to-channel skew is minimized.
2. Set up the DTG so that a channel (CH1 for example), is set to be a clock pattern of alternating 1 and 0 (101010… binary) starting with 1 (rising edge).
3. Set the output frequency to 250 MHz. (This may require you to set the DTG base clock to 500 MHz for this pattern to represent 250 MHz at the channel output.)
4. Set another channel of the DTG (CH2 for example) to a data pattern representing half the period of CH1 (for example 001100110011...binary, starting with 00).
5. Connect the setup and hold test fixtures to the DTG channels that you have set up. Connect 50 Ω SMA terminations to the test fixtures.
6. Connect the DTG channel that you set up as a clock to the appropriate TLA CK[x] input.
7. Connect the other DTG channel to two of the TLA data channels that you want to test.

   To test other TLA data channels simultaneously and your DTG has additional outputs available, set up those DTG channels like the first data channel, and connect them to the other logic analyzer channels that you want to test. (The channels must be in the same probe, and you will need another test fixture for each additional channel pair.) Otherwise, repeat the procedure for each new pair of logic analyzer channels.
8. Set the termination to open on each DTG channel.
9. Set the DTG output voltage levels to 2.0 V High and 0.0 V Low, with no offset.

TLA6000 Setup

1. Start the TLA Application and open the Setup Window.
2. Click the DM button to default the module.
3. Click the Synchronous tab and set the following parameters:
   a. Clock Signal: Choose the clock that you connected the DTG output to.
   b. Max Clock Rate: 450 MHz
   c. Global Threshold: Set to 500 mV.

      With the 50 Ω external termination attached at the SMA fixture end, this sets the logic analyzer threshold voltage levels to one-half the resulting termination voltage, which should be about 500 mV (not 1 V).
4. In the Acquisition Options box, select the following:
   a. Acquisition Length: 1K or greater
   b. Storage Options: Normal
5. Create a new group: right click in the Group Name column.
6. Select Add Group from the pop-up window. Rename the new group Test.
7. In the Probe Channels column, enter the names of the two adjacent data channels that will be used to connect to CH2 of the DTG.

NOTE. *These procedures test two channels. To check more than two channels, be sure to set the group and trigger word widths to the same amount.*

Trigger Logic. To complete the setup, you must configure a trigger to occur whenever the two data lines are neither 00 nor 11 (binary). This will capture the condition when the two data signals are 01 or 10, as they transition to their common values. To set this up, do the following:

8. Open the LA Trigger window and select the Power Trigger tab. Set up three states as shown. (See Figure 3.)

Figure 3: Set the trigger states

Verification Procedure

Complete the following steps to complete this procedure. Record the results on the Calibration Data Sheet.

1. Set the DTG sequencer to RUN and the outputs ON.
2. Press the RUN button on the TLA and wait a few seconds to verify that it does not trigger.
3. Starting from 0.000 ns, increase the delay of the DTG clock channel in 100 ps steps until triggering begins to occur. When the TLA begins to trigger, decrease the delay in 10 ps steps to find the trigger threshold to within 10 ps. Record this delay amount.

   Note that the logic analyzer might trigger because of a glitch when you make a delay change. If the data in the waveform window is correct (all data transitioning at the same time and at the correct frequency), then ignore this "false trigger" and start the logic analyzer again.

   As an alternative, you may want to run the logic analyzer in continuous loop mode if the DTG causes a false trigger on the logic analyzer each time you change the delay. Then observe if the data is correct in the waveform window and ignore any false triggers. Continue increasing the clock delay until the waveform window displays data that was not acquired correctly. Record this delay.
4. Add 0.75 ns to the delay value that you recorded in step 3 and increase the DTG clock delay to match this cumulative value. (For example, if you measured 0.85 ns, increase the delay to 1.60 ns.)
5. Press Run and wait a few seconds to verify that it does not trigger. This verifies that the setup and hold window is less than 0.75 ns, which is the guaranteed specification for a single channel.

   To measure the actual setup and hold window size for your application, slowly decrease the clock delay in steps (waiting a few seconds between steps to verify that it does not trigger), until the logic analyzer triggers. Record this second value. The difference between this second value and the value that you measured in step 3 is the measured setup and hold window size.

Test Fixtures

This section includes information and procedures for building the test fixtures used in the performance verification tests.

Threshold Accuracy Test Fixture

Use this fixture to gain access to the logic analyzer probe pins. The fixture connects all ground pins together, and all signal pins together.

Equipment Required

You will need the following items to build the test fixture:

Item	Description	Example part number
Square-pin strip	0.100 x 0.100, 2 x 8 contacts (or two 1 x 8 contacts)	SAMTEC part number TSW-102-06-G-S
Wire	20 gauge	
Soldering iron and solder	50 W	

Build Procedure

Use the following procedure to build the test fixture.

1. Set the square-pin strip down and lay a wire across one row of pins on one side of the insulator as shown. Leave some extra wire at one end for connecting to a test lead. (See Figure 4.)
2. Solder the wire to each pin in the row.
3. Repeat for the other row of pins.

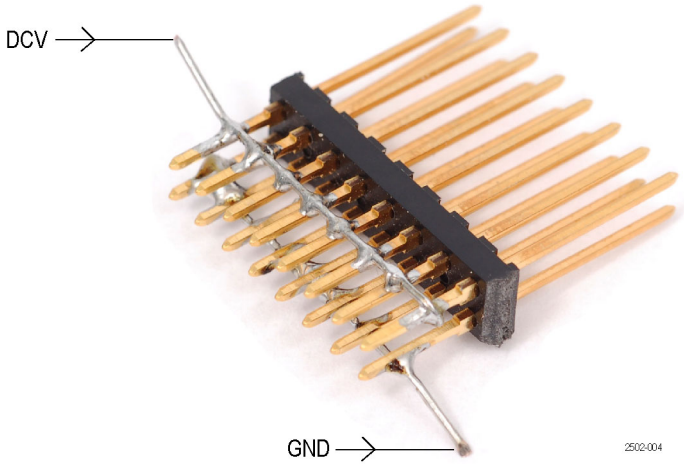


Figure 4: Threshold Accuracy test fixture

Setup and Hold Test Fixture

This fixture provides square-pin test points for logic analyzer probes when they are used to probe in-line SMA connections. Note that you need at least two test fixtures to complete the procedure.

Equipment Required

You will need the following items to build the test fixture:

Item	Description	Example part number
SMA connector (two required for each fixture)	Female, PCB mount	SV Microwave part number 2985-6035, -6036, or -6037
Square-pin strip	0.100 x 0.100, 2 x 2 contacts (or two 1 x 2 contacts)	SAMTEC part number TSW-102-06-G-S
SMA termination	50 Ω, ≥2 GHz bandwidth	Johnson part number 142-0801-866
SMA adapter	Male-to-male	Johnson part number 142-0901-811
Soldering iron and solder	50 W	

Build Procedure

Use the following procedure to build the test fixture.

1. Arrange one SMA connector as shown. (See Figure 5.)
2. Align the square pins at a right angle to the connector.

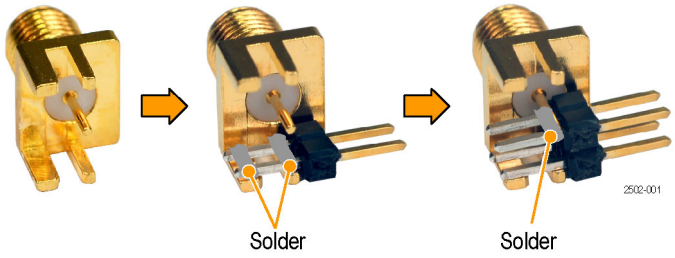


Figure 5: Solder square pins to the SMA connector

3. Solder one set of square pins to the SMA ground conductor.
4. Solder the other set of square pins to the SMA center conductor.

5. Align the second SMA connector to the first as shown and solder the center conductors of the connectors together. (See Figure 6.)

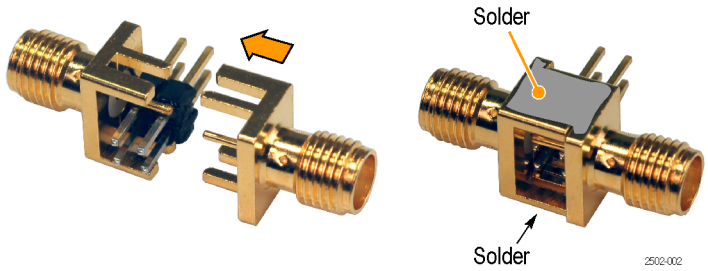


Figure 6: Solder the SMA connectors together

6. Solder the ground conductors of the SMA connectors together.
7. Attach the termination and coupler to the fixture.

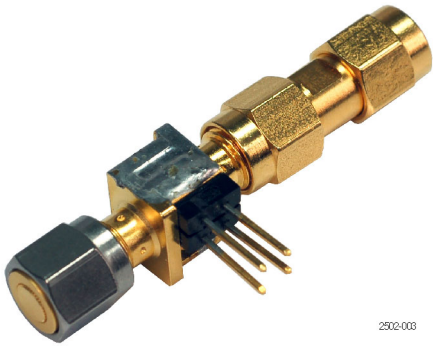


Figure 7: Completed fixture with termination and coupler

Calibration Data Report

Photocopy this table and use it to record the performance test results for your instrument.

TLA6000 Test Record

Instrument model number:
Serial number:
Certificate number:
Verification performed by:
Verification date:

Test Data

Characteristic	Specification	Tolerance	Incoming data	Outgoing data
Clock frequency	10 MHz	±1 kHz (9.9990 MHz-10.0010 MHz)		
Threshold accuracy	+4 V	±100 mV (3.900 V to 4.100 V)		
	-2 V	±100 mV (–1.900 V to –2.100 V)		
Setup and hold window:				
single channel	≤1.00 ns	none		
multiple channels	≤1.50 ns	none		