MIPI® M-PHY

MIPI® M-PHY* Measurements & Setup Library
Methods of Implementation (MOI) for Verification, Debug, Characterization, Conformance and Interoperability Test

077-0518-00

www.tektronix.com

Contacting Tektronix

Tektronix, Inc.
14200 SW Karl Braun Drive or P.O. Box 500
Beaverton, OR 97077 USA

For product information, sales, service, and technical support:

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MODIFICATION RECORD

Sl no	Version	Date	Modification	Page affected
1	0.1 Draft	07/13/2010	First Release with two measurements	
2	0.2 Draft	07/13/2010	First Release with two measurements and Test procedure	
3	0.3 Draft	08/10/2010	Removed all PWM and SYS measurements, ready with 10 setup files	
4	0.4 Draft	09/28/2010	Updated screen short for slew rate	

ACKNOWLEDGMENTS

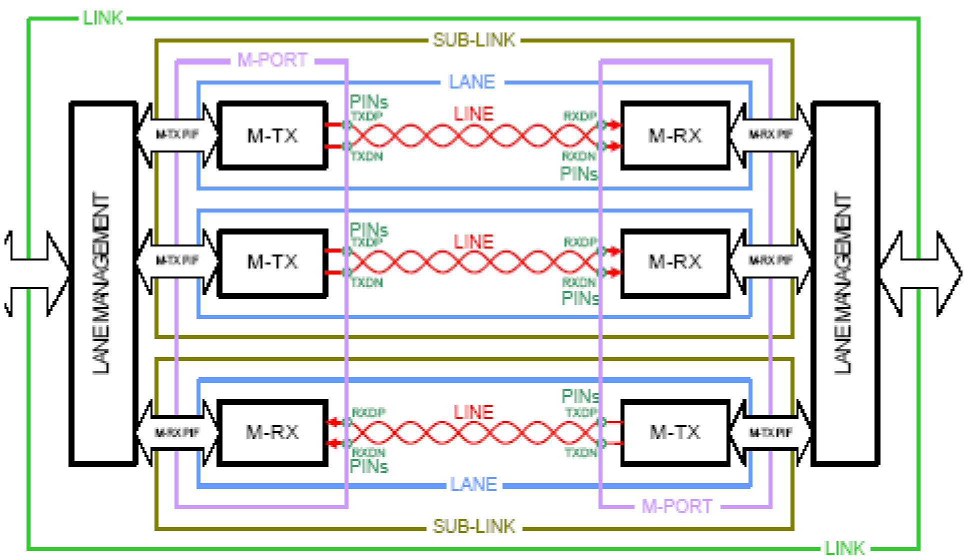
Document has been created by Ramesh P.E & Gejendra Patro, Tektronix, Inc.

INTRODUCTION

Designed to support the DIGIRF V32 protocol, MPHY enables faster data transfer rates with the help of an embedded clock. M PHY is capable of transmitting signals both in the burst mode and in the differential mode of data transfer. Different data rates can be achieved at low speeds and fixed data rates can be achieved at high speeds. M PHY works either with an independent clock embedded at the Transmitter and the Receiver or with a single clock as reference.

The length of the optical fiber converter varies from 10 cm to 1 meter, which operates at faster speed depending on the data rate. Multiple lanes in each direction are incorporated at both Transmitter (TX) and Receiver (RX), which results in a link achieving the required data rate.

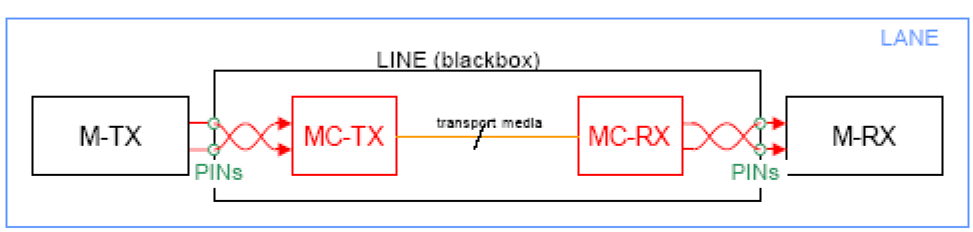
A block diagram of a typical link is as shown below:



A LANE consists of a Single TX, RX and line that connect TX and RX using a differential wire corresponding to two signaling wires DP and DN.

Specifications are defined at the PINS of the M-TX and M-RX. The transmission lines between the two points are called TX lines. A line may contain a converter for other media such as Optical fiber.

For advanced configuration, module and media converters supported are as follows:



An interface based on M-PHY technology shall contain at least one LANE in each direction; there is no symmetry requirement from an M-PHY prospective.

All lanes in a signal link are called SUB links. Two sub links of opposite directions provide bi-directional transport and additional LANE management called LINK. A set of M-TX and M-RX in a device that composes one interface port is denoted as M-Port.

LINE state

Positive differential voltage driven by M-TX is denoted by LINE state DIF-P, a negative differential voltage driven by M-TX is denoted by LINE state DIF-N, and a weak zero differential voltage is maintained by M-RX.

Table 1: Line state

Differential LINE Voltage	M-TX Output Impedance	M-RX Input Impedance	LINE State Set by	LINE State Name
Positive	Low	Any	M-TX	DIF-P
Negative	Low	Any	M-TX	DIF-N
Zero	High	Medium	M-RX	DIF-Z
Unknown or floating	High	High	None	DIF-Q

Termination

M-TX terminates both wires with characteristic impedance during any DIF-P or DIF-N state. M-RX does not terminate the LINE and does so optionally. The option of Terminating or not terminating with characteristic impedance is interchangeable in case of M-RX.

Swing

M-TX supports two drive strengths. One supports 400 mv PK NT (roughly 200 mVPKRT), while small amplitude is 240 mV_NT (120mVPK-RT). Drivers will support bottom if both are supported, default will be large amplitude.

References

[1] DRAFT MIPI Alliance Specification for M-PHY, Version 0.80.00 r0.04 - 12 April 2010

TX TIMERS AND SIGNALING

Overview

The tests provided in this section verify various TX signaling and timing requirements of M-PHY transceivers (M-PHY TX signaling), defined in the M-PHY Specification.

GROUP 1: M-TX REQUIREMENTS

Status

The test descriptions contained in this section are in the draft stage. Additional modifications to both the test descriptions and implementations are expected.

Pay Load

Typical D30.3 pattern:

10 bit pattern consist of the following bits sequence:

1000011100

0111100011

Table 2: Typical M-PHY Signal

Stall	Prepare	Sync Default	Pay Load (D30.3 or CRPAT)	Closure of Burst

Note:

1. *Most of the Measurements are done using Gated Cursor with the Cursor placed in between the payload region.*
2. *Refer to the MPHY specification version .88.*

Test 1.1.1 – Differential DC Output Voltage Amplitude

Purpose

To verify the Differential DC Output Voltage Amplitude ($V_{DIF\_DC\_xx\_xx\_TX}$) of the DUT's transmitter is within the conformance limits, for both Large and Small Amplitudes, and for both terminated and un-terminated cases.

References

[1] M-PHY Specification, Section 5.1.1.2, Line 296

[2] Ibid, Section 5.1.1.6, Table 14

Resource Requirements: See Appendix A.1.

Last Modification: April 27, 2010

Discussion

Section 5 of the M-PHY Specification defines the Electrical Characteristic requirements for M-PHY devices. Included in these requirements is a specification for $V_{DIF\_DC\_TX}$, which is a device's Differential DC Output Voltage Amplitude.

Parameter	Amplitude	Termination	Reference Load	Conformance Min	Conformance Max
VDIF_DC_LA_RT_TX	Large	Terminated	RREF_RT	160mV	240mV
VDIF_DC_SA_RT_TX	Small	Terminated	RREF_RT	100mV	130mV

Table 3: DC Amplitude Parameter Summary

The specification states, "Separate AC and DC parameters are defined for V_{DIF_TX}. The DC parameter $V_{DIF\_DC\_TX}$ is defined for an M-TX which drives a steady DIF-N or a steady DIF-P LINE state into a reference load R_{REF}. An M-TX shall drive differential DC output voltage amplitude which meets the specified limits of $V_{DIF\_DC\_TX}$." [1].

The specification actually defines four different DC amplitude specifications, for both the Large and Small Amplitude configuration cases, as well as the terminated and un-terminated states. These four parameters are defined individually in the specification [2], using separate names. A summary of the parameters is shown in Table 3.

In this test, the DUT's VDIF_DC_xx_xx_TX value will be measured using a high-speed, real-time DSO while the DUT is driving a steady DIF-N or a steady DIF-P LINE state into the specified reference load (RREF_RT, or RREF_NT).

DUT Set Up and Test Procedure:

1. Connect the DUT to the Test System (See Appendix B).
2. Using DUT vendor-specific techniques put the DUT into a state where it is transmitting a HS Burst (*See section on Terminated case*).
3. Launch DPOJET using the main menu → Analyze/Jitter → Eye Analysis. Or, launch the application MIPI ®M-PHY Essential from the Analyze menu.
4. Connect two single-ended probes to Ch1 and Ch2 and use Math1=Ch1-Ch2. If you use a differential probe, connect the probe to Ch1 and go to the Math setup and set Ch1=Math1.
5. Go to Trigger menu, change the trigger Type to Serial, Source to DIF-P (Ch1), Bit rate to 1.248 GB/s, Pattern length is 0111100011 (Binary) 10 bit. See Figure 1.

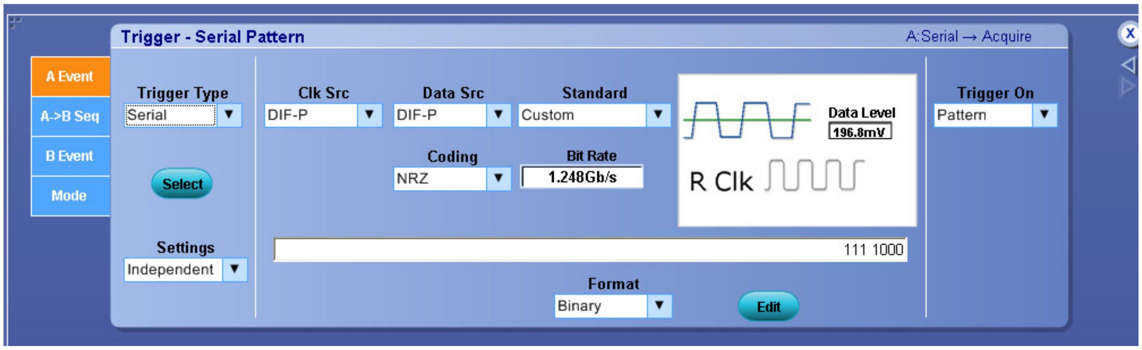


Figure 1: Trigger setup

Terminated case:

1. Connect the DUT to the test setup with R_{REF_RT} terminated across the differential lane. If the signals are connected directly to the oscilloscope, the oscilloscope impedance, which is 50 Ohm, will act as termination.
2. Configure the DUT to transmit data with D30.3 character as payload.
3. Connect the High input impedance Differential probe to the terminated lane.
4. Measure the Mean value of $V_{DIF\text{-}DC\text{-}LA\text{-}RT\text{-}TX}$ using the Post analysis software on the D30.3 pattern.
5. Configure the DUT to transmit a constant DIF-P state using the Small Amplitude Terminated.
6. Measure $V_{DIF\text{-}DC\text{-}SA\text{-}RT\text{-}TX}$ using the DSO.

Unterminated case:

All terminated measurements are not covered at present.

Note: For demo, use AWG and HS_G1_A_Burst_RT.awg files on the AWG7102.

To perform the measurement for HS –TX

HS-TX RT-Termination Mode

1. Set the DUT to operate in HS-TX mode, set the Gear to Highest supported gear, Transmit the **Pattern D.30.3** either in continuous mode or burst mode, and operate on LA mode.
2. Recall the setup file “Test_111_VDIF_DC_LA_RT_TX” under HS-TX, using the main menu → File/Recall…/Setup or click on MIPI Setup.
3. Click on **Single Run** and verify the result as shown below in Figure 2.
4. Verify the DPOJET Measurement result for VDIF-DC-LA-RT-TX is between 160 mV and 240 mV for both DIF-P and DIF-N.

Note: The Gated Cursor must be adjusted if required and should be placed in between the payload region as shown in Figure 2.

Figure 2: VDIF_DC_LA_RT_TX Measurements

1. Set the DUT to operate in HS-TX mode, set the Gear to Highest supported gear, transmit the Pattern D.30.3 either in continuous mode or burst mode, and operate on SA mode.
2. Recall the setup file “Test_111_VDIF_DC_SA_RT_TX” under HS-TX, using the main menu → File/Recall…/Setup, or click on MIPI Setup.
3. Click on **Single Run** and verify the result as shown below in Figure 3.
4. Verify the DPOJET Measurement result for VDIF-DC-SA-RT-TX is between 100 mV and 130 mV for both DIF-P and DIF-N.

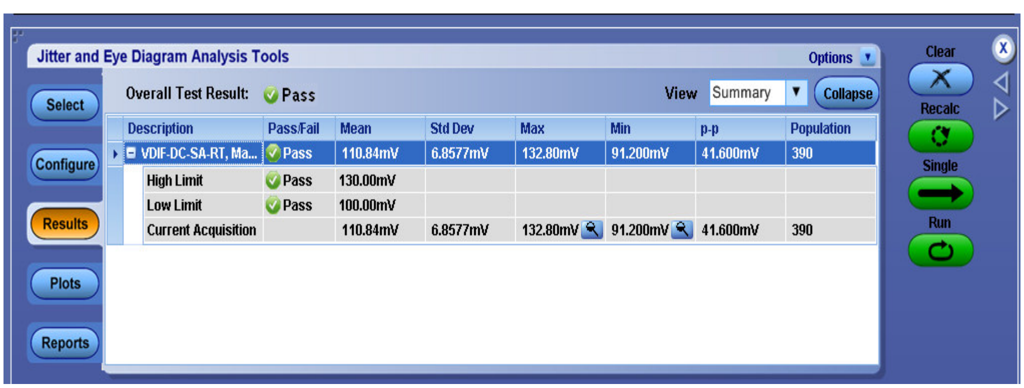


Figure 3: VDIF_DC_SA_RT_TX Measurement

Test 1.1.2 – Differential AC Output Voltage Amplitude

Purpose

To verify the Differential AC Output Voltage Amplitude (VDIF_AC_xx_xx_TX) of the DUT's transmitter is within the conformance limits, for both Large and Small Amplitudes, and for terminated cases.

References

[1] M-PHY Specification, Section 5.1.1.2, Line 297

[2] Ibid, Section 5.1.1.6, Table 14

[3] Ibid, Section 5.1.1.6, Table 14, Note 3

[4] Ibid, Section 5.1.2.8, Line 343

[5] Ibid, Section 5.1.2.11, Table 15

Resource Requirements

See Appendix A.1.

Last Modification

July 13, 2010

Discussion

Section 5 of the M-PHY Specification defines the Electrical Characteristic requirements for M-PHY devices. Included in these requirements is a specification for VDIF_AC_TX, which is a device's Differential AC Output Voltage Amplitude.

The specification states, "The AC parameter VDIF_AC_TX is defined for an M-TX which drives a test pattern into a reference load RREF, where the lower limit of VDIF_AC_TX is defined over the eye opening TEYE_TX as defined in Section 5.1.2.8. The upper limit of VDIF_AC_TX is defined as the maximum differential output voltage, when the M-TX drives a test pattern into a reference load RREF. An M-TX shall drive a differential AC output voltage signal which meets the specified limits of VDIF_AC_TX." [1].

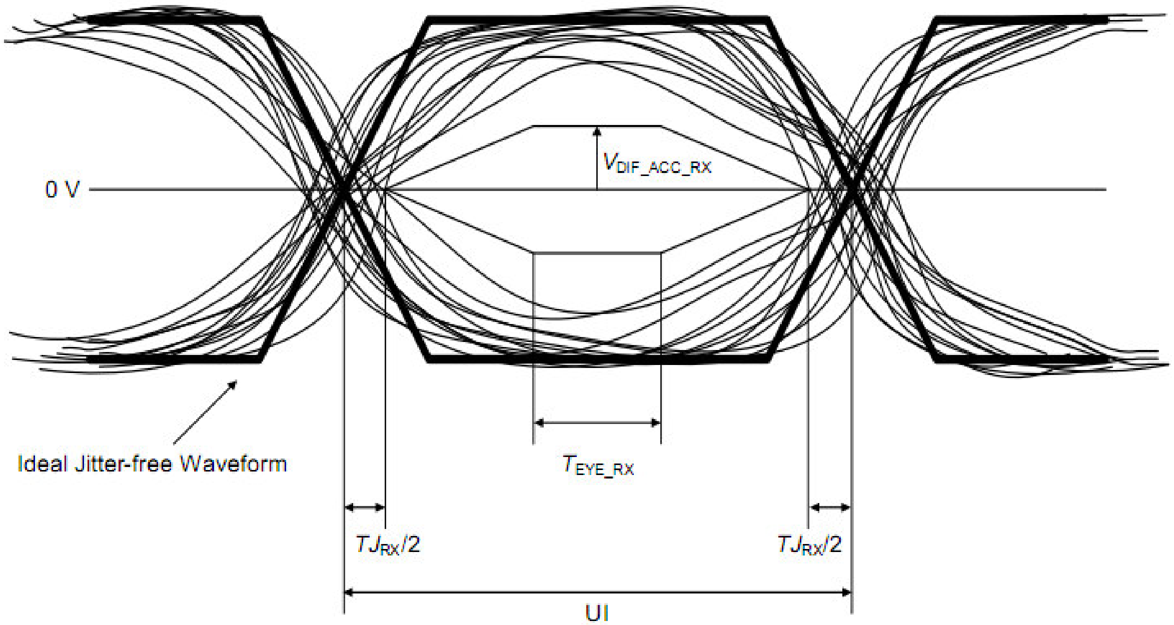


Figure 4: Differential Transmit Eye Diagram

The EYE opening is measured when the DUT is transmitting the Specific CJPAT or CRPAT. The patterns are defined in the specification as part of note 3 table 14 of M-PHY Specification document.

The specification actually defines four different AC amplitude specifications, for both the Large and Small Amplitude configuration cases, as well as the terminated and un-terminated states. These four parameters are defined individually in the specification [2], using separate names. A summary of the parameters is shown below.

Table 4: AC Amplitude Parameter Summary

Parameter	Amplitude	Termination	Reference Load	Conformance Min	Max
$V_{DIF\_AC\_LA\_RT\_TX}$	Large	Terminated	R_{REF_RT}	140mV	250mV
$V_{DIF\_AC\_SA\_RT\_TX}$	Small	Terminated	R_{REF_RT}	80mV	140mV

Unlike the DC specifications, which are defined with respect to static DIF-P and DIF-N states, the AC amplitude parameters limits are defined with the aid of a reference eye mask, and are defined to be measured while the DUT is transmitting specific bit patterns, namely CJTPAT and CRPAT[3]. The eye diagram mask is shown in Figure 4.

Note that while the AC amplitude specifications refer to the eye mask template, the template is merely a graphical representation of the written requirement (shown in Figure 4), which specifies that the absolute value of the AC signal must be greater than the lower limit of $V_{DIF\_AC\_xx\_xx\_TX}$ over the horizontal interval T_{EYE_TX}. (Note that the value of T_{EYE_TX} is defined in a different location in the specification [5], and is defined as a minimum of 0.2 UI_{HS}. Also, the horizontal position of the interval is not strictly defined, and is allowed to be shifted horizontally.)

In this test, the DUT's $V_{DIF\_AC\_xx\_xx\_TX}$ value will be measured using a DSO while the DUT is driving a continuous bit pattern (CJTPAT and CRPAT) into the specified reference load (R_{REF_RT},).

The values of $V_{DIF\_AC\_xx\_xx\_TX}$ for both the Large and Small Amplitude and terminated cases must be within the ranges specified above to be considered conformant.

Test Setup

See Appendix B.1.1.

DUT setup and Test Procedure

1. Connect the DUT to the Test System (See Appendix B).
2. Using DUT vendor-specific techniques, put the DUT into a state where it is transmitting a HS Burst**.** See section on Terminated case.
3. Launch DPOJET using the main menu → Analyze/Jitter → Eye Analysis or, launch the application MIPI ®M-PHY Essential from the Analyze menu.
4. Connect two single-ended probes to Ch1 and Ch2 and use Math1=Ch1-Ch2. If you use a differential probe, connect the Probe to Ch1, and go to Math setup, set Ch1=Math1.
5. Go to Trigger menu, change the trigger Type to Serial, Source to DIF-P (Ch1), Bit rate to 1.248 GB/s, Pattern length is 0111100011 (Binary) 10 bit. Shown as in Figure 4.

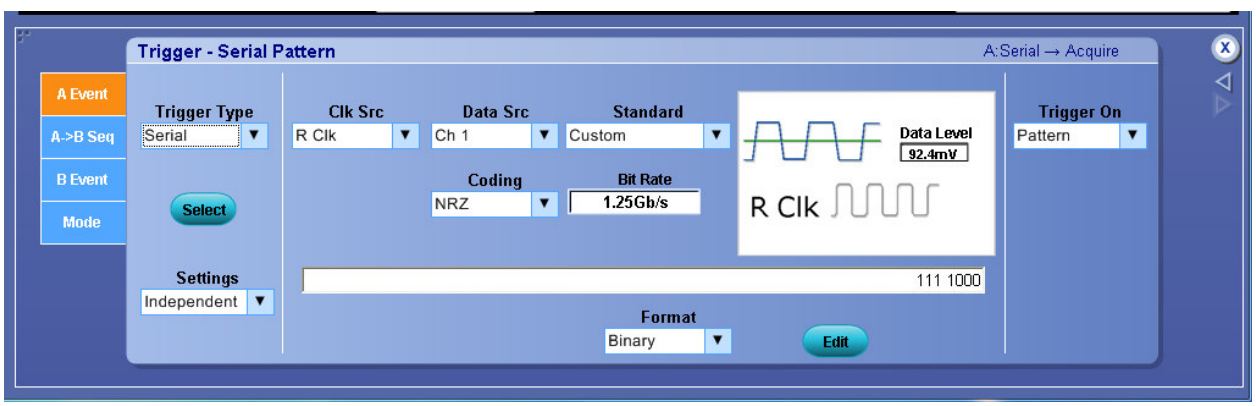


Figure 4: Trigger setup for Differential AC Output Voltage Amplitude

Terminated case:

1. Connect the DUT to the test setup with $\mathbf{R_{REF\_RT}}$ terminated across the differential lane. If the signals are connected directly to the Oscilloscope, the Oscilloscope impedance which is 50 Ohm will act as termination.
2. Configure the DUT to transmit a continuous CJTPAT pattern using the Large Amplitude and measure $V_{DIF-AC-LA-RT-TX\ (CJTPAT)}$.
3. Configure the DUT to transmit a continuous CRPAT pattern using the Large Amplitude and measure $V_{DIF-AC-LA-RT-TX\ (CRPAT)}$.

4. Configure the DUT to transmit a continuous CJTPAT pattern using the Small Amplitude and measure $V_{DIF-AC-SA-RT-TX\ (CJTPAT)}$.
5. Configure the DUT to transmit a continuous CRPAT pattern using the Small Amplitude and measure $V_{DIF-AC-SA-RT-TX\ (CRPAT)}$.

Unterminated case:

All Unterminated measurements are not covered at present

Note: For demo use AWG and Recall HS_G1_A_Burst_RT.awg files on the AWG7102

To perform the measurement for HS –TX

HS –TX RT-Termination Mode

1. Set the DUT to operate on HS-TX mode, set the Gear to Highest supported gear, Send the CJTPAT or CRPAT Pattern, either in continuous mode or burst mode and operate on LA mode.
2. Recall setup file under SYS-TX folder “Test_112_VDIF_AC_LA_RT_TX”, using the main menu → File/Recall…/Setup or click on MIPI Setup.
3. Click on **Single Run** and Verify the result as shown below in the Figure 5 and Figure 6.
4. Verify the DPOJET Measurement result for $V_{DIF-AC-LA-RT-TX}$ is between 140 mV and 250 mV for both the DIF-P and DIF-N cases.

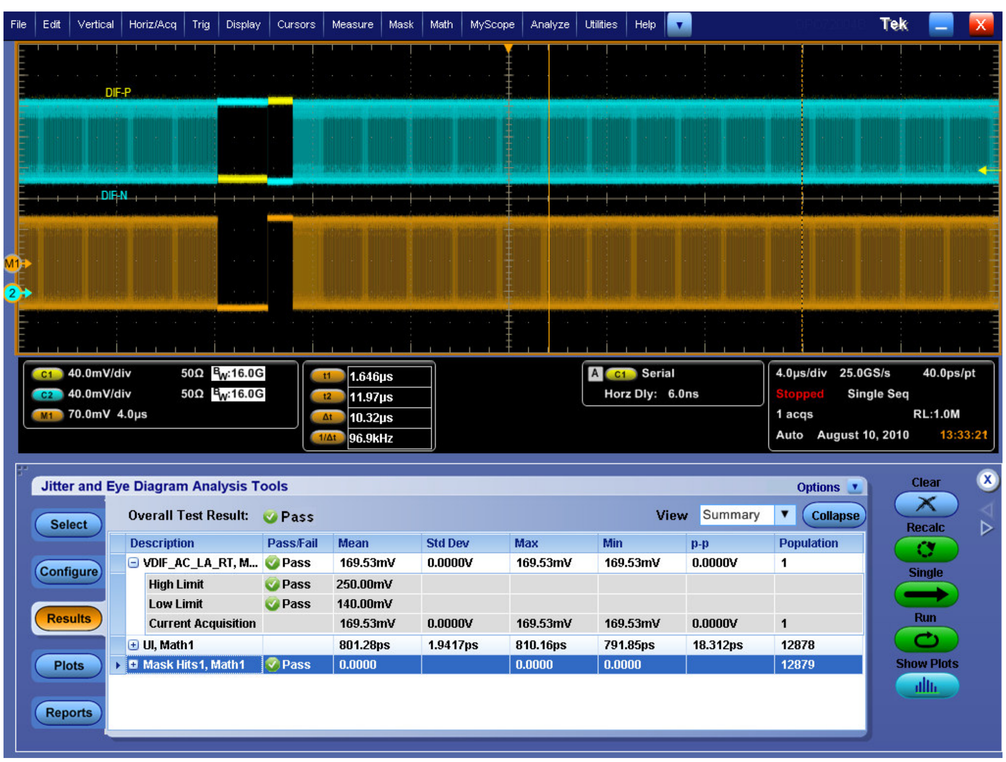


Figure 5: VDIF_AC_LA_RT_TX Measurements

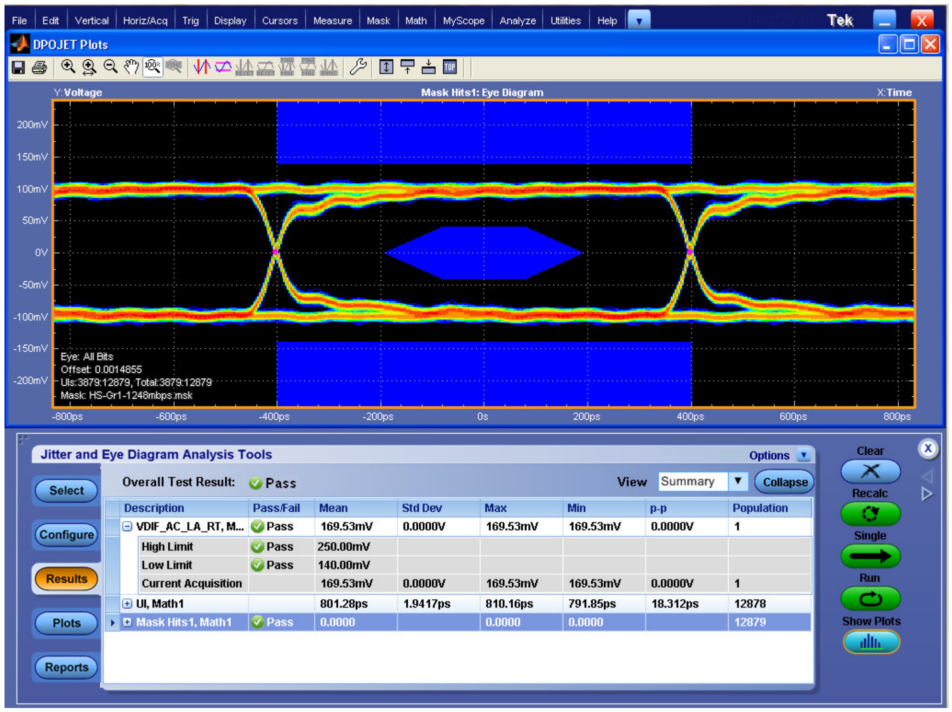


Figure 6: VDIF_AC_LA_RT_TX EYE Diagram

5. Set the DUT to operate on HS-TX mode, set the Gear to Highest supported gear, Send the CJTPAT or CRPAT Pattern either in continuous mode or burst mode and operate on SA mode.
6. Set the DUT to operate on HS-TX mode, set the Gear to Highest supported gear, Send the CJTPAT and CRPAT Pattern either in continuous mode or burst mode and operate on SA mode.
7. Recall setup file under-TX “Test_112_VDIF_AC_SA_RT_TX”, using the main menu → File/Recall…/Setup or click on MIPI Setup.
8. Click on **Single Run** and verify the result as shown below in Figure 7.
9. Verify the DPOJET Measurement Result for $V_{DIF\text{-}AC\text{-}SA\text{-}RT\text{-}TX}$ is between 80mV and 140 mV for both the DIF-P and DIF-N cases.

Figure 7: VDIF_AC_SA_RT_TX Measurements

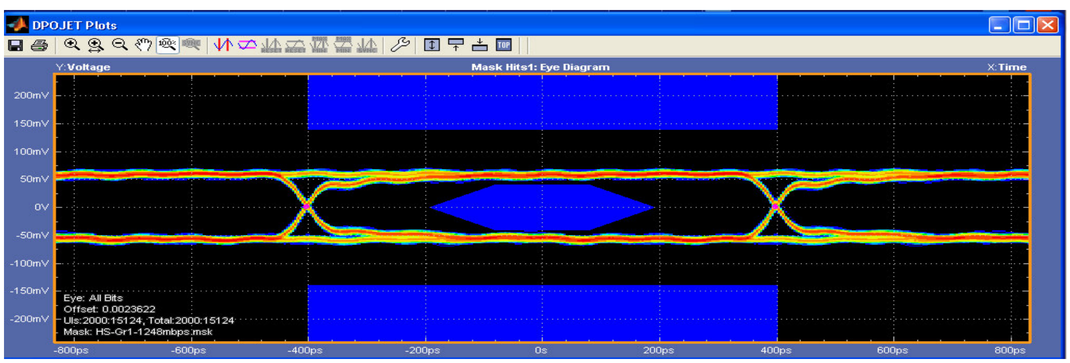


Figure 7 A: VDIF_AC_SA_RT_TX EYE Diagram Measurements

Test 1.1.3 – Common Mode Output Voltage (VCM_TX)

Objective

To measure the common mode voltage when the PHY is signaling data in differential mode and other ends are terminated.

Reference

[1] M-PHY specification 0.88 Table 14

[2] Section 5.1.1.2

[3] Equation 3

To performing the measurement for HX-TX

The common-mode output voltage signal $V_{CM\_TX}(t)$ is defined as the arithmetic mean value of the signal

Voltages $V_{TXDP}(t)$ and $V_{TXDN}(t)$ when the M-TX drives a test pattern into a reference load R_{REF}. V_{CM_TX} is

Defined as the amplitude of $V_{CM\_TX}(t)$. $V_{CM\_TX}(t)$ can be calculated from the following equation:

$$V_{CM\_TX}(t) = \frac{V_{TXDP}(t) + V_{TXDN}(t)}{2}$$

Measurement	Amplitude type	Termination	Load	Minimum Value	Maximum Value
$V_{CM\_LA\_TX}$	Large Amplitude	R_{REF_RT}	50 Ohms	160mV	260mV
$V_{CM\_SA\_TX}$	Small Amplitude	R_{REF_RT}	50 Ohms	80mV	190mV

Probing Type

Single ended and not differential probe

Pre requisite

Oscilloscope Deskew is done and define the math as A as per above equation 1

Acquisition Setup

Based on the operating Data rate, acquire the waveform to occupy the 10000 unit interval.

DUT setup

For all three modes (PWM, HS, SYS), program the DUT to send the Data burst that has more than 10000 UI.

Note: For demo, use HS_G1_A_Burst_RT.awg files on the AWG7102.

PWM mode

Will be available soon.

Algorithm

Identify the start portion of the data payload, consider the record points that covers more than 10000 unit interval, Do math operation to get the Common mode voltage, Measure mean value of the common mode voltage as final value.

DUT setup and Test Procedure

1. Connect the DUT to the Test System (See Appendix B)
2. Using DUT vendor-specific techniques put the DUT into a state where it is transmitting a HS Burst as mentioned in the section on Terminated case.
3. Launch DPOJET using the main menu → Analyze/Jitter → Eye Analysis or Launch the application MIPI ®M-PHY Essential from the Analyze menu.
4. Connect two single ended probes to Ch1 and Ch2.
5. Go to Trigger menu, change the Trigger Type to Serial, Source to (Ch1), Bit rate to 1.248Gb/s, Pattern length is 0111100011 (Binary). See Figure 8.

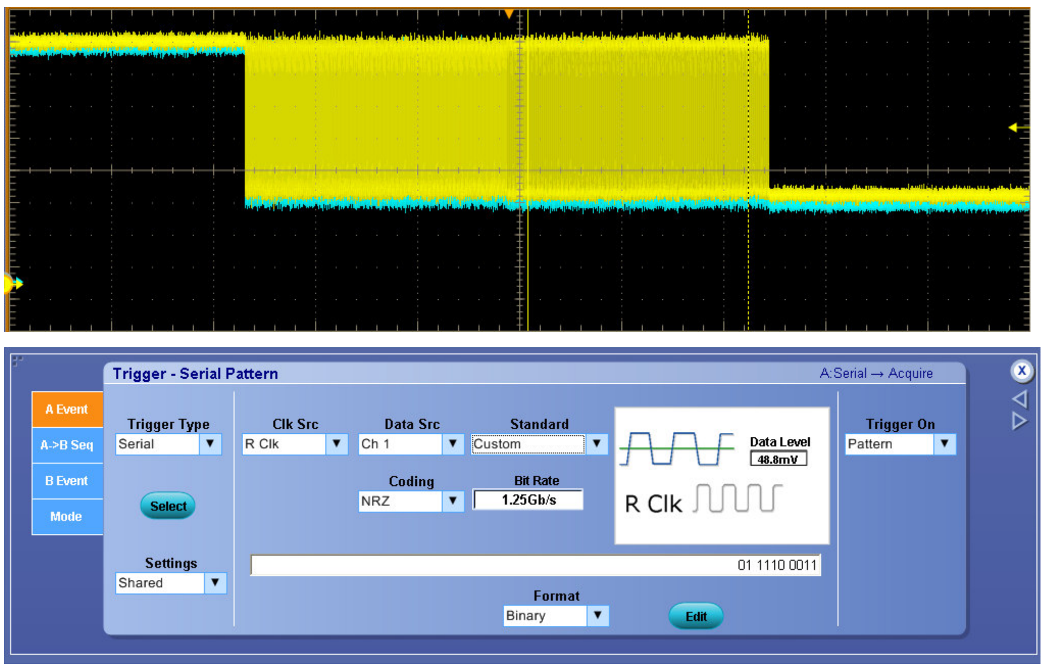


Figure 8: Trigger setup for Common Mode Output Voltage

To perform the measurement for HS –TX

HS –TX RT-Termination Mode

1. Set the DUT to operate on HS-TX mode, set the Gear to Highest supported gear, Send the **D.30.3 Pattern**, either in continuous mode or burst mode and operate on LA mode.
2. Recall Setup file under HS-TX folder "Test_113_$V_{CM-LA-TX}$ _TX", using the main menu → File/Recall…/Setup or click on MIPI Setup.
3. Click on **Single Run** and verify the result as shown below in Figure 9 and Figure 10.
4. Verify the DPOJET Measurement Result for $V_{CM-LA-TX}$ is between 160 mV and 260 mV for both the DIF-P and DIF-N cases.

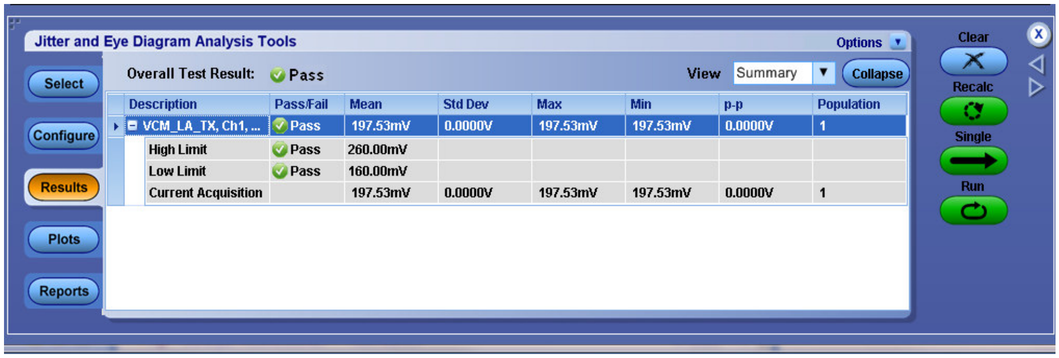


Figure 9: LA Common Mode Output Voltage

5. Set the DUT to operate on HS-TX mode, set the Gear to Highest supported gear, Send the CJTPAT or CRPAT Pattern either in continuous mode or burst mode and operate on SA mode.
6. Set the DUT to operate on HS-TX mode, set the Gear to Highest supported gear, Send the CJTPAT and CRPAT Pattern either in continuous mode or burst mode and operate on SA mode.
7. Recall Setup file under HS-TX "Test_113_VCM-SA-TX", using the main menu → File/Recall…/Setup or click on MIPI Setup.
8. Click on **Single Run** and Verify the result as shown below in the Figure 10.
9. Verify the DPOJET Measurement Result for VCM-SA-TX is between 80mV and 190 mV for both the SE-P and SE-N cases.

Figure 10: LA Common Mode Output Voltage

Test 1.2.1: Rise Time and Fall Time measurement

Objective

Perform the rise time and fall time measurement on differential signaling when the DUT is being operated in HS mode.

References

[1] M-PHY specification 0.88 Table 15

[2] Section 5.1.2.1 Rise time and fall time

Definition

The HS-TX rise and fall times $T_{R\_HS\_TX}$ and $T_{F\_HS\_TX}$, respectively, are defined as transition times between the 20% and 80% signal levels of the differential HS-TX output signal, whose amplitude is defined by $V_{DIF\_DC\_TX}$, when driving a repetitive **D.30.3** symbol sequence into a reference load R_{REF}. The minimum limits of $T_{R\_HS\_TX}$ and $T_{F\_HS\_TX}$ shall be met by an HS-TX when operated in HS-GEAR1. The maximum Transition times are bounded by the HS-TX eye diagram specification.

Limit Values

There is no Max limit specified, It should be interpreted from Eye diagram. According to Eye diagram, the opening of Center vertex is limited by Max RX jitter (See Table 20 of M-PHY specification), which is 0.52UI. It allows about 0.26 UI from the Center of Eye opening or 0.24UI from the Cross over

The Rise Time and Fall Time can be maximum of without failing the Eye diagram can be 0.48 UI.

The other dimension is slew rate limitation which will limit the rate of Rise of the signal. The minimum slew rate for Hs signal is 0.35V/nsec and Maximum is 0.9V/nsec.

The max and min voltage swing for 500mV for LA and 140mV for SA. So for the large swing from slew rate point of view, the max rise time is

$$0.5/0.35 = 1.4285\text{nsec}$$

Minimum is 0.2 UI in HS speed Gear 1 (1457Mbps) is 137 psec, where as the max limit is 1.4285nsec. But according to Eye diagram, the max rise time is 0.48UI, so it will be 322 psec. So I think we have considered the Rise time limit value from the eye diagram as 322 psec.

Measurement	Amplitude type	Termination	Load	Min	Max
TF_HS_TX	Large Amplitude/Small Amplitude	RREF_RT	50 Ohms	0.2UI	0.48UI
TR_HS_TX	Large Amplitude/Small Amplitude	RREF_RT	50 Ohms	0.2UI	0.48UI

Note: The limit value are our opinion, this can be revisited.

DUT setup

Set the DUT to operate at HS mode on the Gear that it is suppose to operate.(Gear1 or Gear 2). Send the Data payload as D30.3 pattern or CRPAT.

Algorithm

Measure the DC differential voltage using the measurement 1.1.1, Calculate the 20% and 80% level, enter those values as part f High and Low configuration

If you are using D30.3 pattern, Use the Cursor to indicate start of the pay load and end of payload, enter the 20% and 80% as ref level for the measurement

Perform the RT and FT measurement using the oscilloscope Built in or DPOJET based measurement.

If the DUT is set to CRPAT, Find the location of D30.3 pattern in CPAT pattern, Measure the RT and FT on the Transition of D30.3 pattern filed.

DUT setup and Test Procedure

1. Connect the DUT to the Test System (See Appendix B).
2. Using DUT vendor-specific techniques put the DUT into a state where it is transmitting a HS Burst as mentioned in the section on Terminated case.
3. Launch DPOJET using the main menu → Analyze/Jitter and Eye Analysis. Or launch the application MIPI ®M-PHY Essential from the Analyze menu.
4. Connect two single ended probes to Ch1 and Ch2 and use Math1=Ch1-Ch2, If Differential probe is used, connect the Probe to Ch1 and go to Math setup, make Ch1=Math1.
5. Go to Trigger menu, change the trigger Type to Serial, Source to DIF-P(Ch1), Bit rate to 1.248Gb/s, Pattern length is 0111100011 (Binary). See Figure 11.

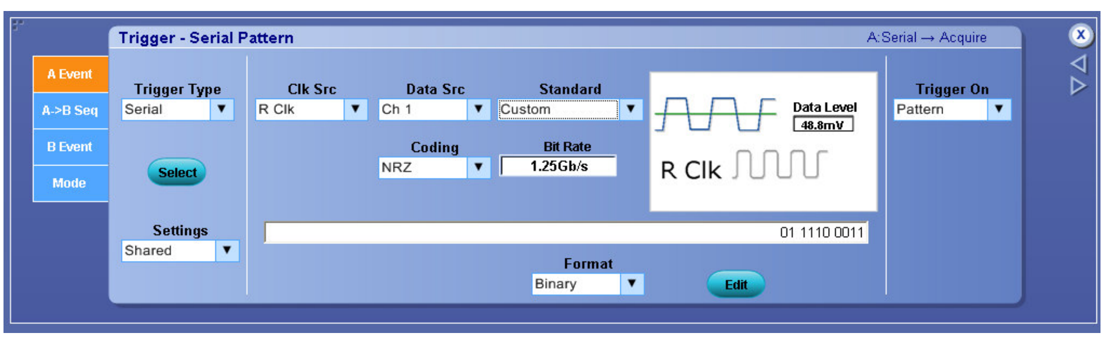


Figure 11: Trigger setup for Rise Time and Fall Time measurement

To perform the measurement for HS –TX

HS –TX RT-Termination Mode

1. Set the DUT to operate on HS-TX mode, set the Gear to Highest supported gear, Send the payload as D30.3 pattern or CRPAT Pattern, either in continuous mode or burst mode and operate on LA mode.
2. Recall Setup file under HS-TX folder "Test_121_RT_FT_LA_HS_TX", using the main menu → File/Recall…/Setup or click on MIPI Setup.
3. Click on **Single Run** and Verify the result as shown below in the Figure 12.
4. Verify the DPOJET Measurement Result for TF_HS_TX is between .02UI and .048UI for both the DIF-P and DIF-N cases.
5. Verify the DPOJET Measurement Result for TR_HS_TX is between .02UI and .048UI for both the DIF-P and DIF-N cases.

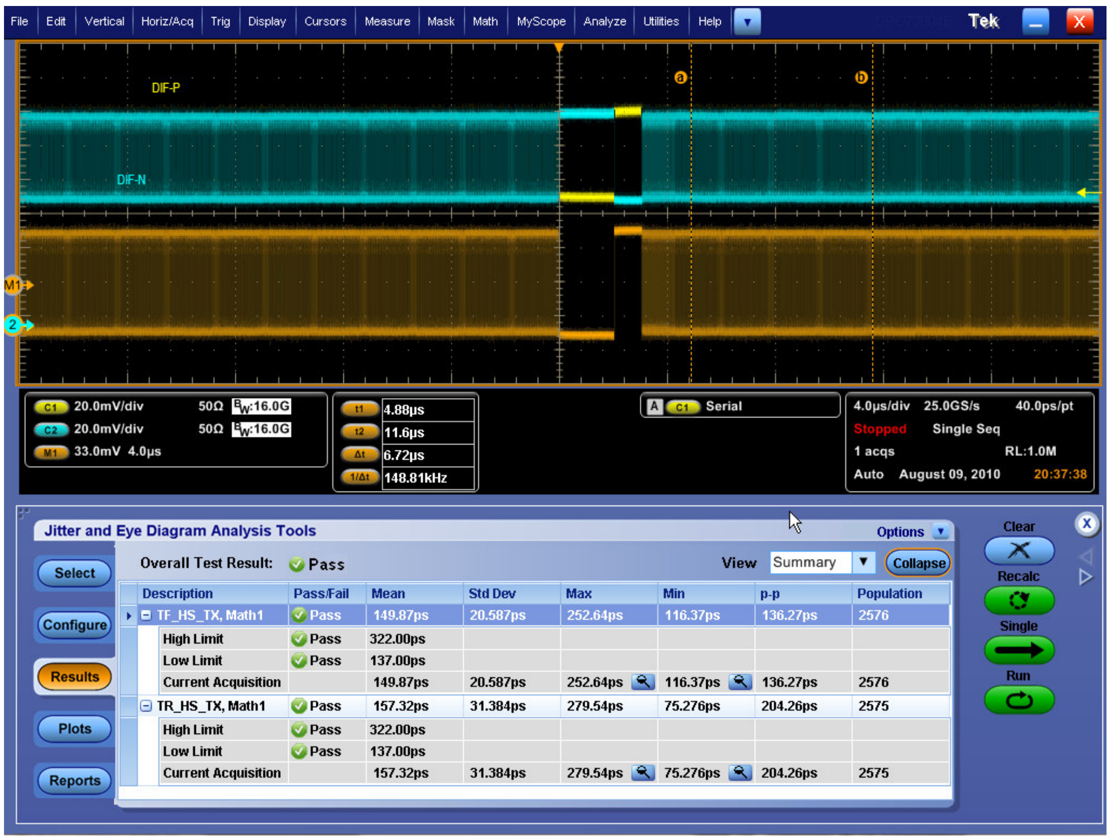
Figure 12: Rise Time and fall Time for LA signals

6. Set the DUT to operate on HS-TX mode, set the Gear to Highest supported gear, Send the CJTPAT and CRPAT Pattern either in continuous mode or burst mode and operate on SA mode.
7. Recall Setup file under HS-TX "Test_121_RT_FT_SA_HS_TX", using the main menu → File/Recall…/Setup or click on MIPI Setup.
8. Click on **Single Run** and Verify the result as shown below in the Figure 13 and Figure 14.

9. Verify the DPOJET Measurement Result for TF_HS_TX is between .02UI and .048UI for both the DIF-P and DIF-N cases.
10. Verify the DPOJET Measurement Result for TR_HS_TX is between .02UI and .048UI for both the DIF-P and DIF-N cases.

Note:

- *The typical UI value for Gear-1 data rate @ 1.248Gbps is 800ps.The below limit value are calculated based on the Gear-1 speed. For a Different data rate, a different limit file will be used.*
- *The Gated Cursor need to be adjusted if required and should be placed in between the payload region as shown in Figure 13.*



Description	Pass/Fail	Mean	Std Dev	Max	Min	p-p	Population
TF_HS_TX, Math1	Pass	149.87ps	20.587ps	252.64ps	116.37ps	136.27ps	2576
High Limit	Pass	322.00ps					
Low Limit	Pass	137.00ps					
Current Acquisition		149.87ps	20.587ps	252.64ps	116.37ps	136.27ps	2576
TR_HS_TX, Math1	Pass	157.32ps	31.384ps	279.54ps	75.276ps	204.26ps	2575
High Limit	Pass	322.00ps					
Low Limit	Pass	137.00ps					
Current Acquisition		157.32ps	31.384ps	279.54ps	75.276ps	204.26ps	2575

Figure 13: Rise Time and fall Time for SA signals

Test 1.1.5 – HS-TX Slew Rate (SRDIF_TX) Measurement

Purpose

To verify that the Slew Rate (SR_{DIF_TX}) of the DUT's HS transmitter is within the conformance limits

References

[1] M-PHY Specification, Section 5.1.2.2, Line 317

[2] Ibid, Section 5.1.2.11, Table 15

Resource Requirements

See Appendix A.1.

Last Modification

April 27, 2010

Discussion

Section 5 of the M-PHY Specification defines the Electrical Characteristic requirements for M-PHY products. Included in these requirements is a specification for SR_{DIF_TX}, which is the HS-TX Slew Rate.

The specification states, "The slew rate SRDIF_TX is defined as the ratio ΔV/ ΔT, where ΔV is the absolute value of the voltage difference of the differential HS-TX output signal voltage measured at the 20% and 80% levels of VDIF_DC_SA_RT_TX and ΔT is the corresponding time difference when the HS-TX drives a reference load RREF with Small Amplitude. The specification limits of SRDIF_TX shall be met by an HS-TX that supports slew rate control and which is operated in HS-G1." [1].

Test Setup

See Appendix B.1.1.

Test Procedure

1. Connect the DUT to the Test Setup,
2. Observable Results:
3. Verify that the maximum $\delta V/\delta t_{SR}$ is less than 150mV/ns across the entire edge, for each Data Lane.
4. Verify that the minimum $\delta V/\delta t_{SR}$ is greater than 30mV/ns across the 400 to 930mV region, for each Data Lane.

Possible Problems

None.

DUT setup and Test Procedure

1. Connect the DUT to the Test System (See Appendix B)
2. Using DUT vendor-specific techniques, put the DUT into a state where it is transmitting a HS Burst.
3. Launch DPOJET using the main menu → Analyze/Jitter → Eye Analysis or launch the application MIPI ®M-PHY Essential from the Analyze menu.
4. Connect two single ended probes to Ch1 and Ch2 and use Math1=Ch1-Ch2, If Diffential probe is used, connect the Probe to Ch1 and go to Math setup, make Ch1=Math1.
5. Go to Trigger menu, change the trigger Type to Serial, Source to DIF-P(Ch1), Bit rate to 1.248Gb/s, Pattern length is 0111100011 (Binary). See Figure 14.

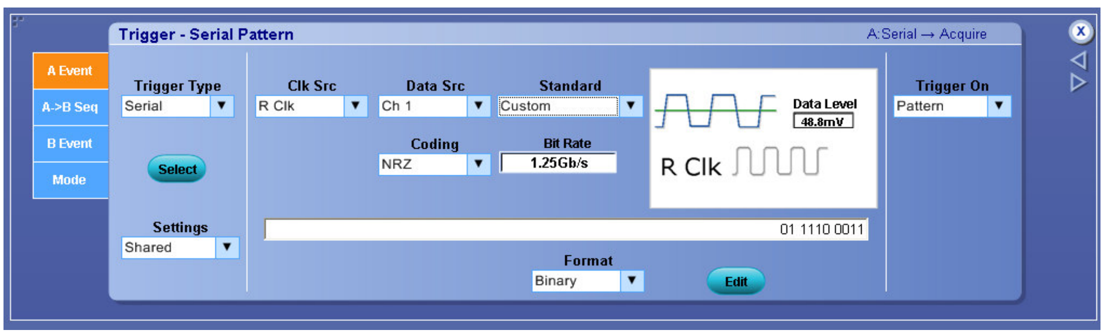


Figure 14: Trigger setup for Slew Rate Measurement

To perform the measurement for HS –TX

HS –TX RT-Termination Mode

1. Set the DUT to operate on HS-TX mode, set the Gear to Highest supported gear, Send the payload as D30.3 pattern or **CRPAT Pattern**, either in continuous mode or burst mode and operate on LA mode.
2. Recall Setup file under HS-TX folder “Test_115_SRDIF_LA_TX_Slew Rate”, using the main menu → File/Recall…/Setup or click on MIPI Setup.
3. Click on **Single Run** and Verify the result as shown in Figure 15.
4. Verify the DPOJET Measurement Result for “SRDIF_LA_TX_Slew Rate” is between 647.5mV/ns to 1.665V/ns for both the DIF-P and DIF-N cases.

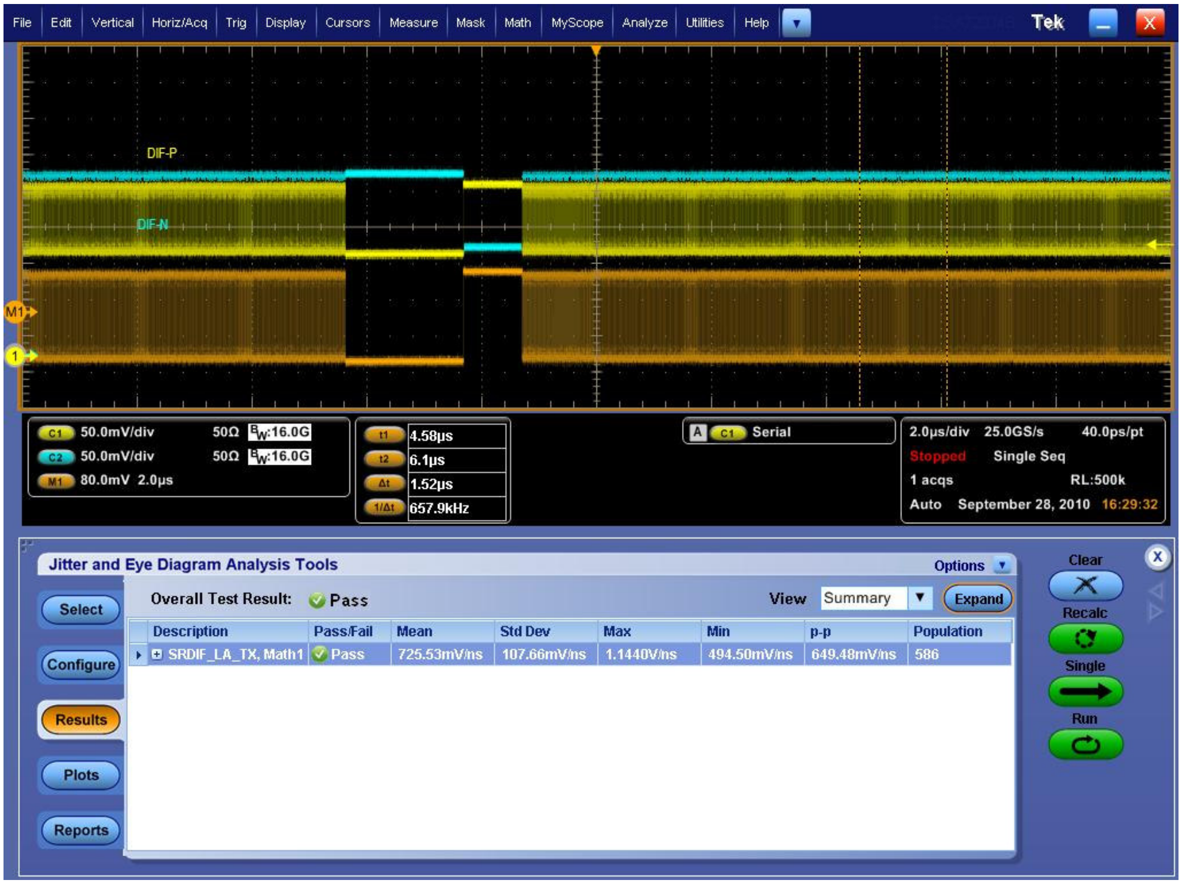


Figure 15: LA Slew Rate Measurement

Note: The Gated Cursor need to be adjusted if required and should be placed in between the payload region as shown in Figure 15.

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5. Set the DUT to operate on HS-TX mode, set the Gear to Highest supported gear, send the CJTPAT and **CRPAT Pattern** either in continuous mode or burst mode and operate on SA mode.
6. Recall Setup file under HS-TX "Test_115_SRDIF_SA_TX_Slew Rate", using the main menu → File/Recall…/Setup or click on MIPI Setup.
7. Click on **Single Run** and Verify the result as shown in Figure 15.
8. Verify the DPOJET Measurement Result for "SRDIF_SA_TX_Slew Rate is between 350mV/ns to 900mV/ns for both the DIF-P and DIF-N cases.

Figure 16: SA Slew Rate Measurement

Note: The Gated Cursor need to be adjusted if required and should be placed in between the payload region as shown in Figure 16.

Appendix A – Resource Requirements

The resource requirements include two separate sets of equipment.

A.1 Equipment for M-PHY* tests

1. Real-time Digital Oscilloscope (any one of the following instruments)
    - Preferred DSA/DPO70604/70804 (6 GHz and above bandwidth)

2. Software
    - DPOJET with MIPI M-PHY option

3. Two probes P7240 for DSA/DPO70K

4. (2) Cables - 1 meter SMA cable

5. (2.) TCA-292MM or TCS-SMA

Appendix B – DUT Connection