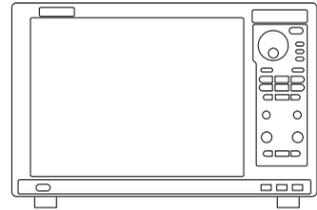


5 Steps to Successful PCI Express Data Capture

Before beginning these procedures, please refer to the *Tektronix Logic Protocol Analyzer Solutions for PCI Express 3.0 Instruction manual* (part number 077-0400-xx) to ensure that you have the proper module and probe type for the link width that you plan to use with your SUT.

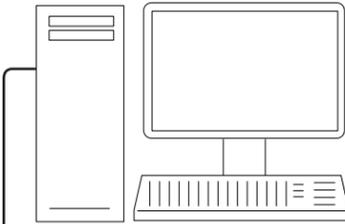
1 CONFIGURE

TLA7012 Portable mainframe configuration

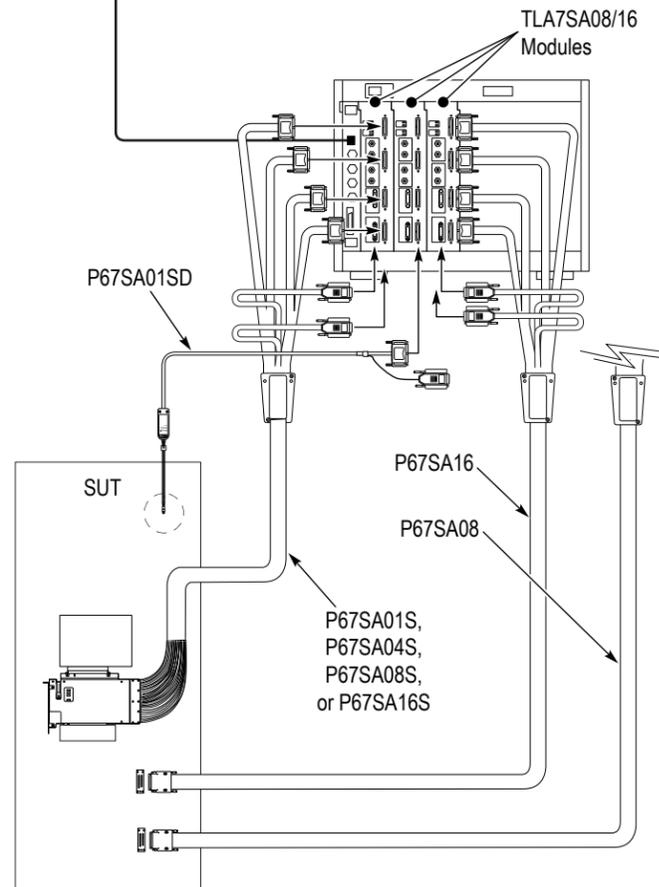
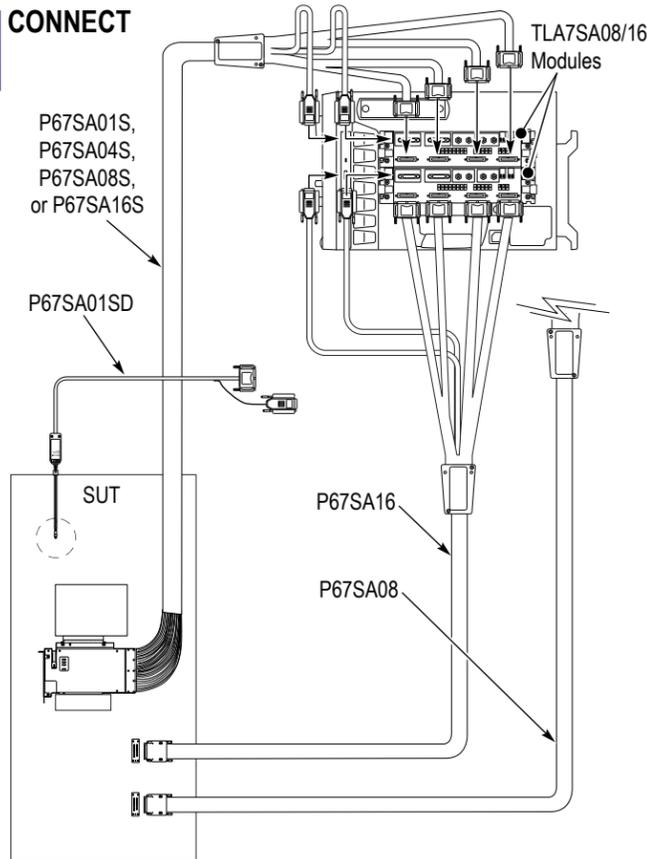


Install the TLA Application software V6.1+. Go to www.tek.com to download the latest software.

TLA7016 Benchtop mainframe configuration



2 CONNECT

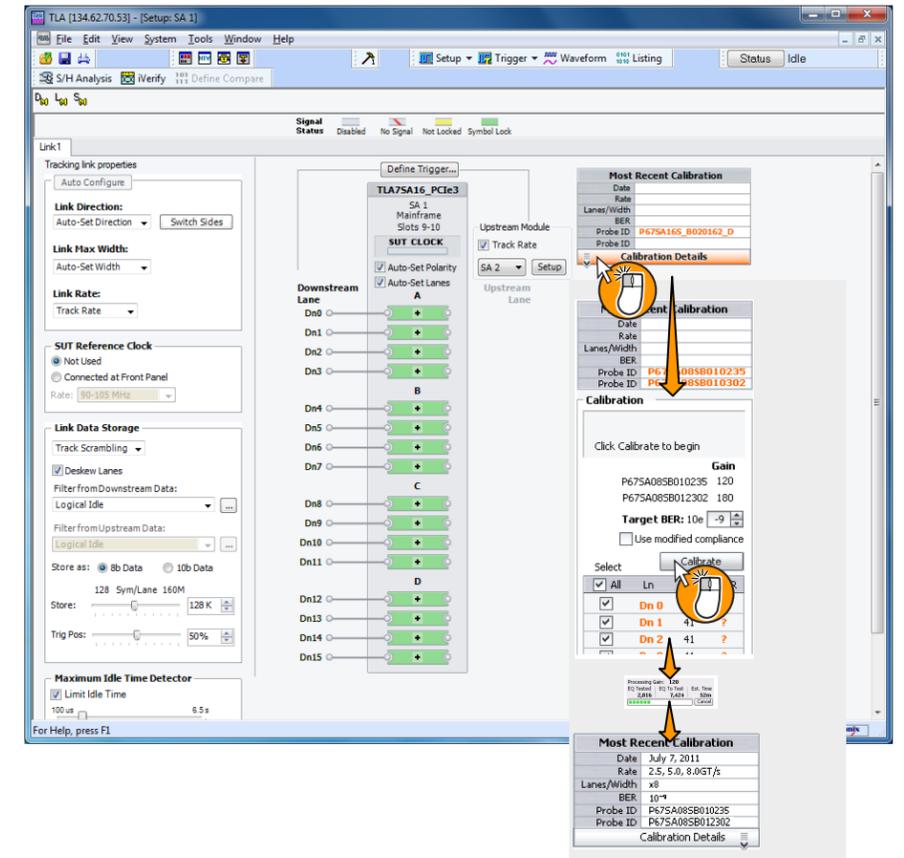


3 CALIBRATE

1. Power on the TLA mainframes and PC, if connected (make sure SUT is off or can be reset).
2. Launch TLA application and connect to the desired TLA instrument (mainframe).

NOTE: The following step is important because the probe might not be calibrated and may not capture training sets indicating the link speed, which is done automatically once the probe is calibrated.

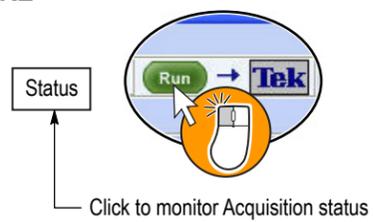
3. In the Setup-SA Window, if using the clock reference cable, select "Connected at Front Panel." If using two modules, connect the clock reference cable to one module. Use clock jumper (part number 174-5392-XX) to connect between both modules.
4. Power on the platform (SUT).
5. In the Setup-SA Window, manually select the Link Rate to match your platform's current PCIe link rate.
6. Configure the SUT for calibration by ensuring the SUT will operate on Reset with ASPM disabled and operating at PCIe maximum link speed with minimal traffic, such as, logical idle. If you made any changes to your SUT, reset it.
7. In the Setup-SA Window, click the "Calibrate" button.
8. Once calibration has successfully completed, manually change the link Rate back to "Track Rate."
9. Reset your SUT so that the TLA will capture the training sets indicating the link speed and width of your SUT.
10. After your SUT has passed its power-on self-tests, verify that the Setup-SA Window indicators are green for each lane, indicating successful symbol lock.



NOTES: Tektronix recommends connecting the clock reference cable (part number 872-0594-XX) and enable it in the SUT (see CALIBRATE step #4), especially if Spread Spectrum or Active State Power Management (ASPM) is enabled. If using the clock reference cable with two TLA7SA08/SA16 modules, use the SMA-to-SMA clock jumper cable (part number 174-5392-XX).

If you don't have a 3-pin 100 MHz reference clock on your SUT, connect the clock reference cable directly to your slot interposer probe.

4 ACQUIRE



Click to monitor Acquisition status

5 ANALYZE

After acquisition is complete, click "View Summary" to confirm that calibration was successful and to get an overview of the PCIe protocol elements acquired. Your screen should show no errors, similar to the screen below.

Summary Statistics	
Average Transaction Latency: 301ns	Total bytes Transmitted: 3.79KB
Utilization: 123K TLP+DLLP pkts/s	757 TLP pkts/s
	123K DLLP pkts/s

Protocol Element	In Viewfinder		In Total		Overview			
	Up	Dn	Up	Dn	Max	Up	Max	Dn
Errors	0	0	103	63	103		63	
TLPs	13	16	655	945	448		470	
MRd	0	2	6	592	6		397	
MWr	0	2	4	299	3		277	
IOrd	0	0	0	0	0		0	
IOWr	0	0	0	0	0		0	
CfgRd	0	6	0	41	0		34	
CfgWr	0	4	0	6	0		4	
Messages	0	1	6	1	6		1	
Completions	13	0	639	6	433		6	
FetchAdd	0	0	0	0	0		0	
Swap	0	0	0	0	0		0	
CAS	0	0	0	0	0		0	
DLLPs	6576	6553	129727	129160	4596		4142	
Ack	16	13	944	650	469		443	
Nak	0	0	0	0	0		0	
PM	0	0	0	0	0		0	
InitFC	51	48	51	48	51		48	

Explore the Setup window to modify the setup, define hardware filters or create a trigger

Click to Open BEV Configuration tab to enable Flow Control BEV

Transaction window displays protocol layer data

Transaction stitching

Click the View Summary button for an overview of the entire acquisition

Training sets (PCIE)

DLLP packets (PCIE)

Errors, PHY layer ordered sets

Bird's Eye View (full acquisition data analysis viewer)

Listing window (lane by lane data)



For further information, go to www.tek.com and download "Tektronix Logic Protocol Analyzer Solutions for PCI Express 3.0, Instruction Manual, Tek P/N: 077-0400-xx". Includes design-in information, such as, probe load models and CAD layout files.