TDSHT3
HDMI Compliance Test Software

Printable Online Help

077-0024-08

Tektronix

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HDMI Compliance Test Software

Printable Online Help

www.tektronix.com
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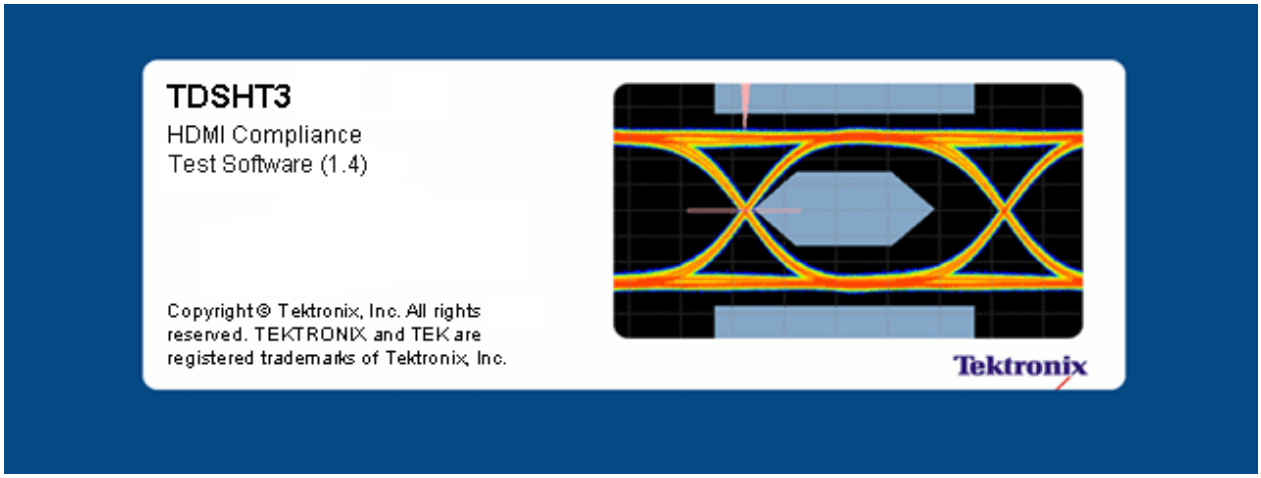
About the TDSHT3 HDMI Compliance Test Software



The TDSHT3 HDMI Compliance Test Software is a High Definition Multimedia Interface (HDMI) compliance test solution. This software helps engineers perform both HDMI physical layer validation and compliance testing. The TDSHT3 HDMI Compliance Test Software provides credible test results in conformance with the HDMI standards and test specifications.

The TDSHT3 HDMI Compliance Test Software offers automated tests for:

Source

- Differential Tests
  - Eye Diagram (see page 218) (Test ID 7-10)
  - Duty Cycle (see page 225) (Test ID 7-8)
  - Rise Time (see page 229) (Test ID 7-4)
  - Fall Time (see page 233) (Test ID 7-4)
  - Clock Jitter (see page 238) (Test ID 7-9)
  - Inter-Pair Skew (see page 245) (Test ID 7-6)
- Single-Ended Tests
  - Intra-Pair Skew (see page 255) (Test ID 7-7)
  - Low Amplitude + (see page 259) (Test ID 7-2)
  - Low Amplitude - (see page 262) (Test ID 7-2)

Sink

- Differential Tests
  - Min/Max-Diff Swing Tolerance (see page 265) (Test ID 8-5)
  - Jitter Tolerance (see page 273) (Test ID 8-7)
  - Deep Color (see page 285) (Test ID 8-25)
  - Audio Clock Regeneration (see page 290) (Test ID 8-21)
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  - DVI Interoperability (see page 313) (Test ID 8-24)
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  - 4Kx2K Video (see page 325) (Test ID 8-30)
  - Extended Colors and Contents (see page 330) (Test ID 8-31)
  - Character Synchronization (see page 336) (Test ID 8-15)
  - Pixel Encoding Requirements (see page 342) (Test ID 8-19)
  - Acceptance of All Valid Packets (see page 348) (Test ID 8-16)
  - Video Format Timing (see page 354) (Test ID 8-20)
- Single-Ended Tests
  - Intra-Pair Skew (see page 360) (Test ID 8-6)

Cable

- Differential Tests
  - Cable Eye Diagram (Passive and Active) (see page 368) (Test ID 5-3)
  - Inter-Pair Skew (see page 379) (Test ID 5-5)

NOTE. *This Cable Inter-Pair Skew test is performed only for* ***repeater cable testing****.*

The software offers automatic “one-button” testing that ensures faster validation with higher reliability and it supports only single-link HDMI device resolutions.

See Also

- (see page 7) Compatibility
- (see page 11) Requirements and Restrictions
- (see page 7) Recommended Accessories

Conventions

The online help system serves as a reference on how to use the TDSHT3 HDMI Compliance Test Software.

- The term “Exit” refers to exiting the application and not the oscilloscope unless otherwise stated.
- The waveforms used are representative and change for different settings and resolutions.
- The TDSHT3 HDMI Compliance Test Software is referred to as TDSHT3 software.
- The screens used are representative and may not match exactly with what you see. However, the functionality of the software is as described.

Feedback

Tektronix values your feedback on our products. To help us serve you better, please send us your suggestions, ideas, or comments on the TDSHT3 software.

Direct your feedback via e-mail to HDMIFeedback@tek.com or FAX at (503) 627-5695 and include the following information:

General Information

- Instrument model number and hardware options, if any
- Probes used
- Your name, company, mailing address, phone number, FAX number, e-mail id
- Please indicate if you would like to be contacted by Tektronix about your suggestions or comments

Program-Specific Information

- Software version number
- Description of the problem such that technical support can duplicate the problem
- The instrument setup file of the oscilloscope and the application are also required to identify the problem
- If possible, save the waveform on which you are performing the test as a `.wfm` file

NOTE. *To find the software version number, click* ***Help > About*** *in the software.*

Once you have gathered this information, you can contact technical support by e-mail. When you use e-mail, be sure to type in the subject line "TDSHT3 HDMI Compliance Test Software Problem," and then attach the **.wfm** files.

Compatibility

For information on oscilloscope compatibility, refer to the *Optional Applications Software on Windows-Based Oscilloscopes Installation Manual*, Tektronix Part Number, 077-0067-XX. The manual is available as a PDF file.

Recommended Accessories

The following probes and test fixtures are recommended for the TDSHT3 software.

Supported Probes

- P7313SMA – 13 GHz recommended differential probe

The following probes can be used with HDMI 1.2 test fixtures:

- P7350 – 5 GHz differential probe
- P7330 – 4 GHz differential probe
- P6330 – 4 GHz differential probe
- P7380 – 8 GHz differential probe
- P7240 – 4 GHz single-ended probe
- P7260 – 6 GHz single-ended probe

The P7350SMA – 5 GHz differential probe can only be used with the HDMI 1.2 TDR fixture and the 1.3 Efficere test fixtures (now available from Tektronix).

Supported 1.3/1.4a Test Fixtures

- TF-HDMI-TPA-STX (Alternate equivalent test fixture, which consists of 1# TF-HDMI-TPA-P, 1# TF-HDMI-TPA-CE)
- TF-HDMI-TPA-S (Alternate equivalent test fixture, which consists of 1# TF-HDMI-TPA-P,2# TF-HDMI-TPA-R,1#TF-HDMI-TPA-C, and 1#TF-HDMI-TPA-CE)
- TF-HDMI-TPA-CE (Alternate equivalent test fixture, which consists of EDID PCB and 1# EDID EEPROM
- TF-HDMIC-TPA-STX (Alternate equivalent test fixture, which consists of 1# TF-HDMIC-TPA-P, 1# TF-HDMI-TPA-CE)
- TF-HDMIC-TPA-S (Alternate equivalent test fixture, which consists of 1# TF-HDMIC-TPA-P,2# TF-HDMIC-TPA-R,1#TF-HDMI-TPA-C, and 1#TF-HDMI-TPA-CE)

- TF-HDMID-TPA-P and TF-HDMID-TPA-R, available from Tektronix
- TF-HDMIE-TPA-KIT, available from Tektronix

The following HDMI 1.2 test fixtures can only work for limited HDMI resolutions.

- HDMI-TPA-P-DI
- HDMI-TPA-P-SE
- HDMI-TPA-P-TDR
- HDMI-TPA-R-DI
- HDMI-TPA-R-SE
- HDMI-TPA-R-TDR

The fixtures are available under the Tektronix ordering system with the following part numbers:

- **TF-HDMI-TPA-S** – HDMI Type A fixture set for Tx, Rx, and Cable testing. It includes the following:
  - One HDMI-TPA-P plug board with SMA cables
  - Two HDMI-TPA-R receptacle board with SMA cables
  - One HDMI-TPA-C calibration board with SMA cables
  - One HDMI-TPA-CE, EDID board with EDID EEPROM
- **TF-HDMI-TPA-STX** – HDMI Type A fixture set for Tx and Rx testing. It includes the following:
  - One HDMI-TPA-P plug board
  - One HDMI-TPA-CE, EDID board with EDID EEPROM
- **TF-HDMI-TPA-CE** – EDID test fixture. It includes the following:
  - One EDID PCB
  - One EDID board with EDID EEPROM
- **TF-HDMIC-TPA-S** – HDMI Type C fixture set for Tx, Rx, and Cable testing. It includes the following:
  - One HDMIC-TPA-P plug board with SMA cables
  - Two HDMIC-TPA-R receptacle board with SMA cables
  - One HDMI-TPA-C calibration board with SMA cables
  - One HDMI-TPA-CE, EDID board with EDID EEPROM
- **TF-HDMIC-TPA-STX** – HDMI Type A fixture set for Tx and Rx testing. It includes the following:
  - One HDMIC-TPA-P plug board
  - One HDMI-TPA-CE, EDID board with EDID EEPROM
- **TF-HDMID-TPA-P** – HDMI Type D fixture set for Tx and Rx testing. It includes one HDMI Type D plug board.

- **TF-HDMID-TPA-R** – HDMI Type D fixture set for Tx, Rx, and Cable testing. It includes one HDMI Type D receptacle board.
- **TF-HDMIE-TPA-KIT** – HDMI Type E fixture set for Tx, Rx, and Cable Testing. It includes the following:
  - One HDMI-TPA-P plug board with SMA cables
  - Two HDMI-TPA-R receptacle boards with SMA cables

Direct Synthesis

- HDMI Direct Synthesis Accessory Kit 020-3018-XX is required for Direct Synthesis setup.

Connectivity

- GPIB (recommended for DPO/DSA/MSO70000 series oscilloscopes)
- USB-GPIB (HS)
- E-Net Switch

Recommended Test Equipment

The compliance test setups use a variety of test equipment. The test setups refer to the test equipment with generic names. Below is a list of suitable test equipment for each type of test equipment.

DTG (Data Timing Generator)

- DTG5000 Series

AFG (Arbitrary Function Generator)

- AFG3000 Series

AWG (Arbitrary Waveform Generator)

- AWG7000 Series

Digital Oscilloscope

- MSO/DPO/DSA72004 Series
- MSO/DPO/DSA71604 Series
- MSO/DPO/DSA71254 Series
- MSO/DPO/DSA70804 Series

Requirements and Restrictions

- TekVISA must be installed on the oscilloscope. If you do not have TekVISA, you can download it from www.tektronix.com/software.
- MATLAB Runtime must be installed on the oscilloscope. If you do not have MATLAB Runtime, the TDSHT3 installer will install it.

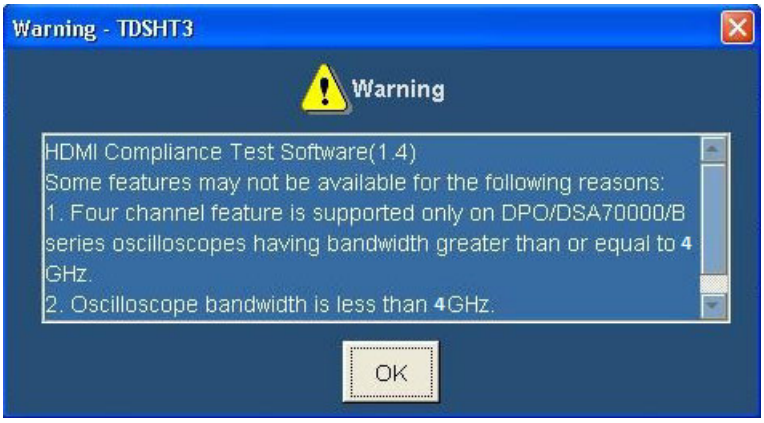
NOTE. *Do not change the oscilloscope settings while a test is running. If you do, the software may give abnormal test results.*

For Better and Reliable Results

- Before you run any test, calibrate the probes and oscilloscope for Signal Path Compensation. On the oscilloscope menu bar, click **Utilities > Instrument Calibration** and then click **Calibrate** to calibrate the oscilloscope.
- If the signal is not connected and the noise level is less than 50 mV, the software detects and gives a message such as “Invalid Signal.”

How to Start the Software

When you start the software, a warning message box may appear.



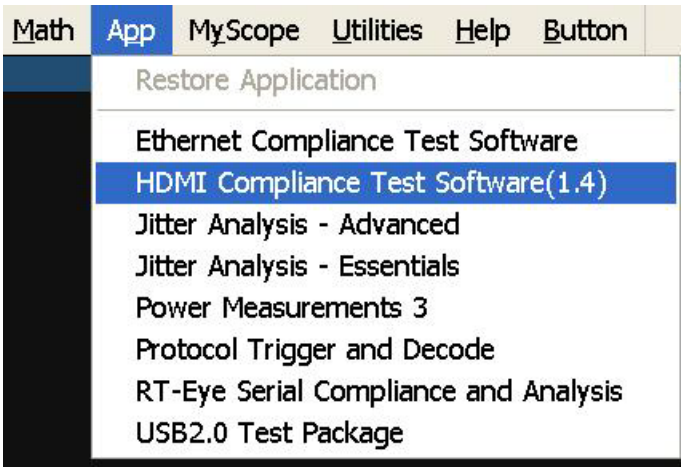
This happens due to the following reasons:

1. **Four channel feature is supported only on DPO70000/B, DSA70000/B, and MSO70000 series oscilloscopes having bandwidth greater than or equal to 4 GHz**. For TDS series oscilloscopes, only two channels are available and the other two channels are displayed as **Not Conn**.
2. **Oscilloscope bandwidth is less than 4 GHz**. For higher resolution HDMI signals, you need at least a 4 GHz oscilloscope. Your oscilloscope bandwidth is less than 4 GHz.
3. **Maximum available record length for two channels is less than 16 M**. For HDMI compliance testing, you need at least a 16 M record length in two channels. This 16 M record length is installed in the following oscilloscopes:
   - Option 4M and above in TDS series oscilloscopes
   - Option 2XL and above in DPO series oscilloscopes

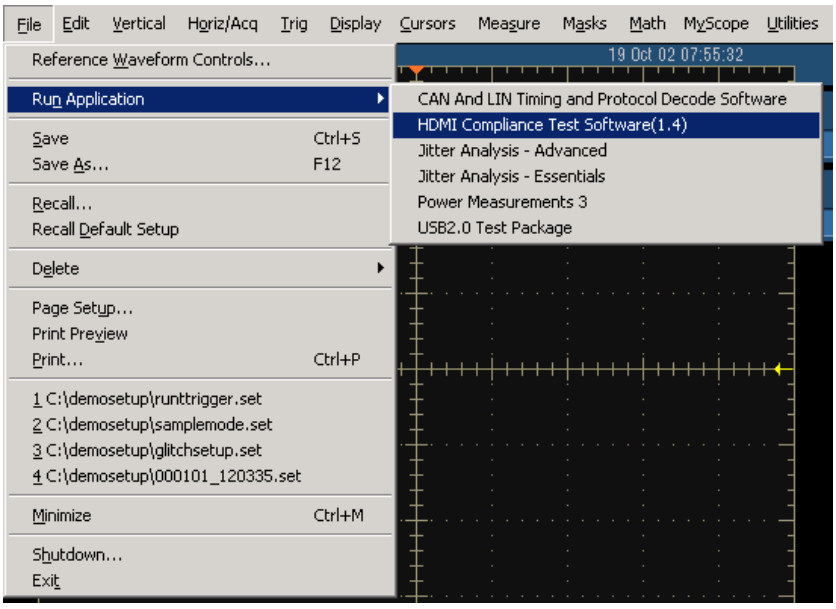
   If these options are not available (installed) in the oscilloscope, the software will run the Eye diagram and Jitter measurements with the maximum available record length.
4. **DDS method is supported only on DPO70000/B/C, DSA70000/B/C, and MSO70000/C series oscilloscopes having bandwidth greater than or equal to 8 GHz**.
5. **TDSHT3 application and the DDS method option license keys are not installed. They are running in trial mode**.
6. **TDSHT3 application is licensed but the DDS method option license key is not installed. The DDS method is running in trial mode**.
7. **DDS method option is not available, trial has expired**. The DDS method trial has expired and this option will not appear in the application.

Depending on the type of oscilloscope that you have, you can start the software in different ways.

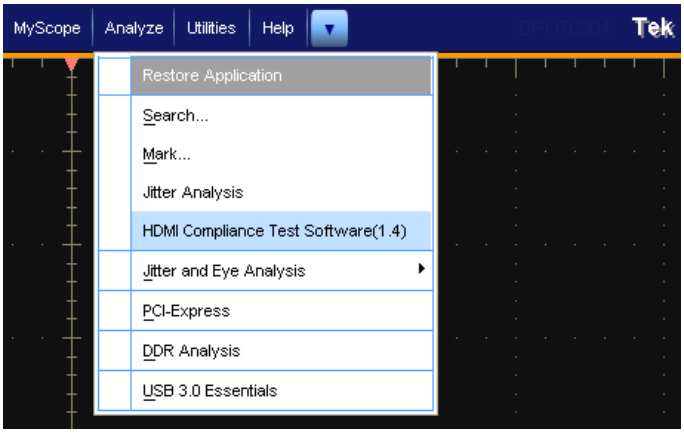
1. For supported B-series oscilloscopes, select **App > HDMI Compliance Test Software(1.4)**.



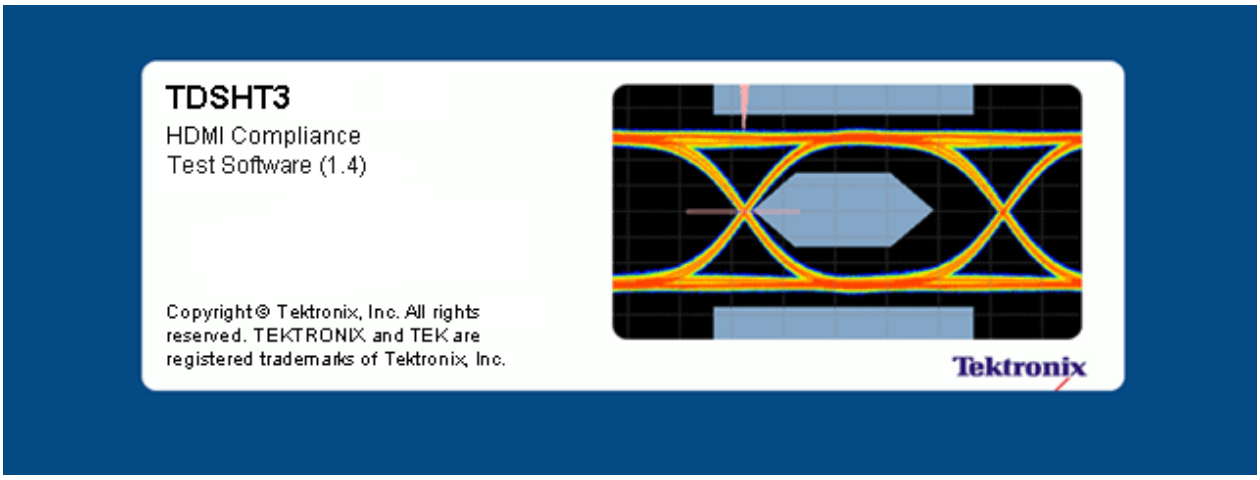
2. For TDS7000-series oscilloscopes, select **File > Run Application >HDMI Compliance Test Software(1.4)**.



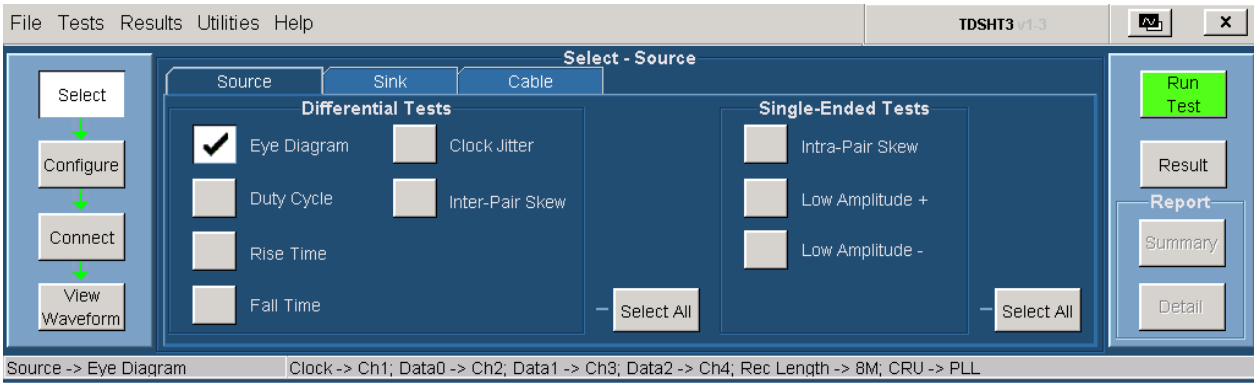
3. For DPO/DSA/MSO70000 series oscilloscopes, select **Analyze > HDMI Compliance Test Software(1.4)**.



4. A splash screen indicates that the software is loading.



5. The oscilloscope display resizes to fit in the upper part of the screen. The lower part of the oscilloscope screen displays the TDSHT3 software.



6. The software is automatically set to its default settings (see page 395).
7. If you gain access to the oscilloscope functions, the oscilloscope display appears full screen and the TDSHT3 software recedes to the background.

How to Minimize and Maximize the Software

The software appears even when you minimize the oscilloscope display.

- To minimize the software, click **File > Minimize**. The TDSHT3 software window minimizes to the Windows taskbar. The upper part of the screen has the oscilloscope display and the lower part of the screen has the desktop.
- To restore the minimized window to its previous size, click its taskbar button.
- To hide the window, click **Hide** on the top-right of the software window.

NOTE. *If you click **Hide**, the TDSHT3 software window goes to the background and the oscilloscope fills the display.*

How to Return to the Software

When you gain access to the oscilloscope functions, the oscilloscope fills the display. To gain access to the oscilloscope functions, do one of the following:

- Choose either the menu bar or the toolbar mode on the oscilloscope, and then gain access to the menus.
- Click **App > Restore Application** for B-series, click **Analyze > Restore Application** for DPO/DSA/MSO70000 series oscilloscopes, or click **APP**

on the top right of the TDS7000 series oscilloscope display to return to the software.

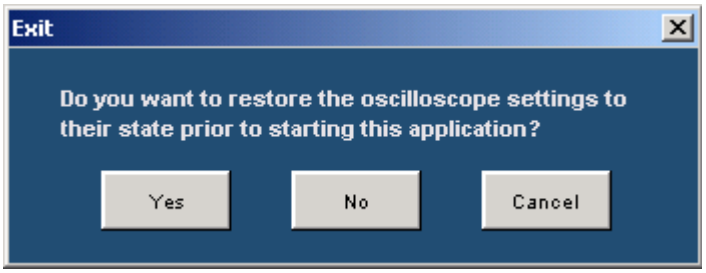
See Also

- (see page 16) Exit

How to Exit the Software

To quit the software:

- On the menu bar, click **File > Exit**.
- The Exit dialog box appears.



- Click **Yes**, **No**, or **Cancel**. Yes is selected by default. When the software runs, it automatically changes some oscilloscope settings. When you quit the software, you can choose whether to retain these settings or restore the previous settings.

NOTE. *Using other methods to quit the software may result in an abnormal exit of the software.*

Software Folders and File Names

The TDSHT3 software uses file name extensions to identify the file type. The following table lists the default folder names and their purpose:

For Windows XP Oscilloscopes

Folder	Purpose
C:\TekApplications\TDSHT3v1-3	This is the software data folder.
C:\TekApplications\TDSHT3v1-3\Images	This folder stores all the images.
C:\TekApplications\TDSHT3v1-3\Data	This folder stores all the software data.
C:\TekApplications\TDSHT3v1-3\setup	This folder stores all the save and recall files.
C:\TekApplications\TDSHT3v1-3\Demo Tools	This folder stores the demo waveforms.
C:\TekApplications\TDSHT3v1-3\Reports	This folder stores the reports.

For Windows 7 Oscilloscopes

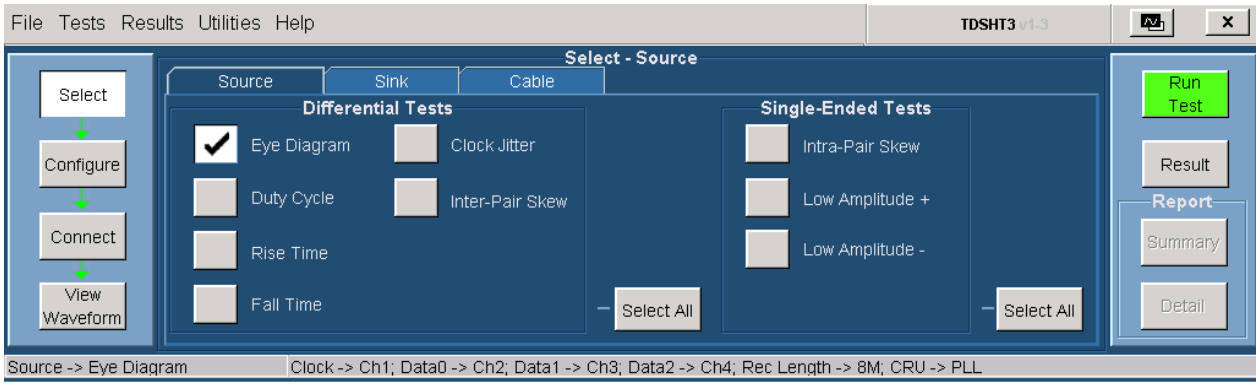
Folder	Purpose
C:\Users\<Username>\Tektronix\TekApplications\TDSHT3v1-3	This is the software data folder.
C:\Users\<Username>\Tektronix\TekApplications\TDSHT3v1-3\Images	This folder stores all the images.
C:\Users\<Username>\Tektronix\TekApplications\TDSHT3v1-3\Data	This folder stores all the software data.
C:\Users\<Username>\Tektronix\TekApplications\TDSHT3v1-3\setup	This folder stores all the save and recall files.
C:\Users\Public\Tektronix\TekApplications\TDSHT3v1-3\Demo Tools	This folder stores the demo waveforms.
C:\Users\<Username>\Tektronix\TekApplications\TDSHT3v1-3\Reports	This folder stores the reports.

Shortcut Keys

Menu	Shortcut key
File	Alt+F
Tests	Alt+T
Results	Alt+R
Utilities	Alt+U
Help	Alt+H
File > Recall Compliance Default	Alt+F+D
File > Recall	Alt+F+R
File > Recall > First Recent	Alt+F+E+1
File > Recall > Second Recent	Alt+F+E+2
File > Recall > Third Recent	Alt+F+E+3
File > Recall > Fourth Recent	Alt+F+E+4
File > Save	Alt+F+S
File > Recall Recent	Alt+F+E
File > Preferences	Alt+F+P
File > Preferences > Position Eye Mask in Center	Alt+F+P+M
File > Preferences > Acquisition Alert Message	Alt+F+P+A
File > Preferences > Jitter Tolerance (No calibration)	Alt+F+P+J
File > Preferences > Single Ended (With 50 ohm term)	Alt+F+P+S
File > Preferences > Set the probe control to internal 3.3 V	Alt+F+P+C
File > Minimize	Alt+F+M
File > Exit	Alt+F+X
Tests > Select	Alt+T+S
Tests > Select > Source	Alt+T+S+S
Tests > Select > Sink	Alt+T+S+K
Tests > Select > Cable	Alt+T+S+C
Tests > Configure	Alt+T+C
Tests > Connect	Alt+T+N
Tests > View Waveform	Alt+T+V
Results > Summary	Alt+R+S
Results > Details	Alt+R+D
Utilities > Deskew	Alt+U+D
Utilities > DTG Pattern List	Alt+U+P
Help > Help Topics	Alt+H+T
Help > About HDMI	Alt+H+A

Software Window

The software window includes a menu bar, selection pane, test selection pane, execution pane, and status bar. The client pane changes between the selection pane, configuration pane, connection pane, and view waveform pane depending on what you have selected in the selection pane. After you run the test, the client pane automatically changes to the result pane.



Interface Controls

The software uses a Windows interface.

NOTE. *The oscilloscope software shrinks to fit in the top part of the display when the TDSHT3 software runs.*

The software interface uses the following controls:

Control	Description
Menu bar	The Menu bar provides access to the software menus. It is located at the top of the software window.
Area/Tab	An Area/Tab control encloses visual frame with a set of related options.
Option button	An Option button allows you to select either a command or a task.
Drop-down list box	A Drop-down list box lists items from which you can select one item.
Field	A Field is a box where you can enter text or values.
Check boxes	Select or clear check boxes to set preferences.

Control	Description
Scroll bar	A Scroll bar is a vertical or horizontal bar at the side or bottom of a display area that is used to move around that area.
Browse	Browse refers to the window where you can browse through a list of folders and files.
Command button	A Command button refers to the usually rectangular button that carries out a command and may initiate immediate action.
Numeric keypad	Use a Numeric keypad to enter numeric values.
Text keypad	Use a Text keypad to enter text.
MP/GP knob	A line between the knob icon and the field indicates which knob you can turn on the oscilloscope to select a value.
F1	F1 help opens help on a topic associated with the currently selected item in your software.

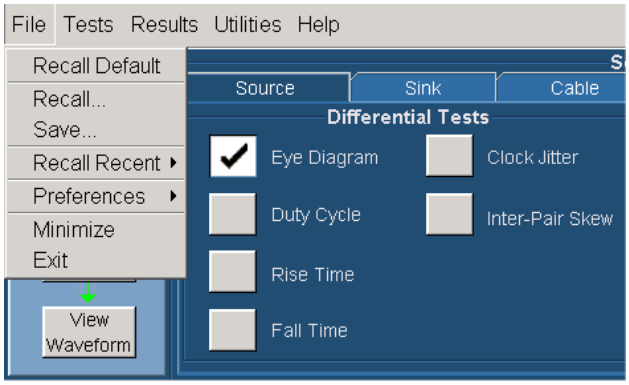
Menu Bar

The menu bar consists of the following menus:

Click these links for information on each of the menus.

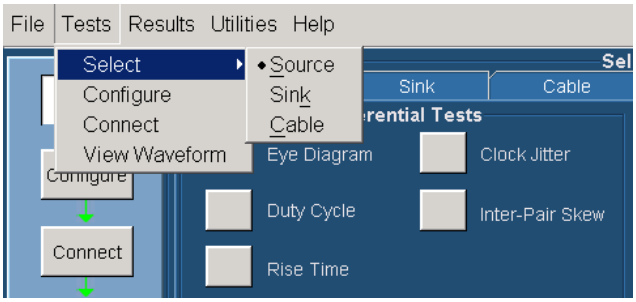
- (see page 21) File menu
- (see page 22) Tests menu
- (see page 22) Results menu
- (see page 23) Utilities menu
- (see page 23) Help menu

File Menu



- Click **File > Recall Default** to recall the default settings for both the software and the oscilloscope.
- Click **File > Recall** to recall the previously saved settings for the software from an `.ini` file.
- Click **File > Save** to save the software settings to an `.ini` file.
- Click **File > Recall Recent** to select among the recently saved and recalled setups.
- Click **File > Preferences** to select one of the available options. Click here (see page 24) for more details.
- Click **File > Minimize** to minimize the software window.
- Click **File > Exit** to quit the software.

Tests Menu

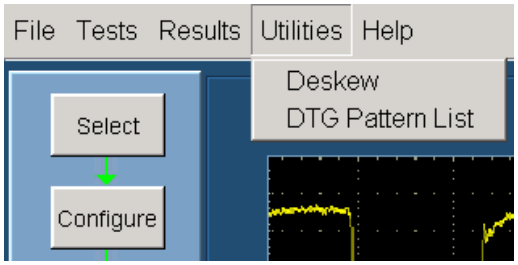


- Click **Tests > Select** to display or modify the test selection for Source, Sink, or Cable in the client pane.
- Click **Tests > Configure** to display or modify the configuration parameters for the selected test(s).
- Click **Tests > Connect** to display the connection instructions for the selected test(s).
- Click **Tests > View Waveform** to display a sample waveform or waveforms based on the settings for the selected test(s).

Results Menu

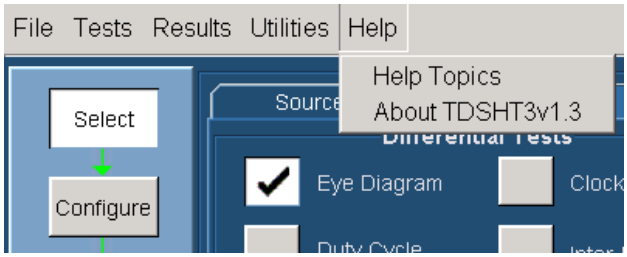
- Click **Results > Summary** to display the result summary of the last test(s) that you conducted.
- Click **Results > Details** to display the detailed results of the last test(s) that you conducted.

Utilities Menu



- Click **Utilities > Deskew** to open the deskew (see page 45) pane. The deskew pane allows you to compensate the skew between the oscilloscope channels.
- Click **Utilities > DTG Pattern list** to open the DTG Pattern list (see page 46) pane. The DTG pattern list allows you to add and delete DTG pattern files.

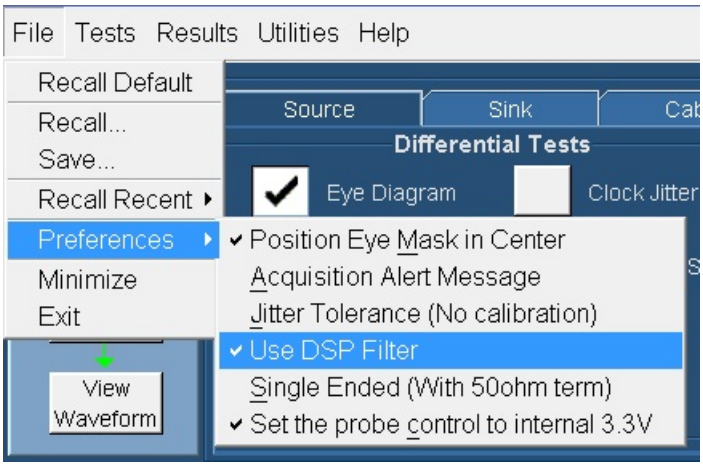
Help Menu



- Click **Help > Help Topics** to display the help for the TDSHT3 software.
- Click **Help > About TDSHT3** to display a dialog box with information about the current TDSHT3 software.

Preferences

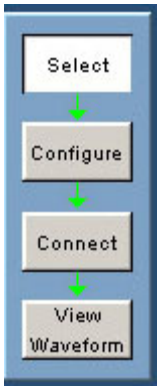
On the menu bar, click **File > Preferences** to select any of the options described in the following table. Click an option again to clear the selection.



Option	Description
Position Eye Mask in Center	Select this option to position the mask at the center of the eye diagram. Clear this option to position the mask to the left of the eye diagram.
Acquisition Alert Message	Select this option to receive an alert message that allows the software to use the custom oscilloscope setup. Clear this option to stop receiving the alert message.
Jitter Tolerance (No calibration)	Select this option if you do not want to run the jitter calibration tests for sink jitter tolerance measurements.
Use DSP Filter	If the oscilloscope chosen for testing has a bandwidth greater than 8 GHz, select this option to apply an 8 GHZ low-pass filter to appropriate tests.
Single Ended (With 50 Ω term)	This option can be selected only when the negative input of the probe is terminated with the 50 Ω terminator. When this option is selected, the single ended measurements will be performed as though a 50 Ω termination is connected.
Set the probe control to internal 3.3 V	This option is applicable to Source measurements on DPO/DSA/MSO70000 series oscilloscopes with P7313SMA probes. When this option is selected, the application sets the probe control to internal and voltage to 3.3 V.

Selection Pane

The selection pane, which is located to the left of the software window, allows you to navigate through the software.



Use the following buttons to do these tasks:

- Click **Tests > Select** to display or modify the test selection for Source, Sink, or Cable in the client pane.
- Click **Tests > Configure** to display or modify the configuration parameters for the selected test(s).
- Click **Tests > Connect** to display the connection instructions for the selected test(s).
- Click **Tests > View Waveform** to display a sample waveform or waveforms based on the settings for the selected test(s).

Execution Pane

The execution pane, which is located to the right of the software window, displays the Run Test and Result buttons. After you successfully run a test, the Summary and Detail buttons are available.

Use the following buttons to do the following tasks:

- Click **Run Test** to run the selected test or tests.
- Click **Result** to display the result pane that shows the test results.
- Click **Summary** to generate a report summary as a `csv` file.
- Click **Detail** to generate the HTML/MHT report. Plots and waveforms are displayed wherever applicable.

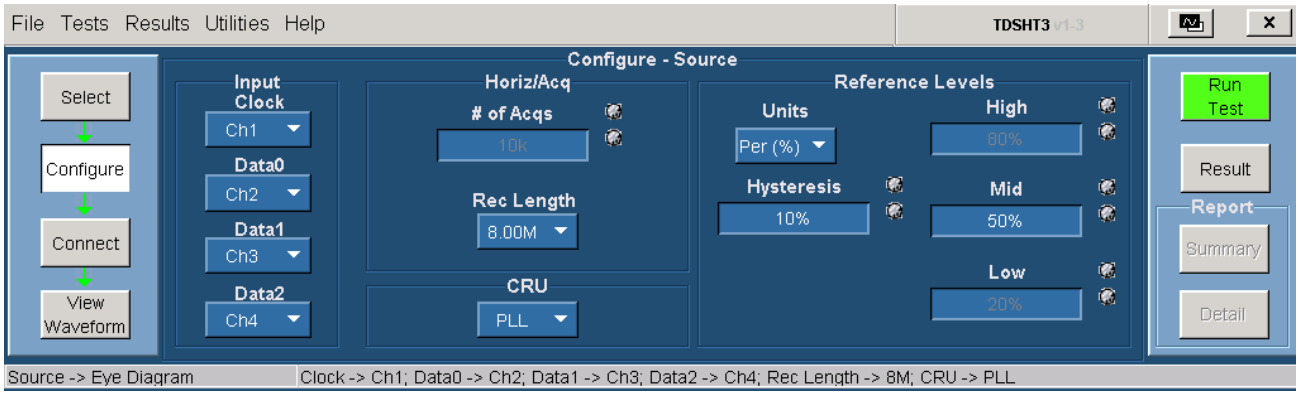
Status Bar

At the bottom of the software window is the status bar, which displays the selected test and the important configuration parameters.

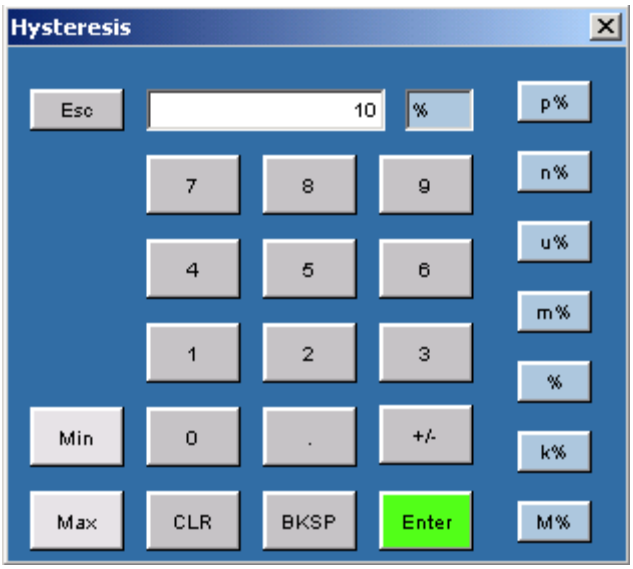
Virtual Keyboard

Virtual Keyboard - Numeric

1. Click any number box to display the icon for the numeric keyboard.



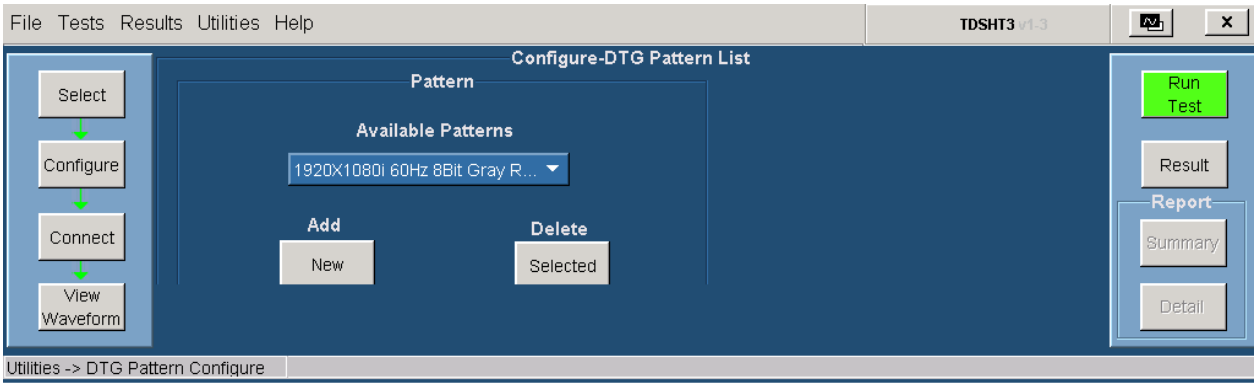
2. Click the icon to display the numeric keyboard.



3. Click the number keys to enter the desired value.
4. Select a unit of measure.
5. Click **Enter** to confirm your entry. Selections are not effective until you click **Enter**.

Virtual Keyboard - Text

1. Click **New** to display the virtual keyboard.



2. Use the text keyboard to enter the required text (such as a file name).

3. Click **Enter** to confirm your entry. Selections are not effective until you click **Enter**.

General Purpose Knob

To use the General Purpose knob, follow these steps:

1. Click any number box to display the connection to one of the general purpose knobs.
2. Turn the corresponding knob on the oscilloscope front panel to adjust the value for the selected parameter.
3. For better resolution, press the **Fine** button.

Enable Remote Control of Test Equipment

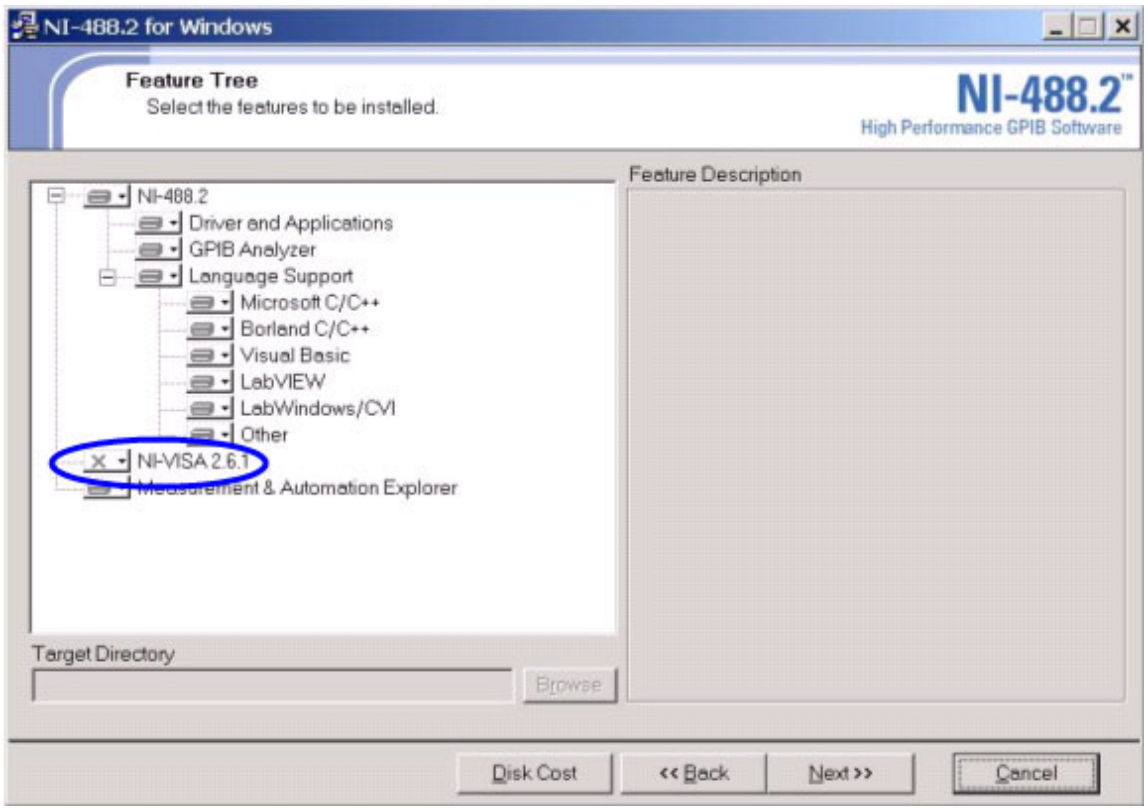
Three methods are available to connect to an AWG, DTG, or AFG. The methods are GPIB-GPIB (recommended), GPIB-USB, and GPIB-ENET.

The following section will guide you through the process of connecting the AWG, DTG, AFG, and the digital oscilloscope used for Sink and Cable tests.

You will need an AWG, an AFG, a DTG, a Digital Oscilloscope, a National Instruments GPIB-USB-B with the included software, an NI-GPIB-HS cable with the included software, and NI-488.2 for Windows.

NI-488.2 Software configuration for TDS series

1. Ensure that NI-VISA is NOT installed.
2. Install NI-488.2 for Windows (version 2.1 or later).



3. Install the Measurement & Automation Explorer software.
4. When prompted, enable the GPIB-USB interface.

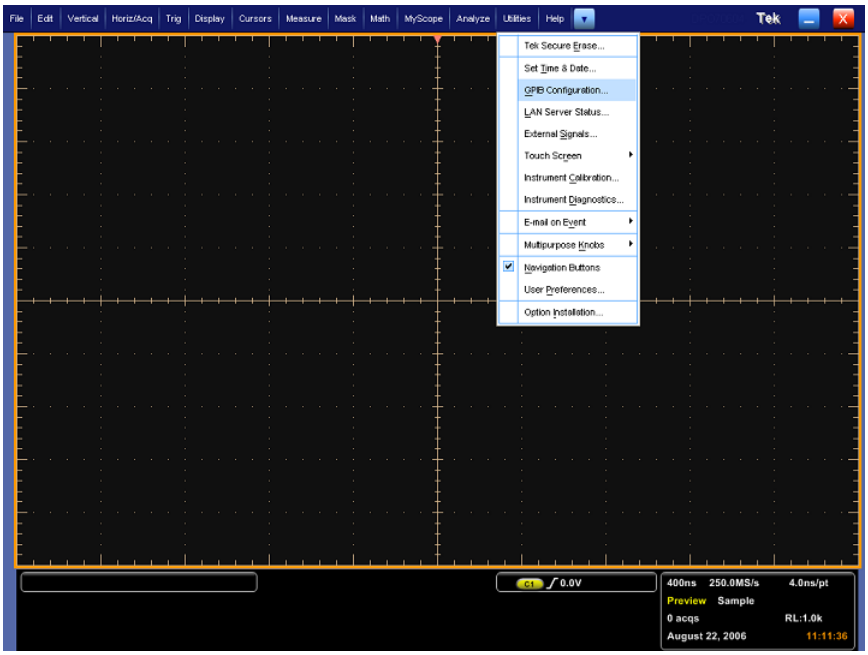
NOTE. *If you already have NI-488.2 installed on your oscilloscope, ensure that you have the appropriate version and installation parameters. Otherwise, remove NI-488.2, and then reinstall the appropriate version.*

5. Restart the oscilloscope.

NI-Software configuration for DPO70000 series

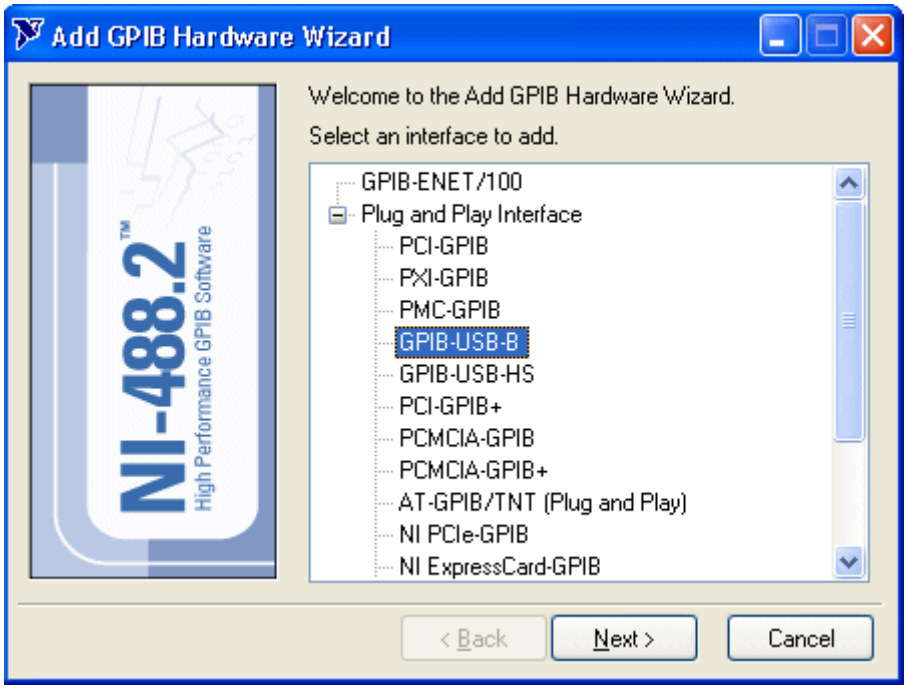
NOTE. *If you are using the NI-Drivers on the DPO70000 series for the first time, perform steps 1 through 9. If not, perform steps 7 through 9.*

1. In the oscilloscope menu, click **Utilities > GPIB Configuration**.



2. In the GPIB Configuration, select Controller. A GPIB Mode Switch dialog box is displayed.
3. Press **OK** to set the mode change and restart the oscilloscope.
4. In the oscilloscope menu, click **Utilities > GPIB Configuration**.
5. Select **Talk/Listen**. A GPIB mode switch dialog box is displayed.
6. Click **OK** to set the mode change and restart the oscilloscope.

   You cannot access the NI software from the **Start > Program** menu. Go to `C:\Program Files\National Instruments\NI-488.2\Bin` location.
7. Double-click **Add GPIB Hardware** to display the Add GPIB Hardware Wizard.

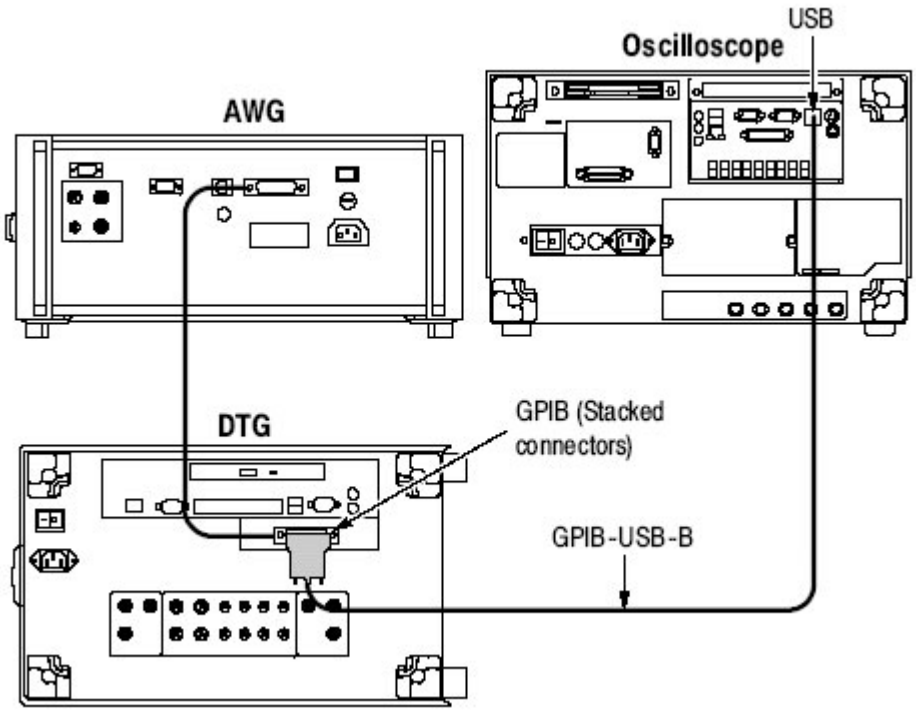


8. Select the appropriate NI hardware from the list (select GPIB-USB-B from the list if it is connected).
9. Press **Next** and finish the installation.

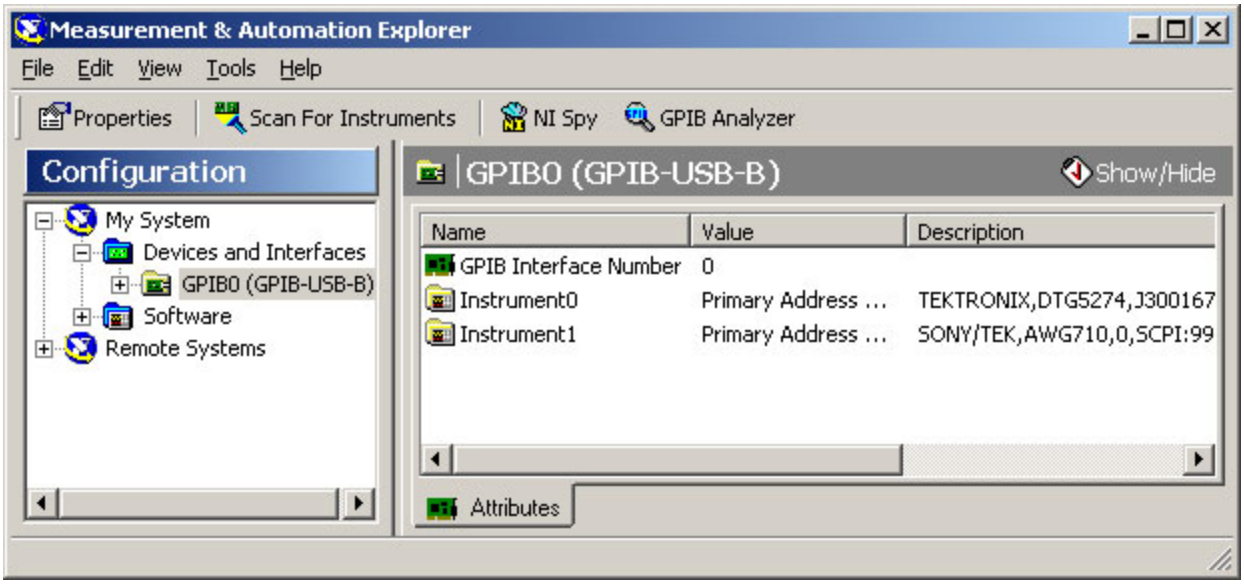
Configure and View Equipment Connections

This section helps you to configure the equipment and view the connections.

1. Configure the DTG GPIB primary address to 1 and the AWG/AFG GPIB primary address to 2.
2. Connect the USB-GPIB controller to the USB port on the oscilloscope. The oscilloscope operating system will detect the USB-GPIB controller and install the appropriate driver for it.
3. Using GPIB cables, connect (stack) both the DTG and AWG/AFG GPIB ports to the GPIB port of the GPIB controller.

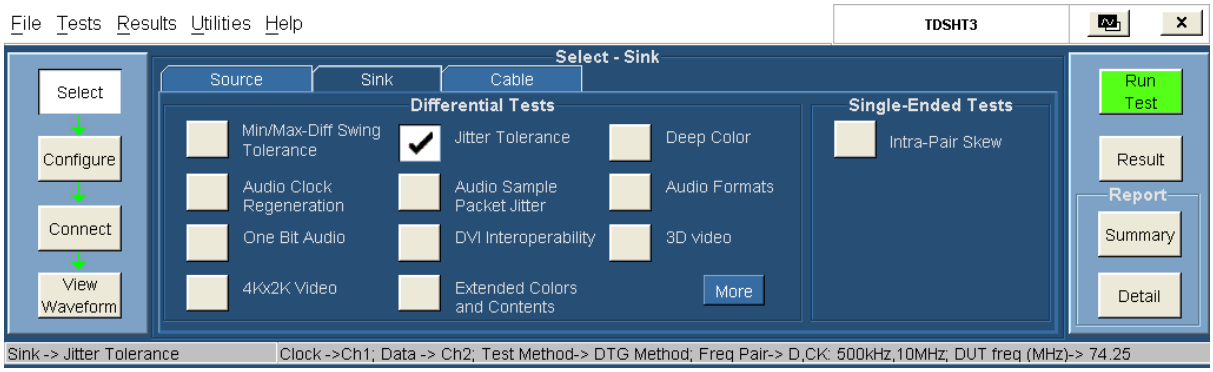


4. Open the Measurement & Automation Explorer software that was installed with the NI-488.2 software.



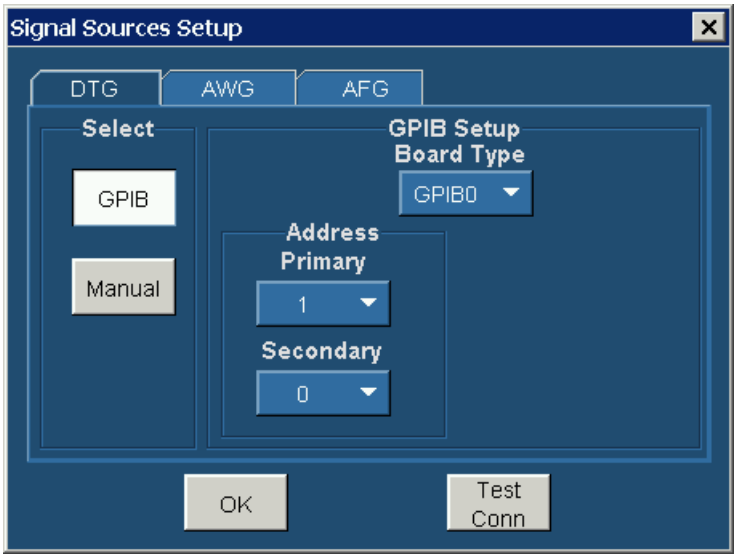
5. In the configuration pane, look under Devices and Interfaces for the GPIB device.
6. Right-click the GPIB device and click **Scan** for Instruments.

7. Note the GPIB Instrument Number and the Primary Address to configure the instrument connection in the TDSHT3 Software.
8. Right-click the instrument, and then click **Communicate with Instrument**.
9. In the NI-488.2 Communicator dialog box, click **Query** and check that "*IDN?" displays a description of the correct equipment.
10. Start the TDSHT3 Software.
11. Click **Select**.
12. Click the **Sink** tab.
13. Select one of the differential tests, such as Jitter Tolerance.



NOTE. *Click **More** to view more differential tests.*

14. Click **Connect**.
15. Click **Signal Sources**. The Signal Sources Setup dialog box appears.



16. In the Signal Sources Setup dialog box, click the **DTG** tab.
17. Configure the GPIB Board Type by using the GPIB Instrument Number that you noted in step 4.
18. Configure the Primary Address by using the address that you noted in step 4.
19. Leave the Secondary Address set to 0.
20. Click **AWG** tab and repeat steps 14 through 16 for the AWG.
21. Click **AFG** tab and repeat steps 14 through 16 for the AFG.
22. Click **Test Conn** and look for a message that the connection is successful.

Configure New IP Address for GPIB-ENET

There are two methods to connect to AWG/DTG. One is the GPIB-USB method and the other, the GPIB-ENET method.

GPIB-ENET and GPIB-ENET/100 for Windows 3.1/95/98/ME/NT/2000/XP

1. Confirm that you have installed the latest NI-488.2 driver software for your device.
2. Connect your GPIB-ENET or GPIB-ENET/100 to an Ethernet network by using a category 5 Ethernet cable to connect the RJ-45 port on your hardware to an Ethernet hub. You could also connect the external hardware directly to your oscilloscope by using an Ethernet crossover cable.
3. Connect the power to your GPIB-ENET or GPIB-ENET/100 and turn it on. When you power on your GPIB-ENET, the POWER LED comes on immediately. The READY LED flashes while it completes its power-on self-test. When the test completes successfully and the IP address is assigned,

the READY LED remains steady, indicating that the unit is ready to operate. To assign your IP address, continue to step 4.

4. Run the Measurement & Automation Explorer software from **Programs > National Instruments**.

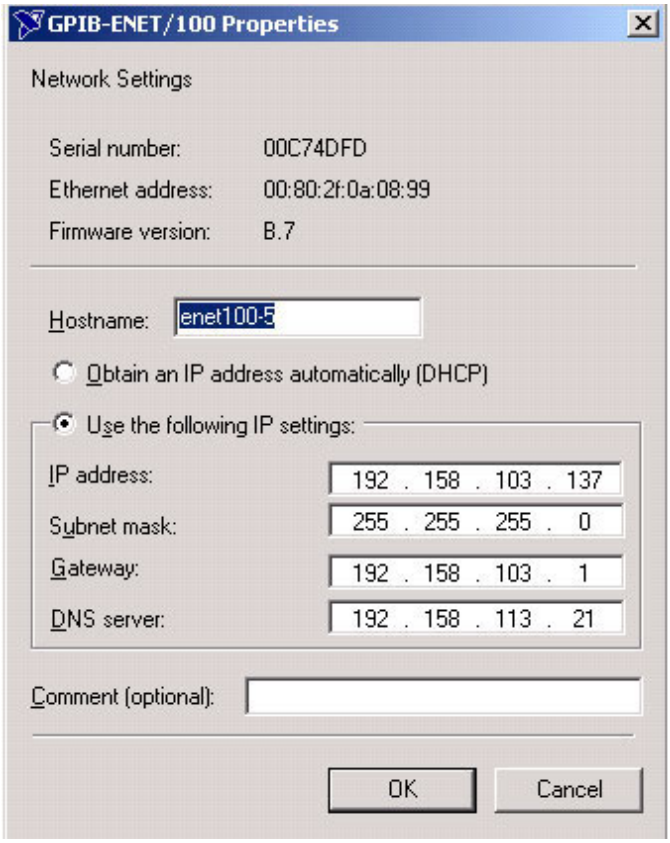
5. Some devices are not Windows Plug and Play compatible, so they do not automatically appear in the Devices and Interfaces list. Other devices may reside in another oscilloscope on your network. To add non-Plug and Play or remote DAQ devices, right-click Devices and Interfaces in the configuration tree, and then click **Create New**. Follow the instructions in the wizard. Select GPIB-ENET/100 or GPIB-ENET interface according to the hardware.

How to Configure GPIB-ENET/100

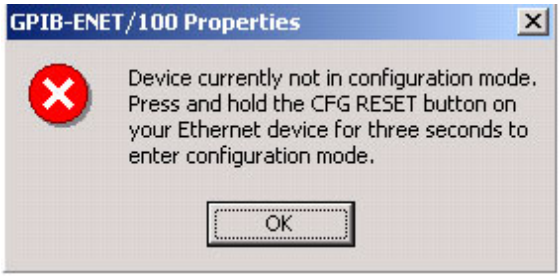
1. To configure an existing National Instruments device, right-click the device name in Devices and Interfaces in the configuration tree, and then click **Properties**. You can also configure existing device properties by clicking **Properties** in the toolbar.

2. To configure the network parameters of your GPIB-ENET/100, right-click your GPIB interface in the configuration tree, and click **Device Configuration**.

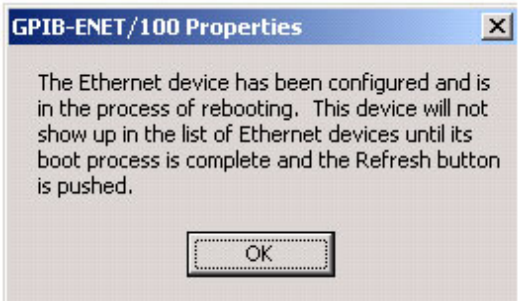
3. Click **Properties**. Configure the IP address as shown in the following figure:



4. After entering the IP settings, click **OK**. A message box appears as follows:



5. After you reset the CFG in the ENET card, click **OK** in the GPIB-ENET/100 Properties message box. The software will configure and another message box appears.



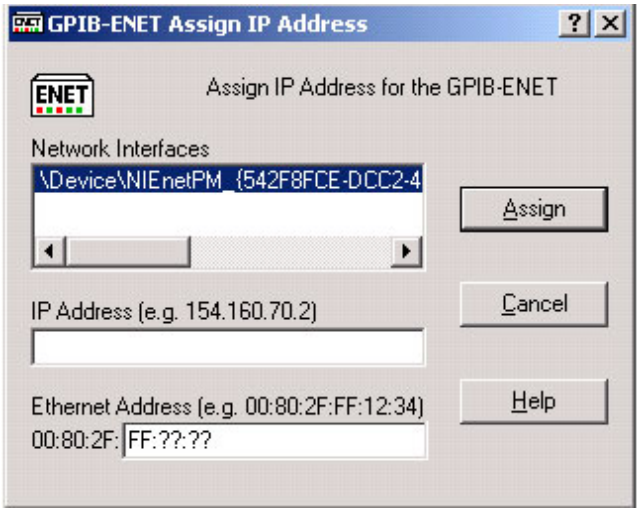
6. Click **OK**. The ENET card is configured.
7. Verify the configuration by pinging the IP address and through ICTA.

How to Configure GPIB-ENET (old card)

1. Right-click **Devices and Interfaces**. Click **Assign IP Address**. A message box appears.

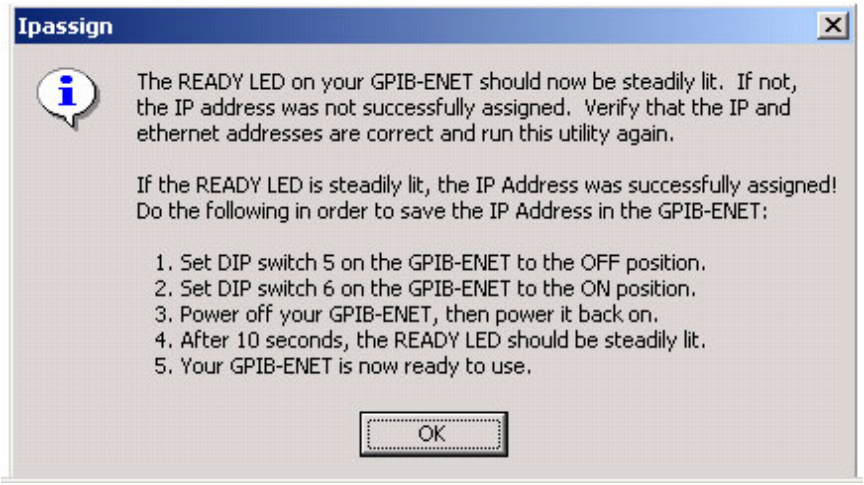
NOTE. *The GPIB software installation is in the path* `C:\Program Files\National Instruments\NI-488.2\GPIB-ENET` *on the oscilloscope.*

2. Run the Measurement & Automation Explorer software. Click **Assign IP Address**. A message box appears.



3. Enter the new IP Address and the Ethernet Address. Click **Assign**. A message box appears.

4. Follow the instructions in the Ipassign message box. Click **OK**. Another message box appears.



5. Follow the instructions in the new Ipassign message box. Click **OK**.

Remote Control Caution

If you run the Sink or Cable tests, the GPIB Bus Timing dialog box appears.

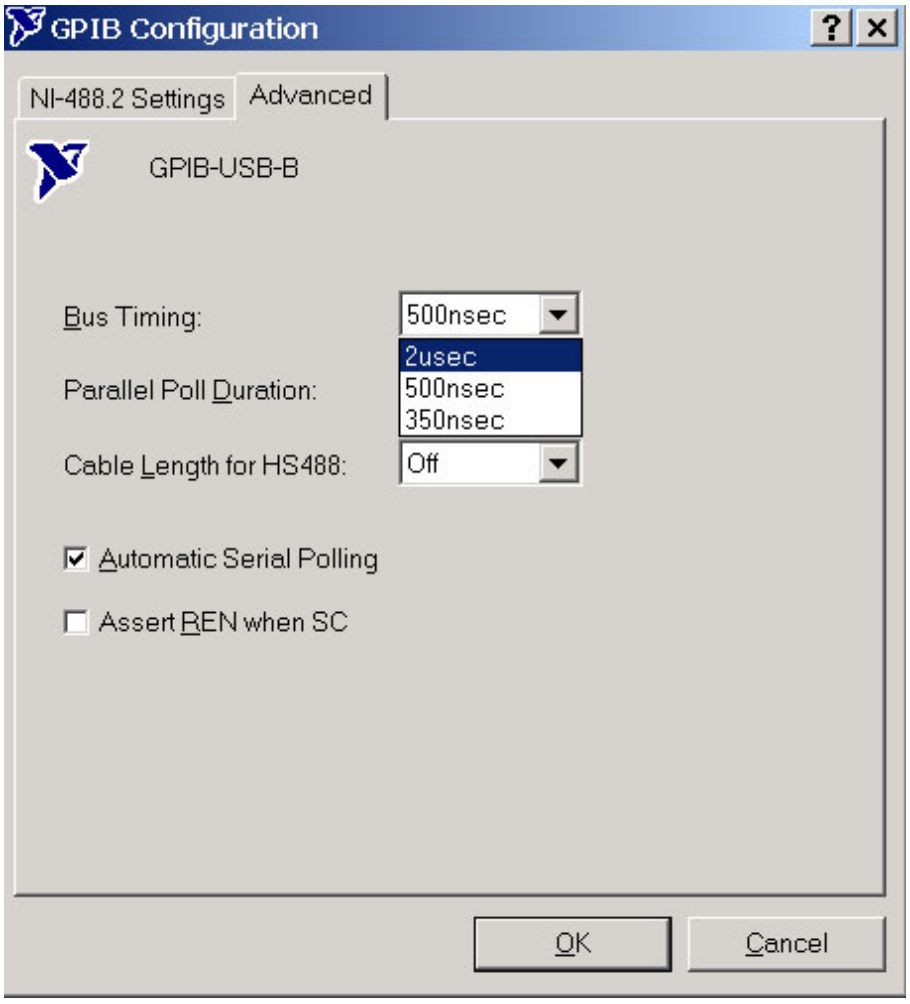
Click **OK** to continue if you are sure that the Bus Timing parameter is already set to 2 µsec. Otherwise, click **Cancel** and follow the procedure in this section on how to change the Bus Timing parameter manually.

Once you have changed the parameter, select the check box if you do not want the dialog box to appear again in the current session. However, if you click **File > Recall Default** or you quit the software, the dialog box appears again when you run the test.

When you install the remote control for the test equipment, the Measurement & Automation Explorer software will be installed on the oscilloscope. Start the software by clicking **Start > Program Files > National Instruments > Measurement & Automation**.

To change the Bus Timing parameter, perform the following steps:

1. Start the Measurement & Automation Explorer software.
2. In the configuration pane, look under Devices and Interfaces for the GPIB device.
3. Right-click the GPIB device and click **Properties**. The GPIB Configuration dialog box appears.
4. In the GPIB Configuration dialog box, click the **Advanced** tab.
5. In the Bus Timing list, select 2 µsec.



6. Quit the TDSHT3 Software and restart the oscilloscope.

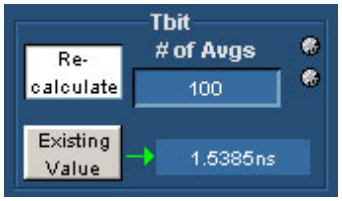
Remote GPIB Commands

The Remote General Purpose Interface Bus (RGPIB) is essentially another way of interfacing with the oscilloscope. It allows you to control much of the functionality of the oscilloscope as defined by the software, from a Remote GPIB controller.

For more information on the RGPIB commands, command syntax, arguments, and sample program, refer to the *TDSHT3 HDMI Compliance Test Software Programmer Online Help*. This is also available as a PDF file, Tektronix Part Number 077-0353-XX.

Calculate Tbit

On the Menu bar, click **Test > Configure** after the measurement is selected from the Select screen.



Tbit is the time that is required to transmit one bit of data. Tbit is one bit time at the specified pixel clock frequency (= T_{PIXEL}/10).

For all the tests that require clock, the software calculates Tbit. For all the other tests, you have an option of either recalculating Tbit or using the previous Tbit value for the test.

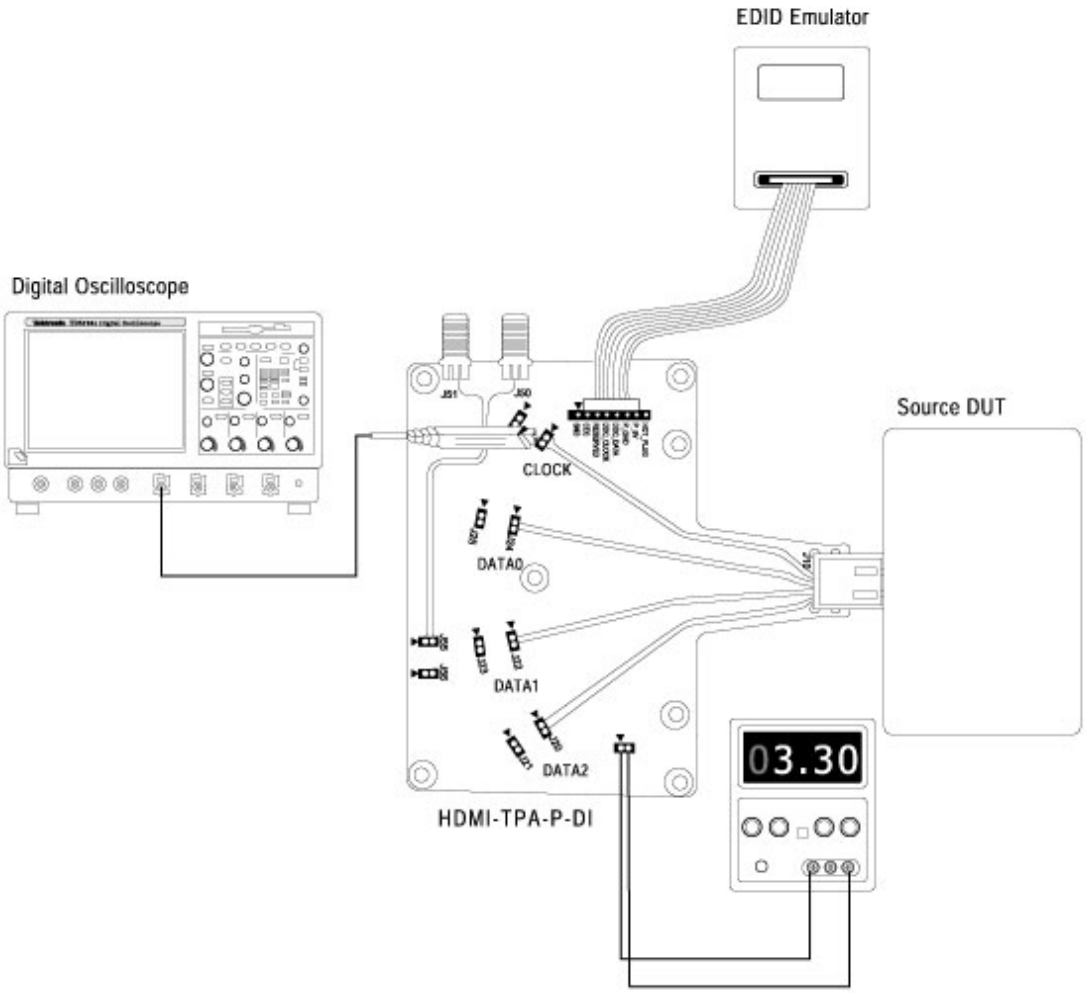
If you click **Re-calculate**, the software computes the specified number of averages of T_{PIXEL} and then calculates Tbit. If you use the existing Tbit value, the software uses the previously calculated Tbit value or you can again recalculate Tbit by using the Tbit pane.

To calculate Tbit for a test, use the Tbit pane. You can calculate Tbit for Rise Time, Fall Time, Inter-Pair Skew, Source Intra-Pair Skew, Low Amplitude +, Low Amplitude –, and Sink Intra-Pair Skew test if the clock is not connected.

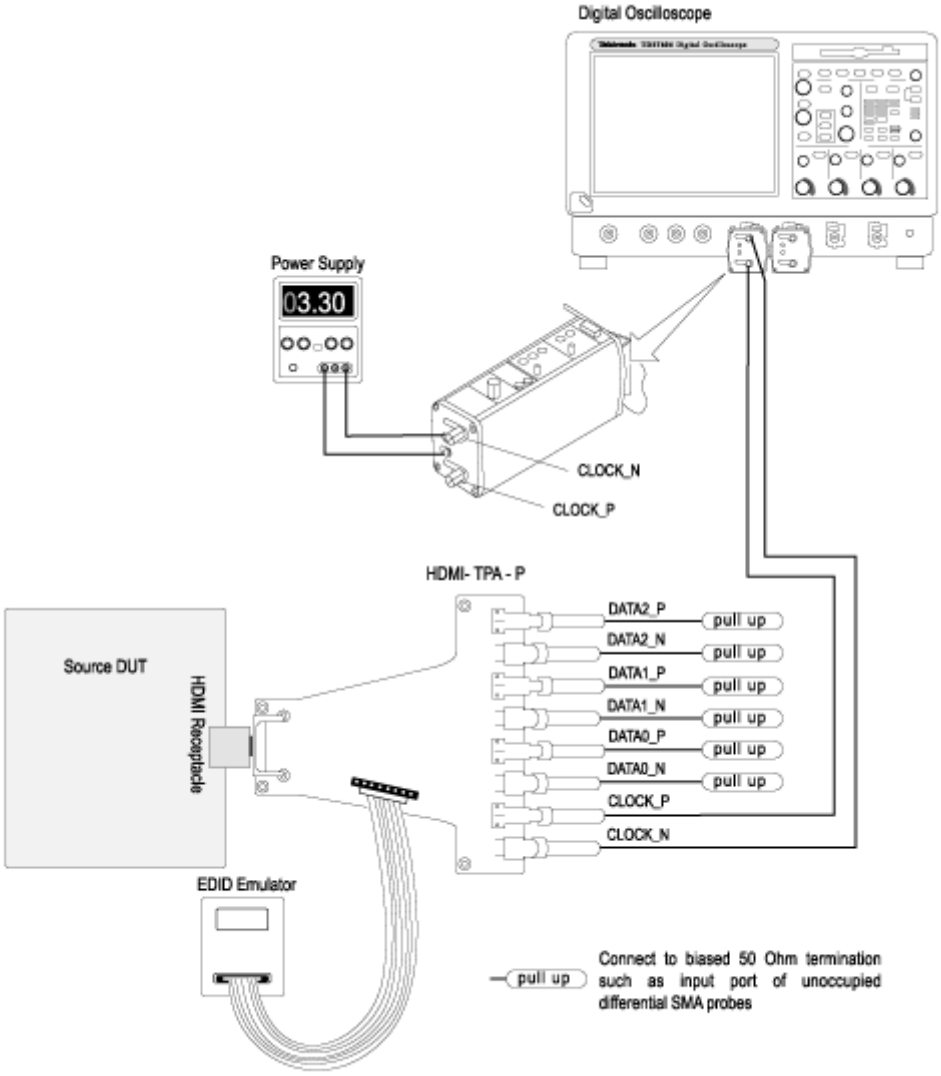
To Calculate Tbit

1. Set up the connections as shown in the following diagram:

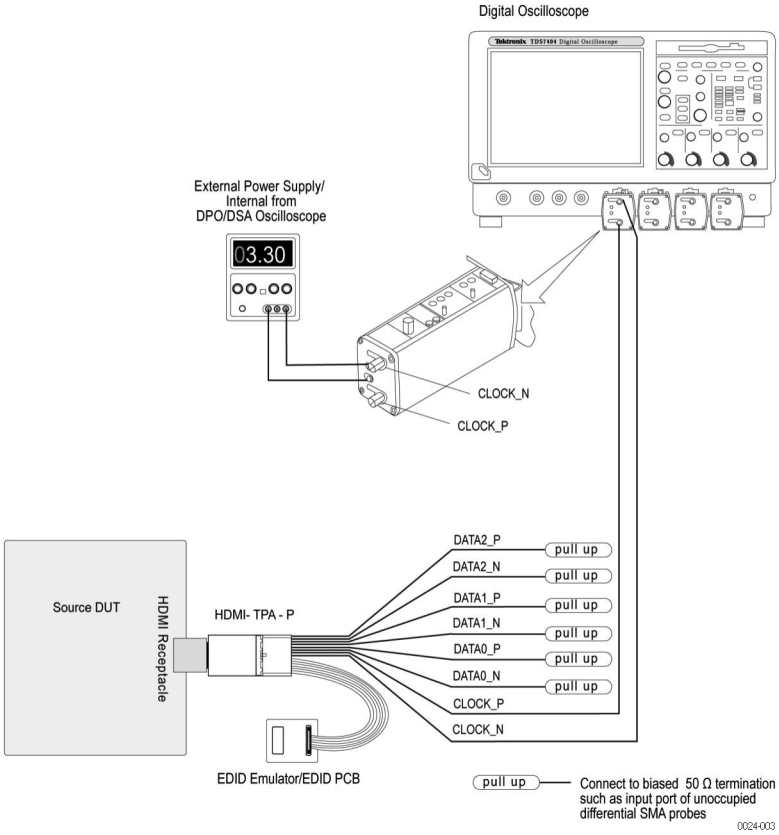
   Setup 1: Connections to calculate Tbit



Setup 2: Connections to calculate Tbit with the Efficere Test Fixture



Setup 3: Connections to calculate Tbit with the Wilder Test Fixture



NOTE. *You can also use the EDID PCB instead of the EDID Emulator.*

- Connect a TPA-P-DI adapter to a Source DUT HDMI output connector.
- Connect a power supply to a TPA board.
- Configure the Source DUT to output a video format with the required supported pixel clock frequency.
- Connect a TMDS Clock to the configured oscilloscope channel by using a differential probe.

2. In the Tbit pane, do the following:

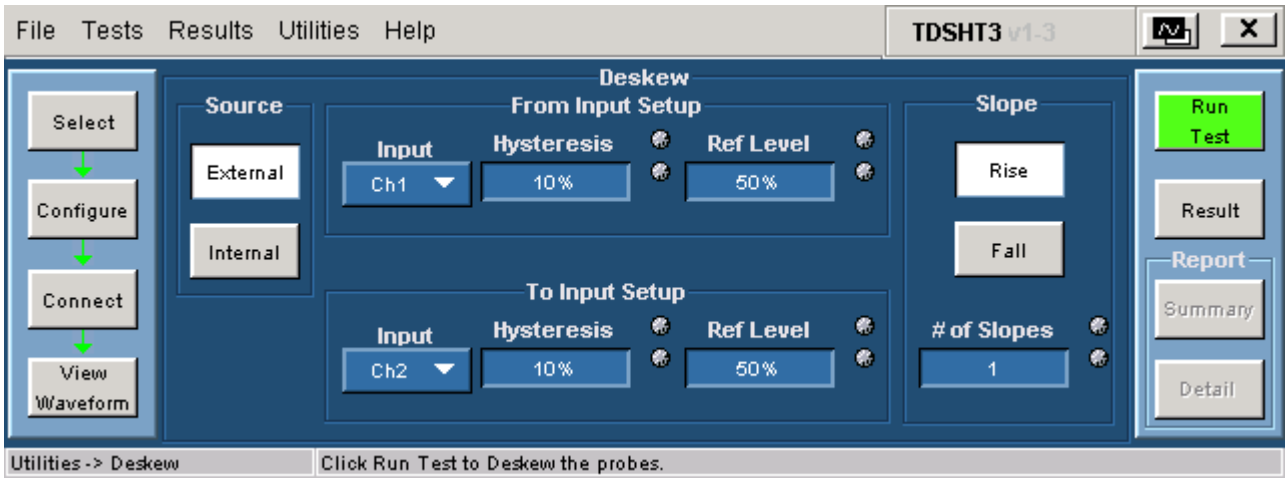
- Enter the desired number of periods that are considered to calculate Tbit. The default value is 100.
- Click **Re-calculate** to recalculate the Tbit value.
- Click **Existing Value** to use the previously calculated Tbit value.

NOTE. *Tbit value is used for oscilloscope setup and limit calculations. If the DUT's display resolution and the refresh rate changes, you have to recalculate Tbit.*

Deskew

Deskew is recommended before you conduct any skew test. To ensure accurate results, deskew the test setup before you conduct the tests from your device under test.

1. On the menu bar, click **Utilities > Deskew**.

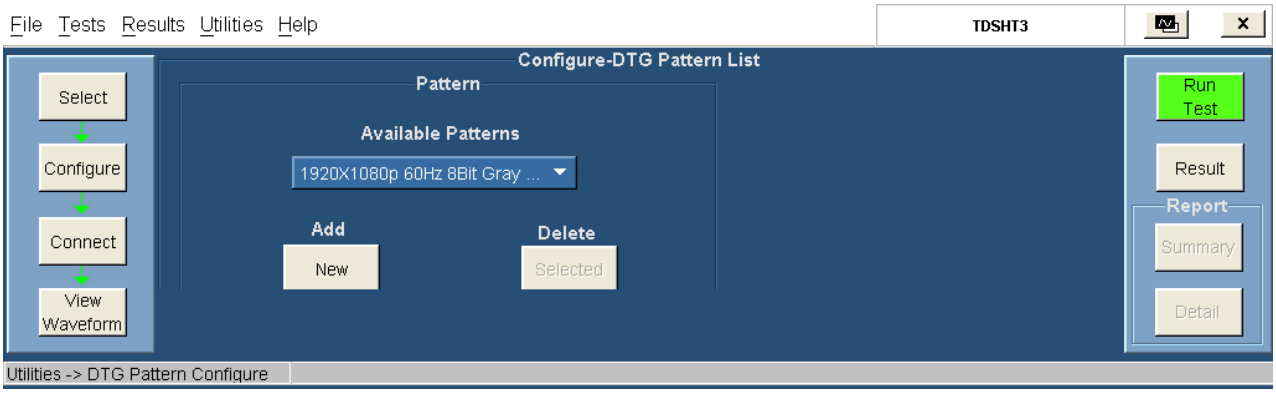


2. In the source pane, do the following:
   - Click **External** if you will use an external signal source (such as the clock signal of DUT).
   - Click **Internal** to probe the compensation signal on an oscilloscope.
3. Select the input channels between which you want to perform the deskew operation. Hysteresis and Ref Level are available only for an external source.
4. In the slope pane, do the following:
   - Click **Rise** to calculate the average of the number of slopes and then set the skew for a rising pulse.
   - Click **Fall** to calculate the average of the number of slopes and then set the skew for a falling pulse. You do not have to calculate the average of the number of slopes for a falling pulse for an internal source.
   - Enter the required number of slopes to enable to set the skew for either a rising pulse or a falling pulse. Ensure that the required number of slopes is present in the acquisition.

5. Set up the oscilloscope as follows:
   - Set the acquisition rate so that there are two or more samples on the deskew edge using the horizontal scale knob.
   - Adjust the signals and display them on the screen using the vertical scale and position knobs.
   - Set the record length so that there are more samples for the edges in the acquisition.
6. Click **Run Test** to deskew the probes.

Configure-DTG Pattern List

1. On the menu bar, click **Utilities > DTG Pattern List**.



2. In the Pattern pane, the Available Patterns drop-down list displays all the available patterns (including the newly added ones). The DTG pattern selected from the Configure screen is displayed as the default pattern in the Available Patterns list.
3. Click **New** to add a new DTG pattern. Type the name of the pattern and click **Enter** to save the pattern. All the newly added patterns will be available in Cable Eye Diagram (Passive and Active), Sink Min/Max Diff, and Sink Jitter Tolerance measurements. The newly added pattern files should have a `.dtg` extension.

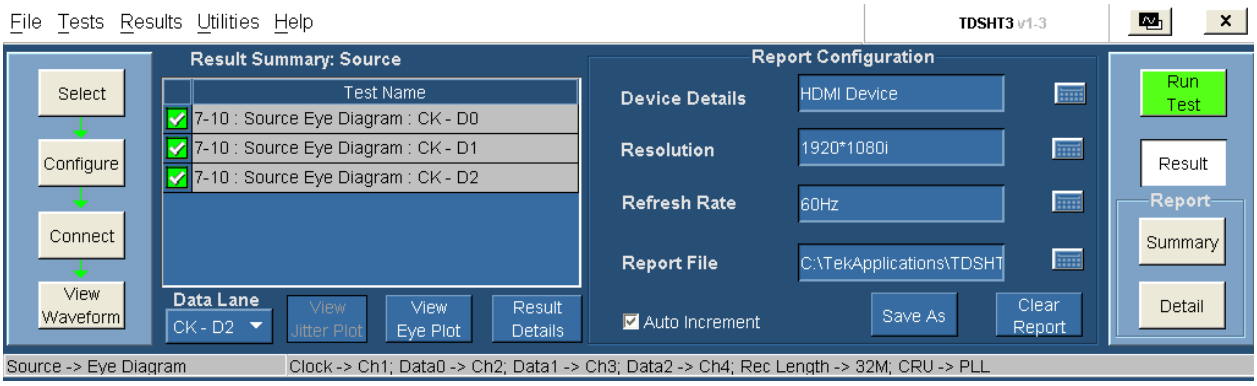
4. To delete an added pattern, select the pattern from the Available Patterns list. Click **Selected** to delete the selected pattern. The default patterns installed by the application cannot be deleted.

NOTE. *All the folders of the application should have unique DTG pattern names.*

View the Results

- On the menu bar, click **Results > Summary** to display the result summary of the last test(s) that you conducted.
- Click **Results > Details** to display the detailed results of the last test(s) that was conducted.

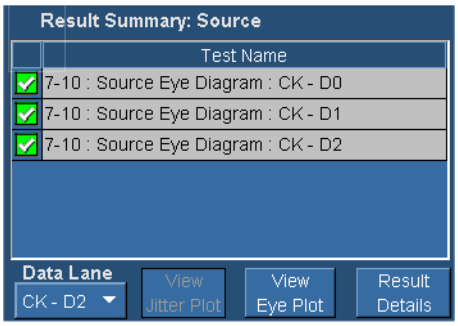
The result pane, which is located at the center of the software window, appears as shown in the following figure:



The result pane includes the result summary pane and the report configuration pane.

View the Result Summary

The result summary pane displays the test results.



This icon indicates that the test has passed.

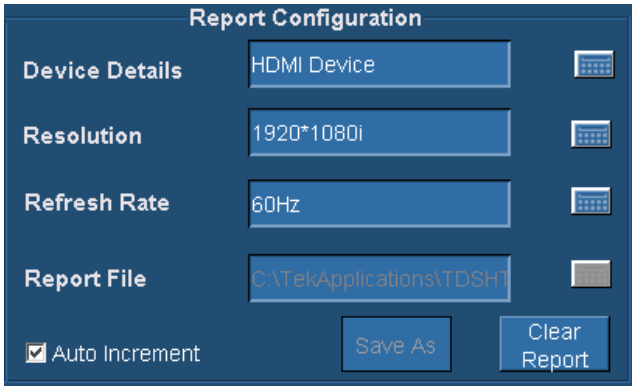
This icon indicates that the test has failed.

This icon indicates that the test could not be run due to an error.

- Status (displays the status of the test as Pass, Fail, or Error)
- Test Name (displays the test id, test name, and selected lanes)
- Data Lane (displays the eye diagram plot of the selected data lane pair)
- View Jitter Plot (displays the jitter plot). This option is available if you have successfully run the clock jitter test.
- View Eye Plot (displays the eye plot). This option is available if you have successfully run the eye diagram test.
- Result Details (displays the Result Details (see page 50) dialog box that shows the details of test results categorized as test name, specification range, measured value, result, and remarks.)

Configure the Report

Set the report details to identify and generate the report automatically. You can also set a default report file.

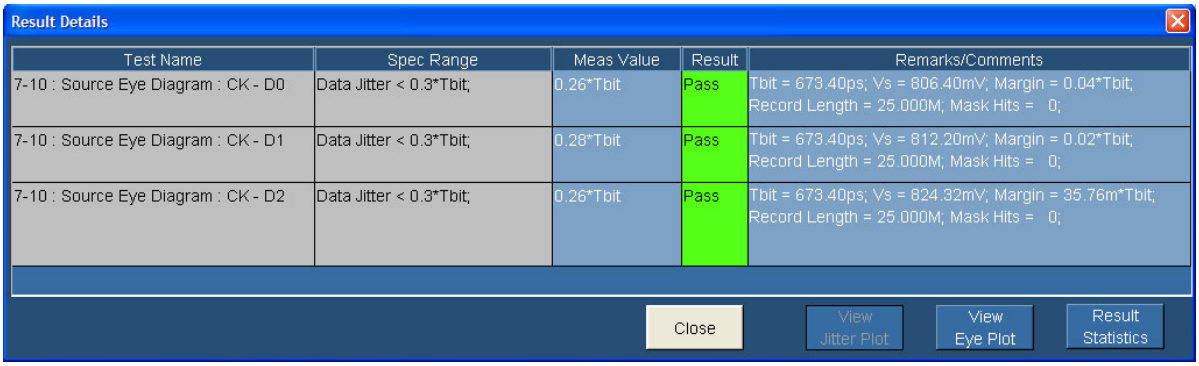


In the report configuration pane, you can configure the following parameters:

- The Device Details box allows you to specify the device-related information on which the test is conducted.
- The Resolution box allows you to specify the resolution on which the test is conducted.
- The Refresh Rate box allows you to specify the refresh rate at which the test is conducted.
- The Report File box allows you to specify the path and the file where the generated report will be saved. However, a default file name and path already exists.
- Select the Auto Increment check box to generate a new report. Selecting this option does not overwrite the existing report. However, it adds the date and time to the existing file name.
- Click **Save As** to save the generated reports. The Save File dialog box is displayed. Enter a file name and save the report.
- Click **Clear Report** to clear all the results and records of the earlier tests.

View the Result Details

In the Result Summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected lanes)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the measured value)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the results of Tbit, Vswing, and Margin). If the test could not be run, an error code (see page 397) appears.
- View Jitter Plot (displays the jitter plot). This option is available if you have successfully run the clock jitter test.
- View Eye Plot (displays the eye plot). This option is available if you have successfully run the eye diagram test.
- Result Statistics (displays statistics based on the tests)

NOTE. *The parameters in the Result Details dialog box may change depending on the test that you run.*

View the Result Statistics

Click **Result Statistics** to display statistics based on the tests in the Result Details dialog box.

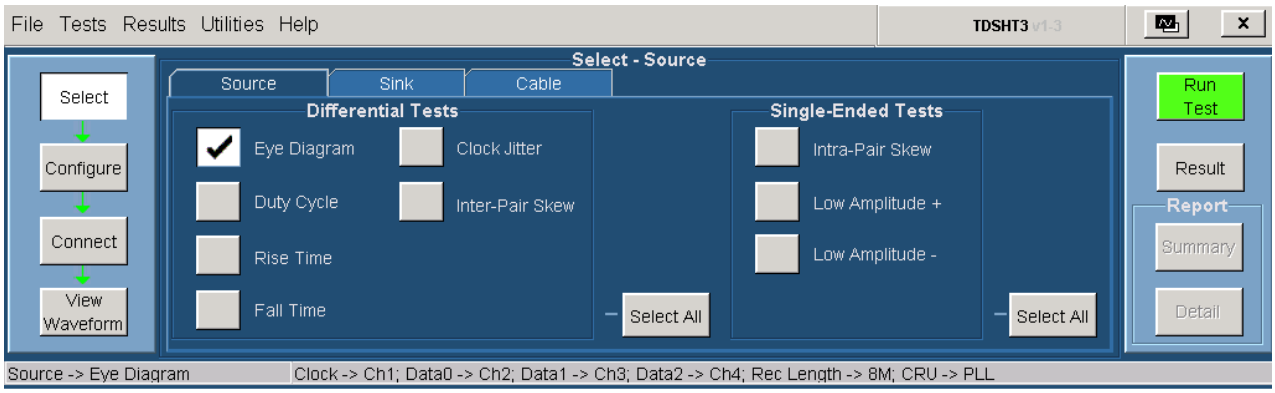
The software calculates statistics for each selected test, and logs the statistics on a cycle-by-cycle basis in a large waveform. The standard statistics are for the Maximum, Minimum, Mean, Standard Deviation, and Population.

Options	Description
Test Name	The Test Name column displays the test id, test name, and selected lanes.
Population	The software calculates this statistic by using the following equation: Population (X) = N

Options	Description
Min	The software calculates this statistic by using the following equation: Min (X) = Lowest value of X
Max	The software calculates this statistic by using the following equation: Max (X) = Highest value of X
Mean	The software calculates this statistic by using the following equation: $Mean\ (X) = \overline{X} = \frac{1}{N}\sum_{n=1}^{N} X_n$
Std Dev	The software calculates this statistic by using the following equation: $Standard\ Deviation\ (X) = \sigma_x = \sqrt{\frac{1}{(N-1)}\sum_{n=1}^{N}(X_n - \overline{X})^2}$
Pk-Pk	The software calculates this statistic by using the following equation: Xppn = Max(X) – Min(X)

NOTE. *Result Statistics is not available for Source tests such as Duty Cycle, Inter-Pair Skew, Intra-Pair Skew, Low Amplitude +, Low Amplitude –, and all Sink tests.*

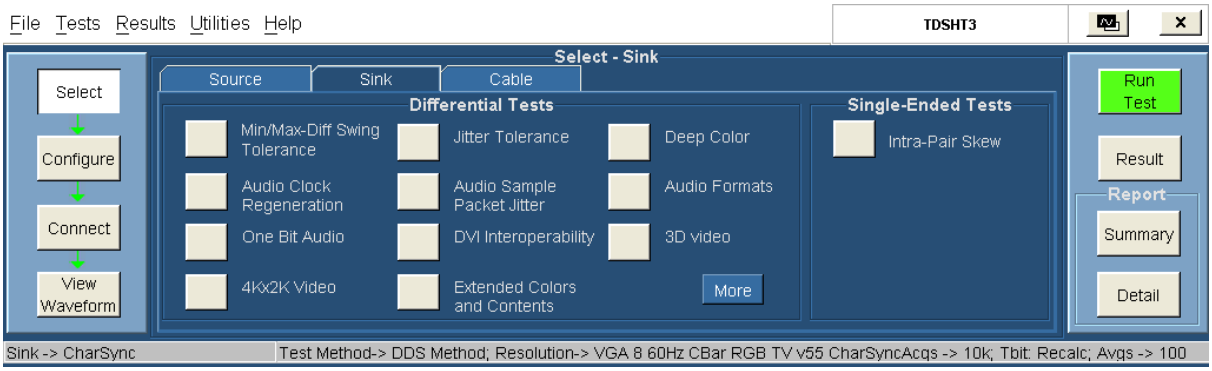
Select a Source Test



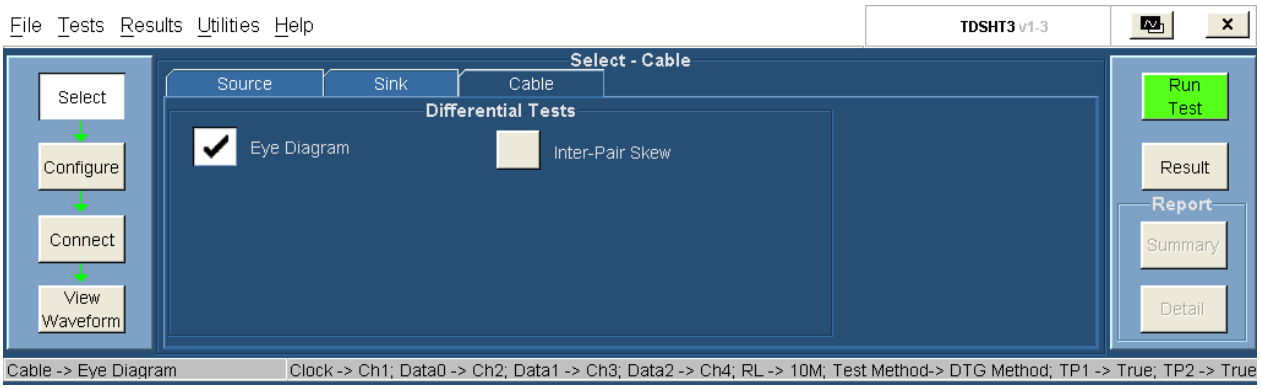
1. Click **Tests > Select > Source**.
2. Select the differential test(s) or single-ended test(s) that you want to perform.
3. To select all of the Differential Tests or all of the Single-Ended Tests, click the associated **Select All** button (which will change to **Clear All**).

Select a Sink Test

1. Click **Tests > Select > Sink**.
2. Select the differential test(s) or single-ended test that you want to perform.
3. Click **More** to view more differential tests.



Select a Cable Test



1. Click **Tests > Select > Cable**.
2. Select the differential test(s) that you want to perform.

Configure Parameters for the Source Tests

On the menu bar, click **Tests > Configure** to configure the parameters for the selected test(s).

In the configure pane, you will see the factory default configuration for the test you selected. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application. For more information about configuration, refer to How to... Test and go to a specific test.

The following table shows the parameters that you can configure for source (differential tests):

	Parameters available for each test					
Parameters	**Eye Diagram**	**Duty Cycle**	**Rise Time**	**Fall Time**	**Clock Jitter**	**Inter-Pair Skew**
Source input	Clock, Data0, Data1, and Data2	Clock	Clock, Data0, Data1, and Data2	Clock, Data0, Data1, and Data2	Clock	Clock, Data0, Data1, and Data2
Clock	Yes	—	—	—	Yes	Yes
Hysteresis	Yes	—	—	—	Yes	Yes
Mid Ref Level	Yes	—	—	—	Yes	Yes
Low Ref Level	—	—	Yes	Yes	—	—
High Ref Level	—	—	Yes	Yes	—	—
Record Length	Yes	—	—	—	Yes	—
Tbit	—	Yes	Yes	Yes	—	Yes
# of Acqs	—	Yes	Yes	Yes	—	—
Units	Yes	—	Yes	Yes	Yes	Yes
CRU	Yes	—	—	—	Yes	—

The following table shows the parameters that you can configure for source (single-ended tests):

	Parameters available for each test		
Parameters	**Intra-Pair Skew**	**Low Amplitude +**	**Low Amplitude –**
Source Input	Clock+ and Clock– Data0/Data1/Data2 and Data0/Data1/Data2	Clock+ and Clock– Data0/Data1/Data2 and Data0/Data1/Data2	Clock+ and Clock– Data0/Data1/Data2 and Data0/Data1/Data2
Avcc	—	Yes	Yes
Tbit	Yes	Yes	Yes
# of Acqs	Yes	Yes	Yes

Configure Parameters for the Sink Tests

On the menu bar, click **Tests > Configure** to configure the parameters for the selected test.

In the configure pane, you will see the factory default configuration for the test you selected. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application. For more information about configuration, refer to How to... Test and go to a specific test.

The following table shows the parameters that you can configure for sink (differential tests):

	Parameters available for each test					
Parameters	Min/Max-Diff Swing Tolerance (DTG Method)	Min/Max-Diff Swing Tolerance (DDS Method)	Jitter Tolerance (DTG Method)	Jitter Tolerance (DDS Method)	Deep Color (DTG Method)	Deep Color (DDS Method)
Source Input	Clock/Data	Clock/Data	Clock and Data	Clock and Data	—	—
Clock	—	—	Yes	Yes	—	—
Pattern List	Yes	Yes	Yes	Yes	Yes	Yes
DTG Output	Yes	—	Yes	—	Yes	—
Cable Emulator	—	—	—	Yes	—	—
Markers	—	Yes	—	Yes	—	Yes
Frequency Pair	—	—	Yes	Yes	—	—
DUT Freq (MHz)	—	—	Yes	Yes	—	—
Jitter Insertion Type	—	—	Yes	Yes	—	—
Jitter Amplitude	—	—	Yes	—	—	—
Resolution	—	—	—	—	Yes	Yes
Refresh Rate	—	—	—	—	Yes	Yes
Deep Color Bits	—	—	—	—	Yes	Yes

Parameters	Parameters available for each test					
	Audio Clock Regeneration (DTG Method)	Audio Clock Regeneration (DDS Method)	Audio Sample Packet Jitter (DTG Method)	Audio Sample Packet Jitter (DDS Method)	Audio Formats (DTG Method)	Audio Formats (DDS Method)
Source Input	Yes	Yes	Yes	Yes	Yes	Yes
Clock	Yes	Yes	Yes	Yes	Yes	Yes
Pattern List	Yes	Yes	Yes	Yes	Yes	Yes
DTG Output	Yes	—	Yes	—	Yes	—
Cable Emulator	—	—	—	—	—	—
Markers	—	Yes	—	Yes	—	Yes
Frequency Pair	—	—	—	—	—	—
DUT Freq (MHz)	—	—	—	—	—	—
Jitter Insertion Type	—	—	—	—	—	—
Jitter Amplitude	—	—	—	—	—	—
Resolution	—	—	—	—	—	—
Refresh Rate	—	—	—	—	—	—
Deep Color Bits	—	—	—	—	—	—

	Parameters available for each test					
Parameters	One Bit Audio (DTG Method)	One Bit Audio (DDS Method)	DVI Inter-operabil-ity (DTG Method)	DVI Inter-operabil-ity (DDS Method)	3D Video (DTG Method)	3D Video (DDS Method)
Source Input	Yes	Yes	Yes	Yes	Yes	Yes
Clock	Yes	Yes	Yes	Yes	Yes	Yes
Pattern List	Yes	Yes	Yes	Yes	Yes	Yes
DTG Output	Yes	—	Yes	—	Yes	—
Cable Emulator	—	—	—	—	—	—
Markers	—	Yes	—	Yes	—	Yes
Frequency Pair	—	—	—	—	—	—
DUT Freq (MHz)	—	—	—	—	—	—
Jitter Insertion Type	—	—	—	—	—	—
Jitter Amplitude	—	—	—	—	—	—
Resolution	—	—	—	—	—	—
Refresh Rate	—	—	—	—	—	—
Deep Color Bits	—	—	—	—	—	—

Parameters	Parameters available for each test			
	4Kx2K Video (DTG Method)	4Kx2K Video (DDS Method)	Extended Colors and Contents (DTG Method)	Extended Colors and Contents (DDS Method)
Source Input	Yes	Yes	Yes	Yes
Clock	Yes	Yes	Yes	Yes
Pattern List	Yes	Yes	Yes	Yes
DTG Output	Yes	—	Yes	—
Cable Emulator	—	—	—	—
Markers	—	Yes	—	Yes
Frequency Pair	—	—	—	—
DUT Freq (MHz)	—	—	—	—
Jitter Insertion Type	—	—	—	—
Jitter Amplitude	—	—	—	—
Resolution	—	—	—	—
Refresh Rate	—	—	—	—
Deep Color Bits	—	—	—	—

The following table shows the parameters that you can configure for sink (single-ended tests):

Parameters	Parameters available for each test	
	Intra-Pair Skew (DTG Method)	Intra-Pair Skew (DDS Method)
Source Input	Clock	Clock
Tbit	Yes	Yes
Skew Channel	Yes	Yes
Pattern List	Yes	Yes
DTG Output	Yes	—
Analog	—	Yes
Skew on one channel	Yes	Yes
Skew on all Channels	Yes	Yes

Configure Parameters for the Cable Tests

On the menu bar, click **Tests > Configure** to configure the parameters for the selected test.

In the configure pane, you will see the factory default configuration for the test you selected. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application. For more information about configuration, click the How to...Test help topic, and then go to the specific test.

Eye Diagram (Passive) and Inter-Pair Skew cable test parameters

Parameters	Eye Diagram (Passive) (DTG Method)	Eye Diagram (Passive) (DDS Method)	Inter-Pair Skew (DDS Method)
Source Input	Clock, Data0, Data1, and Data2	Clock, Data0, Data1, and Data2	Clock, Data0, Data1, and Data2
Clock	Yes	Yes	Yes
Hysteresis	Yes	Yes	Yes
High Ref Level	Yes	Yes	Yes
Mid Ref Level	Yes	Yes	Yes
Low Ref Level	Yes	Yes	Yes
Record Length	Yes	Yes	—
Ref Level Units	Yes	Yes	Yes
TP1, TP2, TP5	TP1 and TP2	TP1, TP2, and TP5	—
Pattern List	Yes	—	—
Cable Frequency	—	Yes	Yes
DTG Output	Yes	—	—
Cable Equalizer	Yes	Yes	—
Rise Time Filter	Yes	—	—
CRU	Yes	Yes	—
Jitter Insertion	Yes	Yes	—
# of Avgs	—	—	Yes
Tbit	—	—	Yes
Markers	—	—	Yes
VTerm	0.0 V	0.0 V	Yes

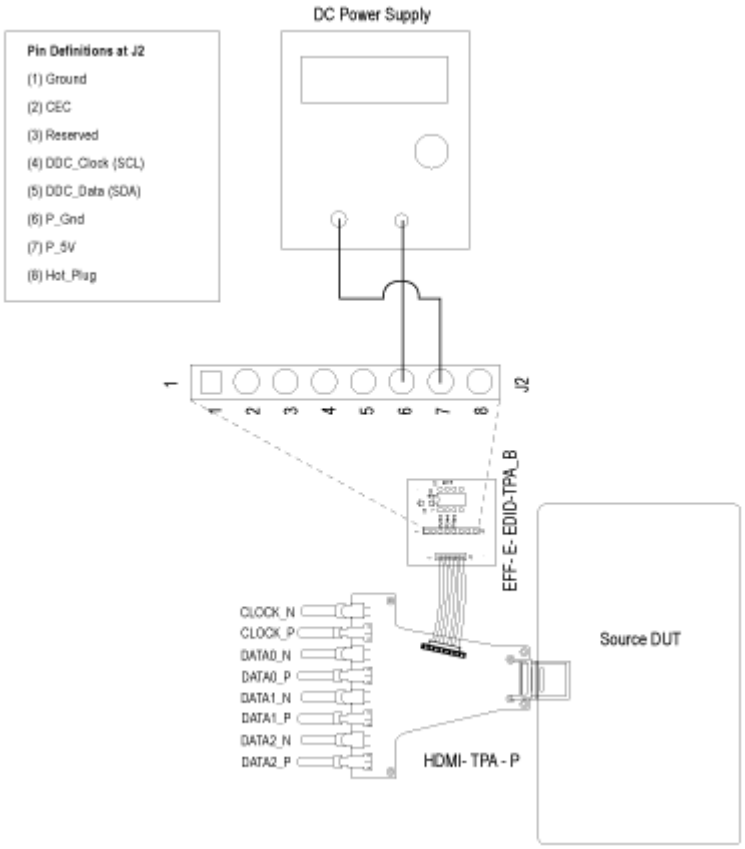
NOTE. *This Cable Inter-Pair Skew test is performed only for* ***repeater cable testing****.*

Eye Diagram (Active) cable test parameters

Parameters	Eye Diagram (Active) (DTG Method)
Source Input	Clock, Data0, Data1, and Data2
Clock	Yes
Hysteresis	Yes
High Ref Level	Yes
Mid Ref Level	Yes
Low Ref Level	Yes
Record Length	Yes
Ref Level Units	Yes
TP1, TP2, TP5	TP1 and TP2
Pattern List	Yes
Cable Frequency	—
DTG Output	Yes
Cable Equalizer	Yes
Rise Time Filter	Yes
CRU	Yes
Jitter Insertion	Yes
# of Avgs	—
Tbit	—
Markers	—
VTerm	3.3 V

Connect the EDID Emulator for Source Tests

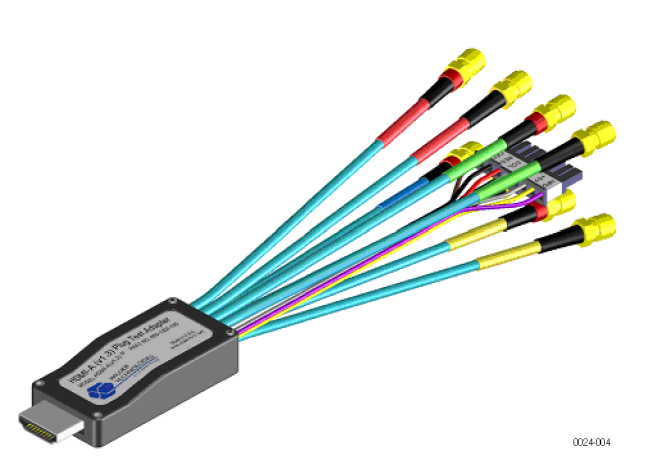
The EDID-PCB or EDID Emulator can be used in the following Source connection diagrams.



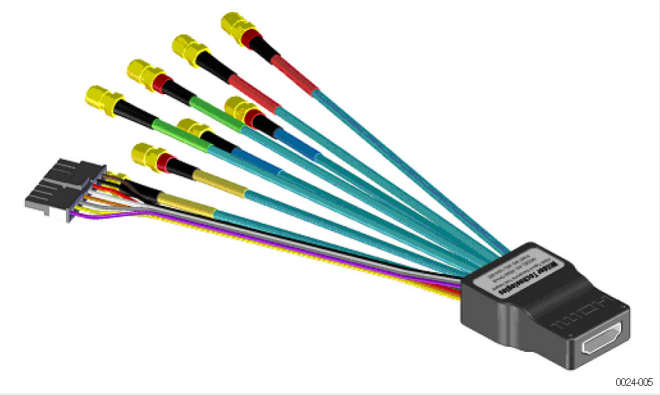
HDMI Test Fixtures

Type-D fixture is required for the new mobile application as per the CTS 1.4a. For all the Source and Sink test measurements, use the Type-D fixture in place of Type-A (see page 62), Type-C, and Type-E (see page 63) fixtures while making connections. For setup details, refer to the appropriate connection diagrams in this manual.

The following figure shows the Type-A alternate equivalent plug:

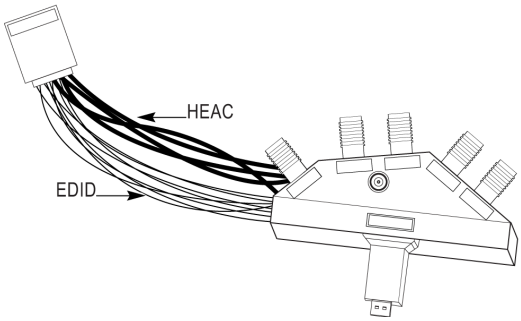


The following figure shows the Type-A alternate equivalent receptacle:

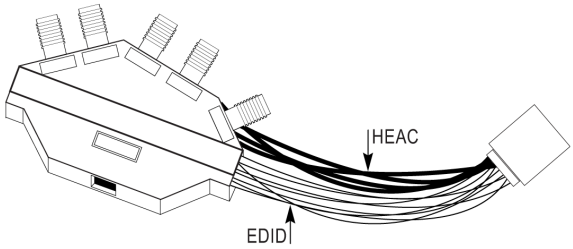


The following figure shows a graphical representation of the Type-D Plug and Receptacle fixtures.

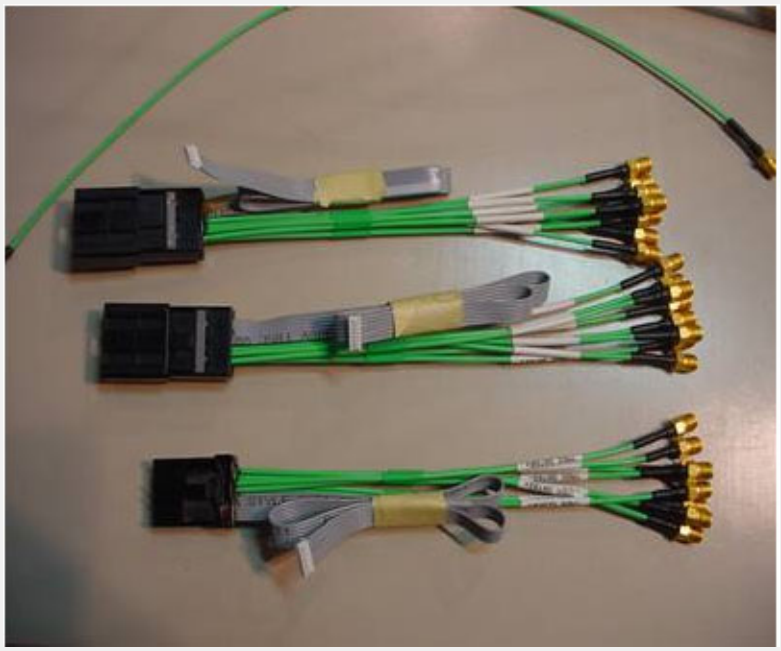
TPA-P



TPA-R



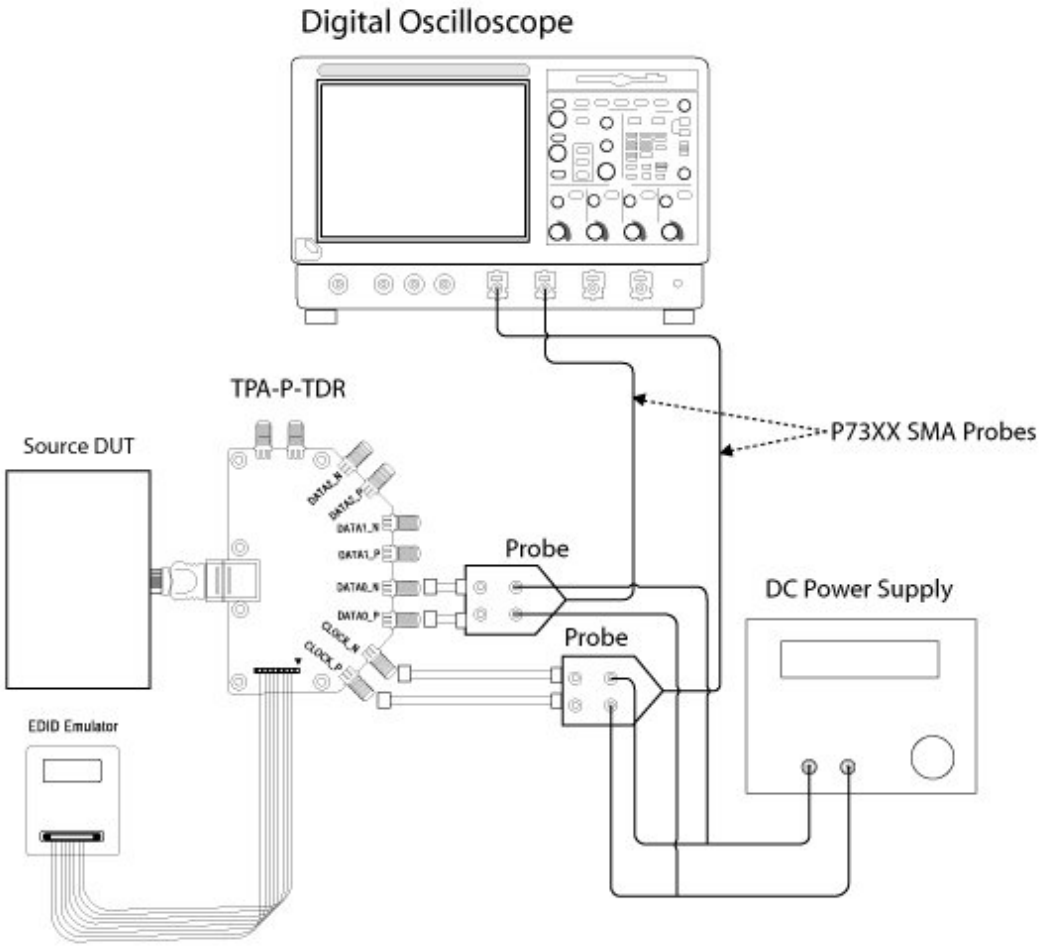
The following figure shows the Type-E fixture:



Make Connections for Source Eye Diagram

On the menu bar, click **Tests > Connect** and make the connection as follows. Refer to EDID Emulator for Source Tests (see page 61) for EDID emulator connections.

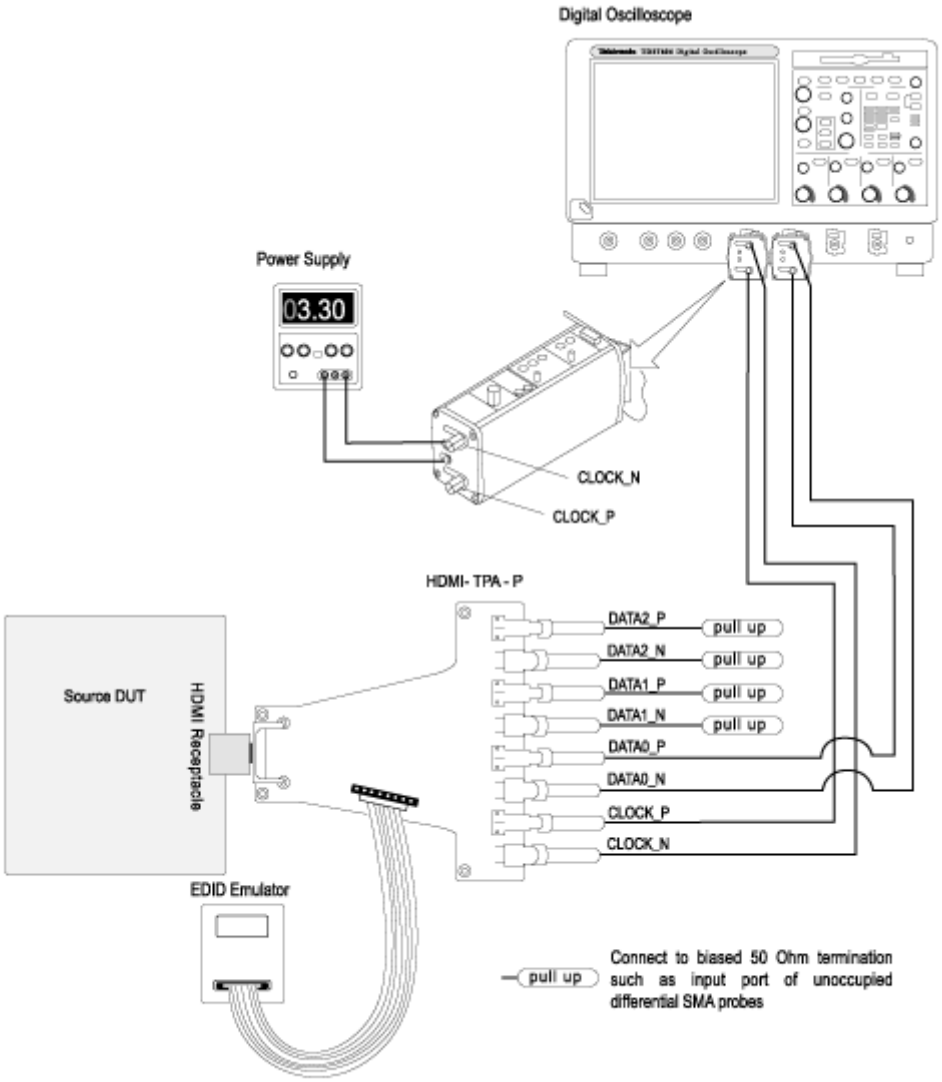
Method 1: Connections for Source Eye Diagram



NOTE. *You can also use the EDID PCB instead of the EDID Emulator.*

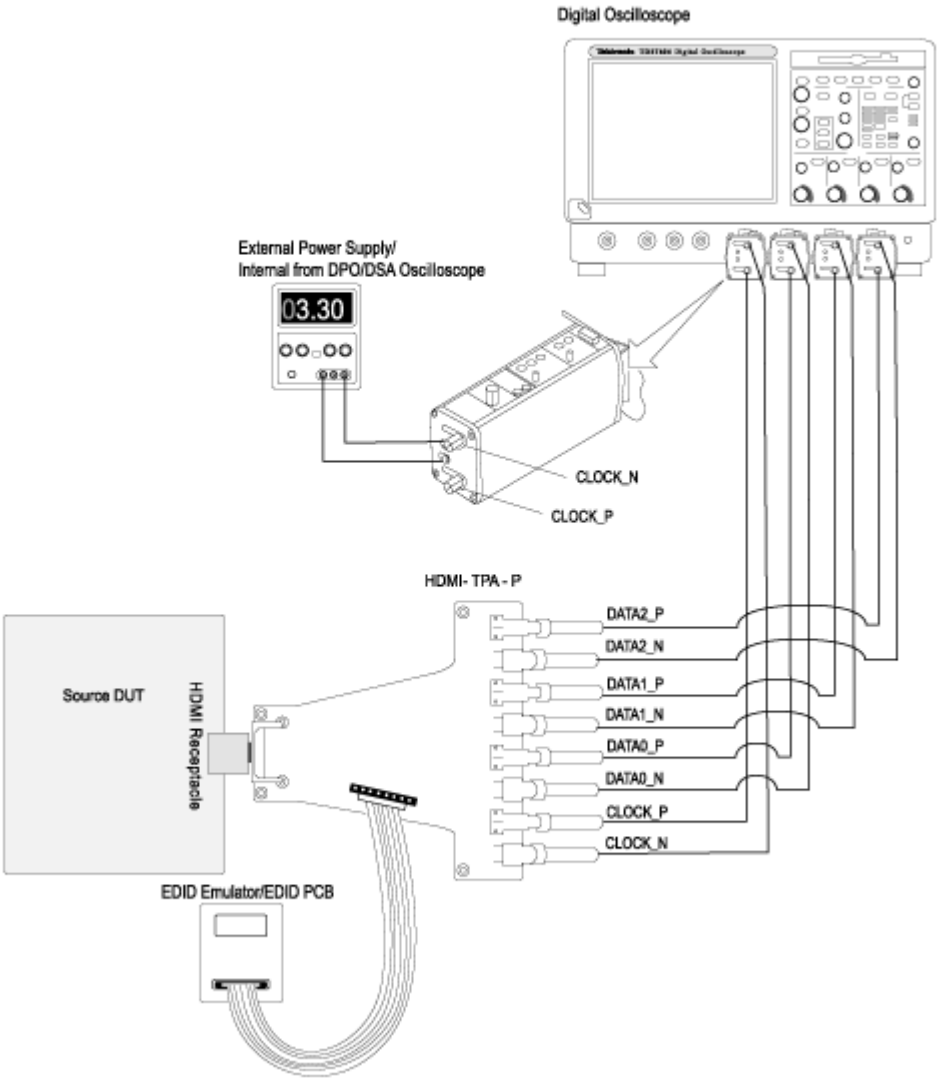
NOTE. *Appropriate HDMI fixtures to be used based on the application.*

Method 2: Connections for Source Eye Diagram with the Efficere Test Fixture



NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

For 4-Channel



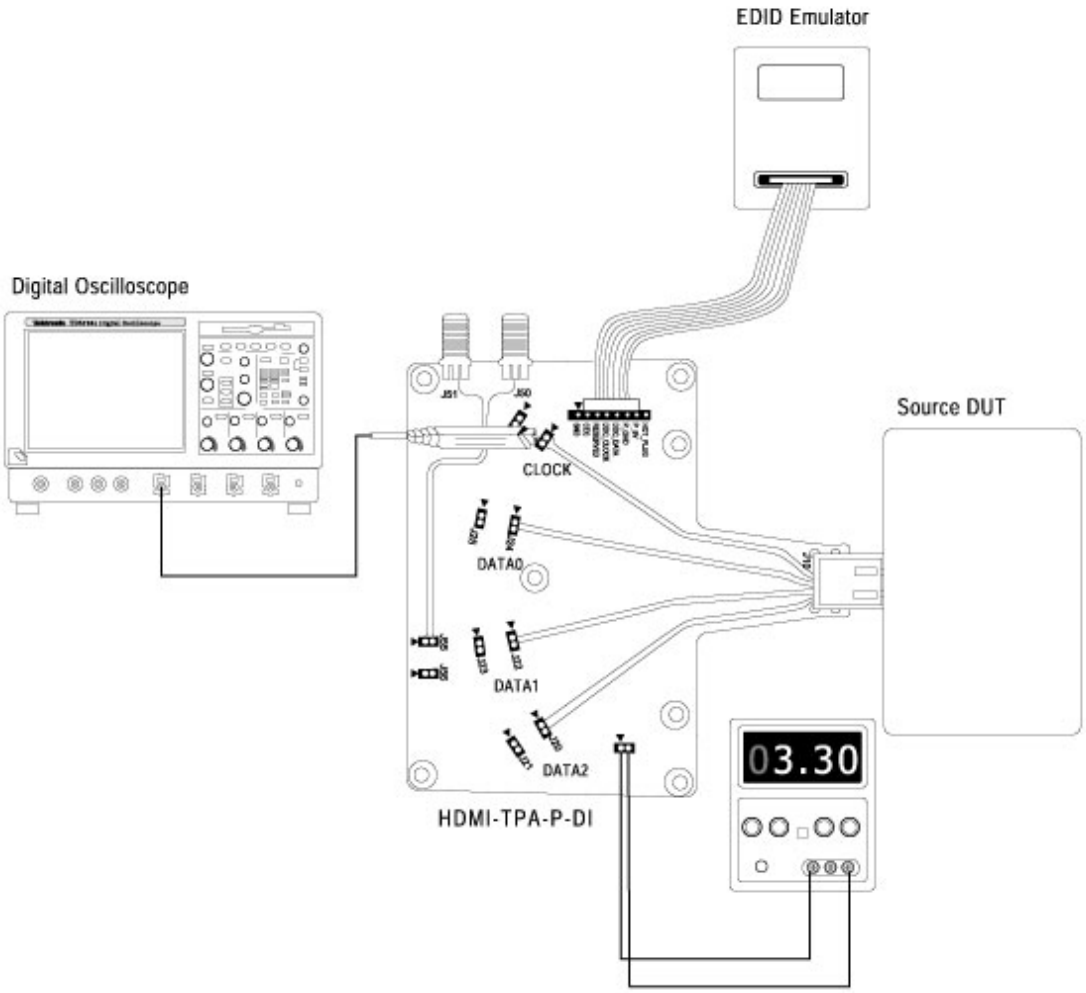
NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

1. Connect the HDMI output of the source DUT to the TPA-P-TDR/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.
3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Connect a TMDS Clock to the configured oscilloscope channel by using a SMA differential probe.
5. Connect the TMDS Data pair(s) on which you will conduct the test to the configured oscilloscope channel by using a SMA differential probe.
6. Configure the Source DUT to output the required video format.

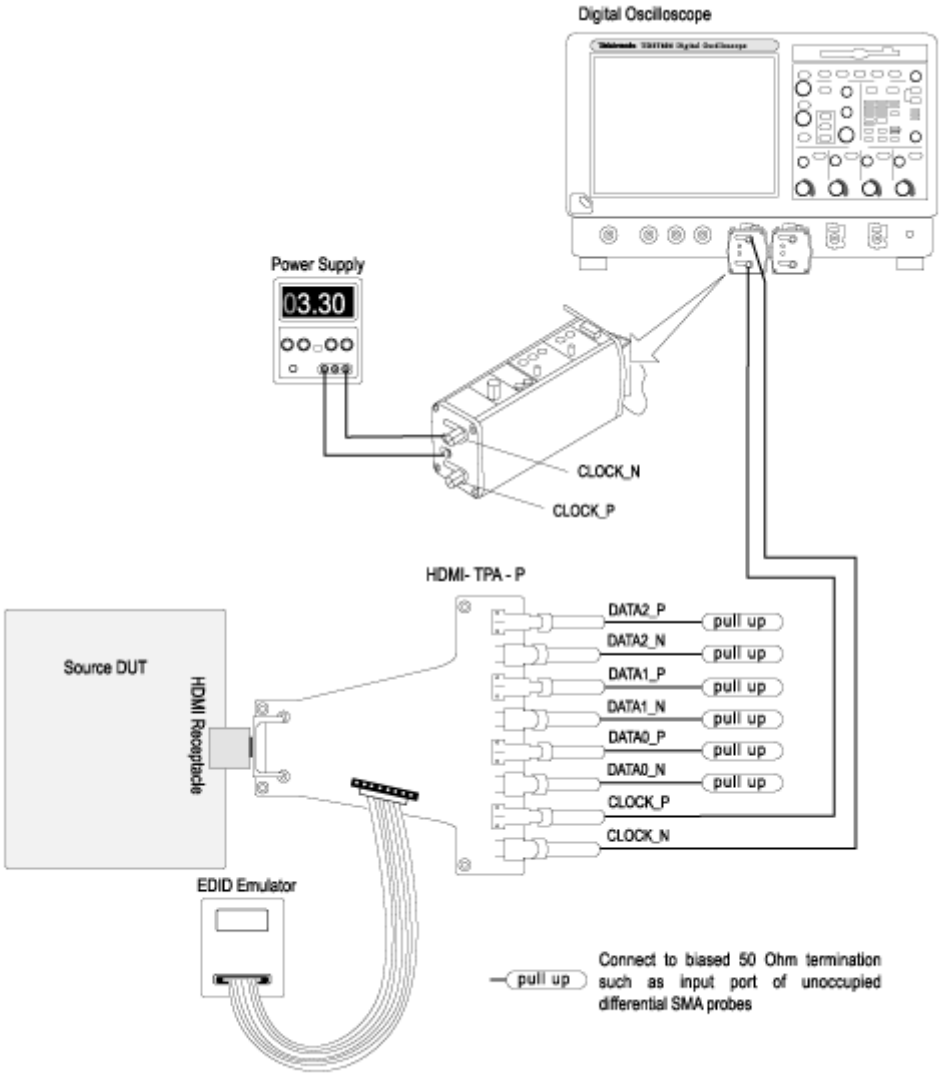
Make Connections for Duty Cycle

On the menu bar, click **Tests > Connect** and make the connection as follows. Refer to EDID Emulator for Source Tests (see page 61) for EDID emulator connections.

Method 1: Connections for Source Duty Cycle



Method 2: Connections for Source Duty Cycle with the Efficere Test Fixture



NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

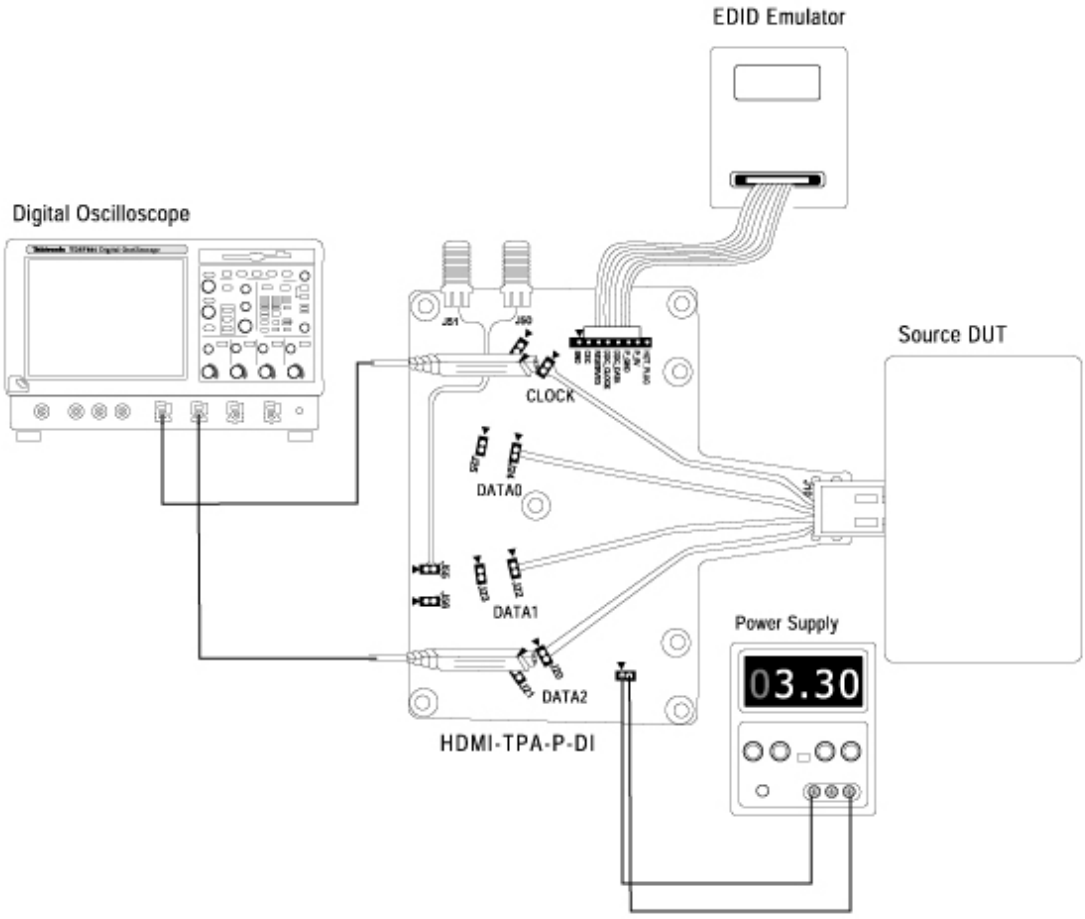
1. Connect the HDMI output of the source DUT to the TPA-P-DI/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Configure the Source DUT to output a video format with the required supported pixel clock frequency.
5. Connect a TMDS Clock to the configured oscilloscope channel by using a differential probe.

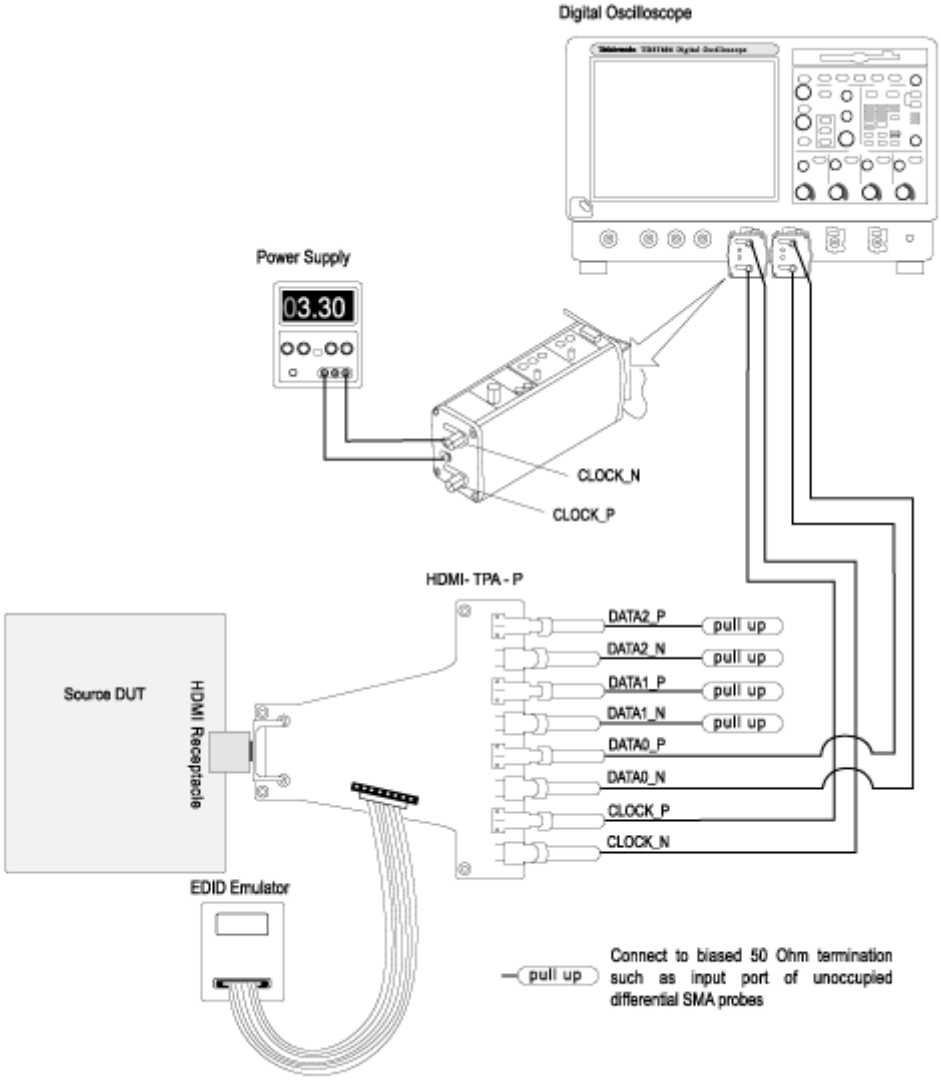
Make Connections for Rise Time

On the menu bar, click **Tests > Connect** and make the connection as follows. Refer to EDID Emulator for Source Tests (see page 61) for EDID emulator connections.

Method 1: Connections for Source Rise Time

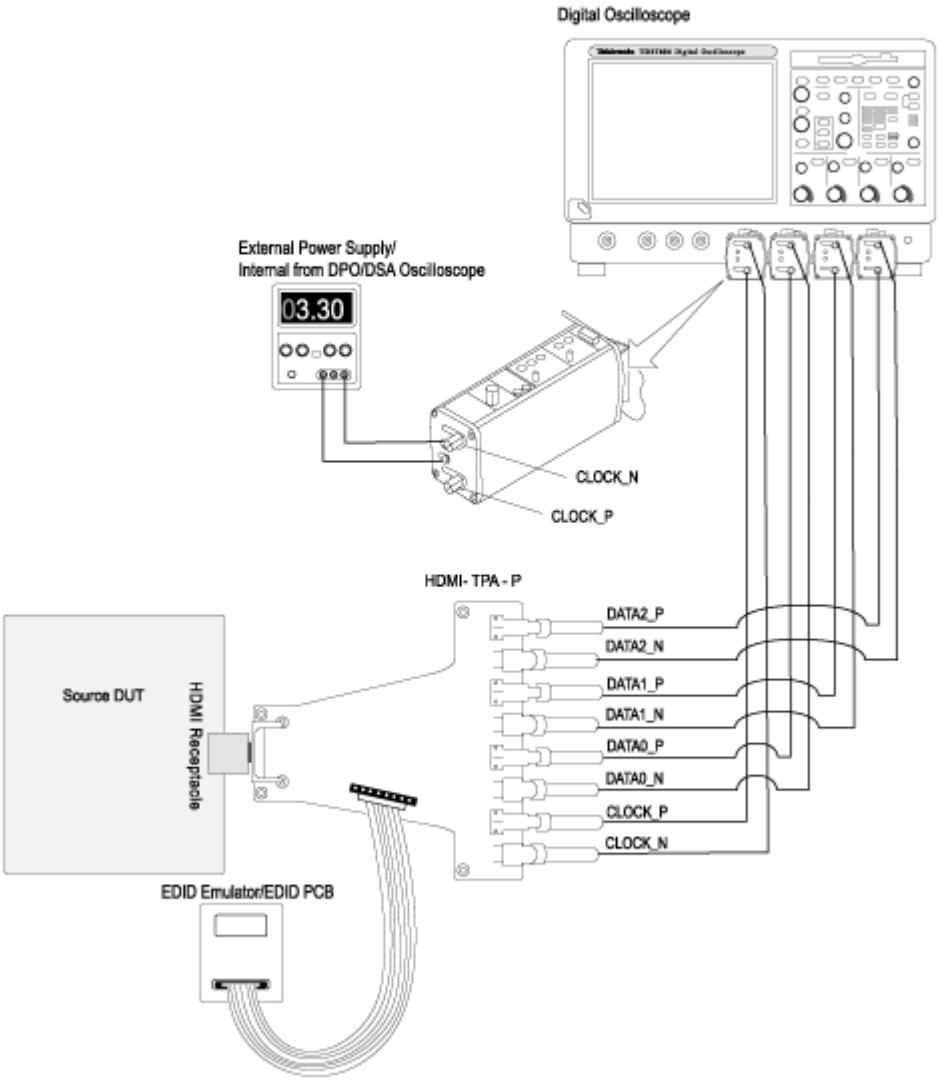


Method 2: Connections for Source Rise Time with the Efficere Test Fixture



NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

For 4-Channel



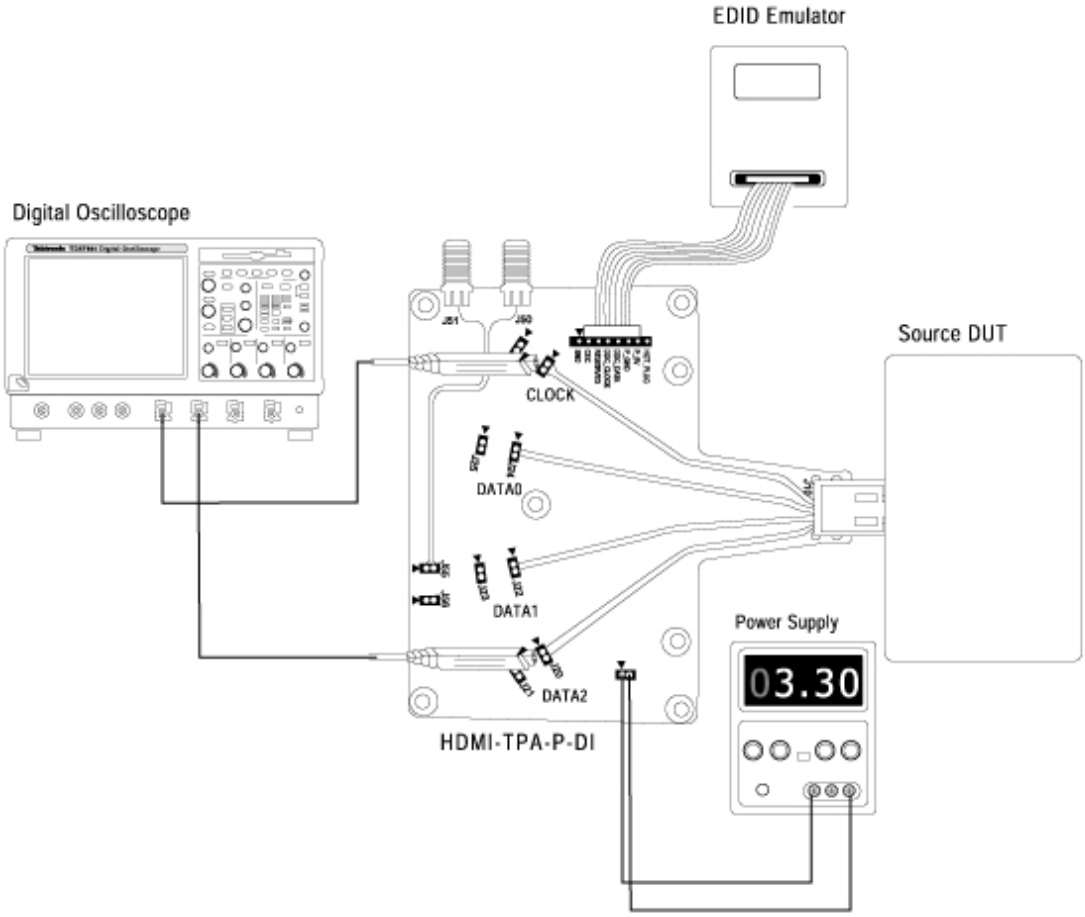
NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

1. Connect the HDMI output of the source DUT to the TPA-P-DI/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.
3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Configure the Source DUT to output a video format with the required supported pixel clock frequency.
5. Connect a differential probe(s) to a TMDS_DATA/CLOCK.
6. If you have selected **Re-calculate Tbit** in the configuration pane, connect the Clock channel to the configured oscilloscope channel by using a second differential probe(s).

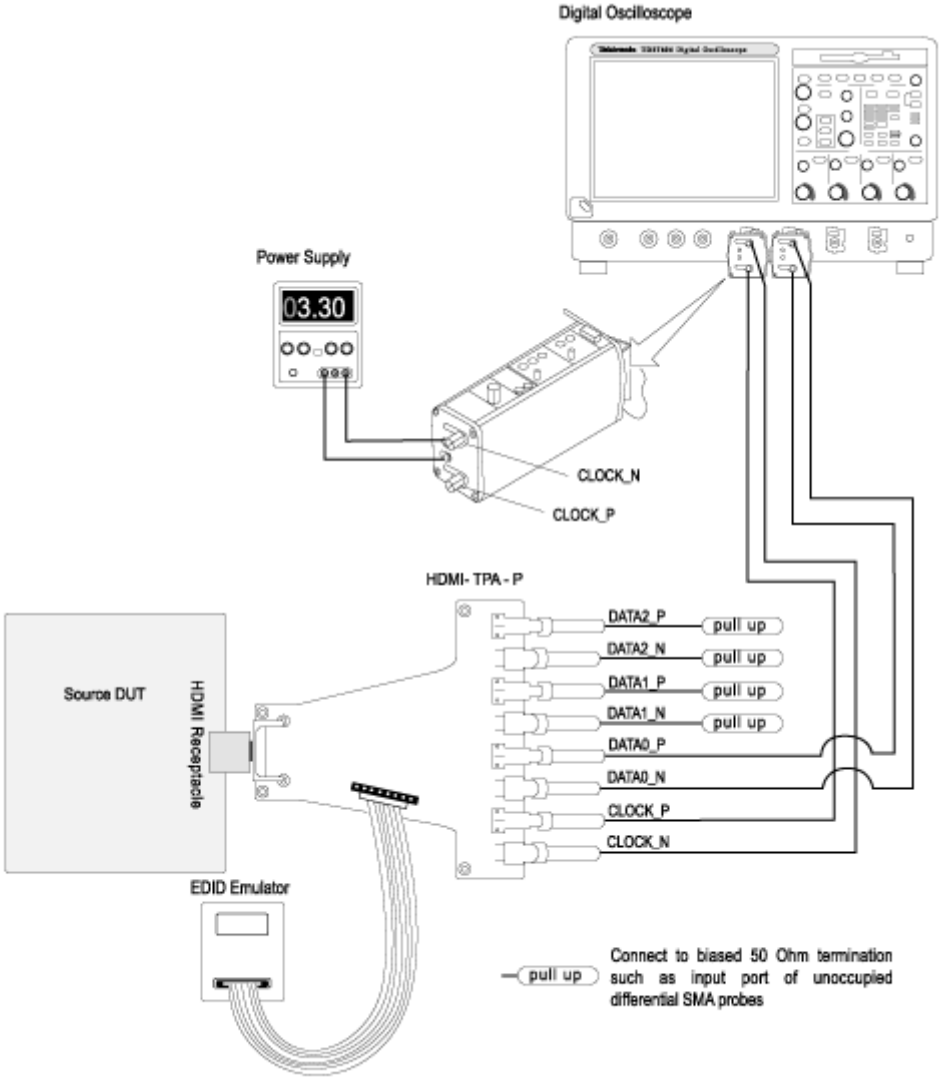
Make Connections for Fall Time

On the menu bar, click **Tests > Connect** and make the connection as follows. Refer to EDID Emulator for Source Tests (see page 61) for EDID emulator connections.

Method 1: Connections for Source Fall Time

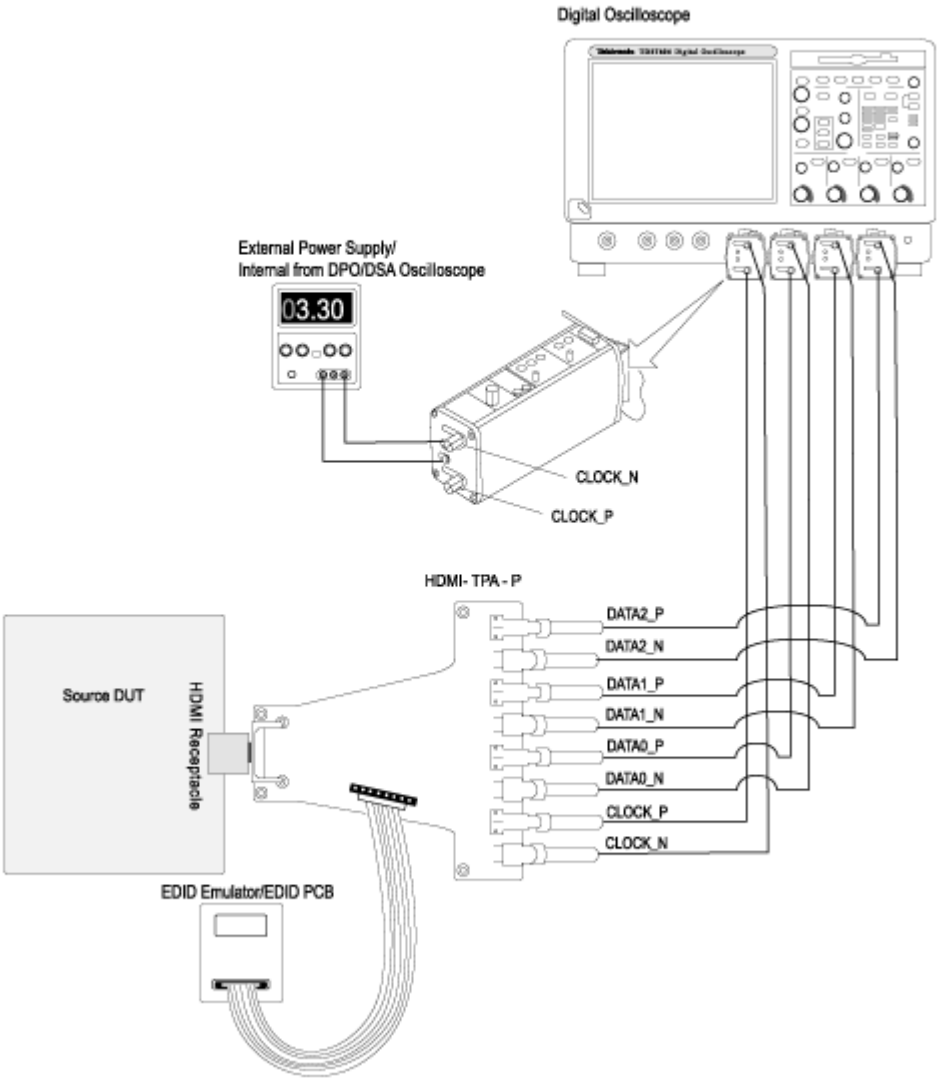


Method 2: Connections for Source Fall Time with the Efficere Test Fixture



NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

For 4-Channel



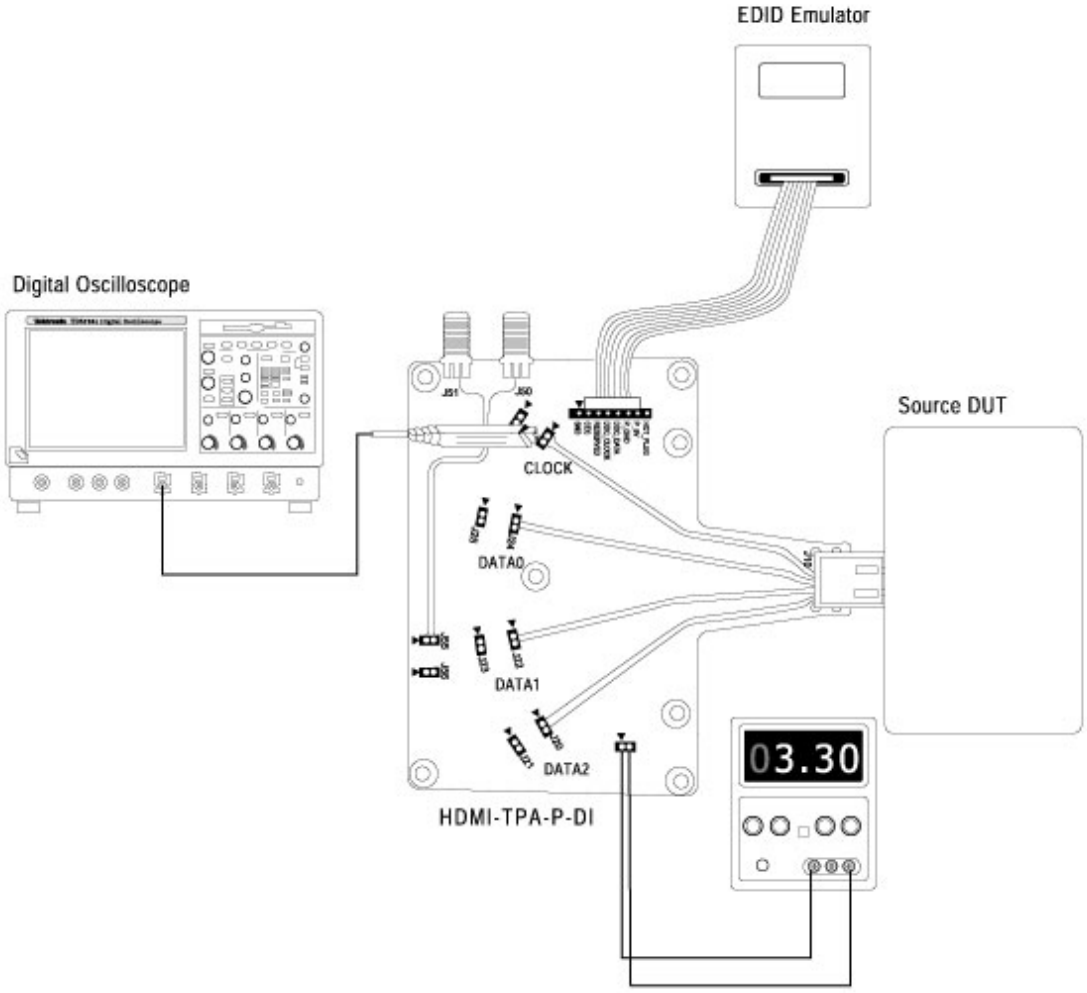
NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

1. Connect the HDMI output of the source DUT to the TPA-P-DI/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.
3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Configure the Source DUT to output a video format with the highest supported pixel clock frequency.
5. Connect a differential probe(s) to TMDS_DATA/CLOCK.
6. If you have selected **Re-calculate Tbit** in the configuration pane, connect the Clock channel to the configured oscilloscope channel by using a second differential probe(s).

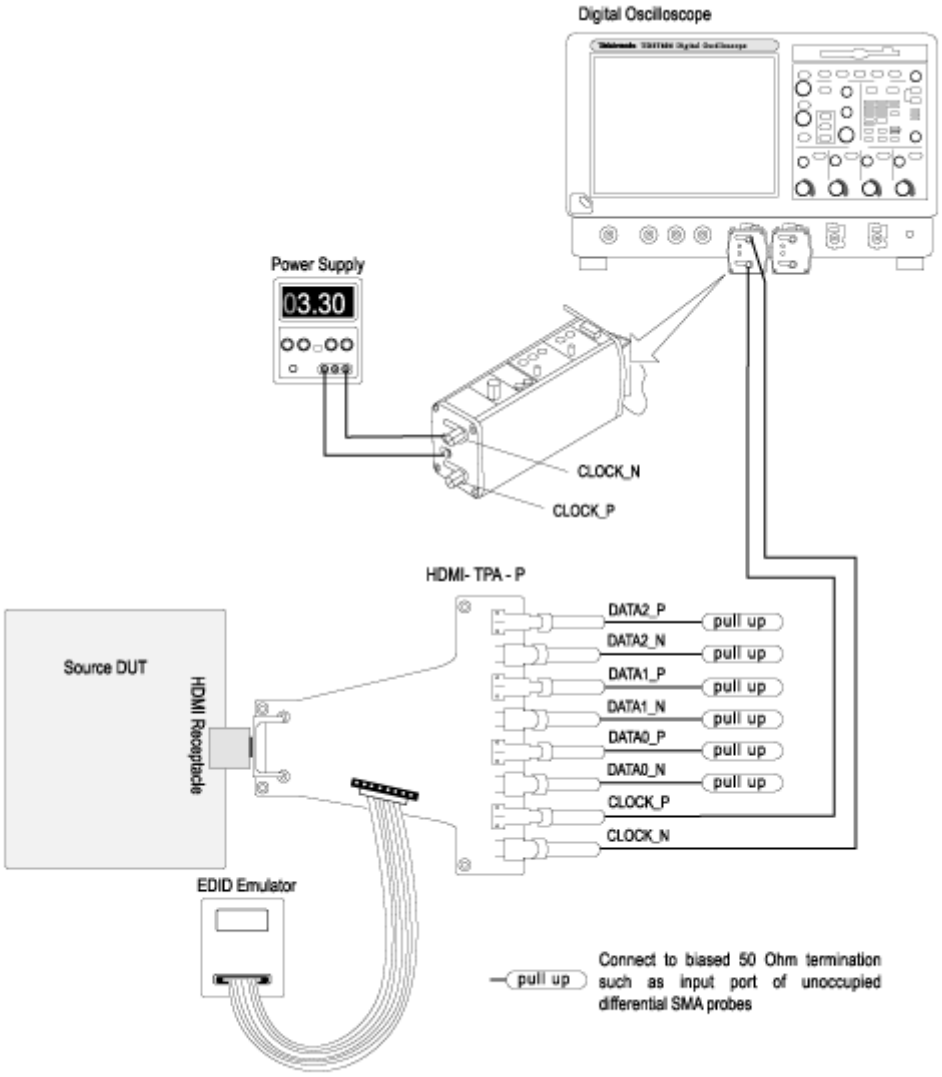
Make Connections for Clock Jitter

On the menu bar, click **Tests > Connect** and make the connection as follows. Refer to EDID Emulator for Source Tests (see page 61) for EDID emulator connections.

Method 1: Connections for Source Clock Jitter



Method 2: Connections for Source Clock Jitter with the Efficere Test Fixture



NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

1. Connect the HDMI output of the source DUT to the TPA-P-DI/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Configure the Source DUT to output a video format with the required supported pixel clock frequency.
5. Connect a TMDS Clock to the configured oscilloscope channel by using a differential probe.

Make Connections for Inter-Pair Skew

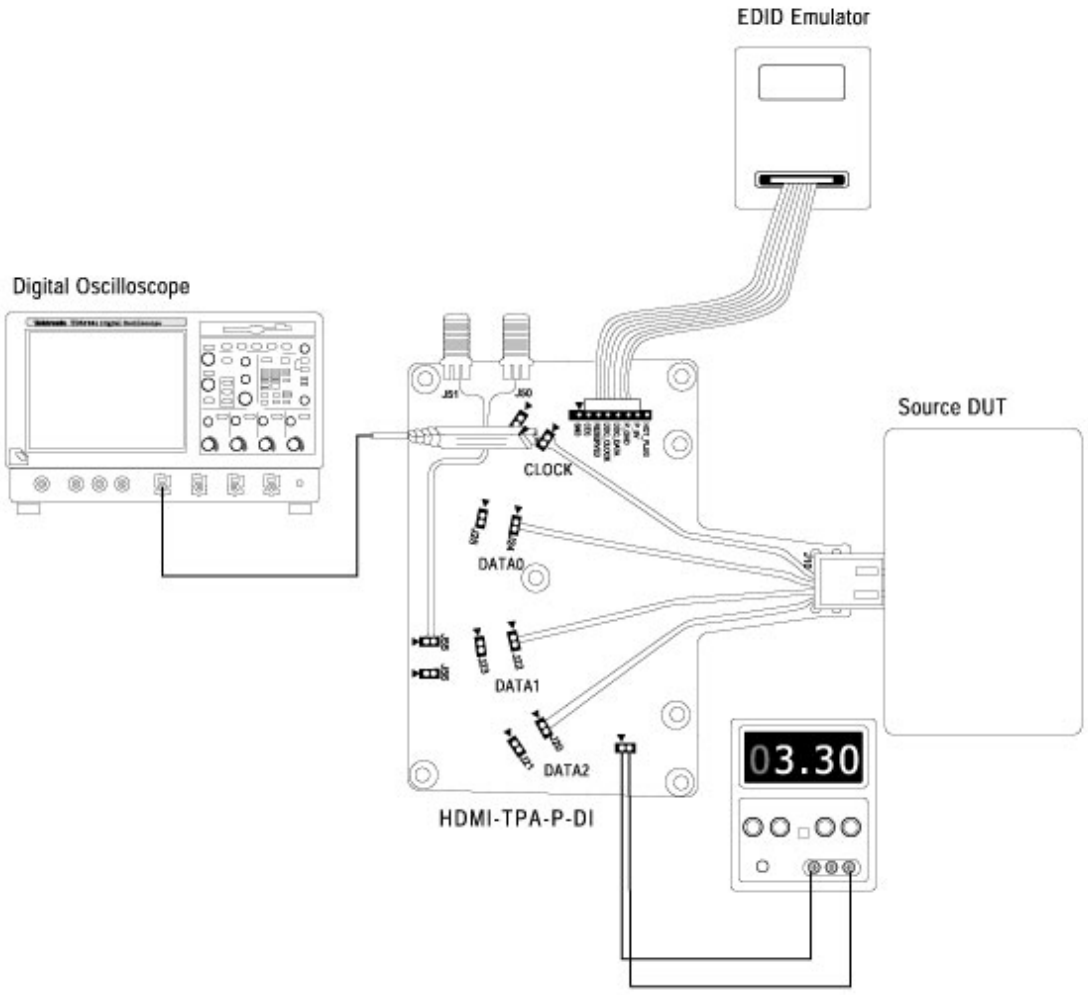
On the menu bar, click **Tests > Connect**. Refer to EDID Emulator for Source Tests (see page 61) for EDID emulator connections.

Setup 1

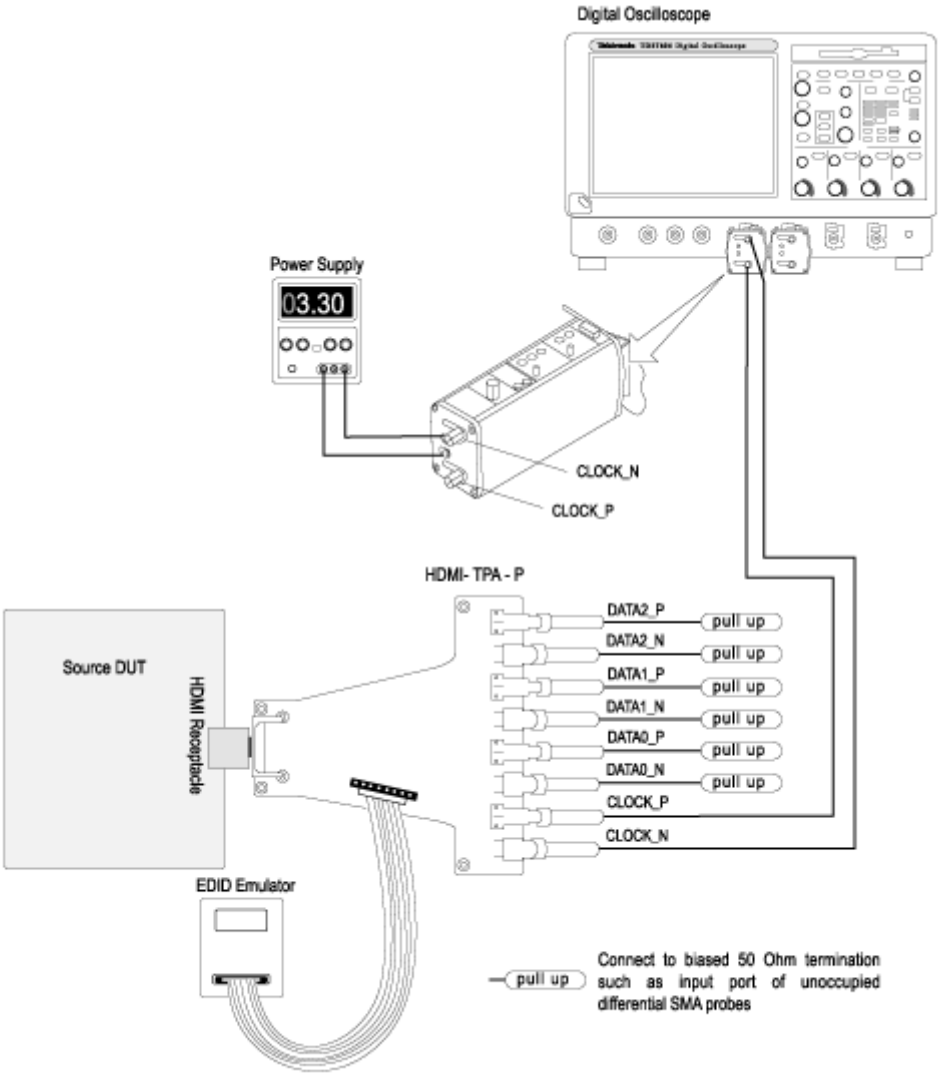
Use this setup if you selected **Re-calculate Tbit** in the configuration pane.

Make the connections as follows:

Method 1: Connections for Inter-Pair Skew (Re-calculate Tbit option selected).



Method 2: Connections for Inter-Pair Skew with the Efficere Test Fixture (Re-calculate Tbit option selected)



NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

1. Connect the HDMI output of the source DUT to the TPA-P-DI/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

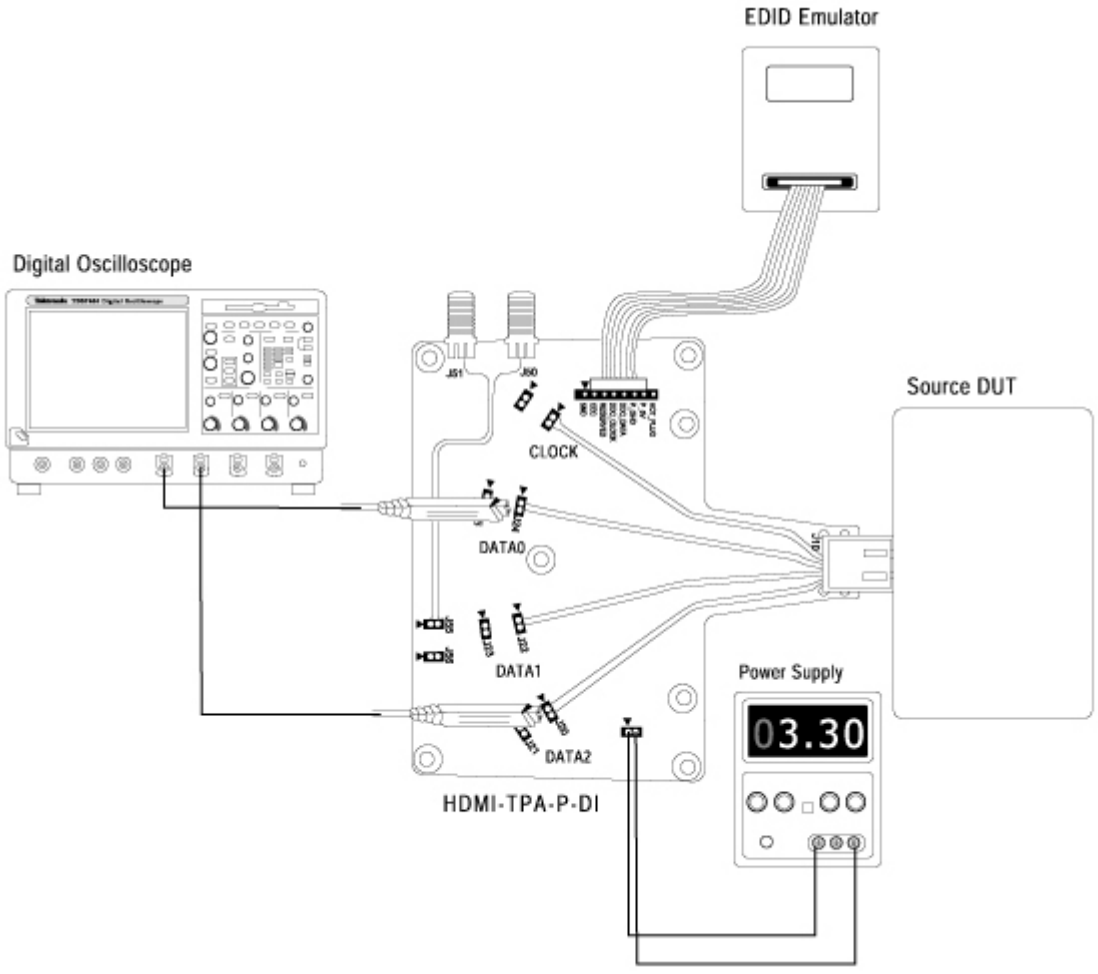
3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Configure the Source DUT to output a video format with the required supported pixel clock frequency.
5. Connect a TMDS Clock to the configured oscilloscope channel by using a differential probe.

Setup 2

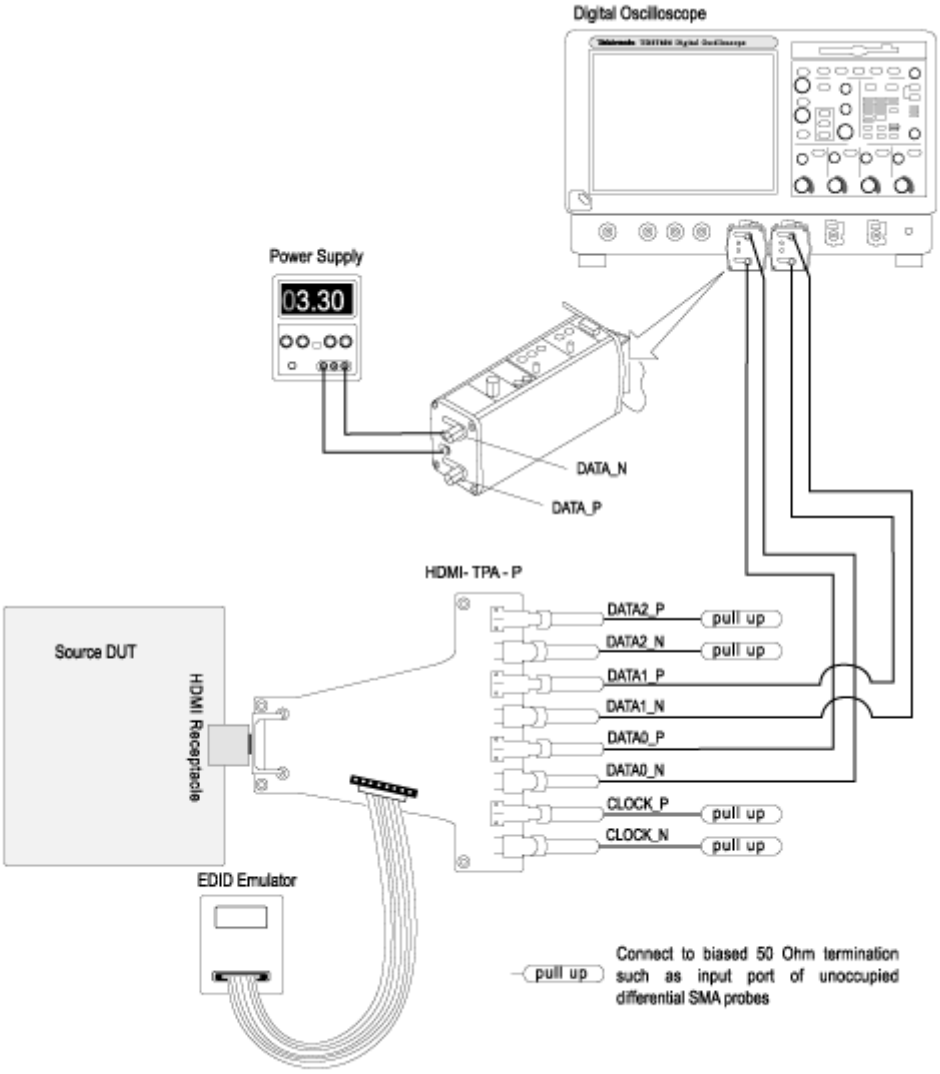
Use this setup if you selected **Existing Tbit** value or if you are calculating the inter-pair skew.

Make the connections as follows:

Method 1: Connections for Source Inter-Pair Skew (Existing Tbit option selected)

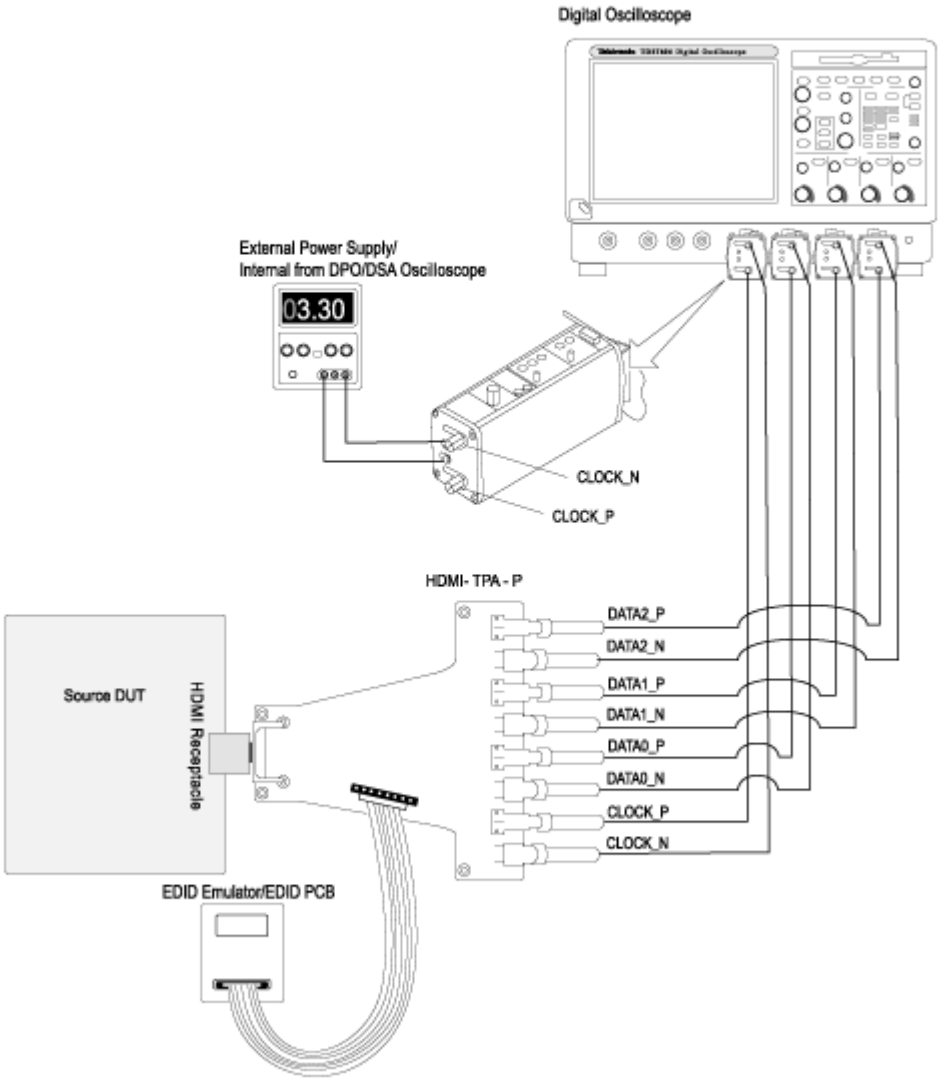


Method 2: Connections for Source Inter-Pair Skew with the Efficere Test Fixture (Existing Tbit option selected)



NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

For 4-Channel



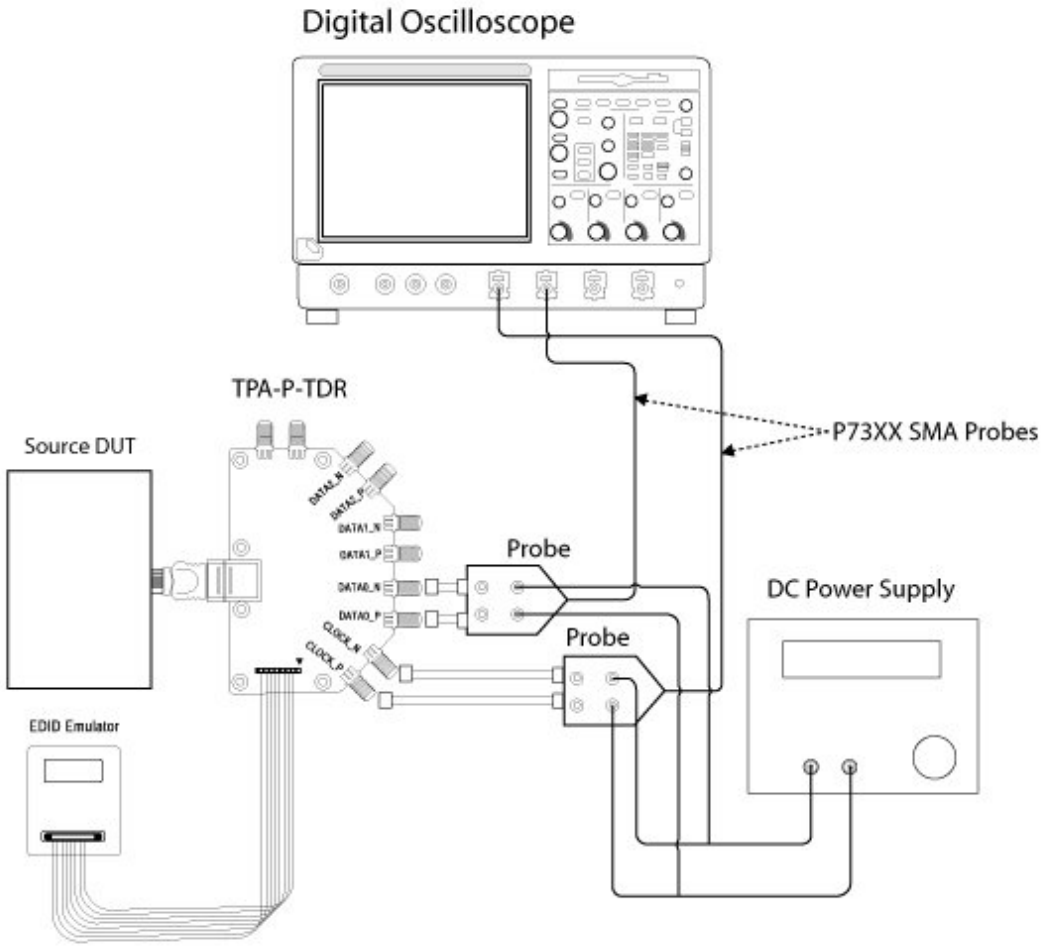
NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

1. Connect the HDMI output of the source DUT to the TPA-P-DI/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.
3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Connect the TMDS_CLOCK to the configured oscilloscope channel by using a differential probe.
5. Connect a TMDS_DATA<X> to the configured oscilloscope channel by using a second differential probe.
6. Connect the TMDS_DATA<Y> pair on which you will conduct the test to the configured oscilloscope channel by using a third differential probe.
7. Connect the TMDS_DATA<Z> pair on which you will conduct the test to the configured oscilloscope channel by using a fourth differential probe.
8. Configure the Source DUT to output the required video format.

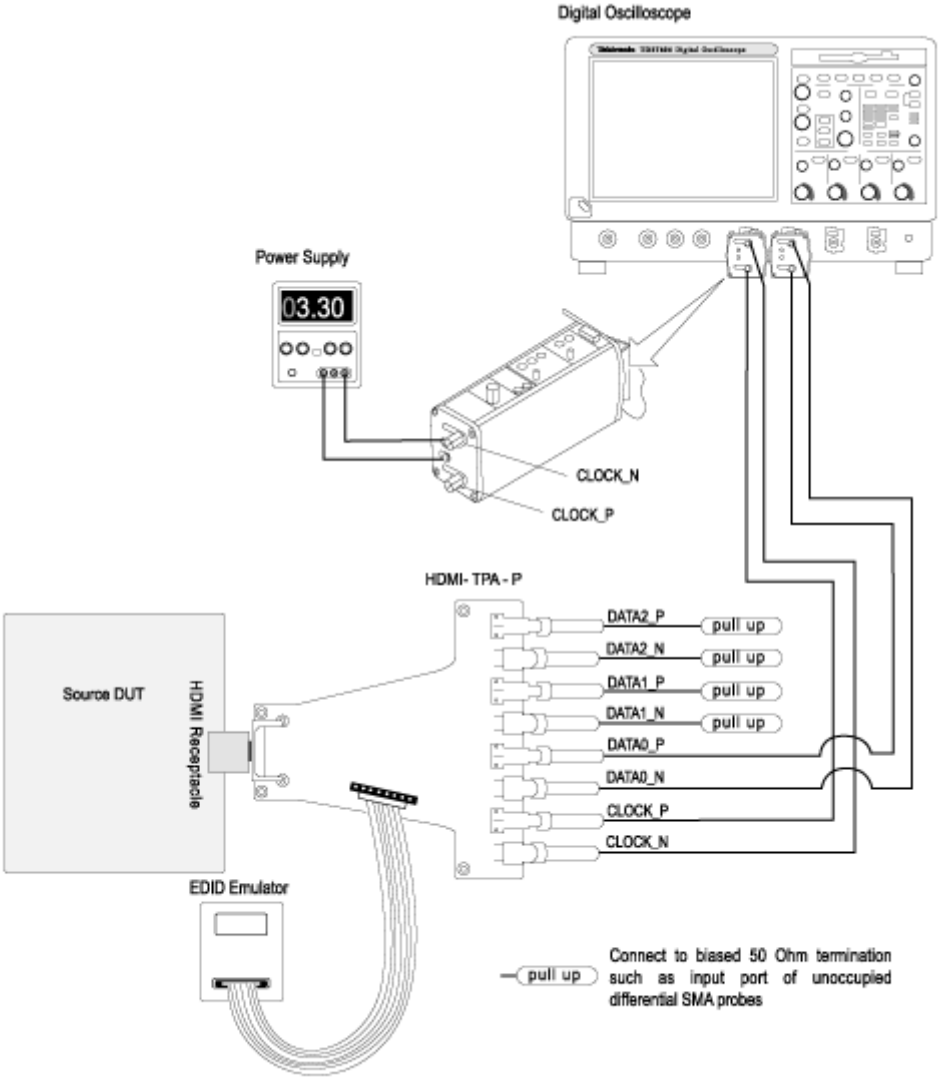
Make Connections for Differential Tests Select All

On the menu bar, click **Tests > Connect** and make the connection as follows. Refer to EDID Emulator for Source Tests (see page 61) for EDID emulator connections.

Method 1: Connections for Source Differential tests (with Select All option)

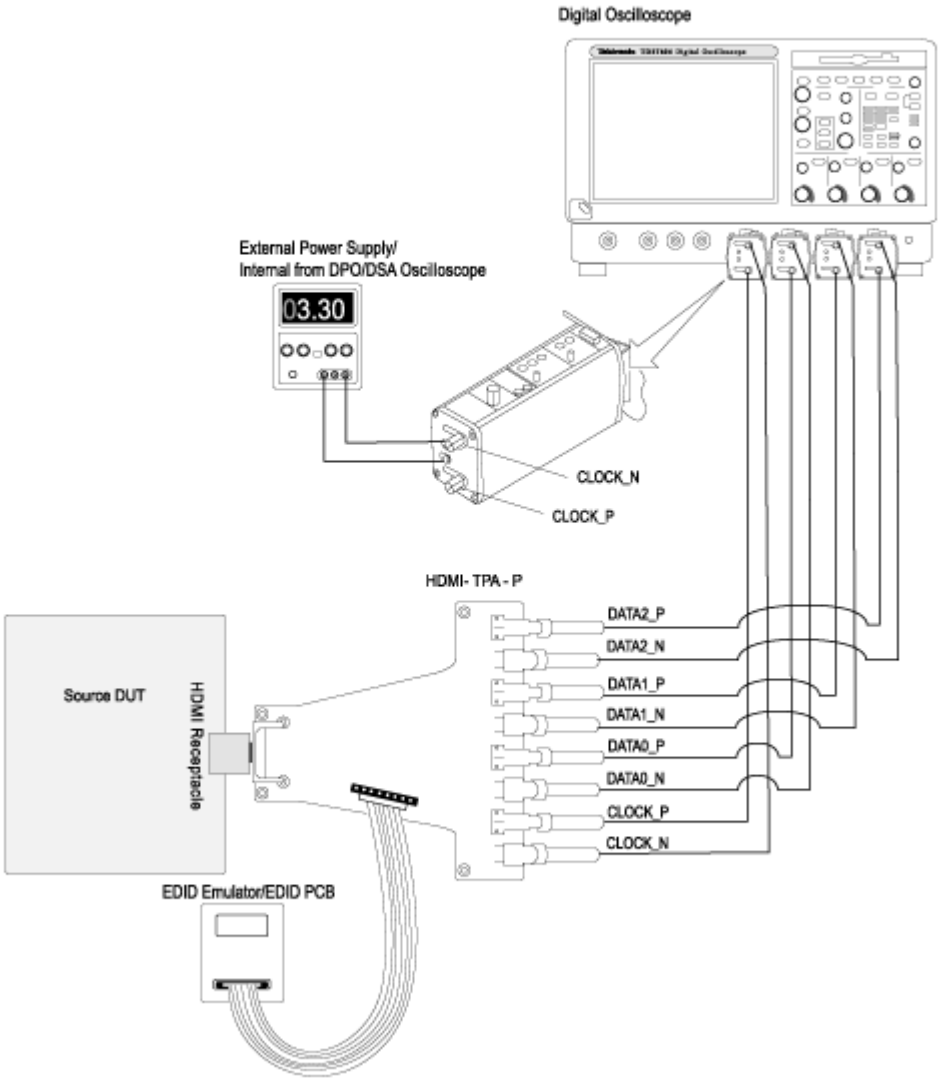


Method 2: Connections for Source Differential tests with the Efficere Test Fixture (Select All option)

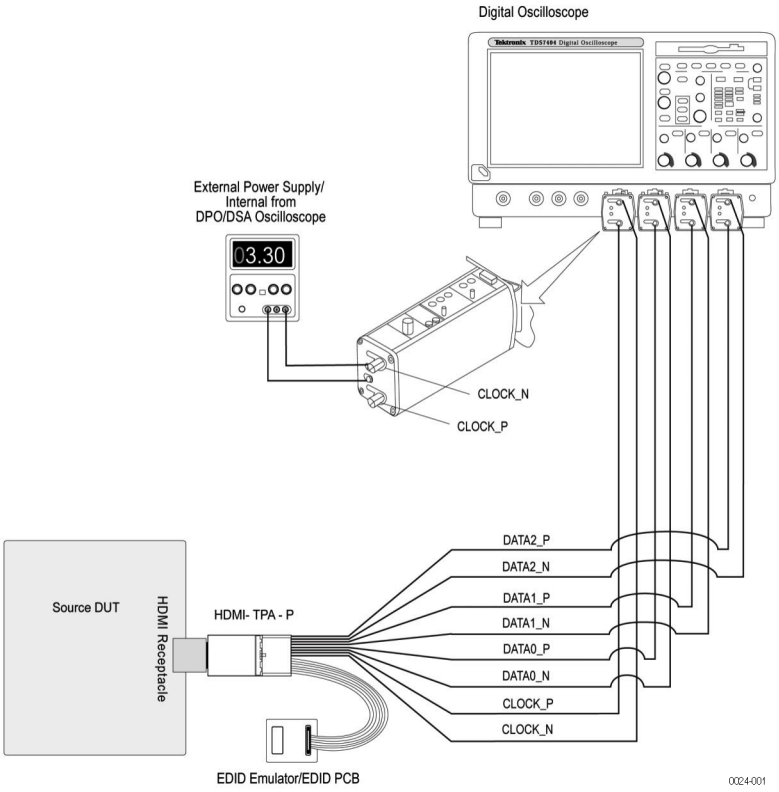


NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

For 4-Channel with the Efficere test fixture



For 4-Channel with the Wilder test fixture



NOTE. *You can also use the EDID PCB instead of the EDID Emulator.*

1. Connect the HDMI output of the source DUT to the TPA-P-DI/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.
3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Connect a TMDS Clock to the configured oscilloscope channel by using a differential probe.
5. Connect the TMDS Data pair(s) on which you will conduct the test to the configured oscilloscope channel by using a second differential probe(s).
6. Configure the Source DUT to output the required video format.

Make Connections for Source Intra-Pair Skew

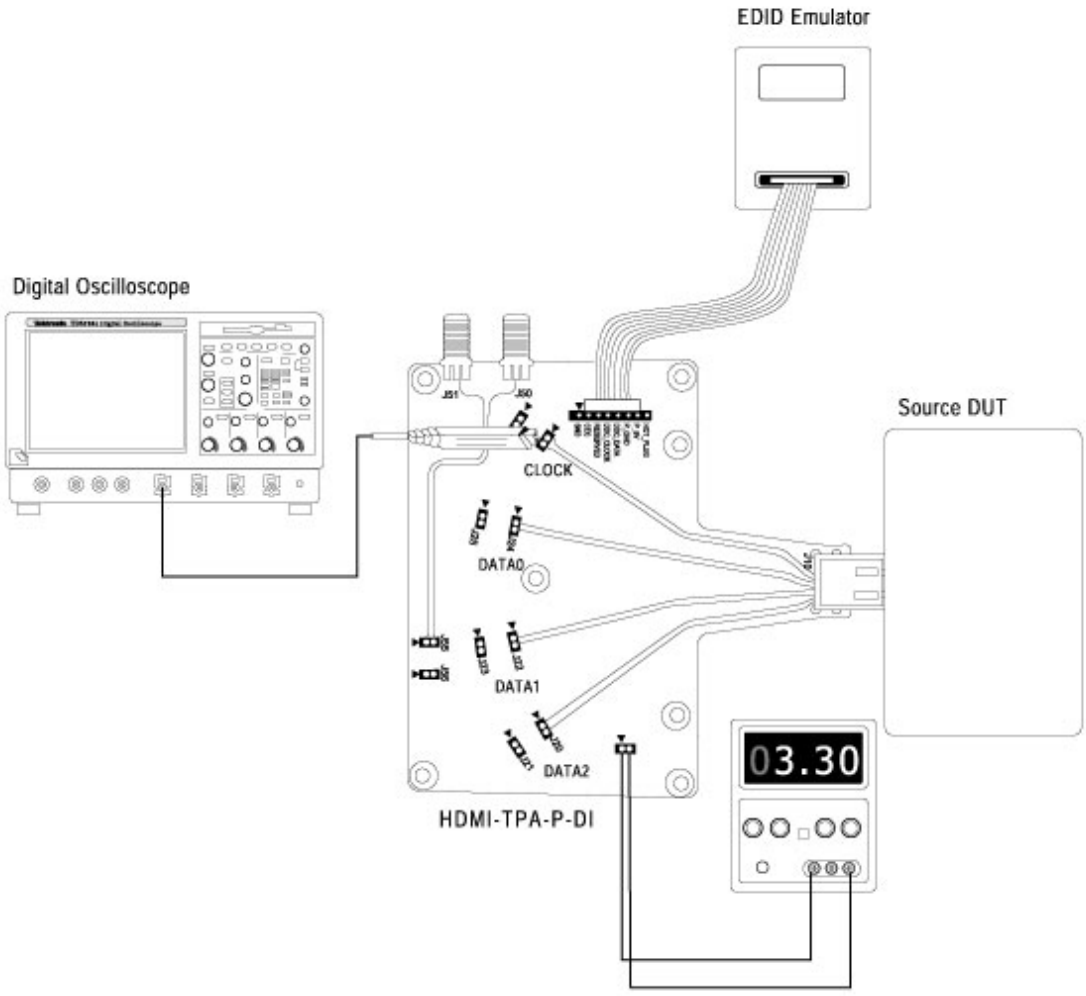
On the menu bar, click **Tests > Connect**. Refer to EDID Emulator for Source Tests (see page 61) for EDID emulator connections.

Setup 1

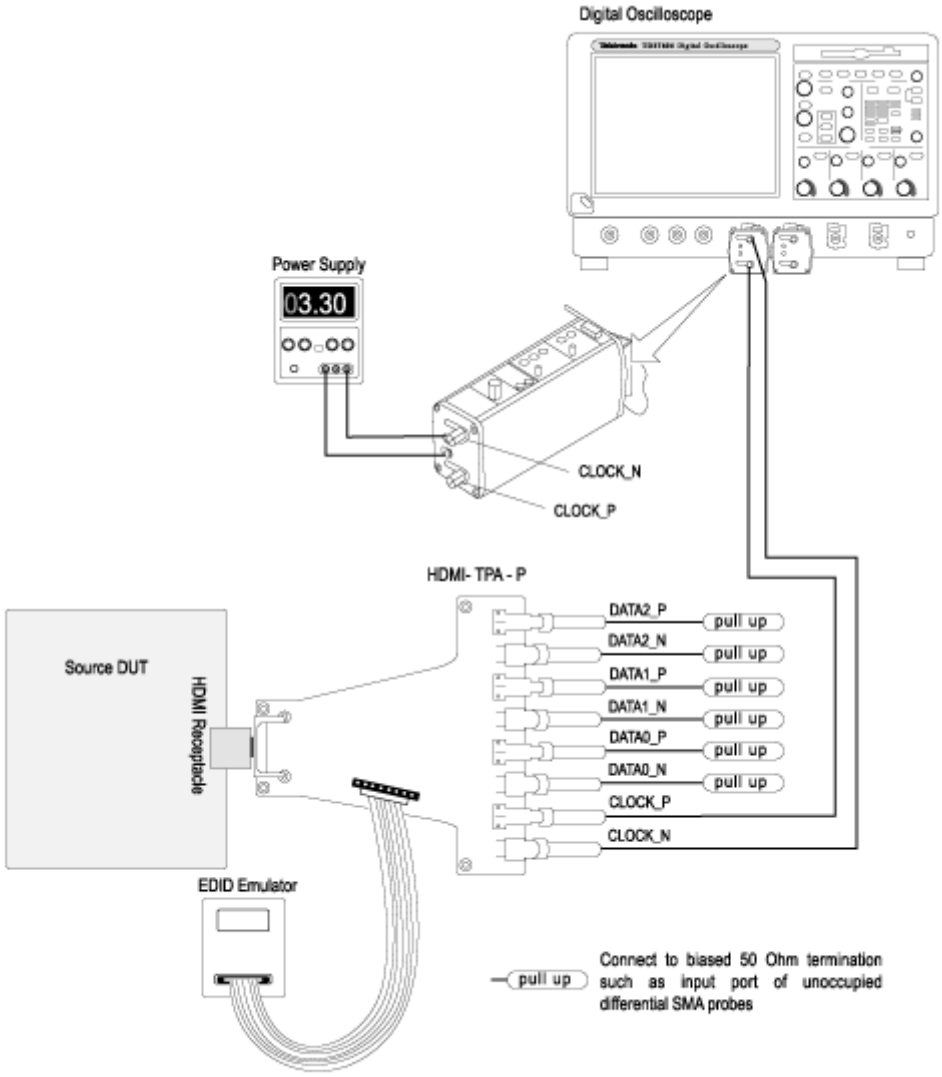
Use this setup if you have selected **Re-calculate Tbit** in the configuration pane.

Make the connections as follows:

Method 1: Connections for Source Intra-Pair Skew test (Re-calculate Tbit option selected).



Method 2: Connections for Source Intra-Pair Skew test with the Efficere Test Fixture (Re-calculate Tbit option selected).



NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

1. Connect the HDMI output of the source DUT to the TPA-P-DI/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

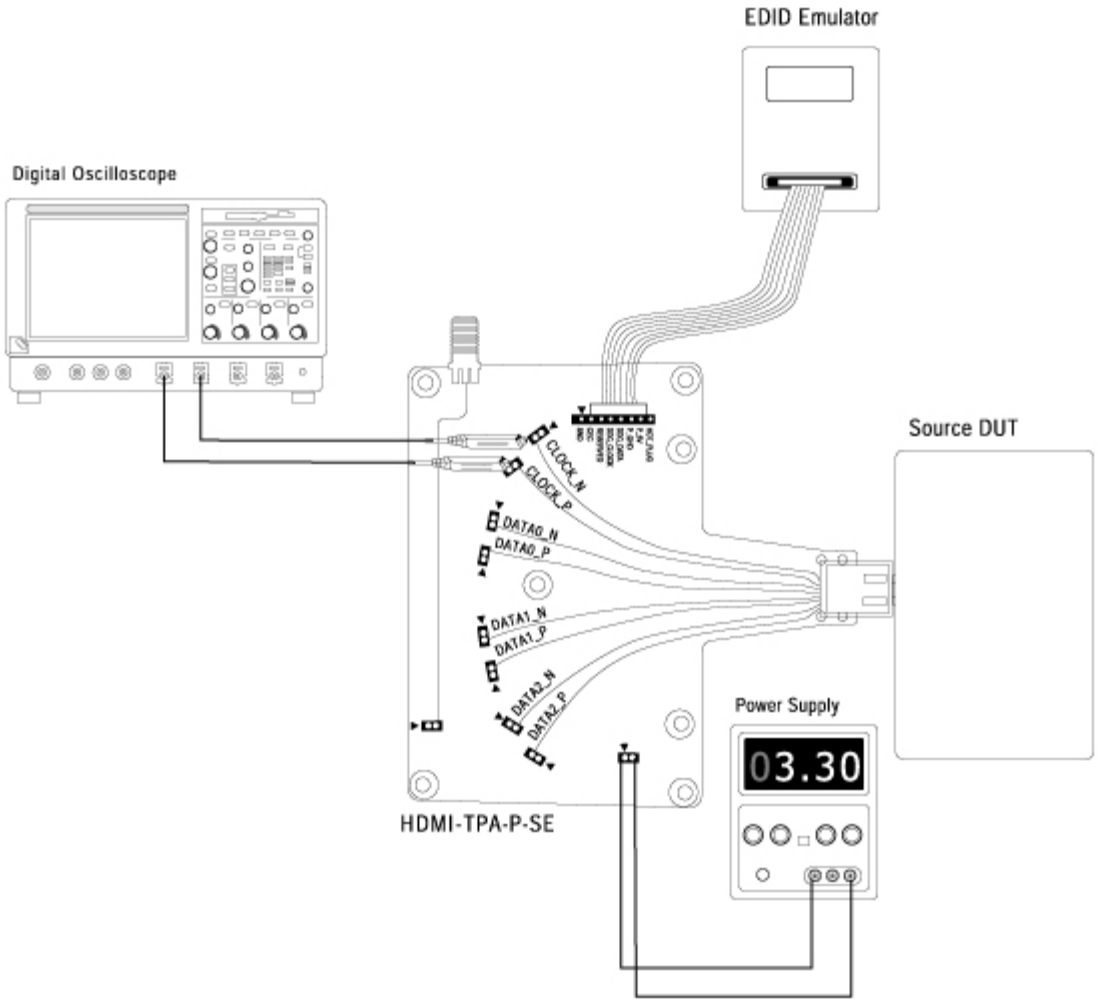
3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Configure the Source DUT to output a video format with the required supported pixel clock frequency.
5. Connect a TMDS Clock to the configured oscilloscope channel by using a differential probe.

Setup 2

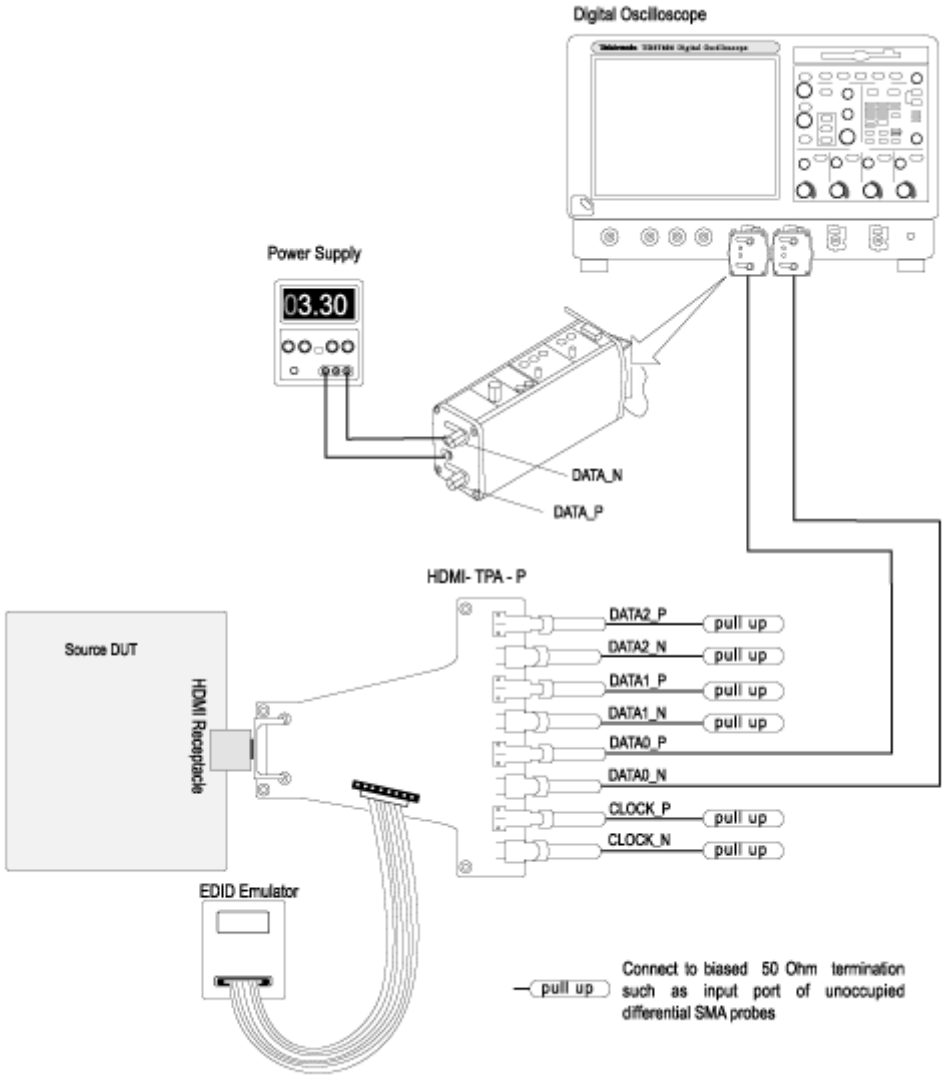
Use this setup if you have selected the **Existing Tbit** value or if you are calculating the intra-pair skew.

Make the connections as follows:

Method 1: Connections for Source Intra-Pair Skew test (Existing Tbit option selected).



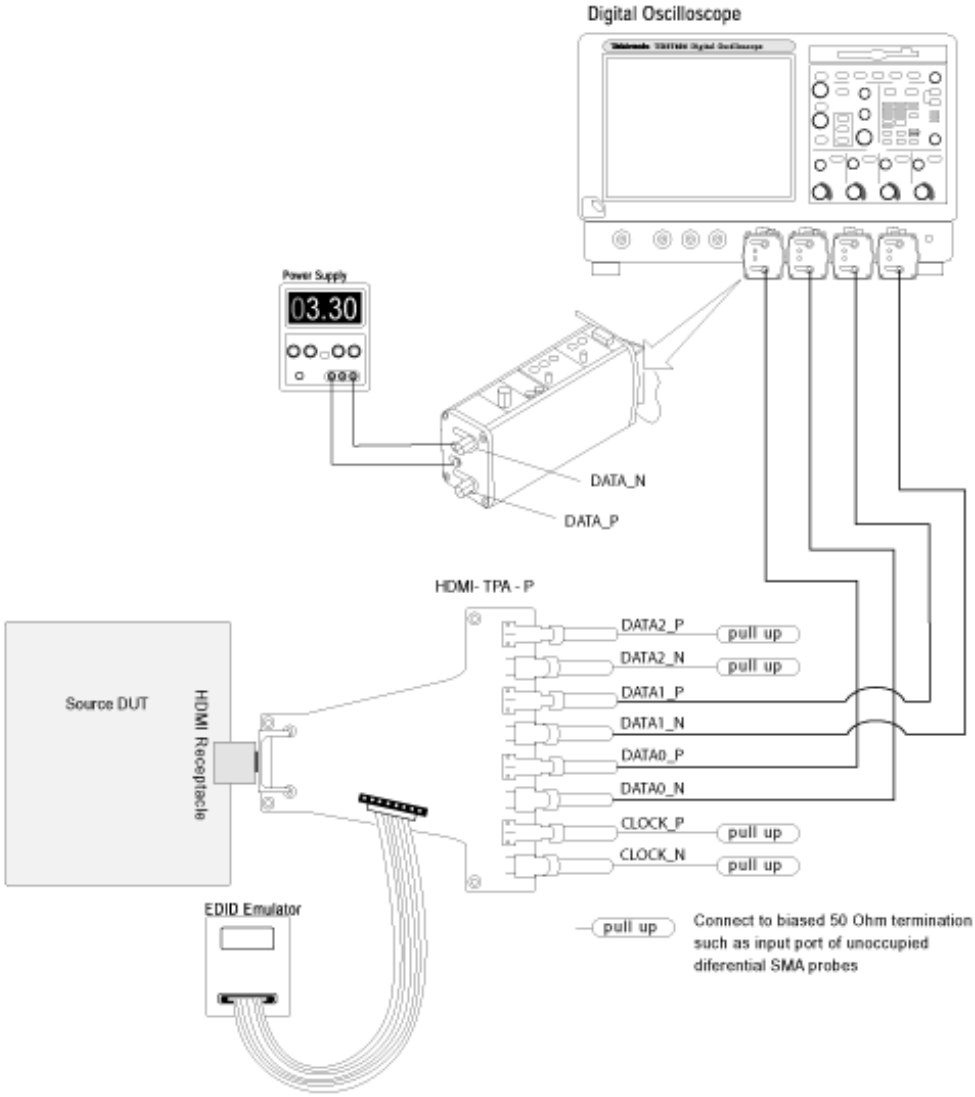
Method 2: Connections for Source Intra-Pair Skew test with the Efficere Test Fixture (Existing Tbit option selected).



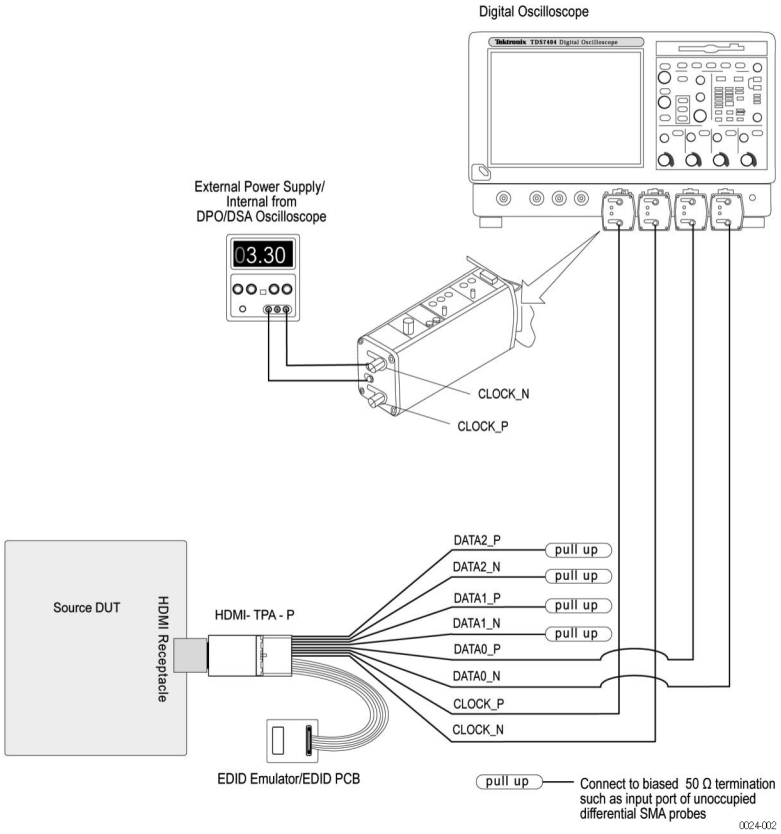
NOTE. *For single-ended tests, the default setup is that the –ve input of the probe is configured to be kept open. To perform the single-ended tests with the -ve input terminated with a 50 ohm terminator, ensure that the single-ended (With 50 ohm term) option is selected in the* *Preferences (see page 24)* *menu.*

NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

For 4-Channel with Efficere test fixture.



For 4-Channel with Wilder test fixture.



NOTE. *For single-ended tests, the default setup is that the –ve input of the probe is configured to be kept open. To perform the single-ended tests with the -ve input terminated with a 50 ohm terminator, ensure that the single-ended (With 50 ohm term) option is selected in the* *Preferences (see page 24)* *menu.*

NOTE. *You can also use the EDID PCB instead of the EDID Emulator.*

1. Connect the HDMI output of the source DUT to the TPA-P-SE/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.
3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Connect the first single-ended probe to TMDS_DATA<X>+/TMDS_CLOCK+.
5. Connect the second single-ended probe to TMDS_DATA<X>– /TMDS_CLOCK–.

6. Connect the third single-ended probe to TMDS_DATA<X>+/TMDS_CLOCK+.
7. Connect the fourth single-ended probe to TMDS_DATA<X>– /TMDS_CLOCK–.
8. Configure the Source DUT to output a video format with the required supported pixel clock frequency.

Make Connections for Low Amplitude +

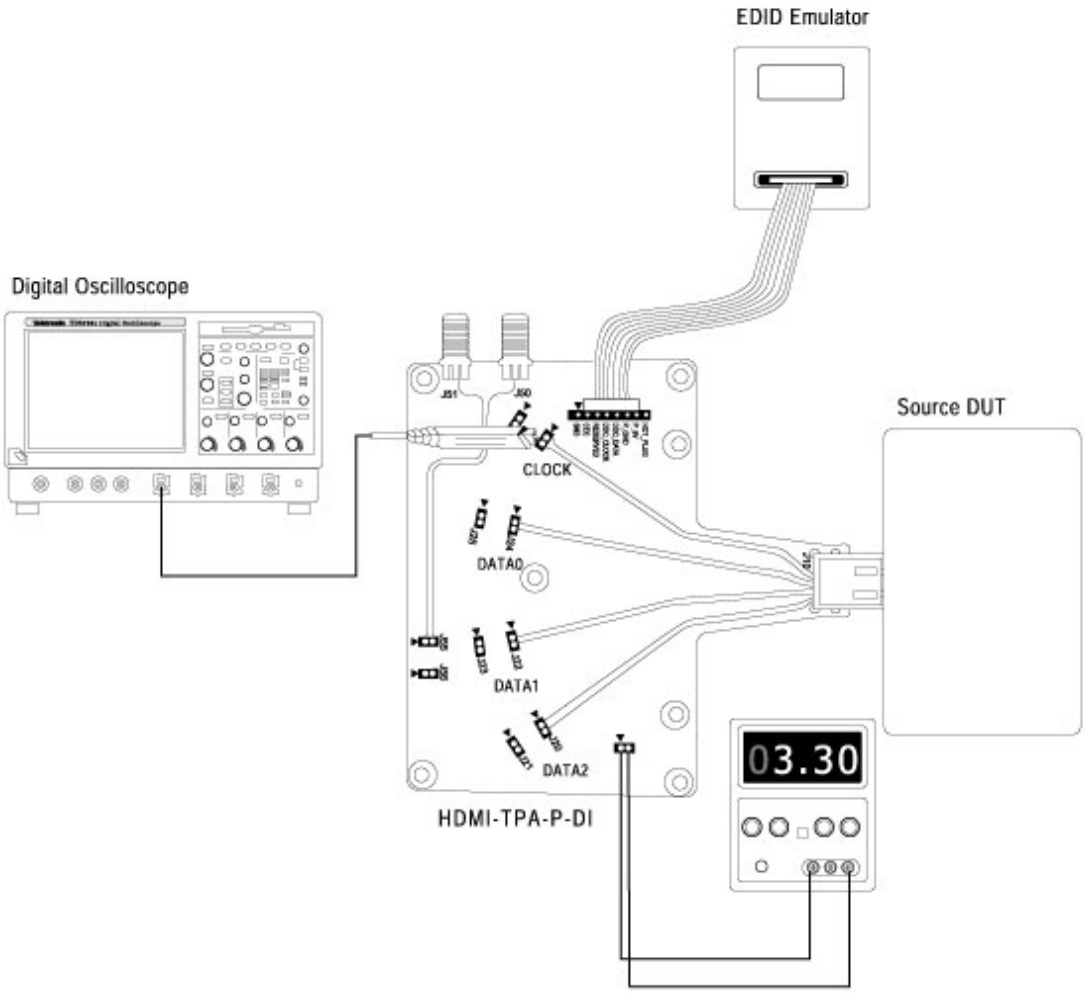
On the menu bar, click **Tests > Connect**. Refer to EDID Emulator for Source Tests (see page 61) for EDID emulator connections.

Setup 1

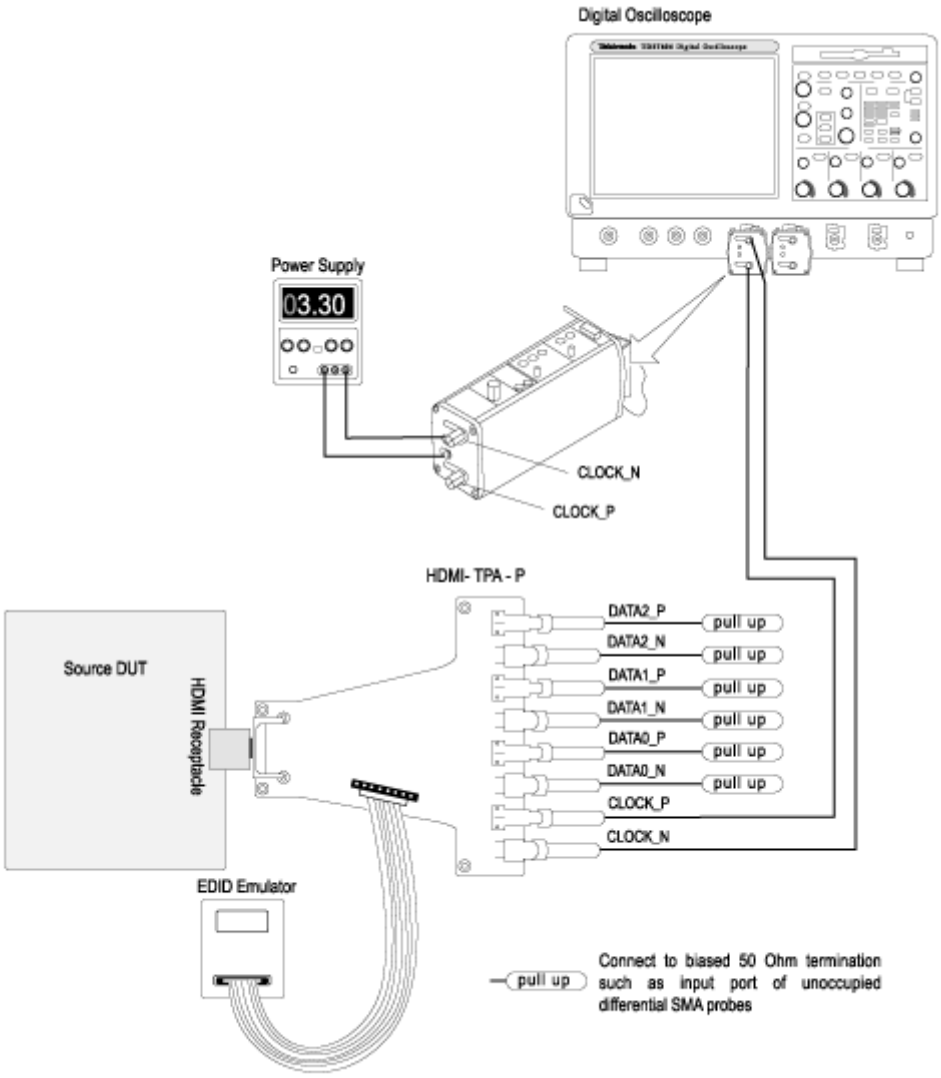
Use this setup if you have selected **Re-calculate Tbit** in the configuration pane.

Make the connections as follows:

Method 1: Connections for Low Amplitude + (Re-calculate Tbit option selected).



Method 2: Connections for Low Amplitude + with the Efficere Test Fixture (Re-calculate Tbit option selected).



NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

1. Connect the HDMI output of the source DUT to the TPA-P-DI/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

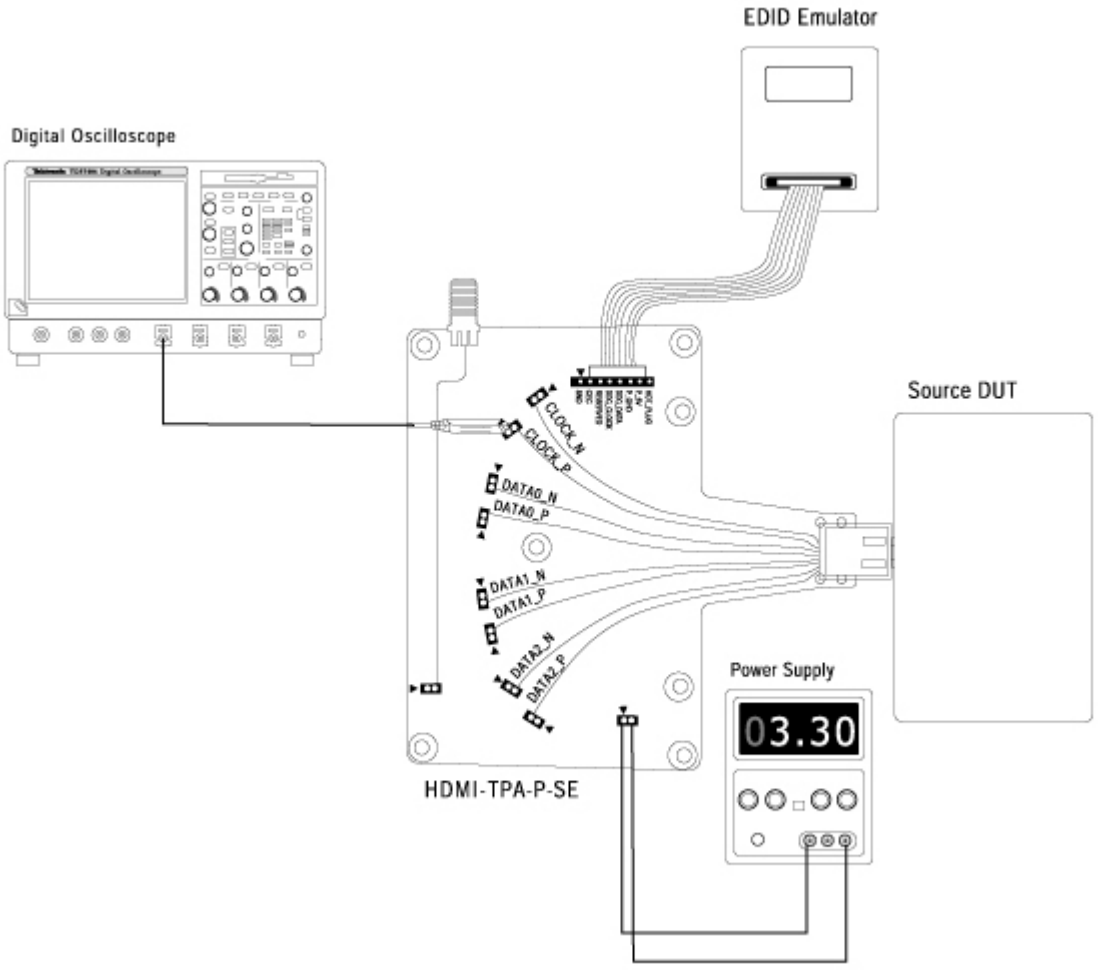
3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Configure the Source DUT to output a video format with the required supported pixel clock frequency.
5. Connect a TMDS Clock to the configured oscilloscope channel by using a differential probe.

Setup 2

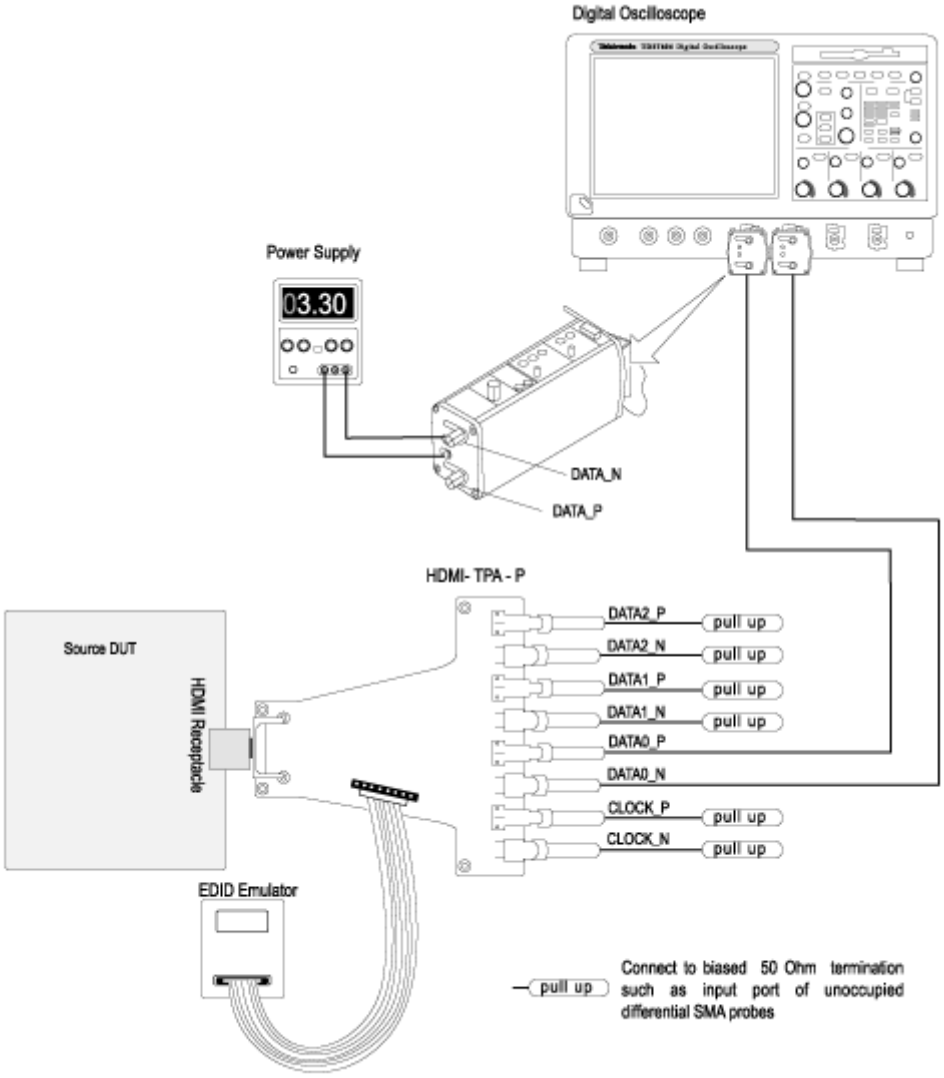
Use this setup if you have selected **Existing Tbit** value or if you are calculating low amplitude.

Make the connections as follows:

Method 1: Connections for Low Amplitude + (Existing Tbit option selected).



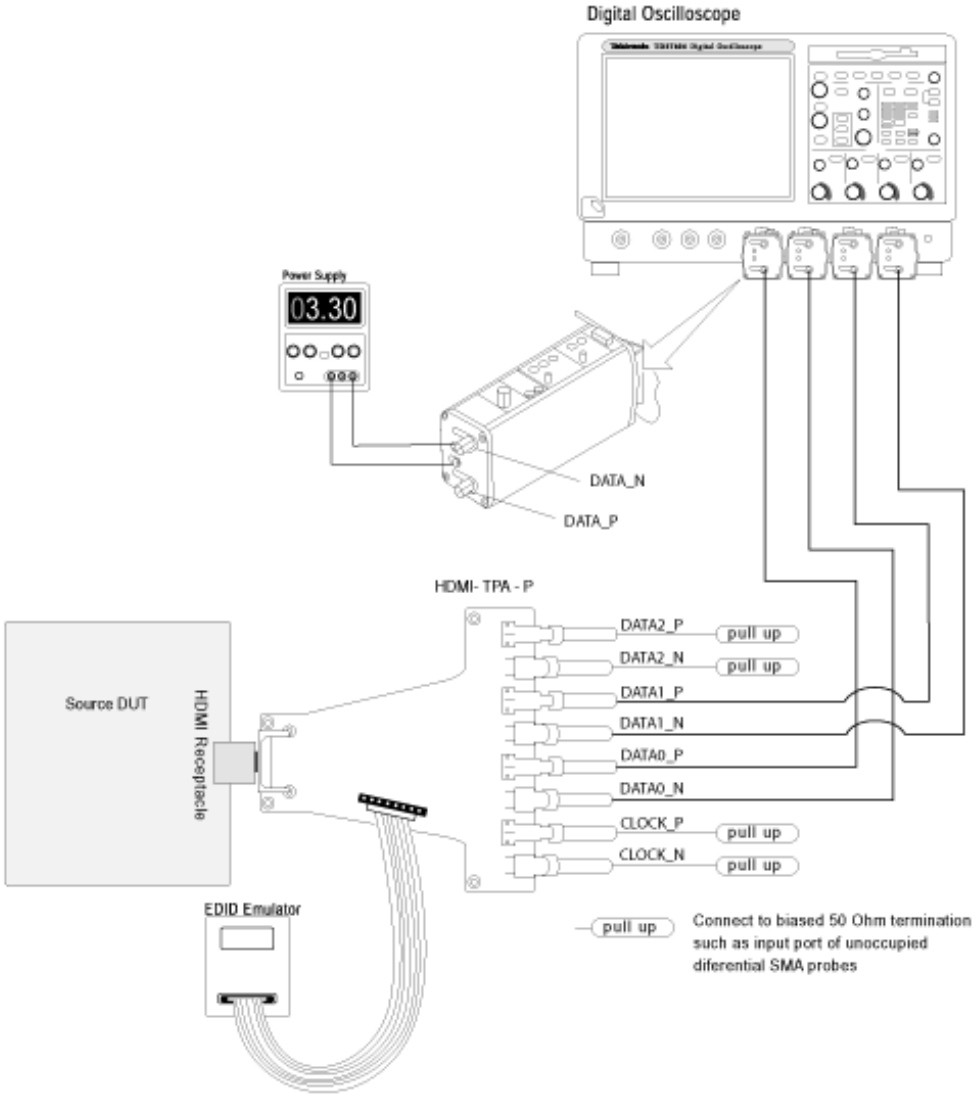
Method 2: Connections for Low Amplitude + with the Efficere Test Fixture (Existing Tbit option selected).



NOTE. *For single-ended tests, the default setup is that the –ve input of the probe is configured to be kept open. To perform the single-ended tests with the -ve input terminated with a 50 ohm terminator, ensure that the single-ended (With 50 ohm term) option is selected in the* *Preferences (see page 24)* *menu.*

NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

For 4-Channel.



NOTE. *For single-ended tests, the default setup is that the –ve input of the probe is configured to be kept open. To perform the single-ended tests with the -ve input terminated with a 50 ohm terminator, ensure that the single-ended (With 50 ohm term) option is selected in the* *Preferences (see page 24)* *menu.*

NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

NOTE. *Connecting Ch2 and Ch4 is not a must for this measurement.*

1. Connect the HDMI output of the source DUT to the TPA-P-SE/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.
3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Connect the first single-ended probe to TMDS_DATA<X>+/TMDS_CLOCK+.
5. Connect the second single-ended probe to TMDS_DATA<X>+/TMDS_CLOCK+.
6. Configure the Source DUT to output a video format with the required supported pixel clock frequency.

Make Connections for Low Amplitude -

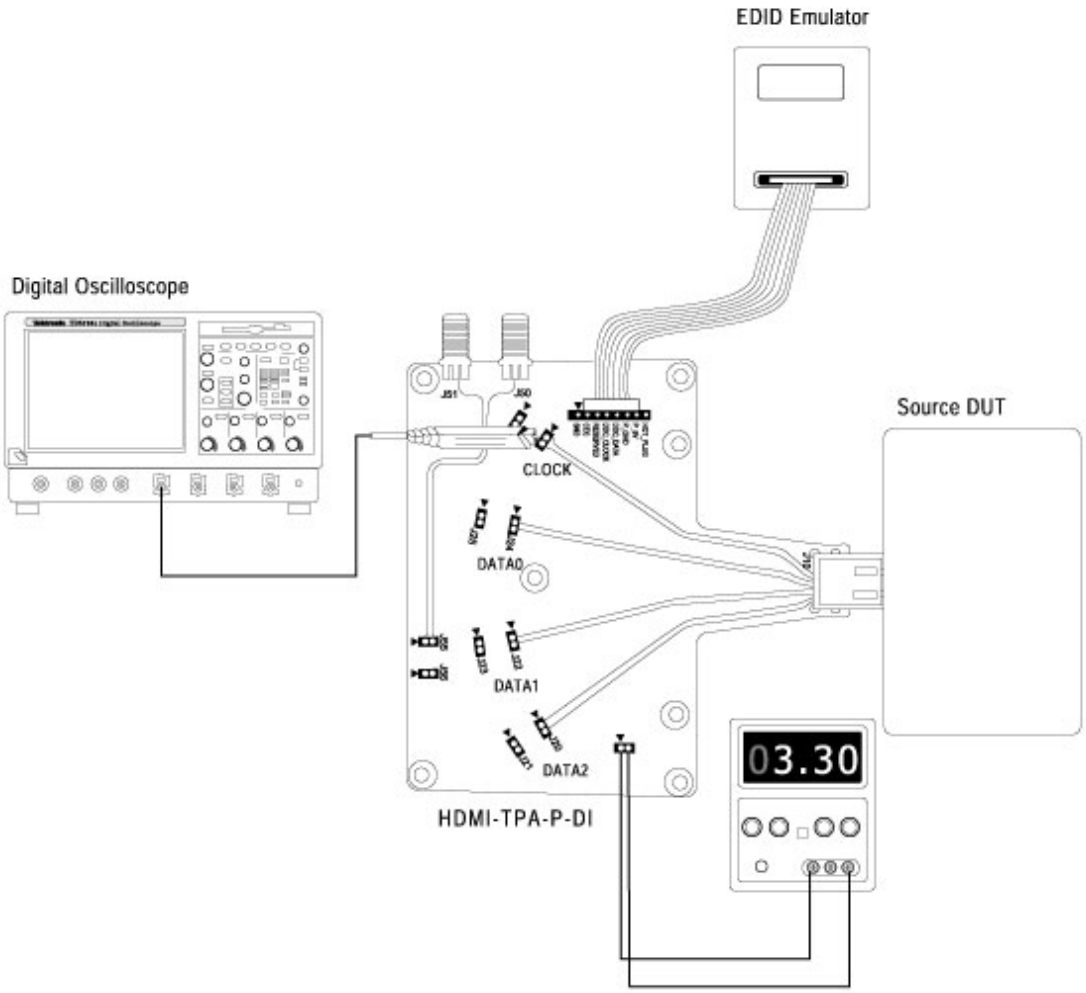
On the menu bar, click **Tests > Connect**. Refer to EDID Emulator for Source Tests (see page 61) for EDID emulator connections.

Setup 1

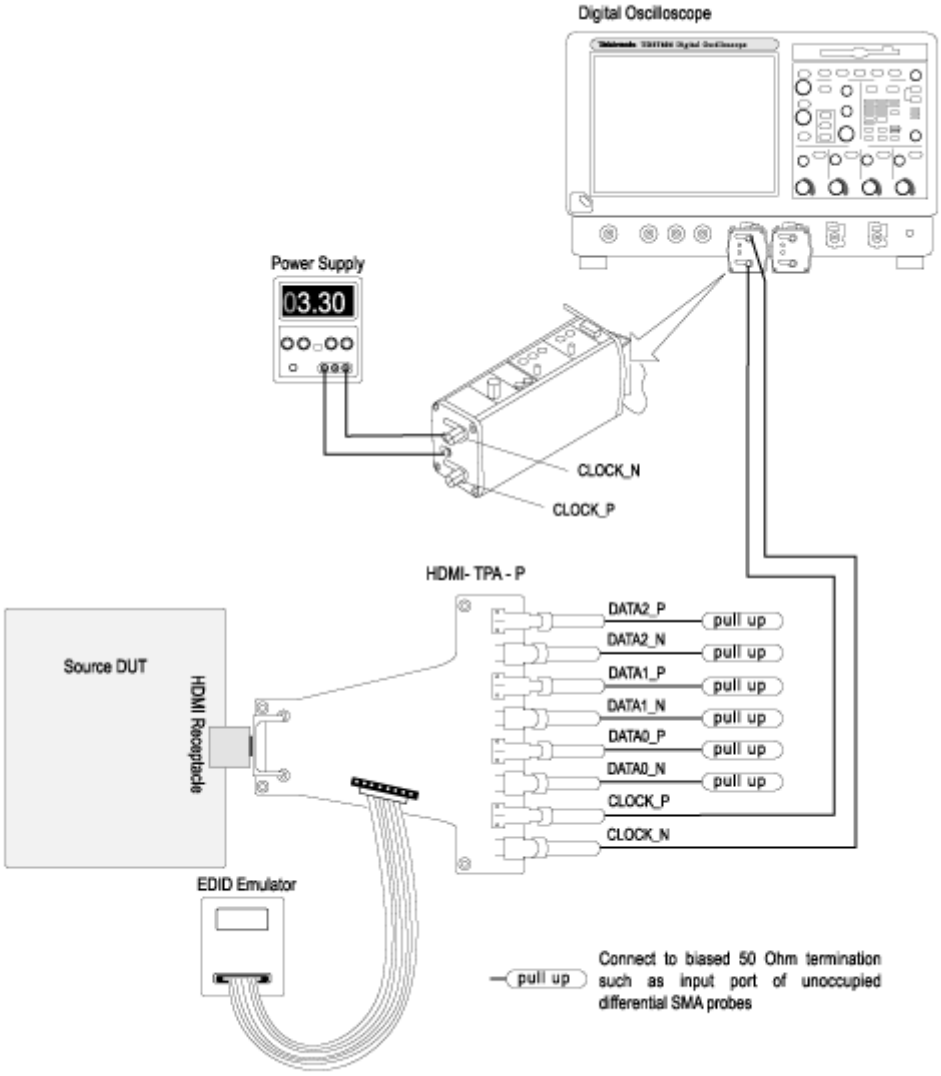
Use this setup if you have selected **Re-calculate Tbit** in the configuration pane.

Make the connections as follows:

Method 1: Connections for Low Amplitude – (Re-calculate Tbit option selected).



Method 2: Connections for Low Amplitude – with the Efficere Test Fixture (Re-calculate Tbit option selected).



NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

1. Connect the HDMI output of the source DUT to the TPA-P-DI/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 3.3 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

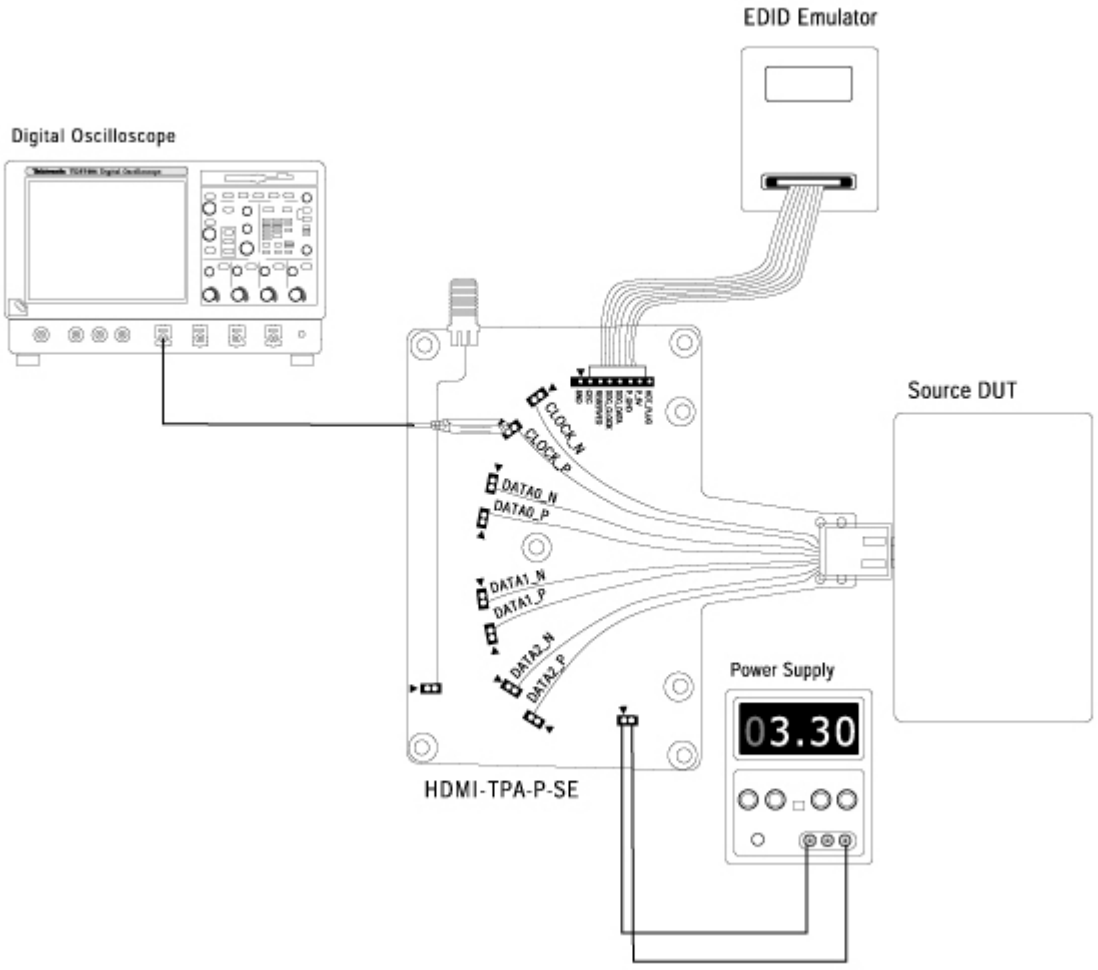
3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Configure the Source DUT to output a video format with the required supported pixel clock frequency.
5. Connect a TMDS Clock to the configured oscilloscope channel by using a differential probe.

Setup 2

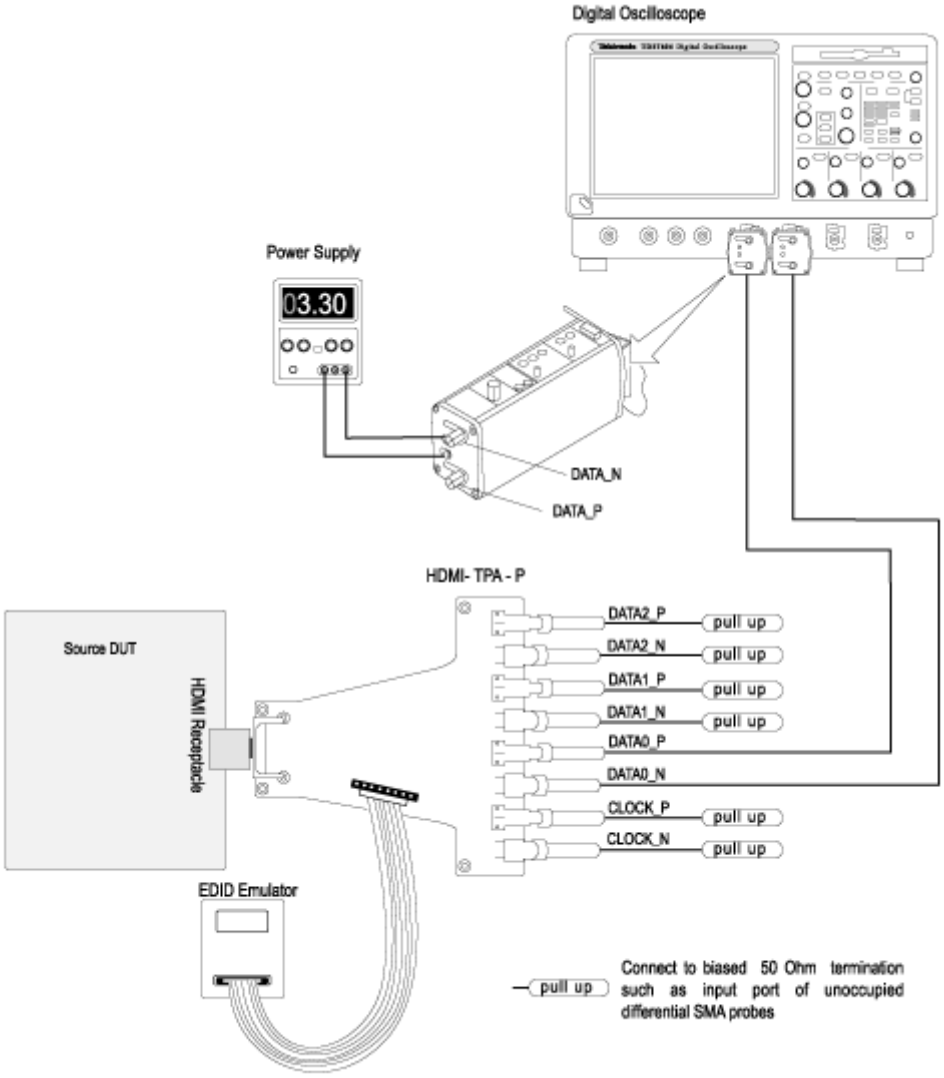
Use this setup if you have selected **Existing Tbit** value or if you are calculating low amplitude.

Make the connections as follows:

Method 1: Connections for Low Amplitude - (Existing Tbit option selected).



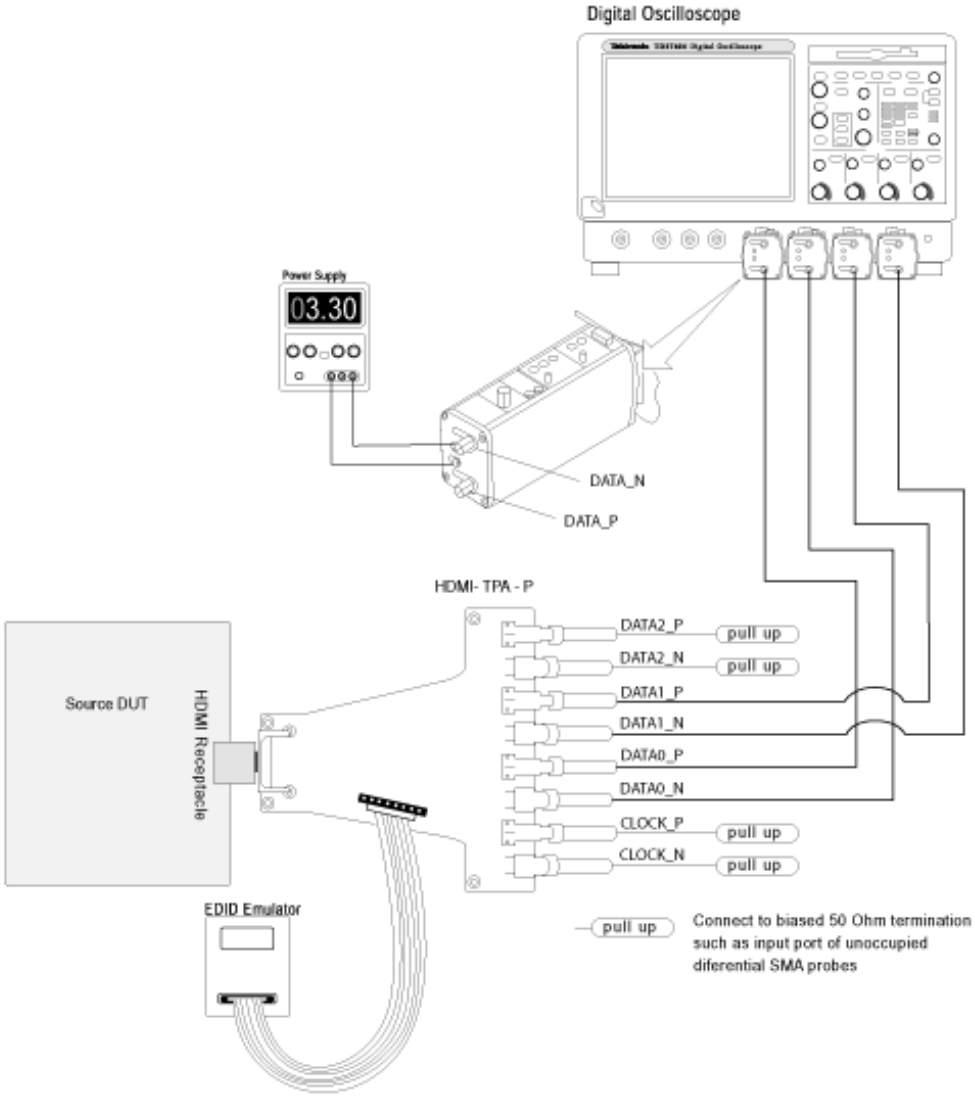
Method 2: Connections for Low Amplitude - with the Efficere Test Fixture (Existing Tbit option selected).



NOTE. *For single-ended tests, the default setup is that the –ve input of the probe is configured to be kept open. To perform the single-ended tests with the -ve input terminated with a 50 ohm terminator, ensure that the single-ended (With 50 ohm term) option is selected in the* *Preferences (see page 24)* *menu.*

NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

For 4-Channel.



NOTE. *For single-ended tests, the default setup is that the –ve input of the probe is configured to be kept open. To perform the single-ended tests with the -ve input terminated with a 50 ohm terminator, ensure that the single-ended (With 50 ohm term) option is selected in the* *Preferences (see page 24)* *menu.*

NOTE. *You can also use the EDID PCB instead of the EDID Emulator and Wilder test fixture instead of Efficere test fixture.*

NOTE. *Connecting Ch1 and Ch3 is not a must for this measurement.*

1. Connect the HDMI output of the source DUT to the TPA-P-SE/ET-TPA-P adapter.
2. Connect a power supply to the TPA adapter and set the power supply to 0 V. For DPO/DSA/MSO70000 series oscilloscopes, this is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.
3. Connect the EDID emulator to the TPA adapter and set the emulator for the required resolution (refer to the EDID emulator user manual).
4. Connect the first single-ended probe to TMDS_DATA<X>+/TMDS_CLOCK+.
5. Connect the second single-ended probe to TMDS_DATA<X>–/TMDS_CLOCK–.
6. Configure the Source DUT to output a video format with the required supported pixel clock frequency.

Make Connections for Min/Max-Diff Swing Tolerance

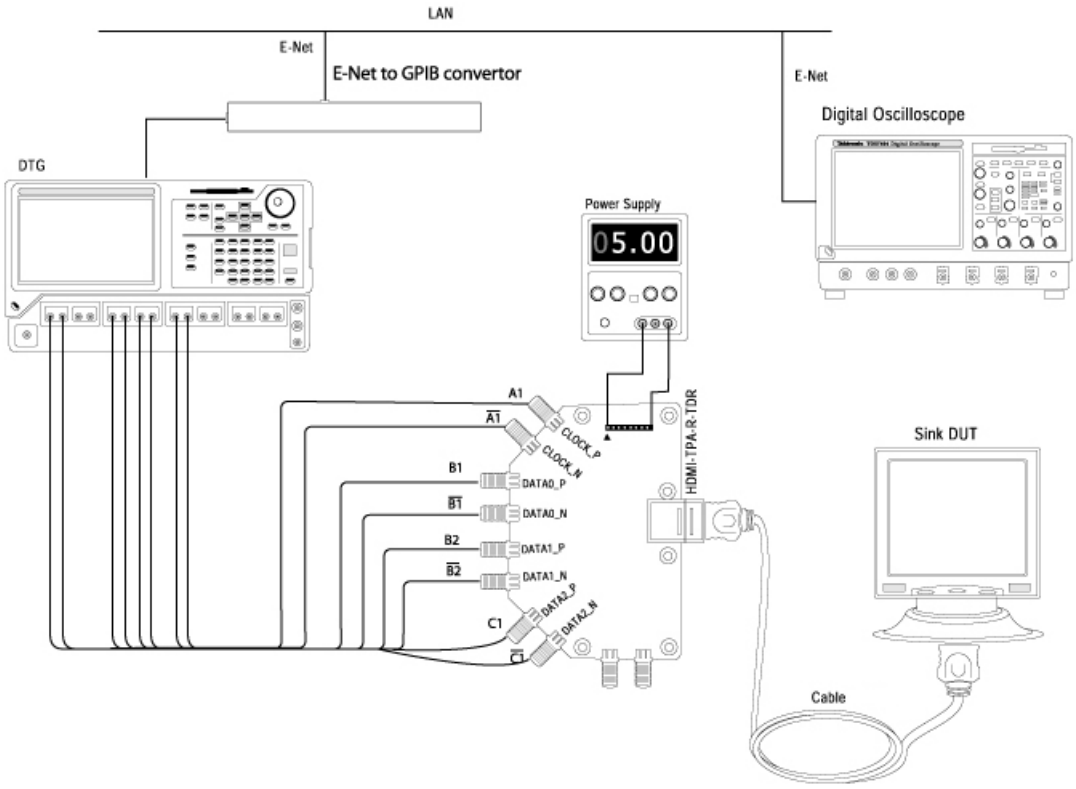
NOTE. *For all the HDMI 1.2 test fixture connections, connect a TTC filter between the DTG and the test fixture.*

On the menu bar, click **Tests > Connect**.

Method 1: Using HDMI 1.2 test fixtures

Setup 1. To find the minimum swing voltage of the Sink DUT

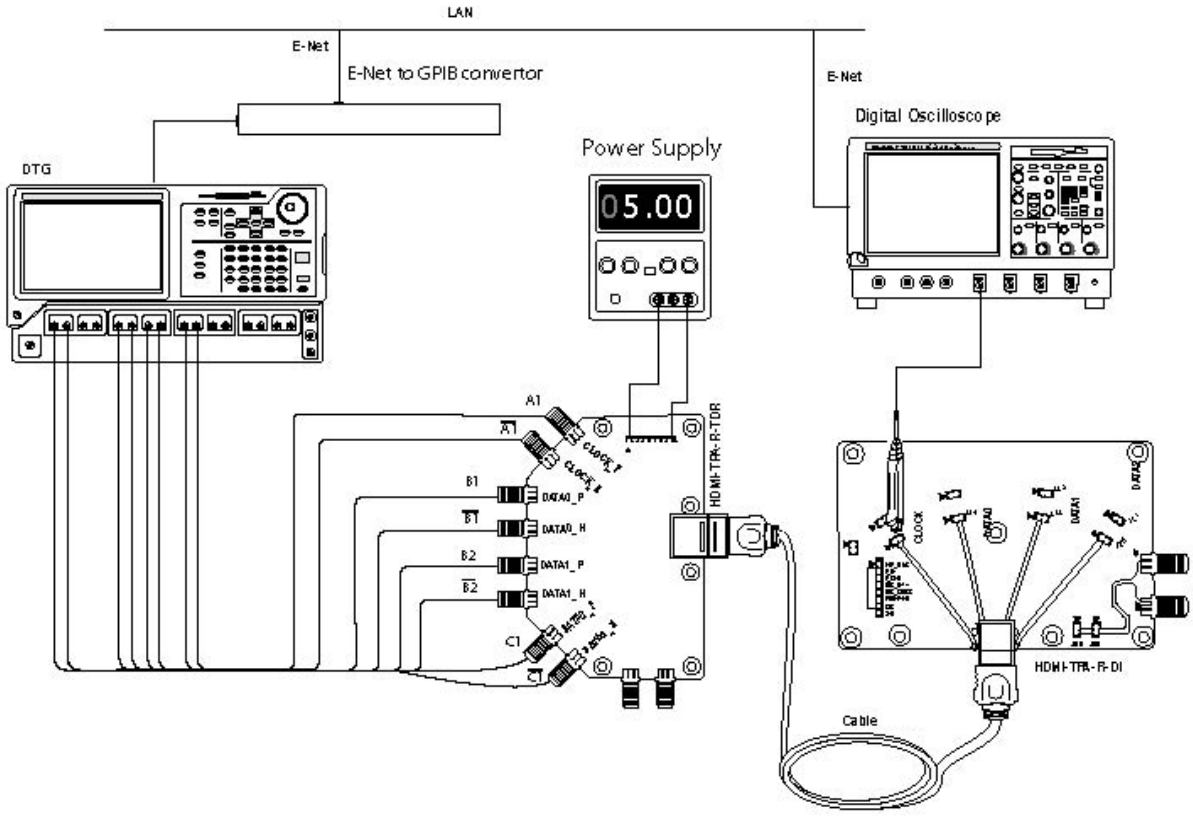
Make the connections as follows:



1. Connect the DTG to the TPA-R-TDR by using eight one-meter or one-and-a-half meter SMA cables:
   - Module A, Channel 1+, 1–: Connect to CLOCK_P, and CLOCK_N
   - Module A, Channel 2+, 2–: No Connection
   - Module B, Channel 1+, 1–: Connect to DATA0_P and DATA0_N
   - Module B, Channel 2+, 2–: Connect to DATA1_P and DATA1_N
   - Module C, Channel 1+, 1–: Connect to DATA2_P and DATA2_N
   - Module C, Channel 2+, 2–: No Connection
2. Connect the Cable Emulator from the TPA-R-TDR to the Sink DUT.
3. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC /CEC Ground (P_GND) on the TPA-R-TDR.

Setup 2. To measure the minimum differential swing voltage by using an oscilloscope

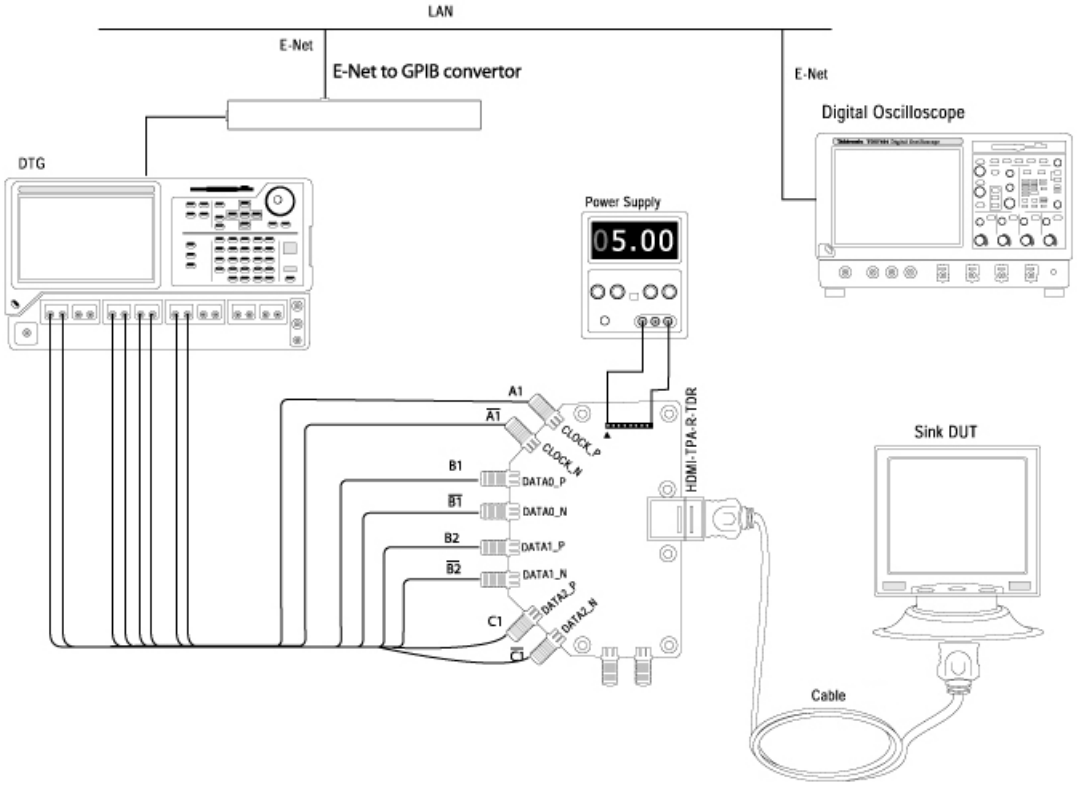
Make the connections as follows:



1. Remove the Sink DUT from the Cable Emulator.
2. Connect the TPA-R-DI test fixture at the end of the Cable Emulator.
3. Connect a TMDS Clock/Data channel to the configured oscilloscope channel by using a differential probe.

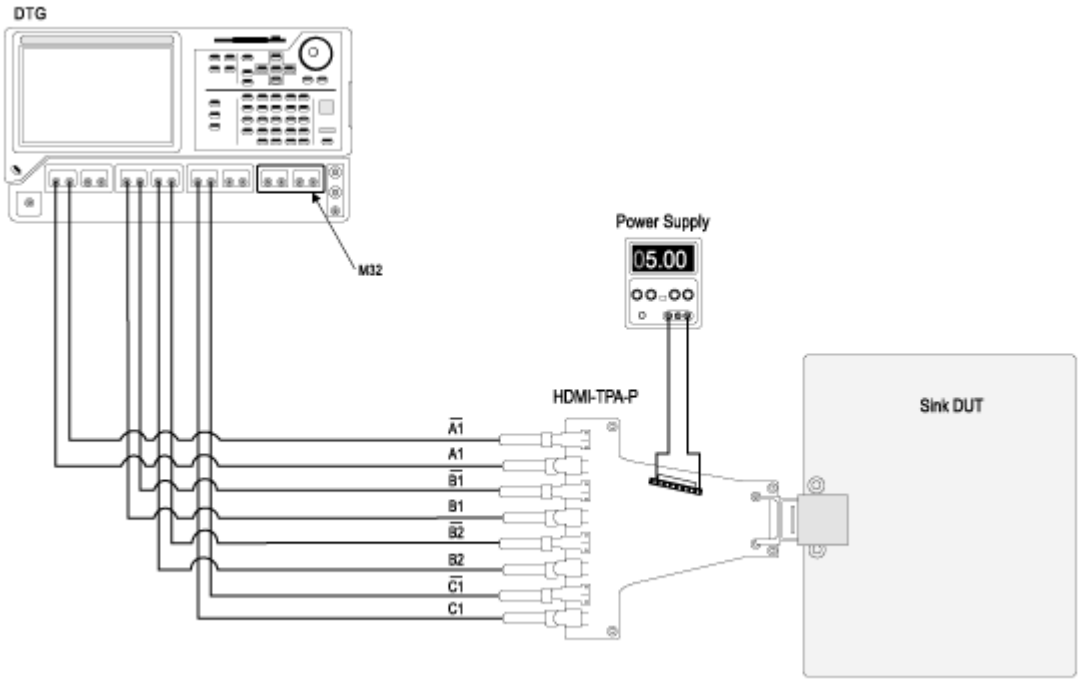
Setup 3. To find the maximum swing voltage of the Sink DUT

1. Remove the TPA-R-DI text fixture at the end of the Cable Emulator.
2. Connect the Sink DUT to the Cable Emulator.

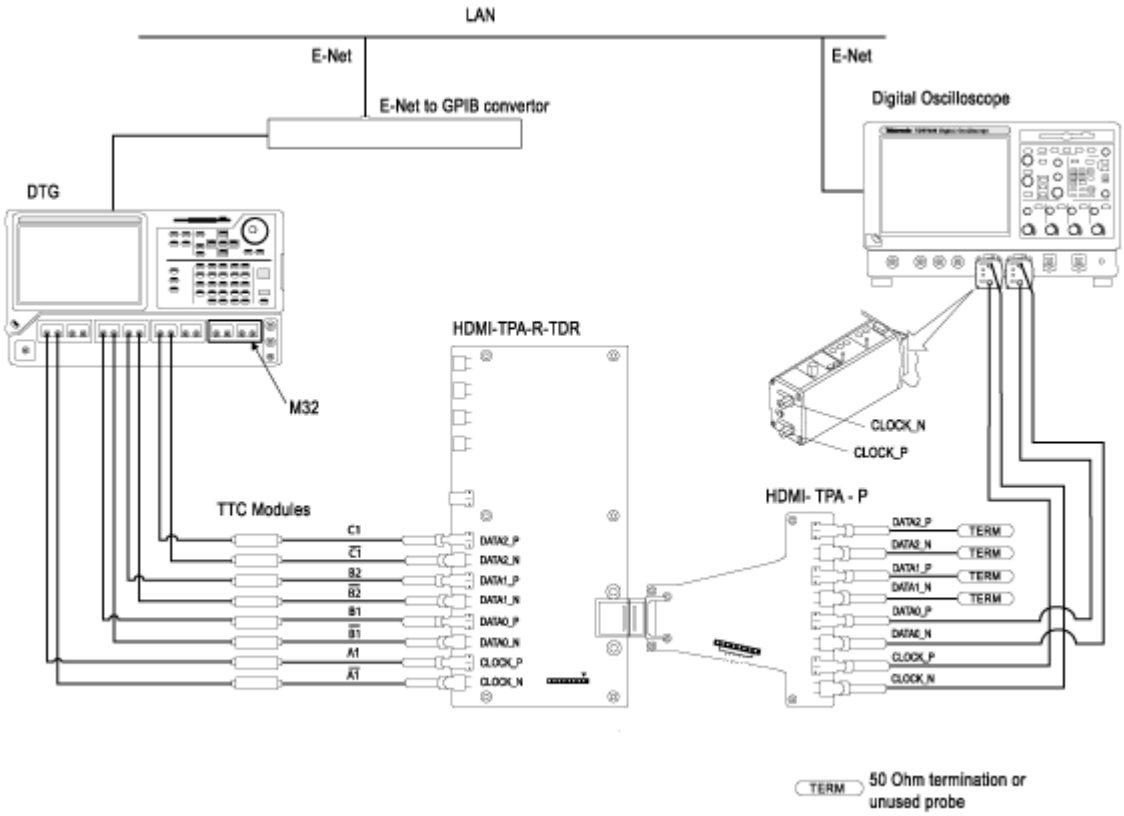


Method 2: Using Efficere test fixtures

Setup 1. To find the Min/Max differential swing voltage of the Sink DUT with the Efficere Test Fixture

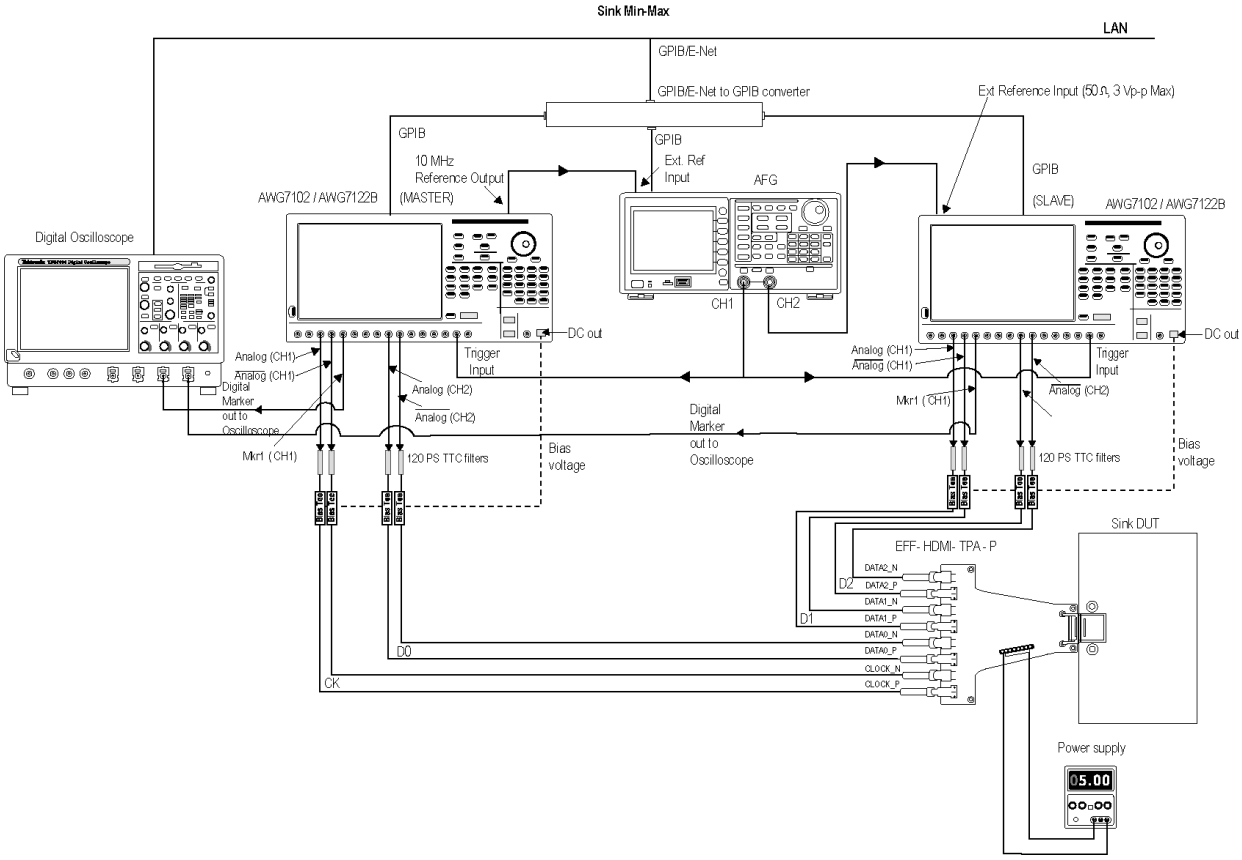


Setup 2. To measure the min/max differential swing voltage of the Sink DUT with the Efficere Test Fixture



For the DDS Method

Setup 1. To test the Sink DUT for Min/Max-Diff Swing Tolerance test compliance



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)

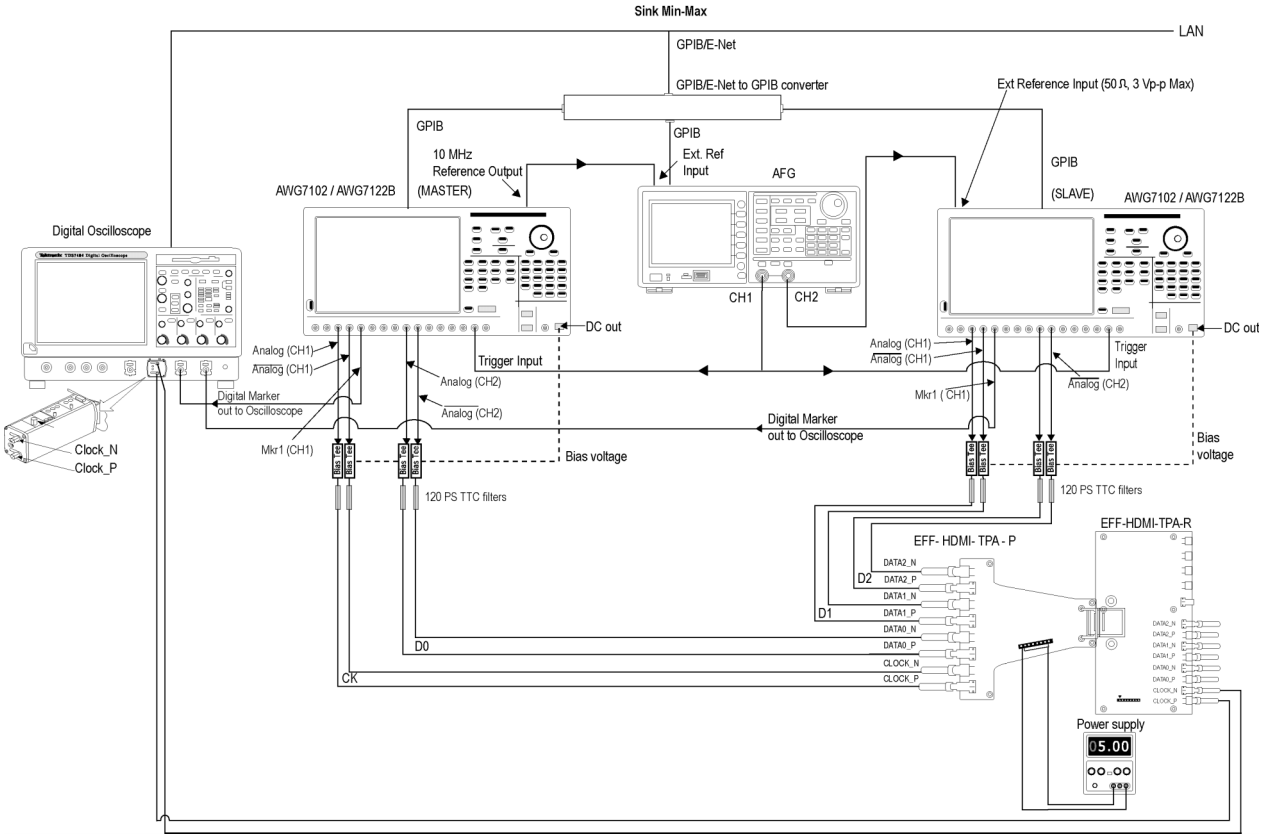
- AWG1 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
  - Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
  - AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)
- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink Min/Max Diff Swing Tolerance Test.
   - Select the resolution of the DUT to be tested.

NOTE. *The software automatically reduces the amplitude of the signal in steps of 10 mV from 170 mV to 90 mV.*

   - Confirm the gray bars on the DUT.
   - Connect the Clock channel to the oscilloscope to measure the differential swing voltage.
   - In the Signal Source dialog box, check the GPIB connection of the two AWGs and the AFG to ensure proper connection.
   - Go to the setup 2 (see page 118).

Setup 2. To measure the Min/Max differential swing voltage



NOTE. *Terminate the lanes that are not connected with a 50 ohm terminator using a Bias-T which is pulled up to 3.3 V.*

1. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively). For connection details, refer to step 3.
2. Connect TPA-P to TPA-R.
3. Connect the Clock output of the TPA-R to the configured oscilloscope channel by using a differential probe.
4. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
5. Once the test completes, you can view the result.

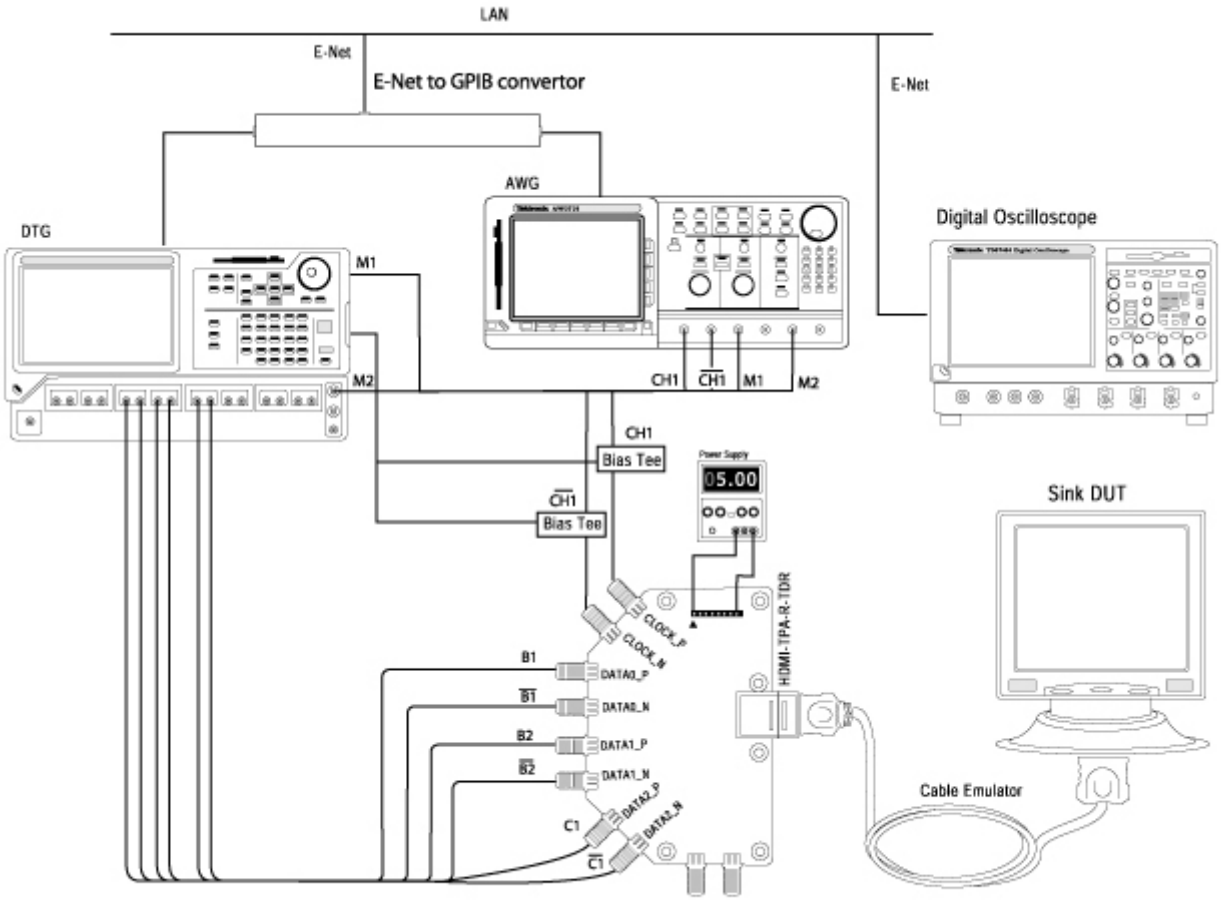
Make Connections for Jitter Tolerance

NOTE. *For all the HDMI 1.2 test fixture connections, connect a TTC filter between the DTG and the test fixture.*

On the menu bar, click **Tests > Connect**.

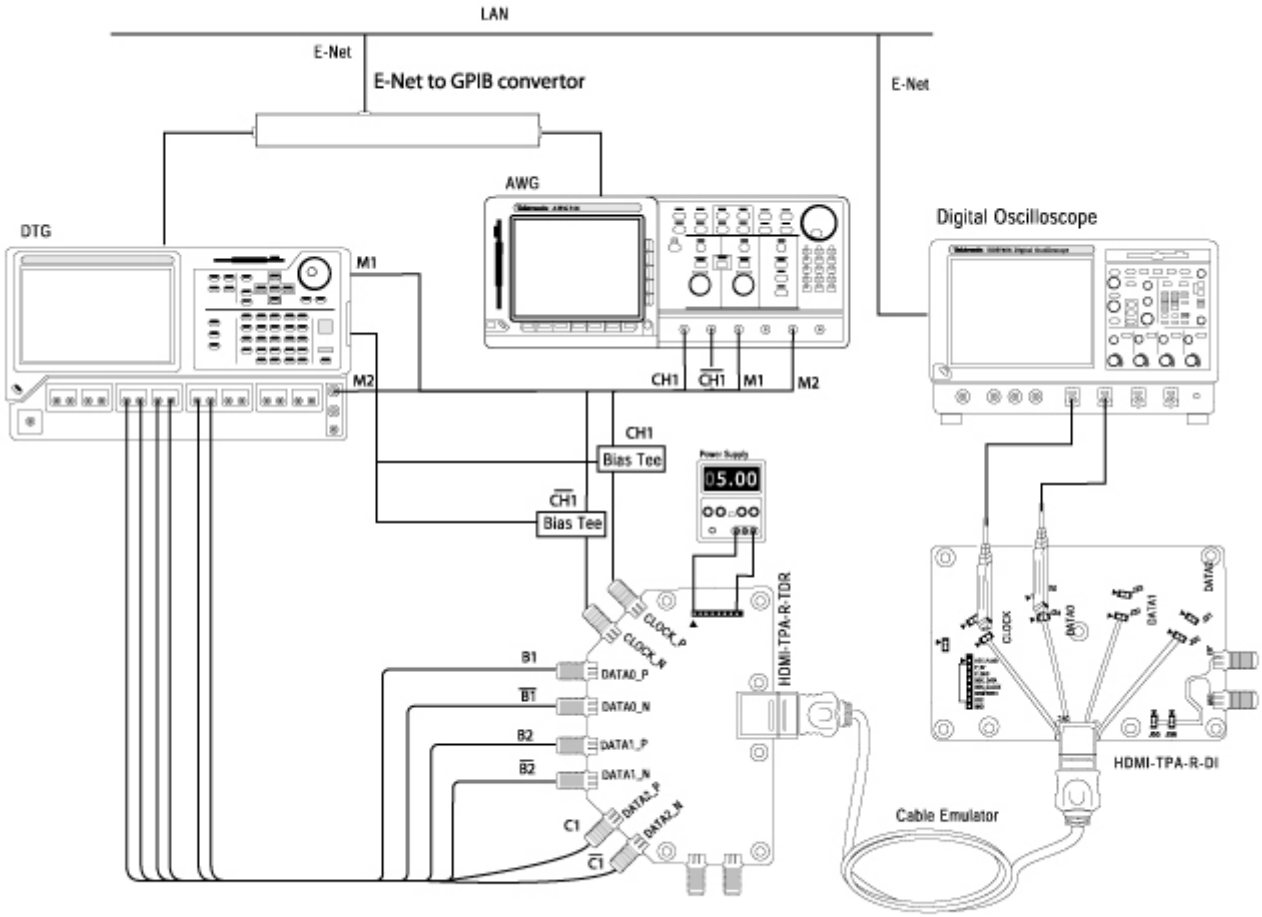
Method 1: Using HDMI 1.2 test fixtures

Setup 1. To find the device tolerance limit for frequencies < 148.5 MHz make the connections as follows:



1. Connect the DTG, AWG, Bias-Tees, and the TPA-R-TDR.
   - AWG Marker 1+ output to DTG External Clock input
   - AWG Marker 2+ output to DTG Trigger In
   - AWG Ch. 1+ output to Bias-Tee signal input (RF)
   - Bias-Tee signal output (RF and DC) to CLOCK_P
   - DTG DC_OUT (1) to Bias-Tee DC-level input (DC)
   - AWG Ch. 1- output to Bias-Tee signal input (RF)
   - Bias-Tee signal output (RF and DC) to CLOCK_N
   - DTG DC_OUT (2) to Bias-Tee DC-level input (DC)
   - DTG Module A, Channel 1+, 1–: No Connection
   - DTG Module A, Channel 2+, 2–: No Connection
   - DTG Module B, Channel 1+, 1–: Connect to DATA0_P and DATA0_N
   - DTG Module B, Channel 2+, 2–: Connect to DATA1_P and DATA1_N
   - DTG Module C, Channel 1+, 1–: Connect to DATA2_P and DATA2_N
   - DTG Module C, Channel 2+, 2–: No Connection
2. Connect the TPA-R-TDR to the Sink DUT by using a Cable Emulator specified for the tested pixel clock rate.
3. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.

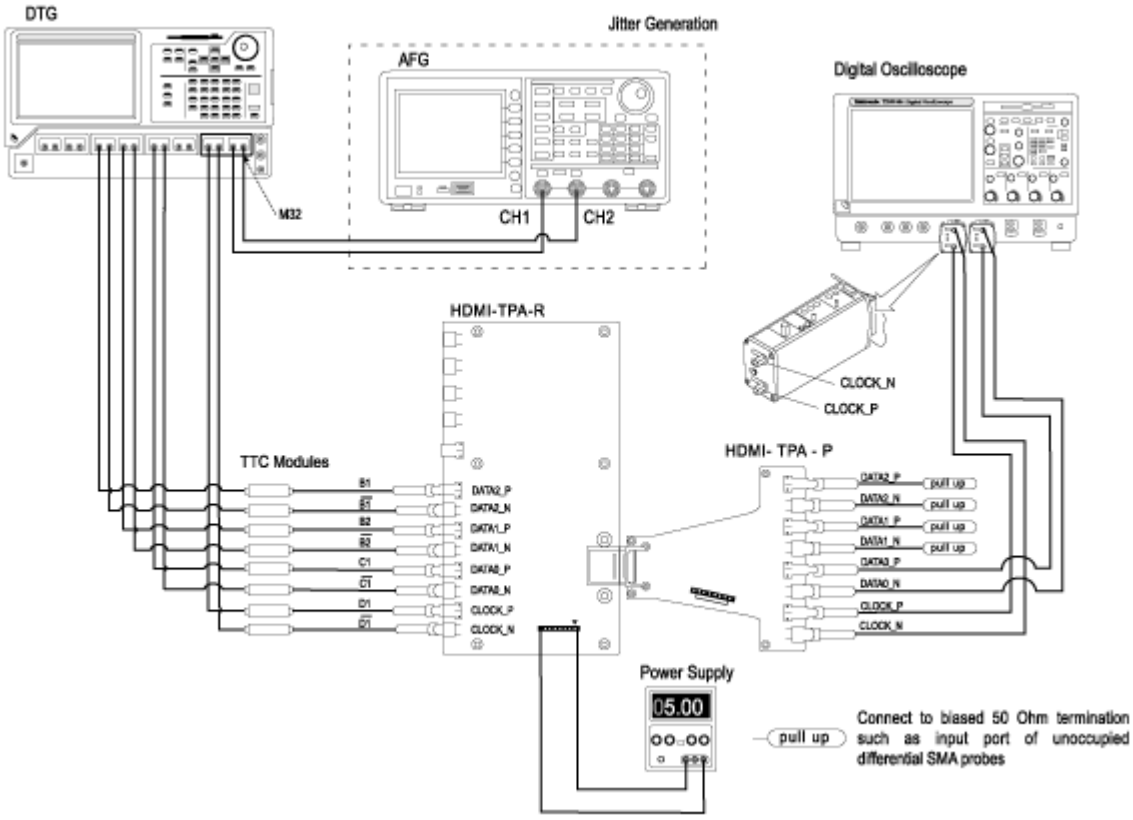
Setup 2. To measure the parameters for frequencies < 148.5 MHz, make the connections as follows:



1. Remove the Sink DUT.
2. Connect the TPA-R-DI test adapter to a cable emulator.
3. Connect a Clock to the configured oscilloscope channel by using a differential probe.
4. Connect the Data pair on which you will conduct the test to the configured oscilloscope channel by using a second differential probe.

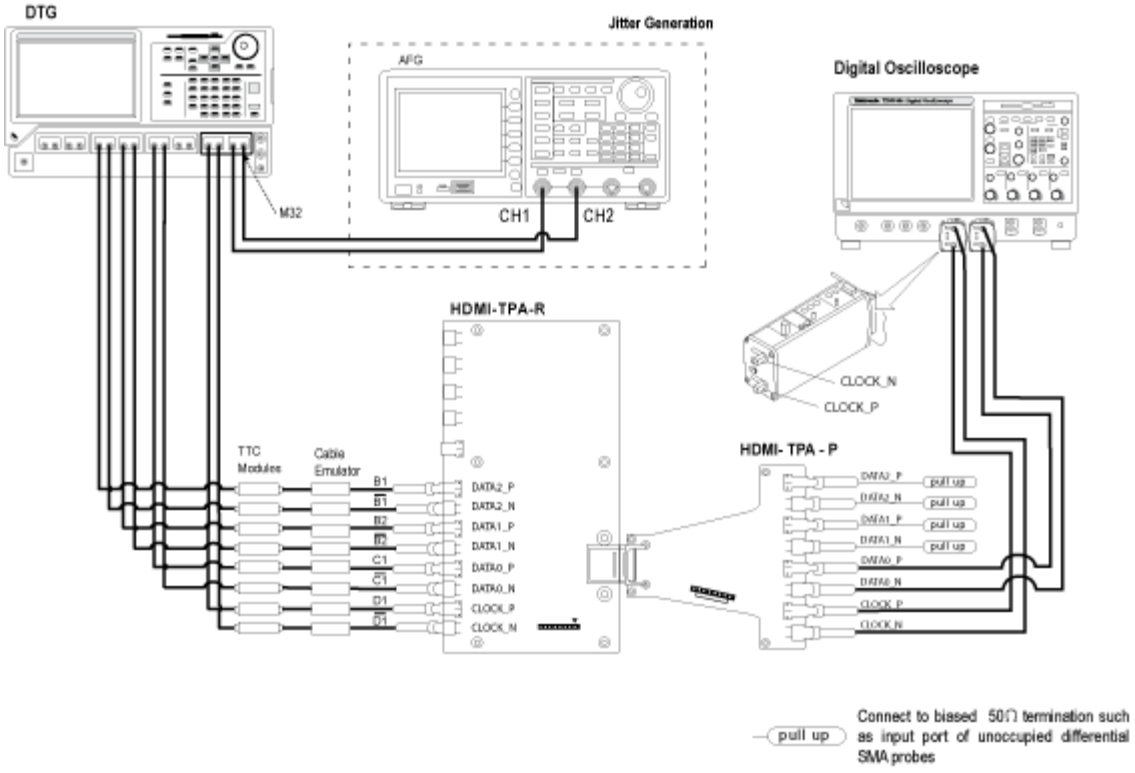
Method 2: Using Efficere test fixtures

Connections for jitter calibration (common to all jitter insertion setups).

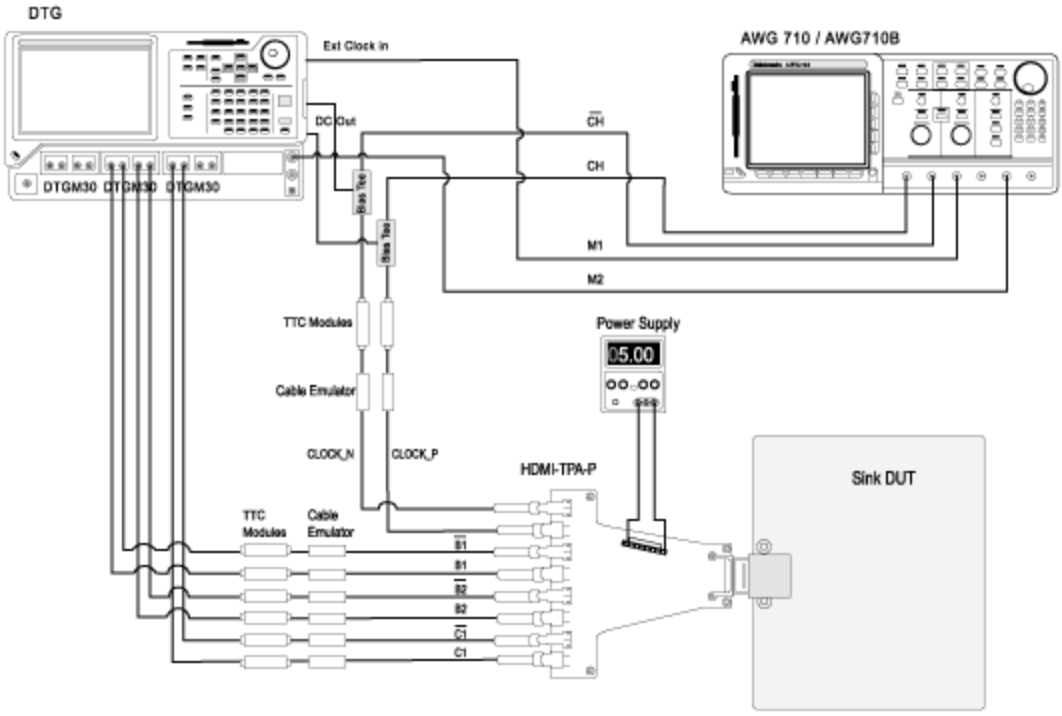


1. Use Jitter Generation block to generate a known amount of jitter (Clock jitter: 0.25 UI, Data jitter: 0.30 UI).
2. Connect the test fixture to the oscilloscope for calibration. The oscilloscope calculates data and clock jitter inserted due to the cables and the test fixtures along with the known amount of jitter.

Connections to adjust the clock jitter at TP2.

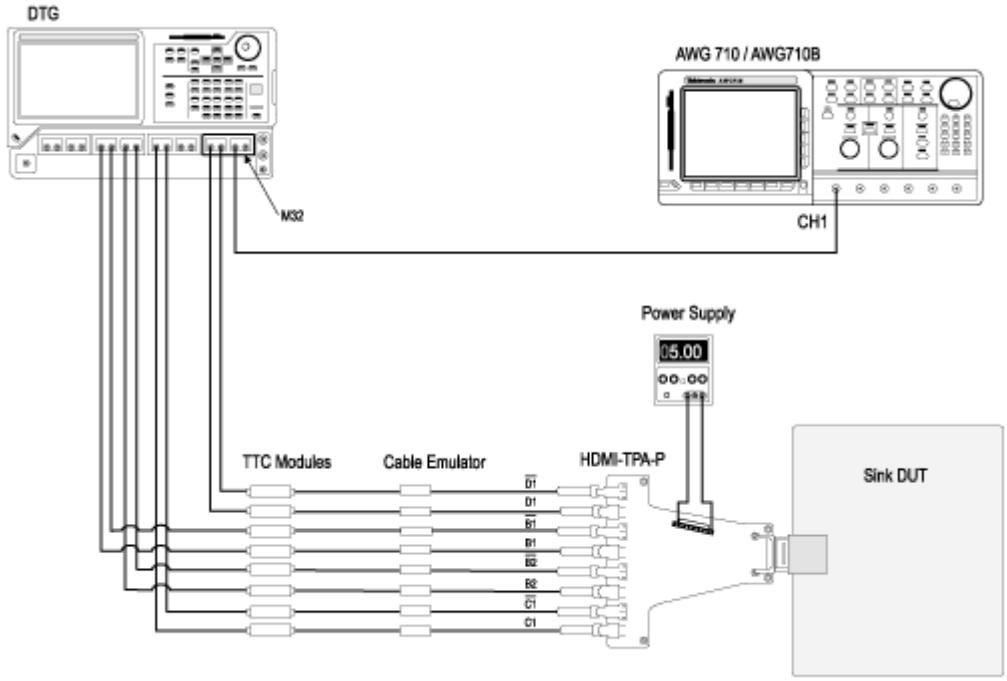


Setup 1a. DTG-AWG for testing resolutions ≤ 74.25MHz



1. Connect the test equipment for the DTG and AWG connection as shown in the setup diagram.
2. When connecting the test fixture to the DUT, use a cable emulator specified for the pixel clock rate being tested.
3. Connect the DTG, AWG, and the oscilloscope according to the Enable Remote Control of Test Equipment (see page 29) procedure.
4. Configure the DUT to receive the HDMI input signal.

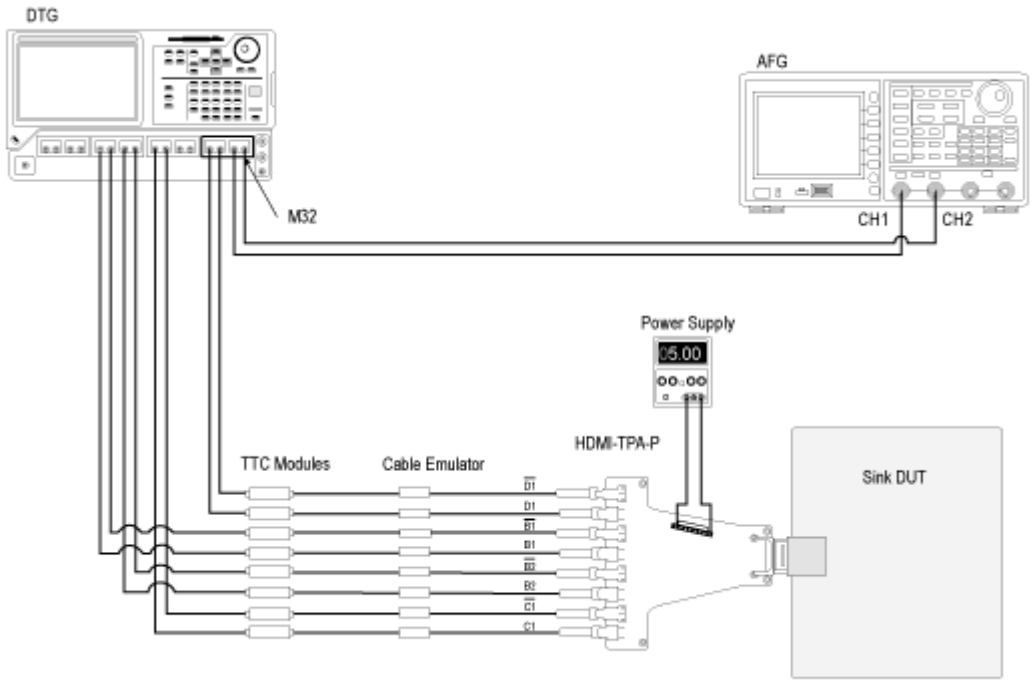
Setup 1b. DTG-AWG for testing resolutions > 74.25MHz



1. Connect the test equipment for the DTG and AWG connection as shown in the setup diagram.
2. Connect the DTG, AWG, and the oscilloscope according to the Enable Remote Control of Test Equipment procedure.
3. Configure the DUT to receive the HDMI input signal.

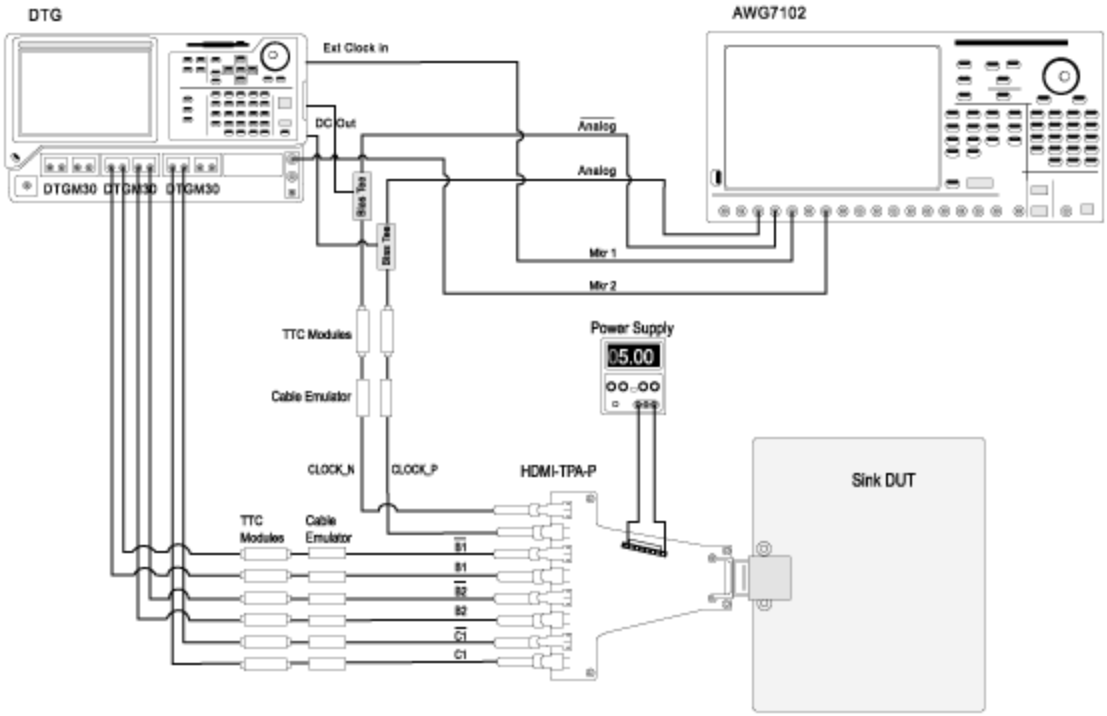
NOTE. *Some of the DUTs work with test fixtures that are not connected to a power supply.*

Setup 2. DTG-AFG jitter tolerance



1. Connect the test equipment for the DTG and AFG connection as shown in the setup diagram.
2. When connecting the test fixture to the DUT, use a cable emulator specified for the pixel clock rate being tested.
3. Connect the DTG, AFG, and the oscilloscope according to the Enable Remote Control of Test Equipment procedure.
4. Configure the DUT to receive the HDMI input signal.

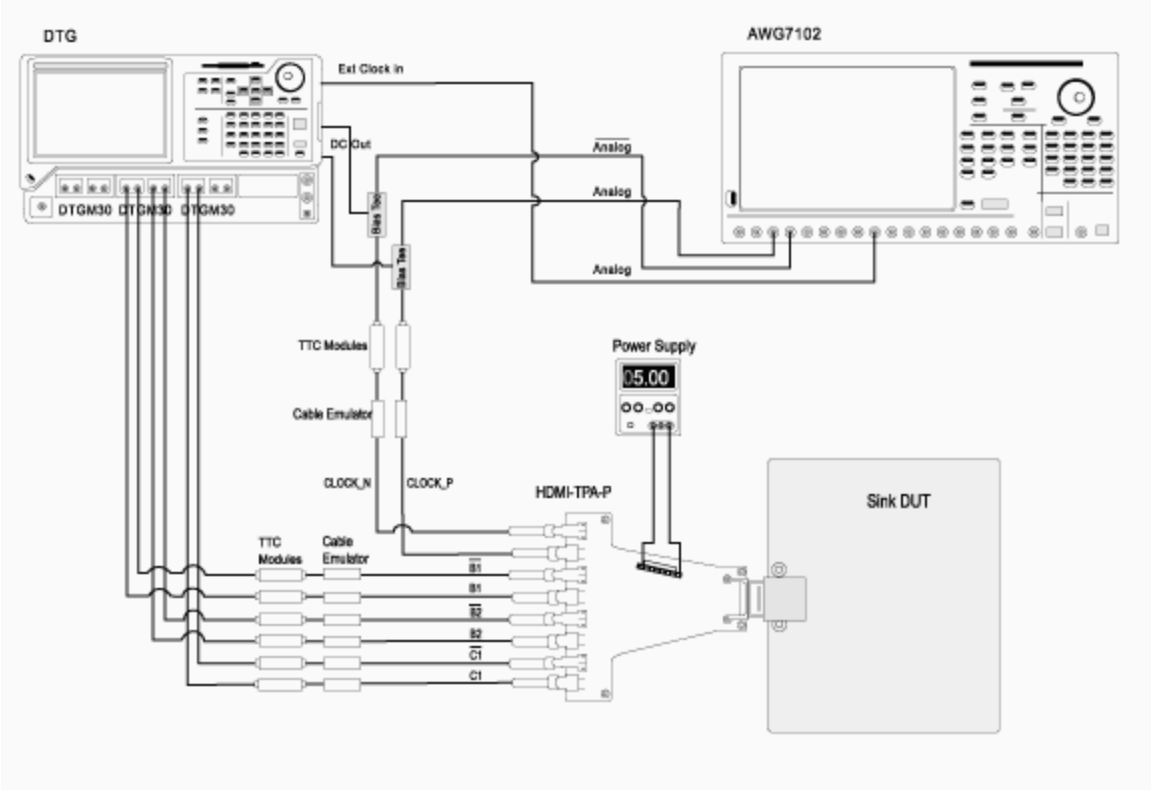
Setup 3. DTG-AWG composite jitter tolerance for all frequencies



1. Connect the test equipment for the DTG and AWG connection as shown in the setup diagram.
2. When connecting the test fixture to the DUT, use a cable emulator specified for the pixel clock rate being tested.
3. Connect the DTG, AWG, and the oscilloscope according to the Enable Remote Control of Test Equipment procedure.
4. Configure the DUT to receive the HDMI input signal.

NOTE. *Mkr2 does not need to be connected to the trigger input of the DTG.*

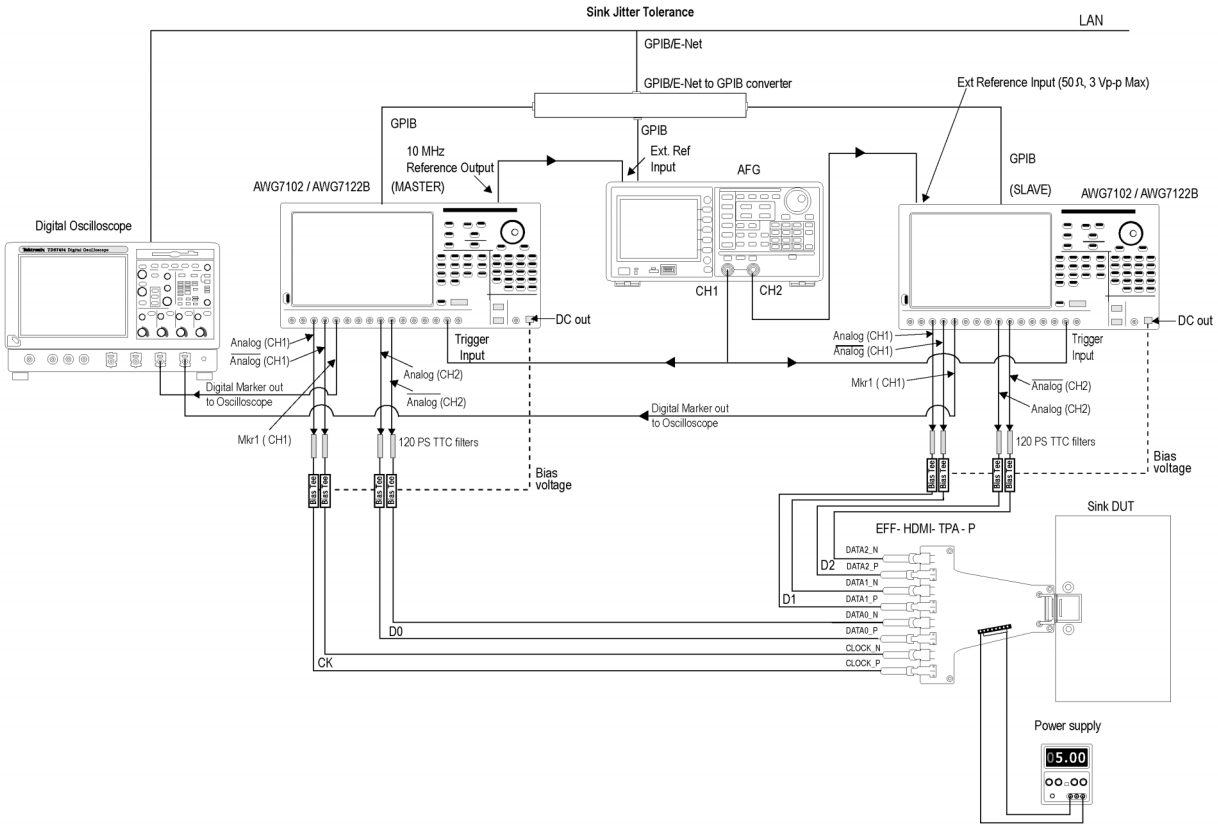
Setup 4. DTG-AWG with separate jitter tolerance for all frequencies



1. Connect the test equipment for the DTG and AWG connection as shown in the setup diagram.
2. When connecting the test fixture to the DUT, use a cable emulator specified for the pixel clock rate being tested.
3. Connect the DTG, AWG, and the oscilloscope according to the Enable Remote Control of Test Equipment procedure.
4. Configure the DUT to receive the HDMI input signal.

For the DDS Method

Setup 1: To test the Sink DUT for Sink Jitter Tolerance test compliance



NOTE. *The DDS method does not need different hardware TTC filters (for each resolution) and cable emulators because their effects are emulated by the software.*

Perform the following steps for each TMDS clock rate supported by the Sink DUT. You do not need to test a particular rate if another rate within +/–10% of that rate has already been tested.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input

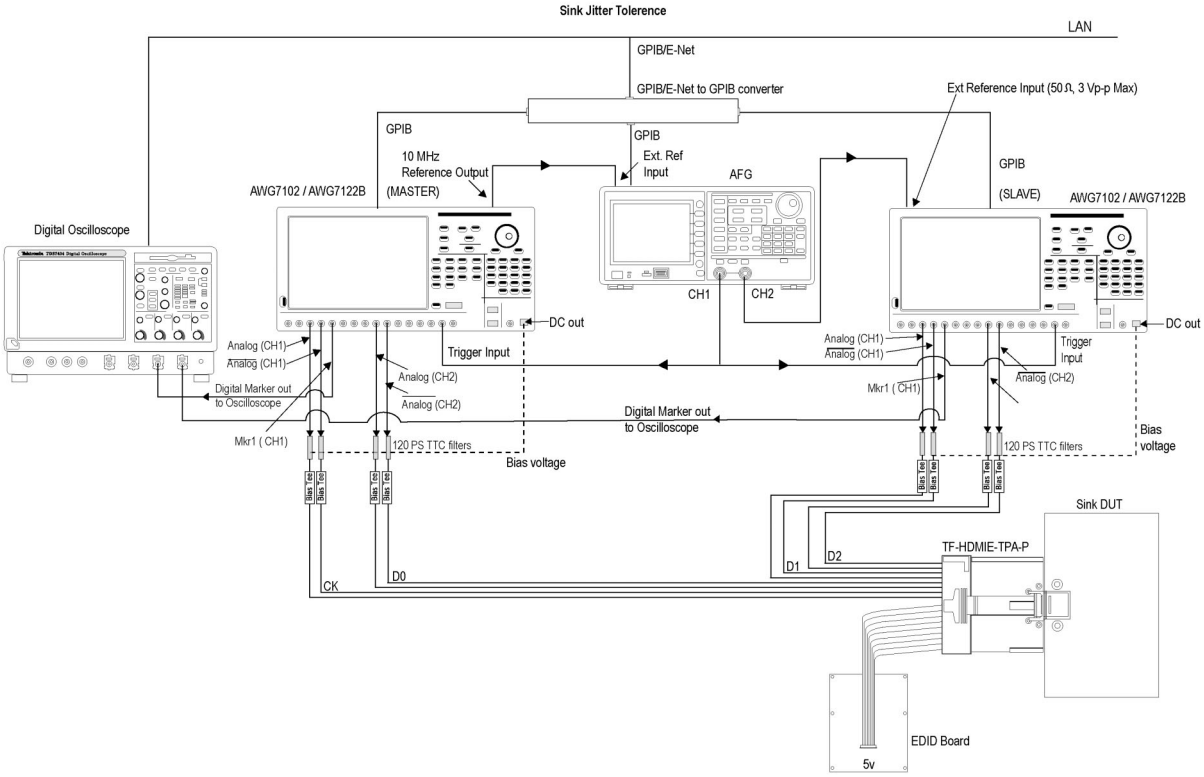
- AWG1 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
  - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
  - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
- AWG1 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
  - Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
  - AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)
- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–

- AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)

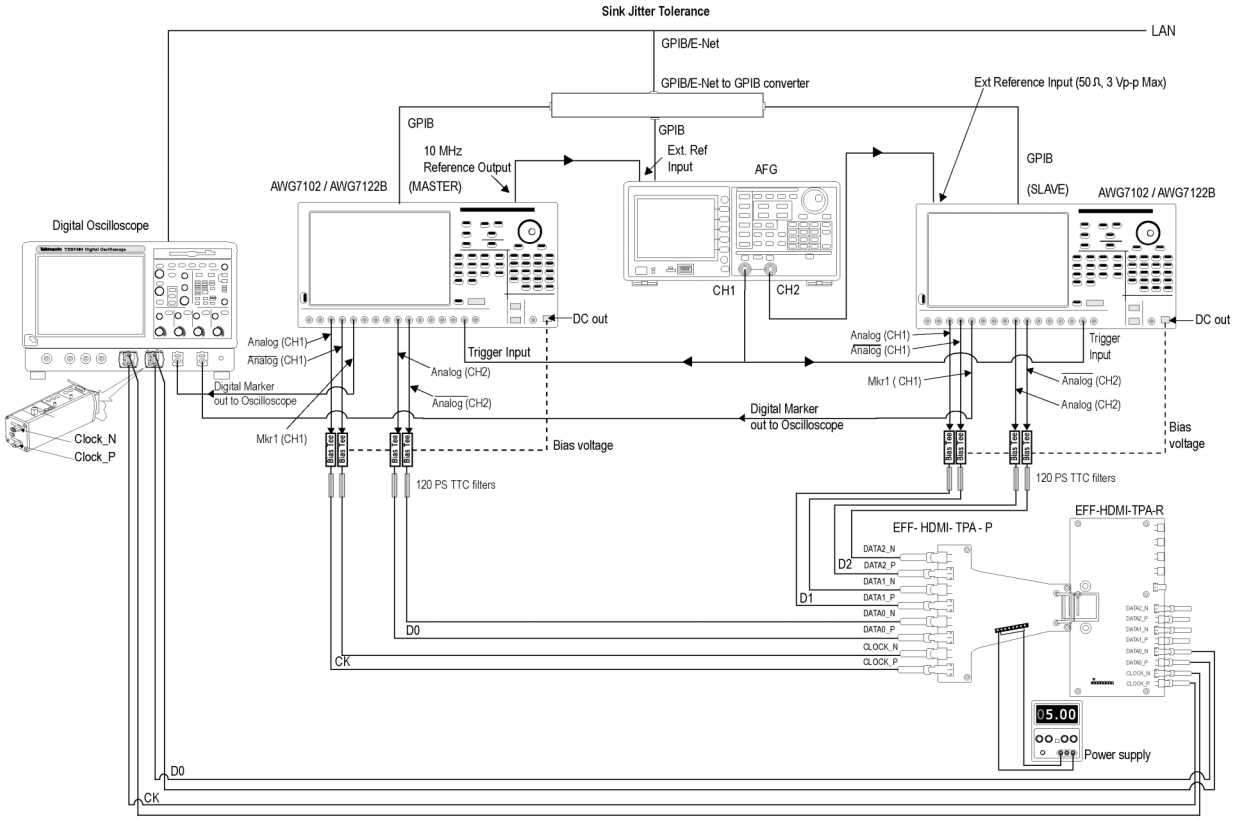
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink Jitter Tolerance Test.
   - Select the resolution of the DUT to be tested.
   - Select the cable emulator to be used for the test (Direct Synthesis method emulates the TTC filters and cable emulators).
   - In the Signal Source dialog box, check the GPIB connection of the two AWGs and the AFG to ensure proper connection.
   - The TDSHT3 software will also change the skew in 0.1 TBit steps automatically, for example, 0.0TBIT, 0.1TBIT, until 0TBIT. In each step, you will be prompted to confirm if the DUT adequately supports the signal.
   - Once the test completes, you can view the result.

Setup 2: To test the automotive Sink DUT for Sink Jitter Tolerance test using Type-E fixture



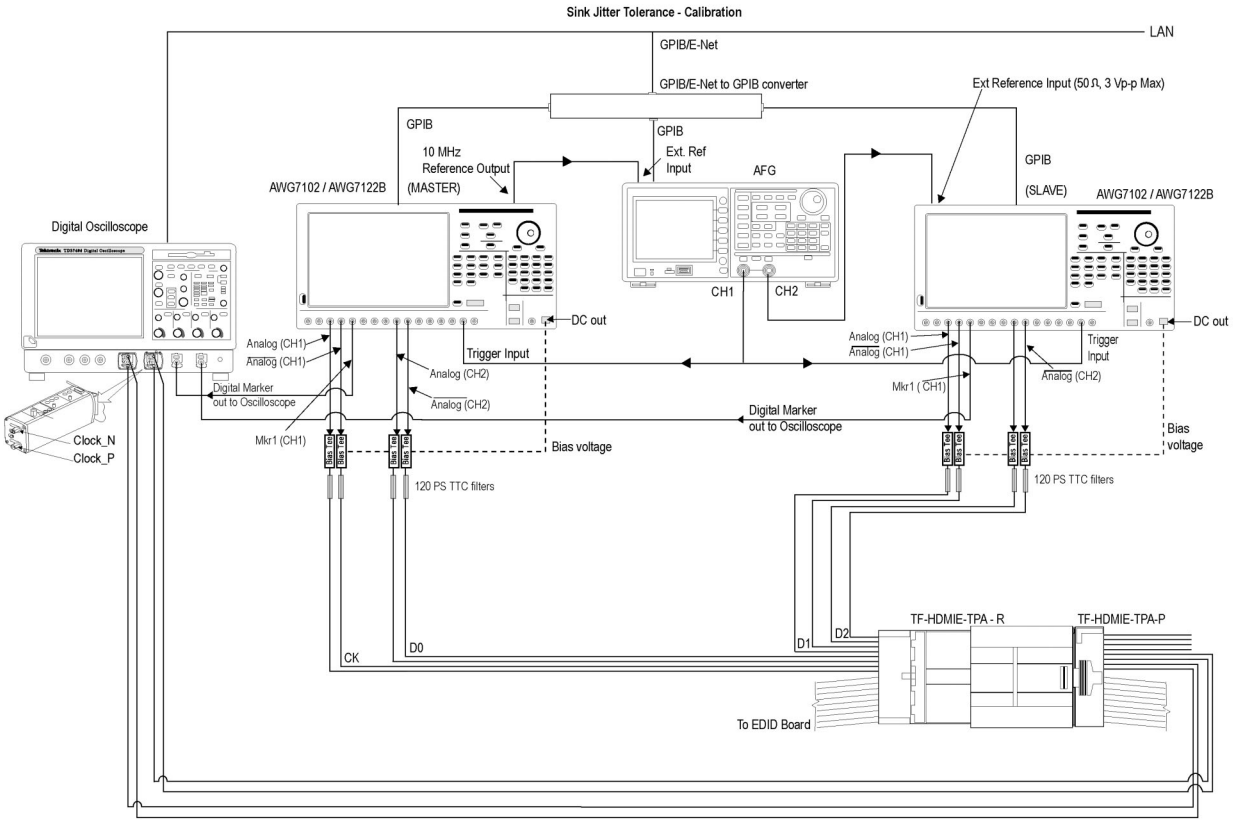
Setup 3: To calibrate the jitter values



NOTE. *Terminate the lanes that are not connected with a 50 ohm terminator using a Bias-T which is pulled up to 3.3 V.*

1. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively). For connection details, refer to step 3.
2. Connect TPA-P to TPA-R.
3. Connect the Clock and Data0 output of the TPA-R to the configured oscilloscope channel by using a differential probe.
4. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
5. Once the calibration is complete, connect the TPA-P to Sink DUT to continue with the test. Refer Setup 1 (see page 129).

Setup 4: To calibrate the jitter values using Type-E fixture



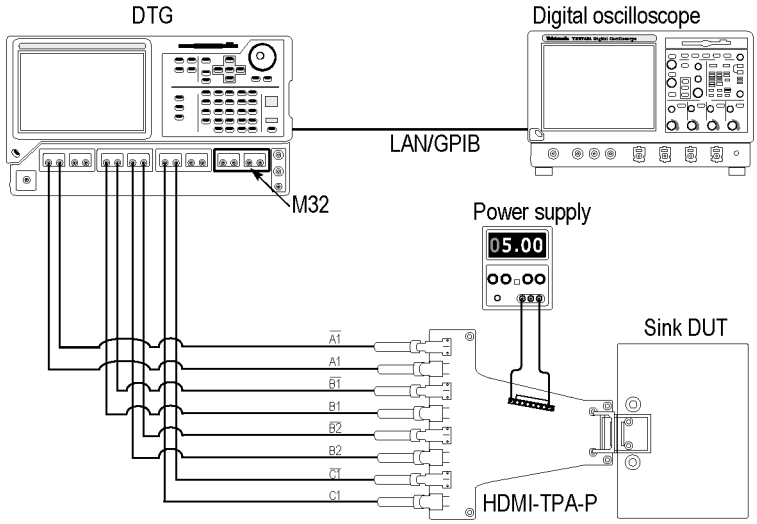
NOTE. *Terminate the lanes that are not connected with a 50 ohm terminator using a Bias-T which is pulled up to 3.3 V.*

Make Connections for Deep Color

On the menu bar, click **Tests > Connect**.

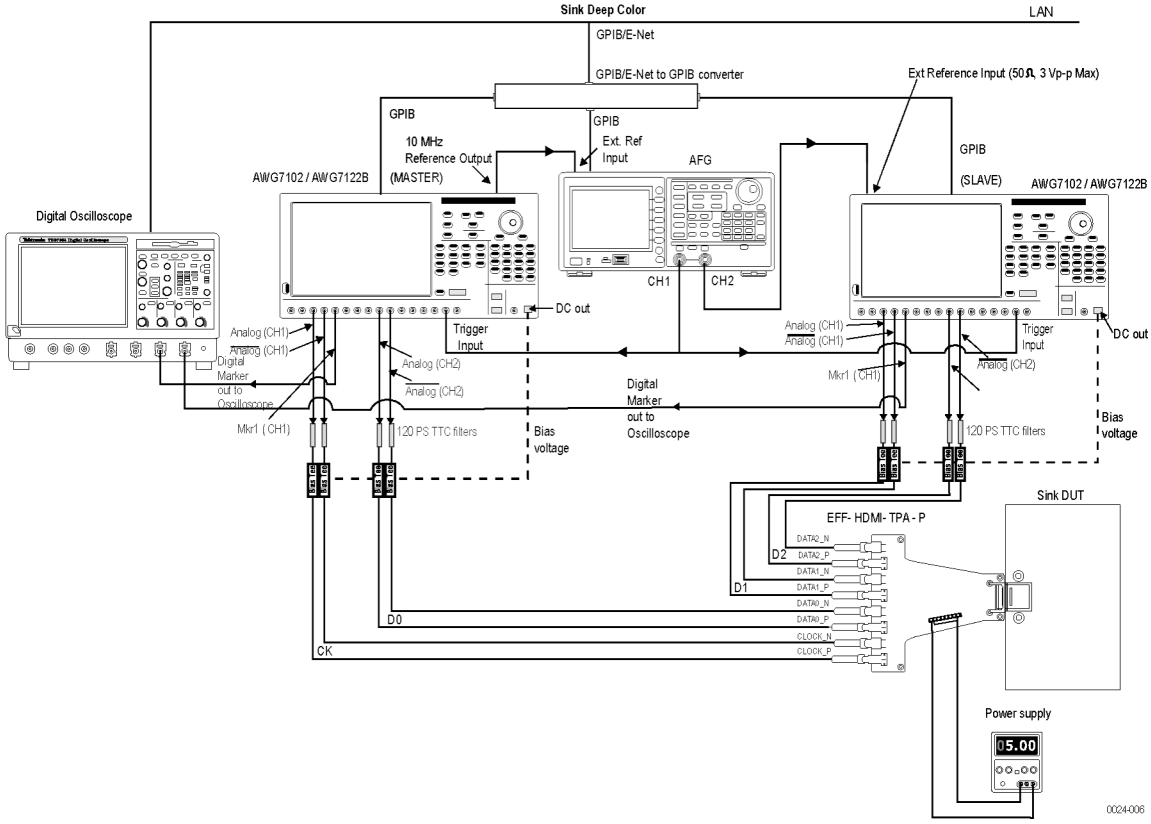
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for Deep Color test compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

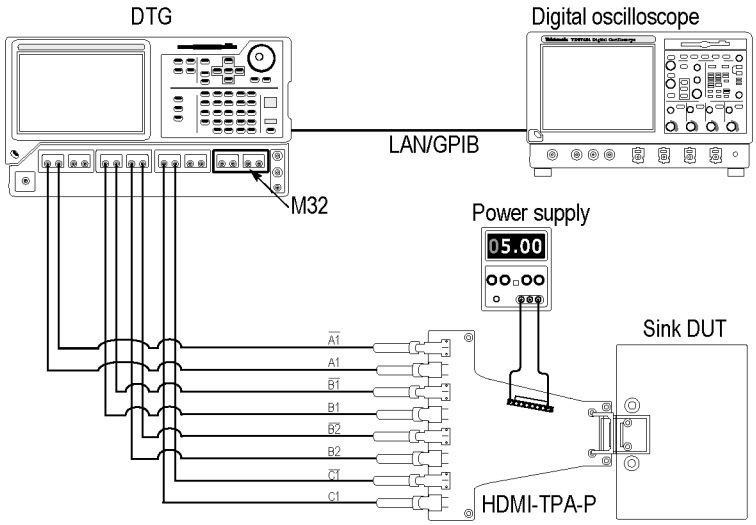
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink Deep Color Test.
   - Select the resolution, refresh rate, and bits of the DUT to be tested.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the gray/color bar is visible on the DUT.

Make Connections for Audio Clock Regeneration

On the menu bar, click **Tests > Connect**.

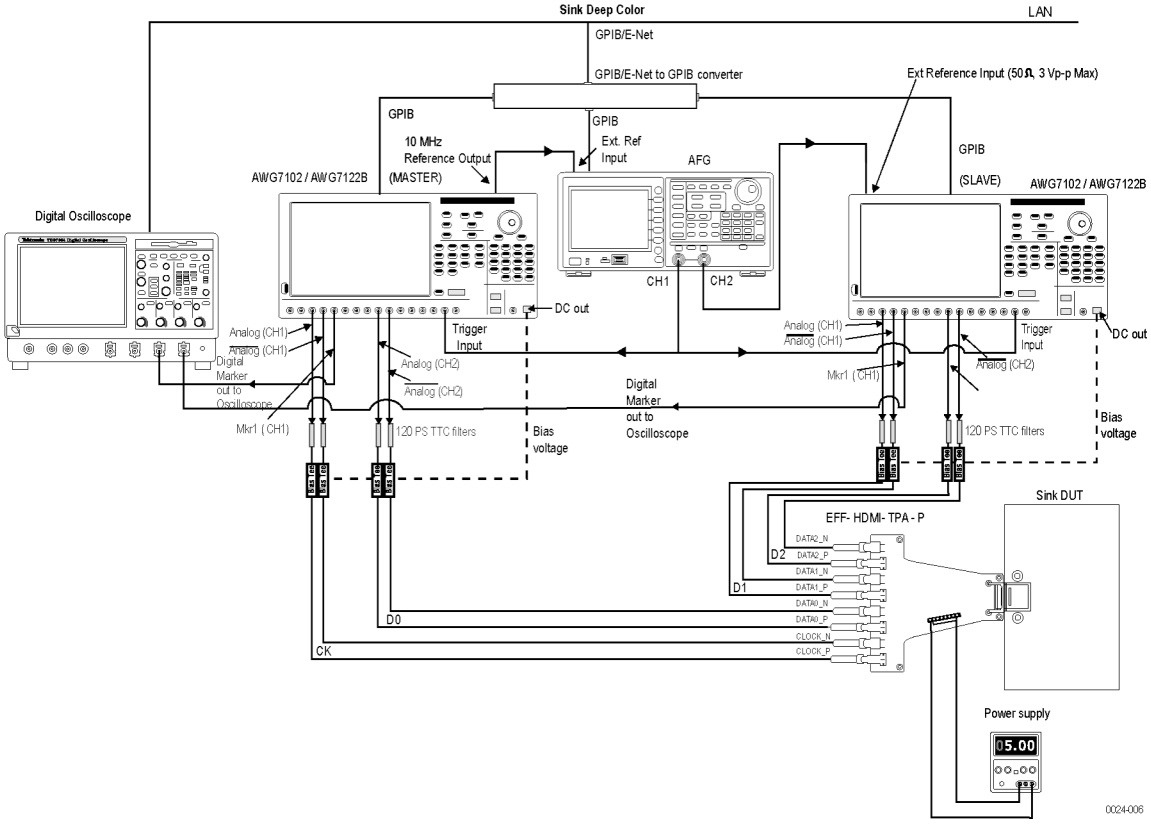
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for Audio Clock Regeneration test compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

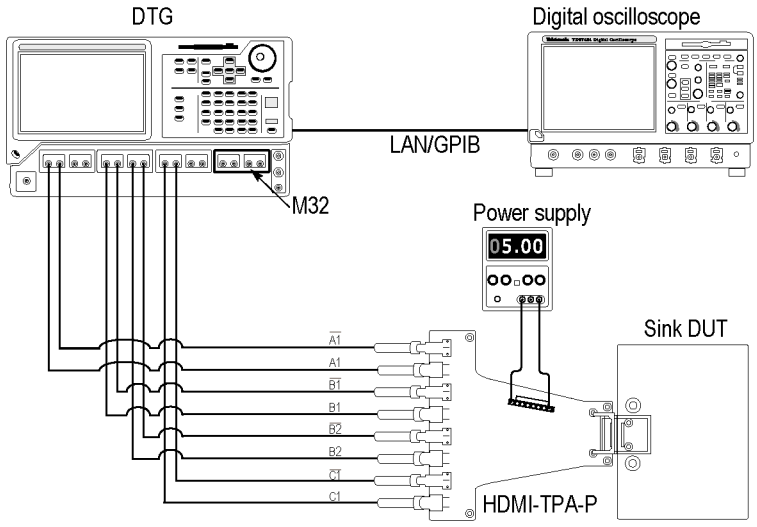
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Audio Clock Regeneration Test.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the gray/color bar is visible on the DUT.

Make Connections for Audio Sample Packet Jitter

On the menu bar, click **Tests > Connect**.

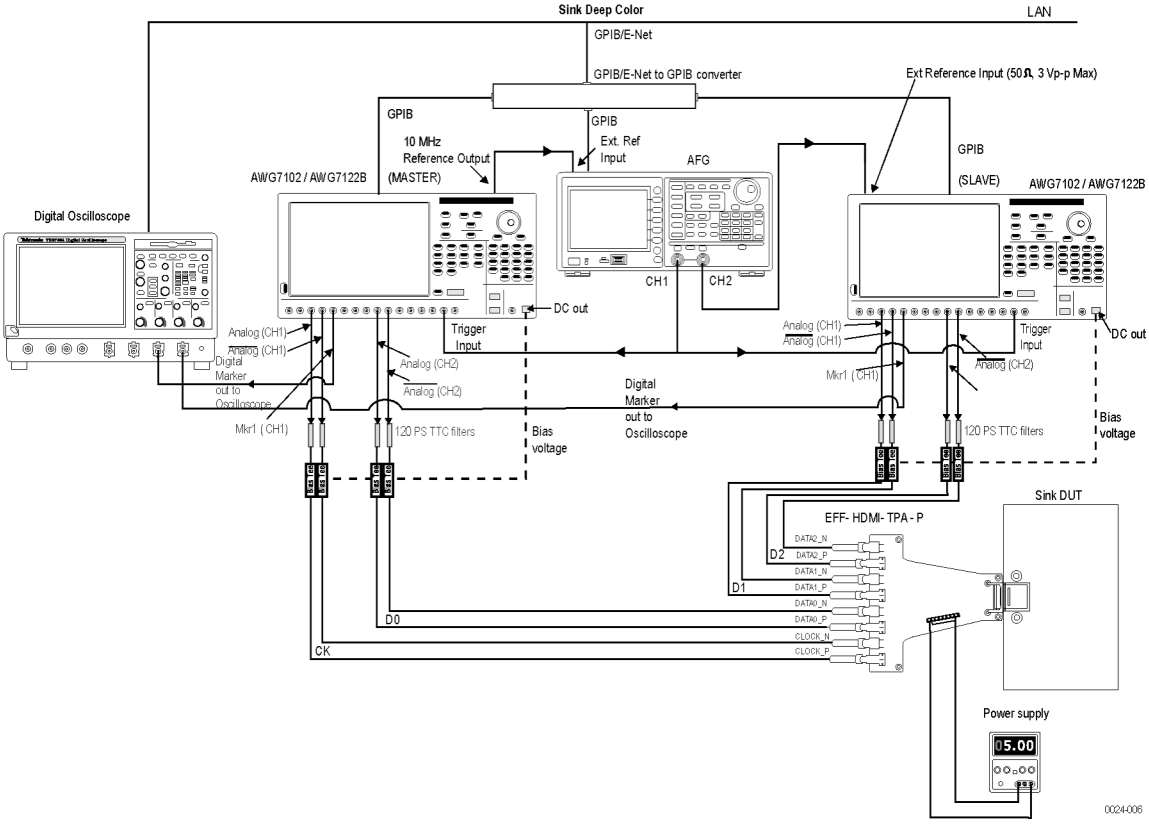
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for Audio Sample Packet Jitter test compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

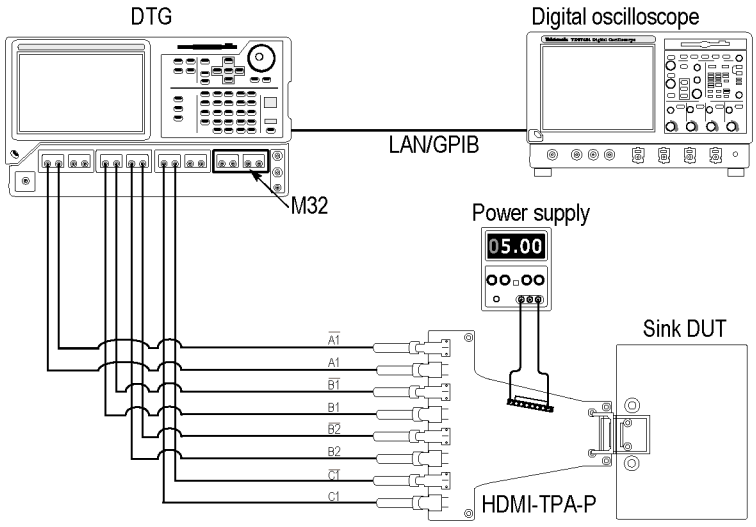
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink Audio Sample Packet Jitter test.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the gray/color bar is visible on the DUT.

Make Connections for Audio Formats

On the menu bar, click **Tests > Connect**.

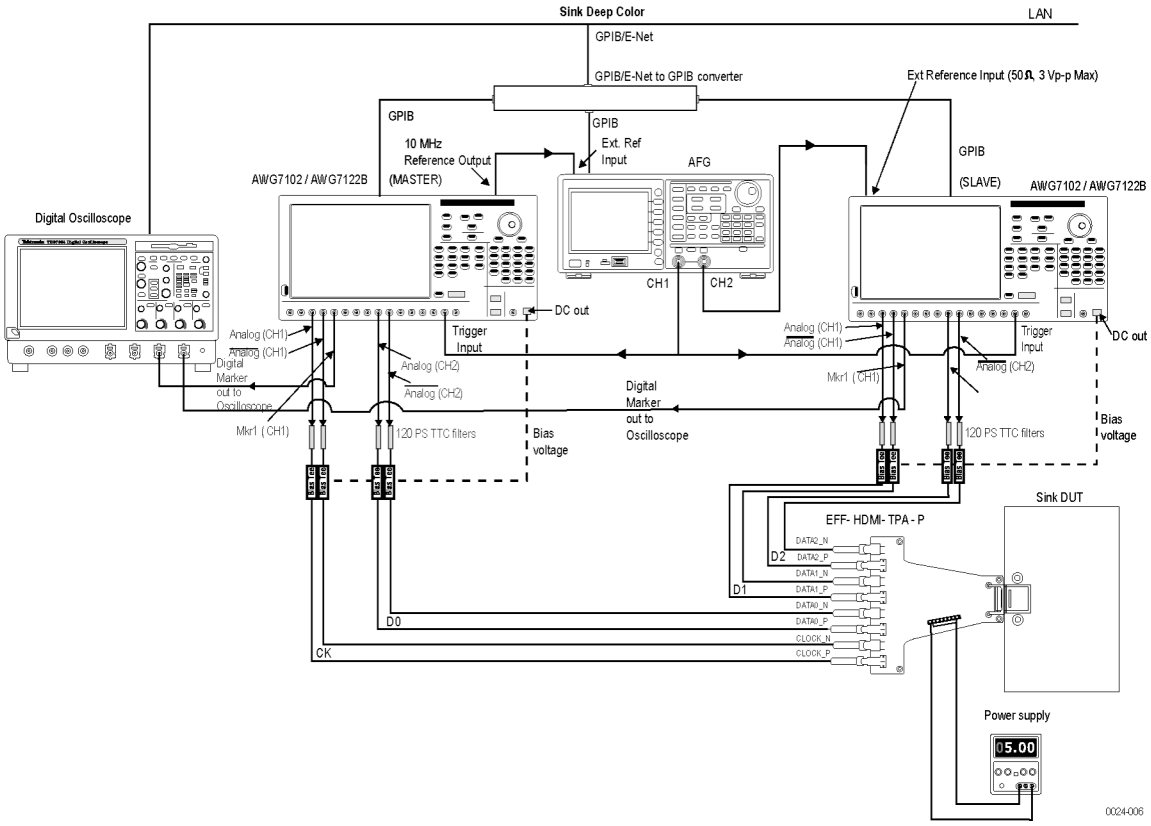
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for Audio Formats test compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

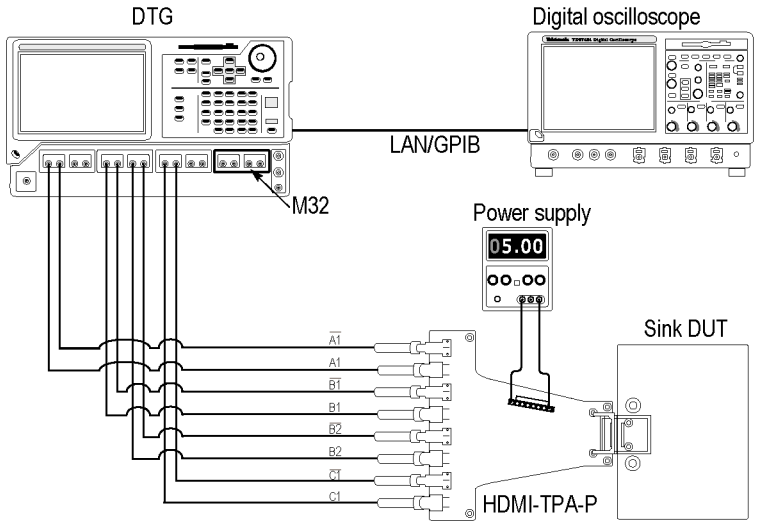
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink Audio Formats Test.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the gray/color bar is visible on the DUT.

Make Connections for One Bit Audio

On the menu bar, click **Tests > Connect**.

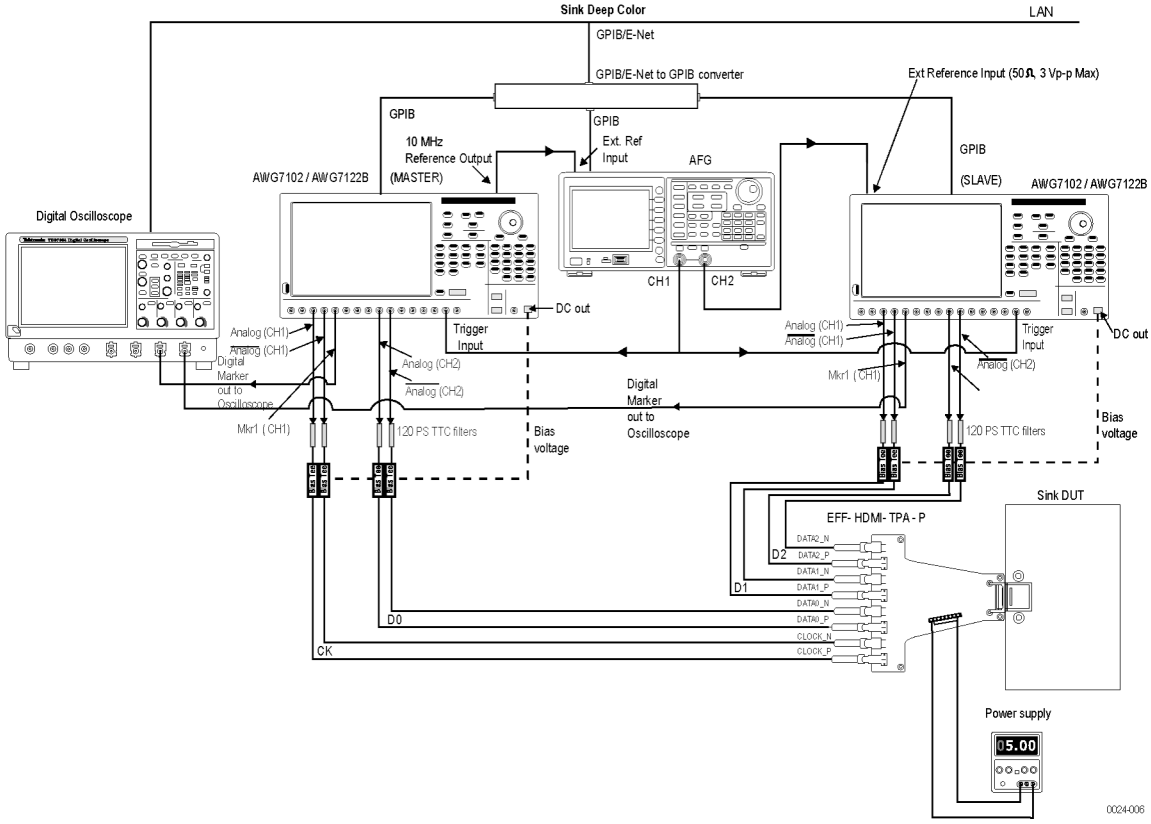
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for One Bit Audio test compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

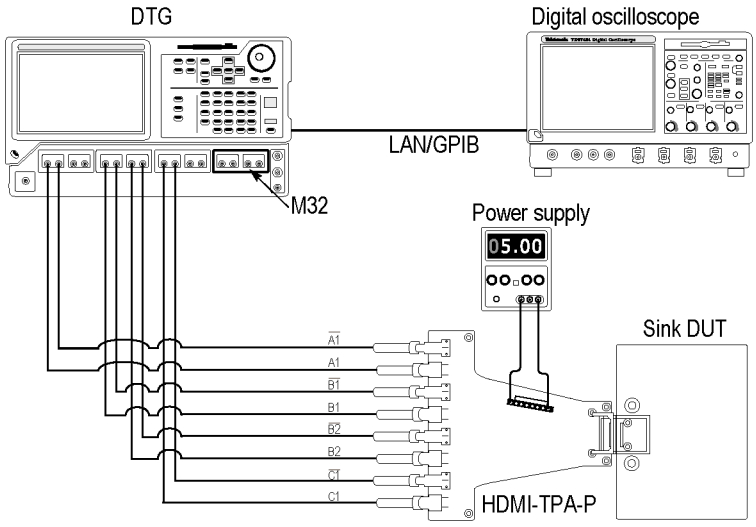
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink One Bit Audio Test.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the gray/color bar is visible on the DUT.

Make Connections for DVI Interoperability

On the menu bar, click **Tests > Connect**.

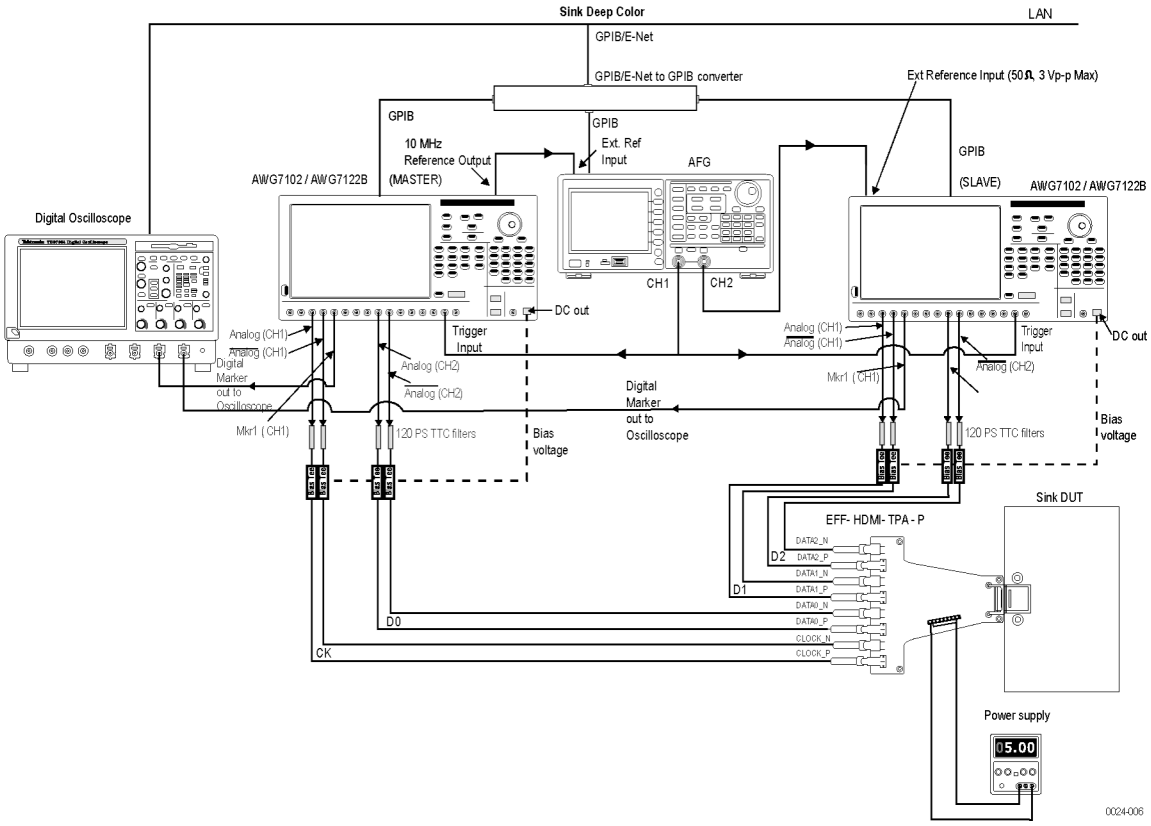
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for DVI Interoperability compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

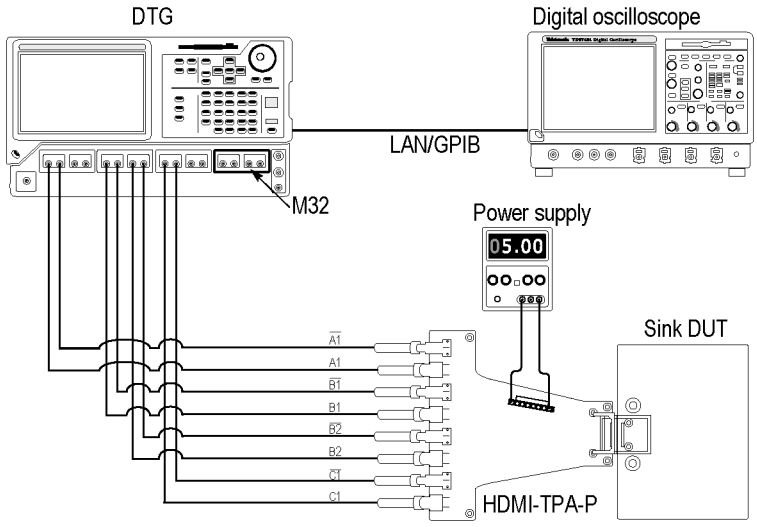
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink DVI Interoperability Test.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the gray/color bar is visible on the DUT.

Make Connections for 3D Video

On the menu bar, click **Tests > Connect**.

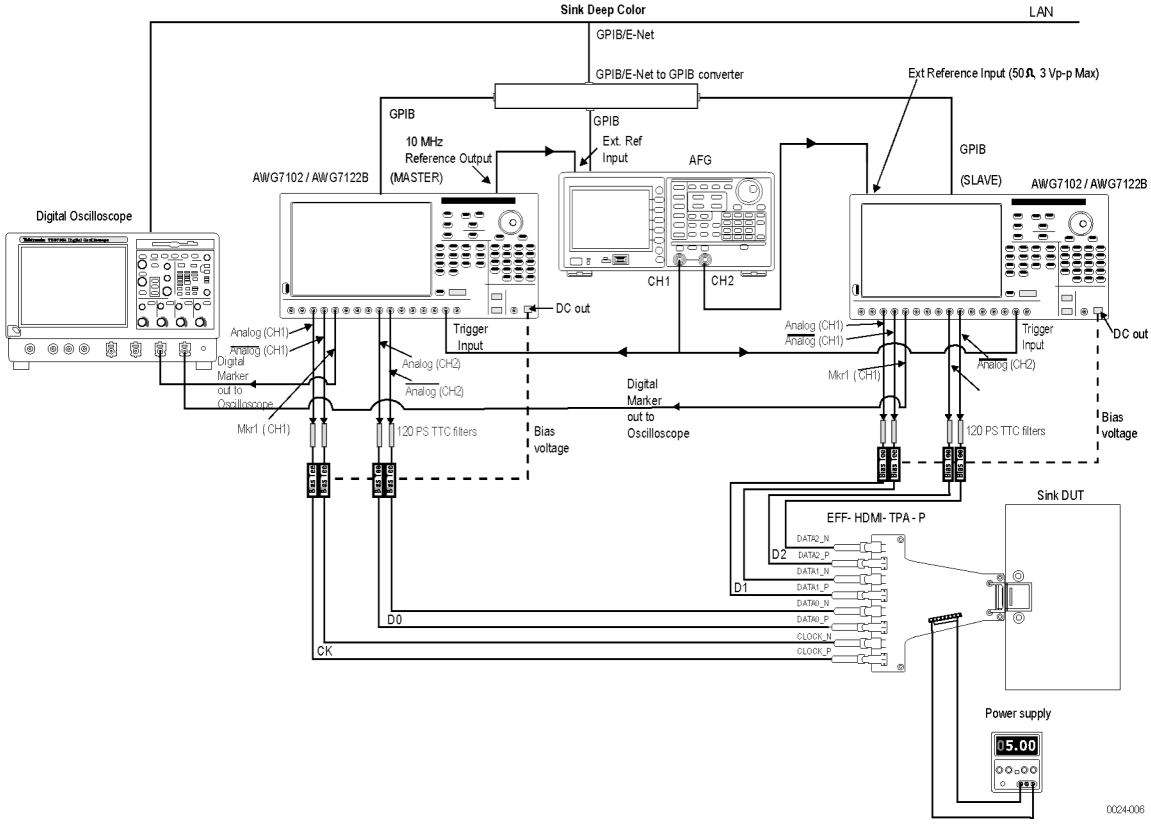
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for 3D Video test compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

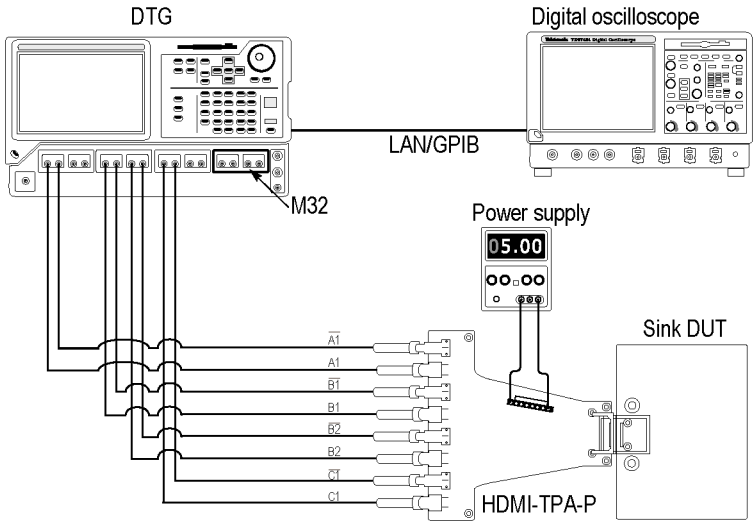
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink 3D Video Test.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the man with a sphere is visible on the DUT.

Make Connections for 4Kx2K Video

On the menu bar, click **Tests > Connect**.

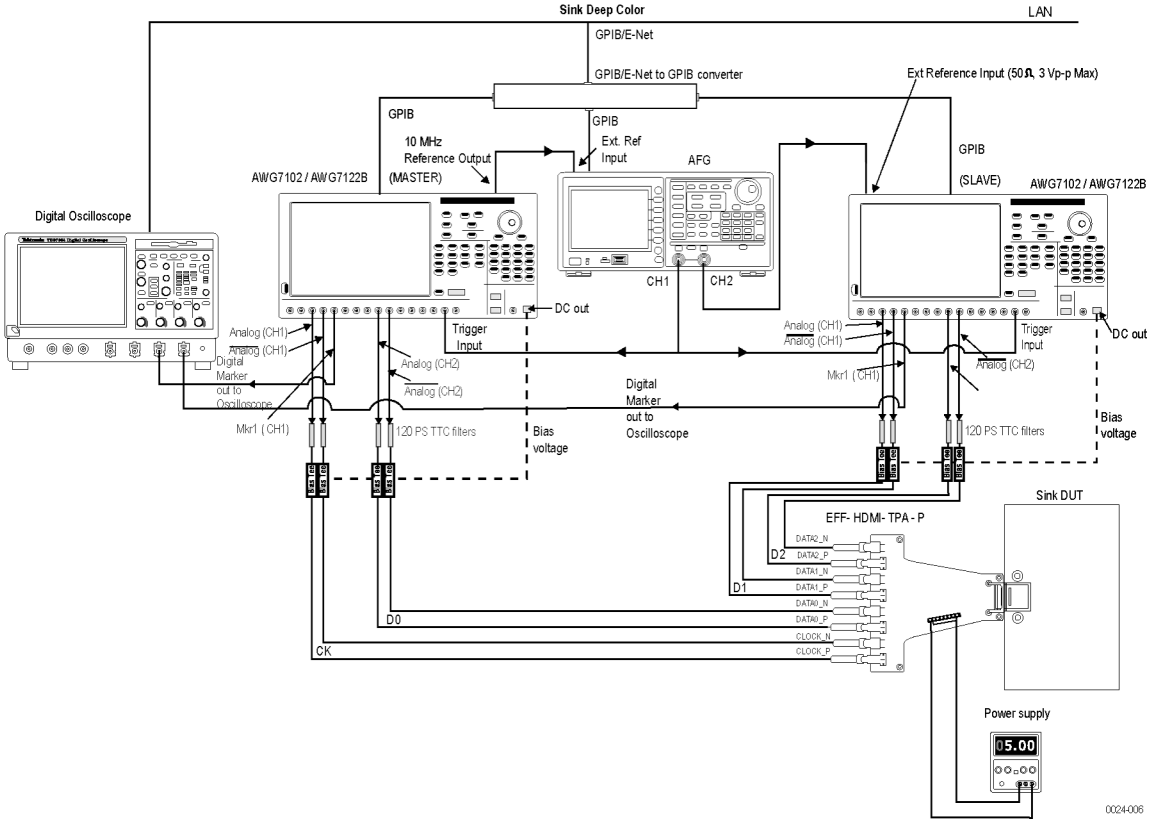
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for 4Kx2K Video test compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

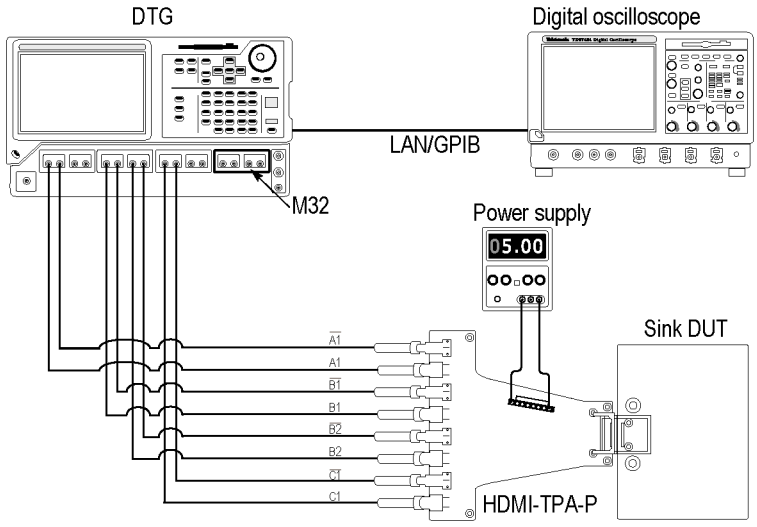
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink 4Kx2K Video Test.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the gray/color bar is visible on the DUT.

Make Connections for Extended Colors and Contents

On the menu bar, click **Tests > Connect**.

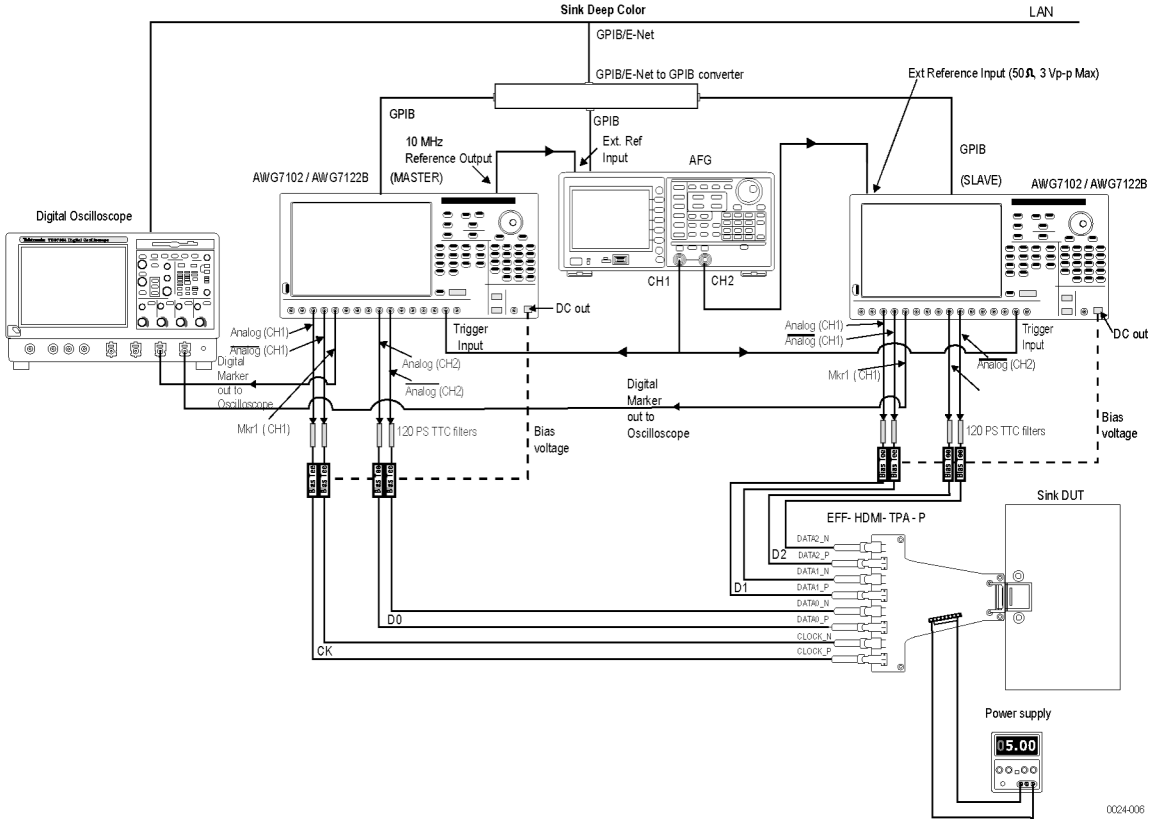
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for Extended Colors and Contents test compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

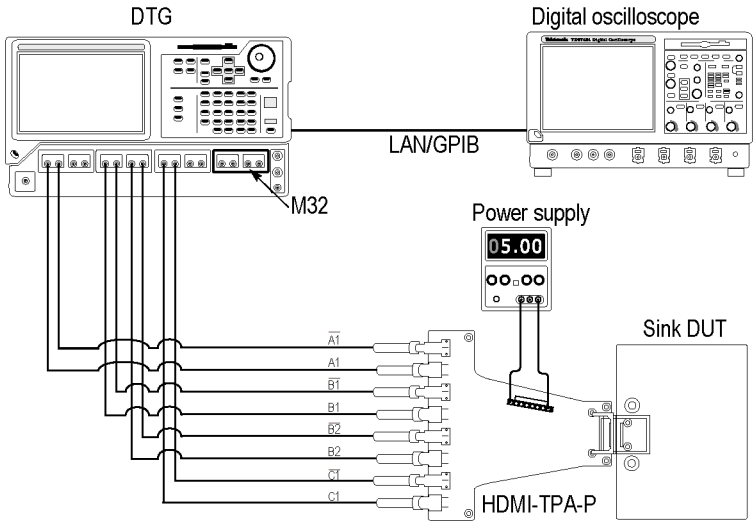
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink Extended Colors and Contents Test.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the gray/color bar is visible on the DUT.

Make Connections for Character Synchronization

On the menu bar, click **Tests > Connect**.

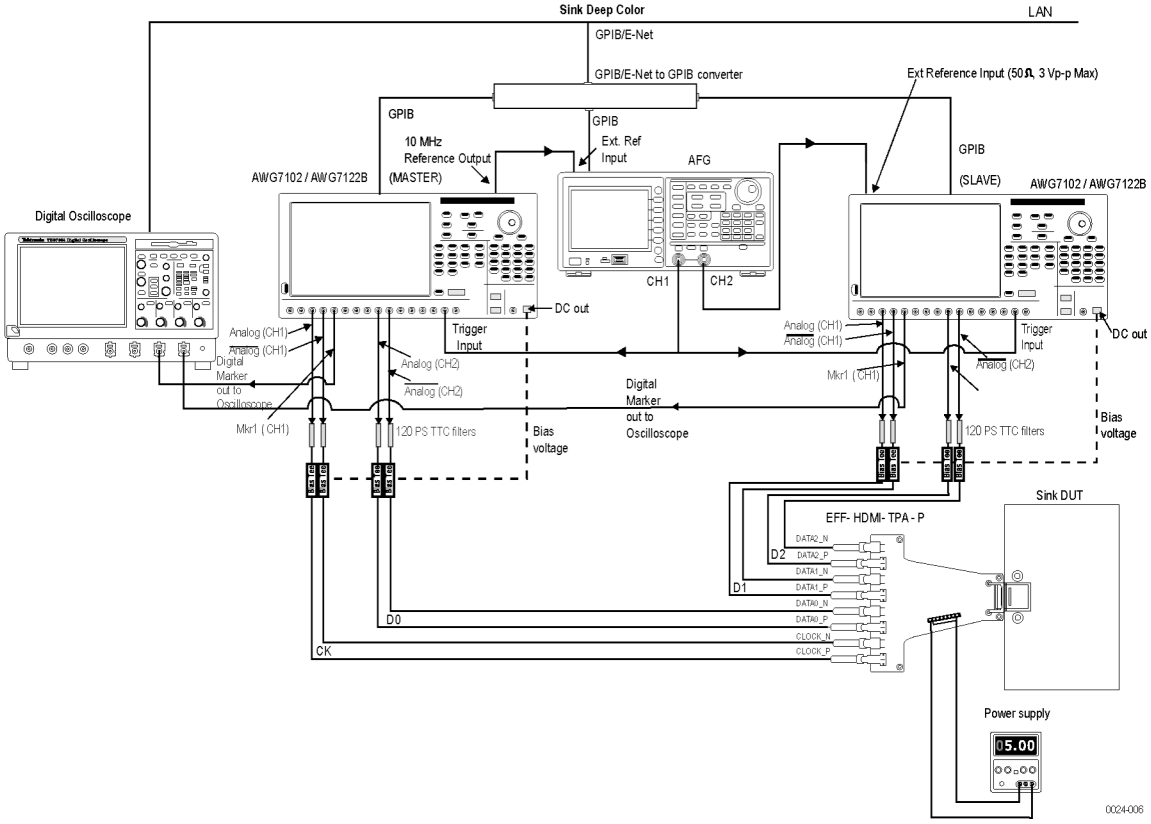
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for Character Synchronization test compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

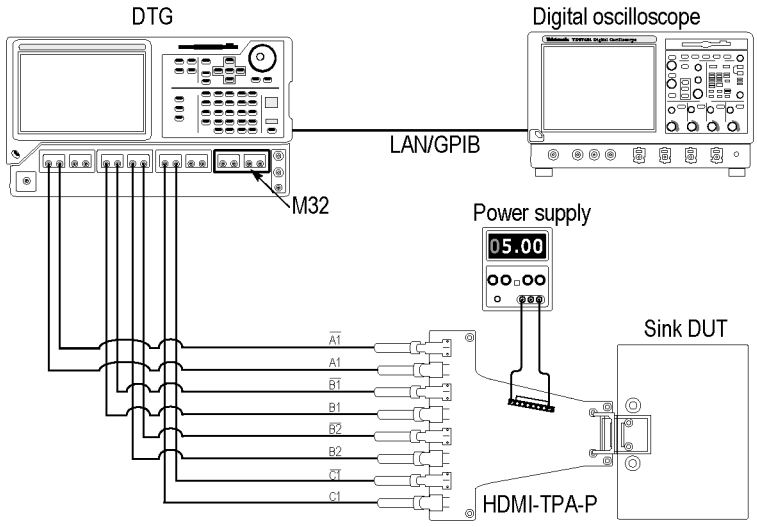
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink Character Synchronization Test.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the gray/color bar is visible on the DUT.

Make Connections for Pixel Encoding Requirements

On the menu bar, click **Tests > Connect**.

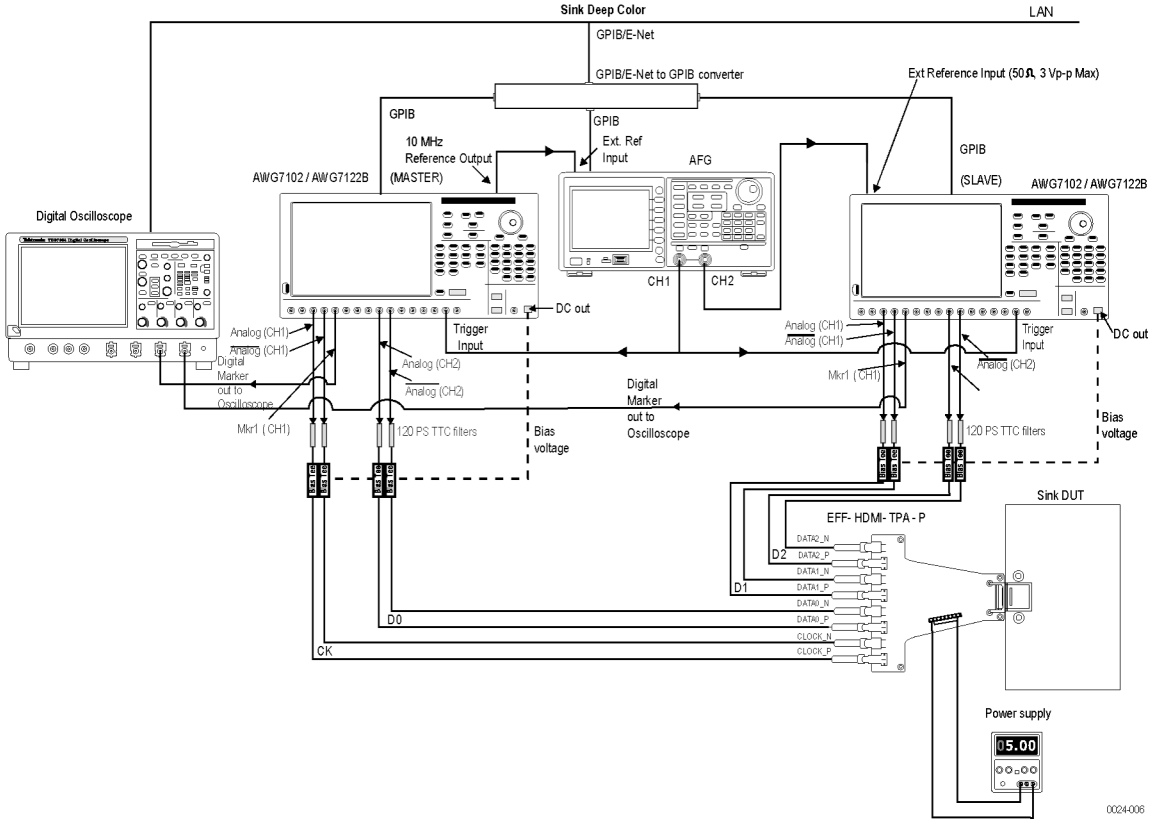
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for Pixel Encoding Requirements test compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

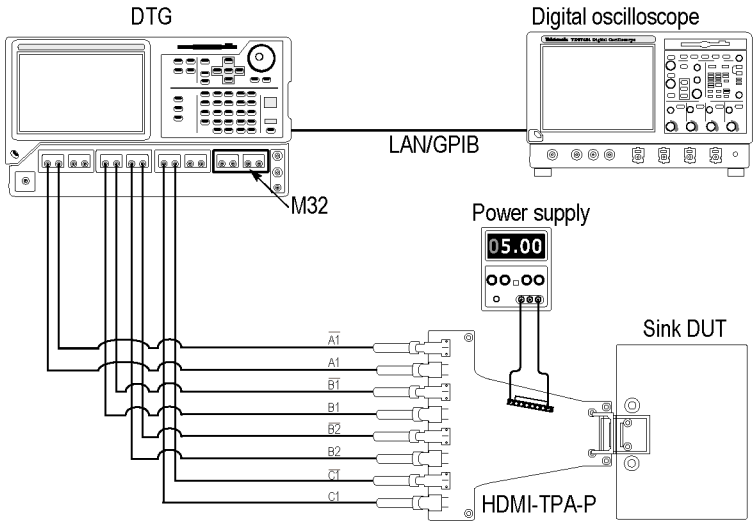
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Pixel Encoding Requirements Test.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the gray/color bar is visible on the DUT.

Make Connections for Acceptance of All Valid Packets

On the menu bar, click **Tests > Connect**.

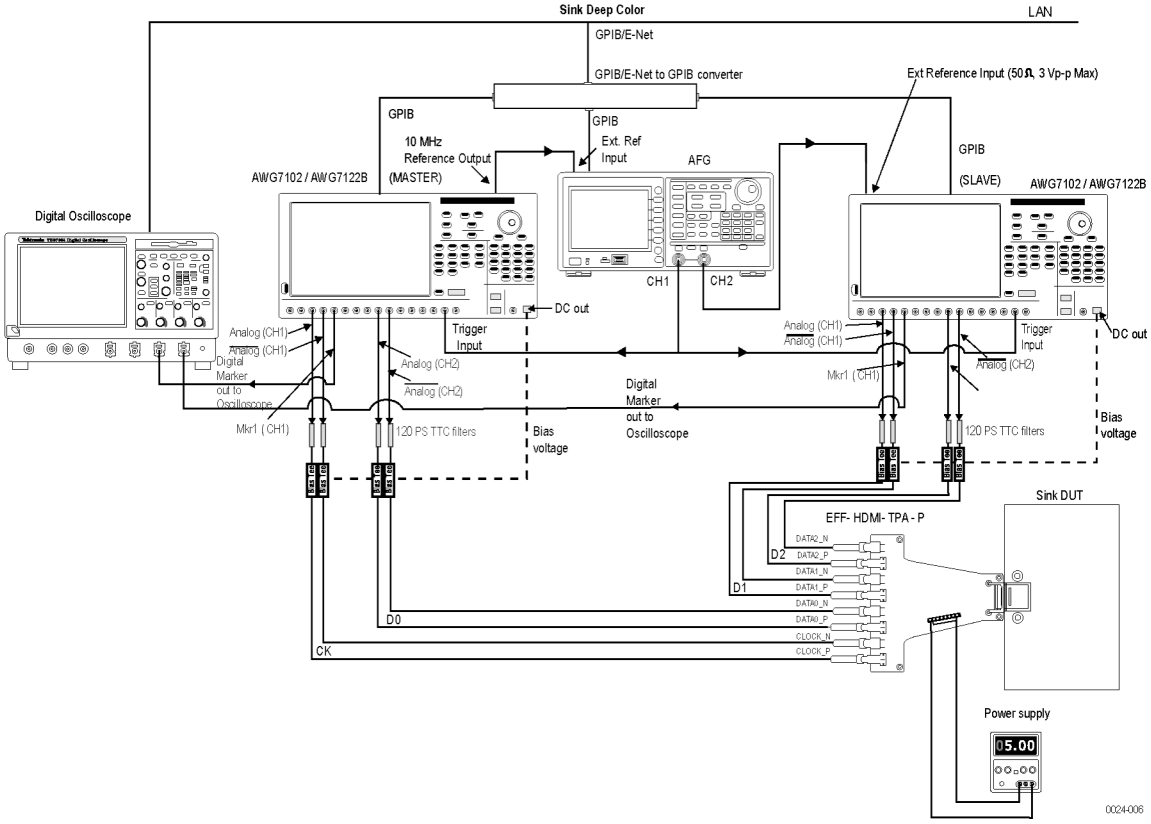
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for Acceptance of All Valid Packets test compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

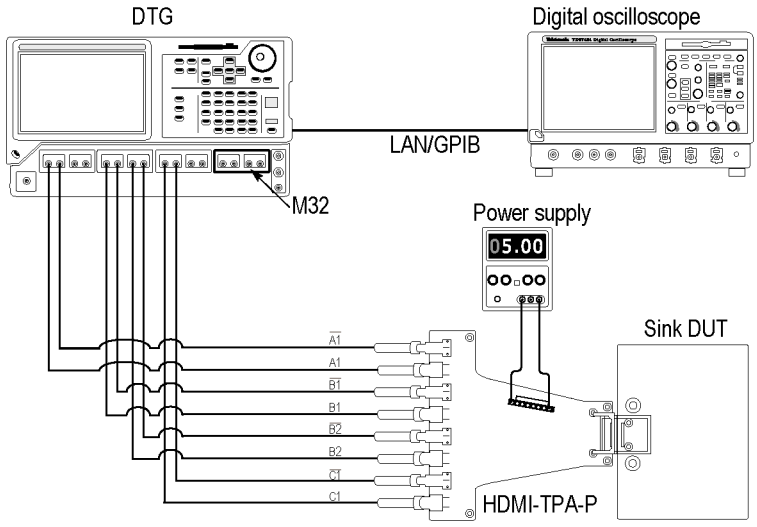
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Acceptance of All Valid Packets Test.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the gray/color bar is visible on the DUT.

Make Connections for Video Format Timing

On the menu bar, click **Tests > Connect**.

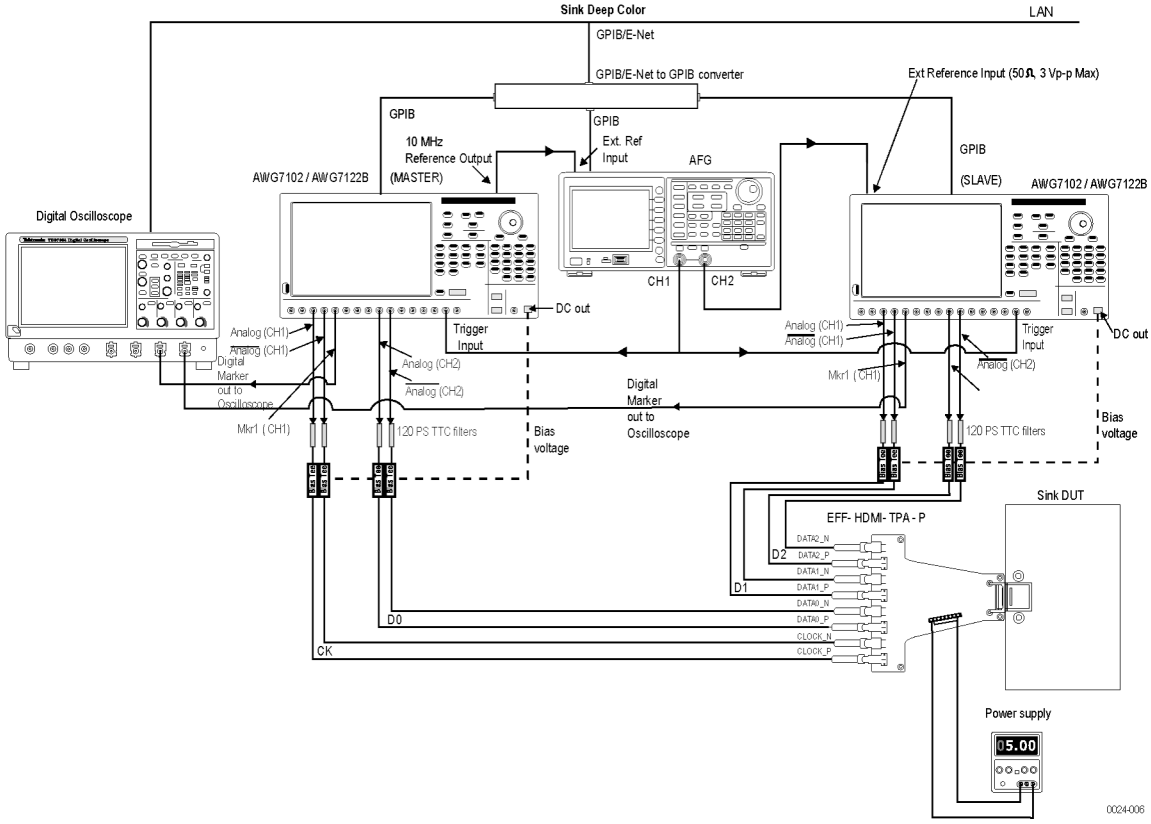
For the DTG Method

Make the connections as follows:



For the DDS Method

To test the Sink DUT for Video Format Timing test compliance.



Perform the following steps for each TMDS clock rate supported by the Sink DUT.

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.

5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Video Format Timing Test.
   - Select the particular pattern(s).
   - Run the measurement.
   - Check if the gray/color bar is visible on the DUT.

Make Connections for Sink Intra-Pair Skew

On the menu bar, click **Tests > Connect**.

NOTE. *The following procedure is for the clock intra-pair skew test. For other pairs, interchange the connection of DATA <X>_P with CLOCK_P and DATA <X>_N with CLOCK_N. Changes the configuration of the DTG Outputs accordingly.*

For example, to calculate the intra-pair skew of Data0:

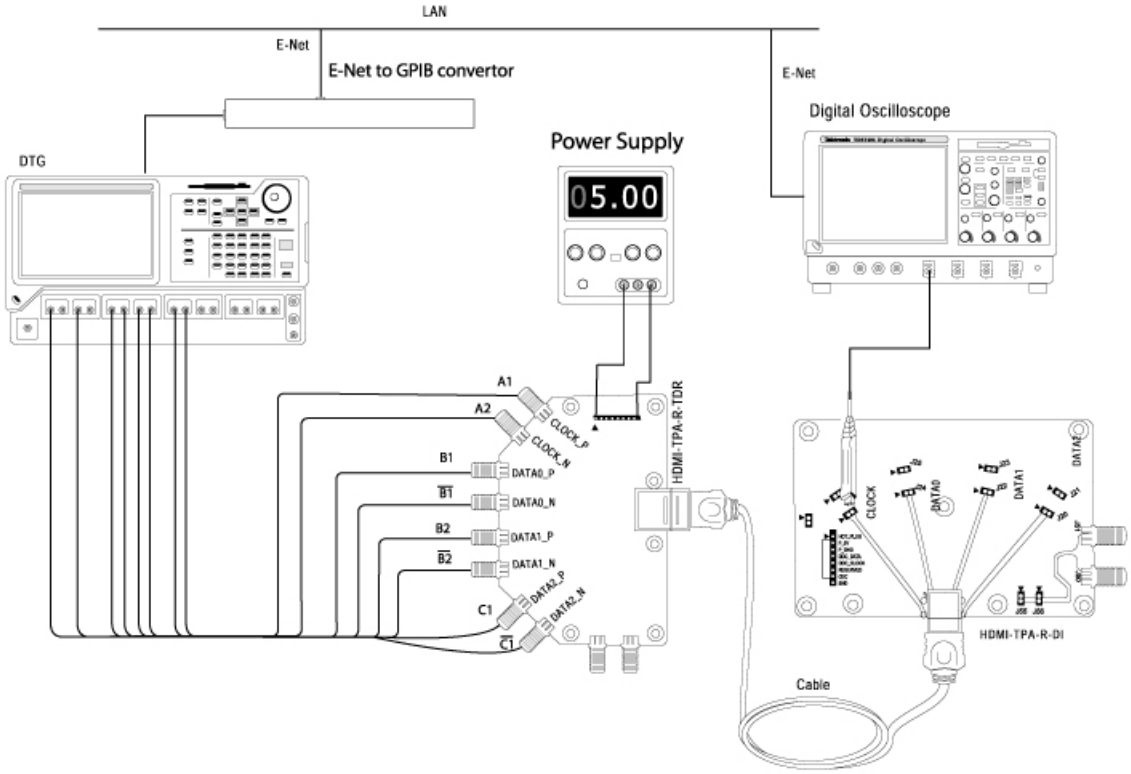
Connect DATA0_P to Module A1+, DATA0_N to DTG Module A2+, CLOCK_P to Module B1+, and CLOCK_N to module B1–.

Method 1: Using HDMI 1.2 test fixtures

Setup 1. To measure Tbit

Make the connections as follows:

NOTE. *Use channel $\overline{A1}$ of the DTG instead of channel A2 (shown in figure) to make connections for Tbit measurements.*

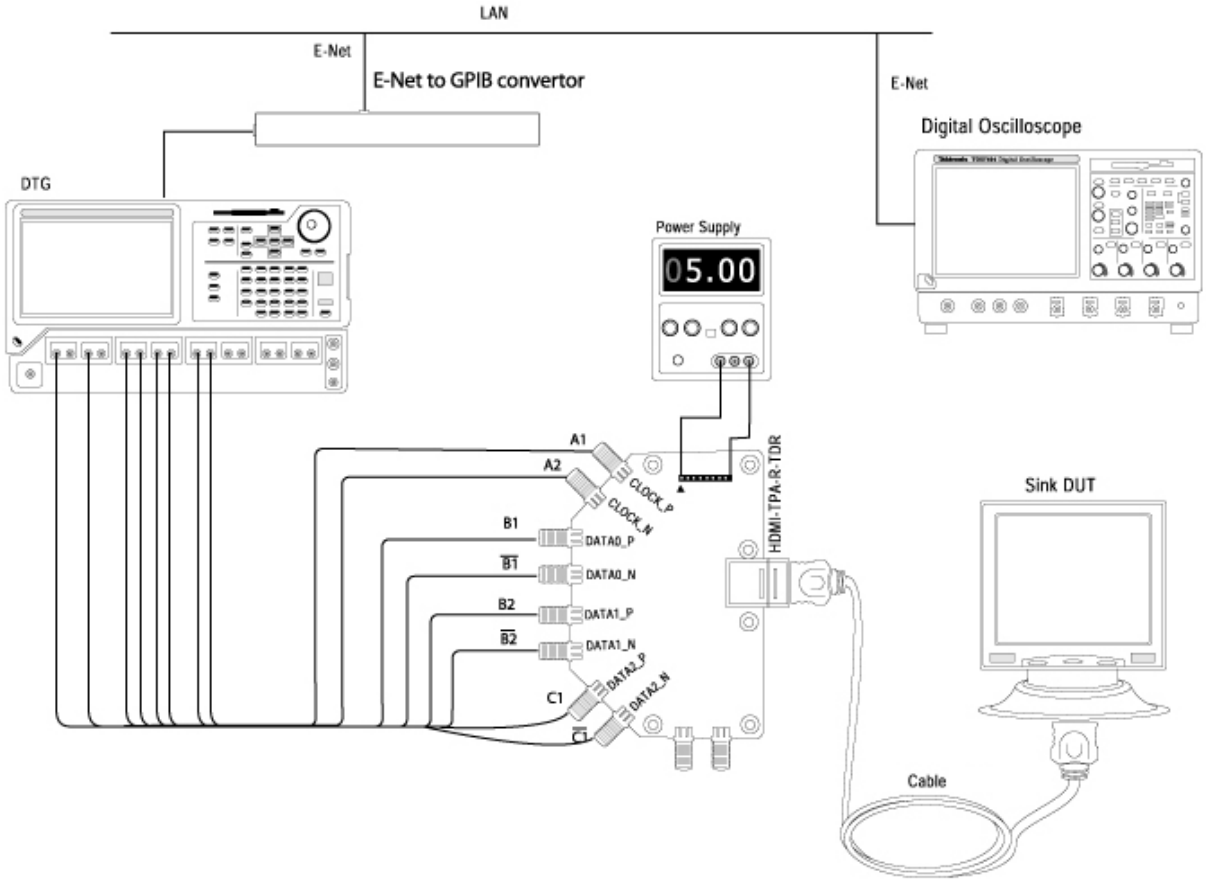


NOTE. *Using the Cable Emulator/Cable is not mandatory. You can connect a TPA-P-TDR fixture directly to the DUT. If you find this inconvenient, use the Cable Emulator/Cable to connect the DUT conveniently.*

1. Connect the DTG to the TPA-R-TDR by using eight one-meter (preferable) or one-and-a-half meter SMA cables:
   - Module A, Channel 1+: Connect to CLOCK_P
   - Module A, Channel 1–: No Connection
   - Module A, Channel 2+: Connect to CLOCK_N
   - Module A, Channel 2-: No Connection
   - Module B, Channel 1+, 1–: Connect to DATA0_P and DATA0_N
   - Module B, Channel 2+, 2–: Connect to DATA1_P and DATA1_N
   - Module C, Channel 1+, 1–: Connect to DATA1_P and DATA1_N
   - Module C, Channel 2+, 2–: No Connection
2. Connect the TPA-R-TDR to the Cable Emulator.
3. Connect the TPA-R-DI to the Cable Emulator.
4. Connect a Clock to the configured oscilloscope channel by using a differential probe.

Setup 2. To find intra-pair skew of the Sink DUT

Make the connections as follows:



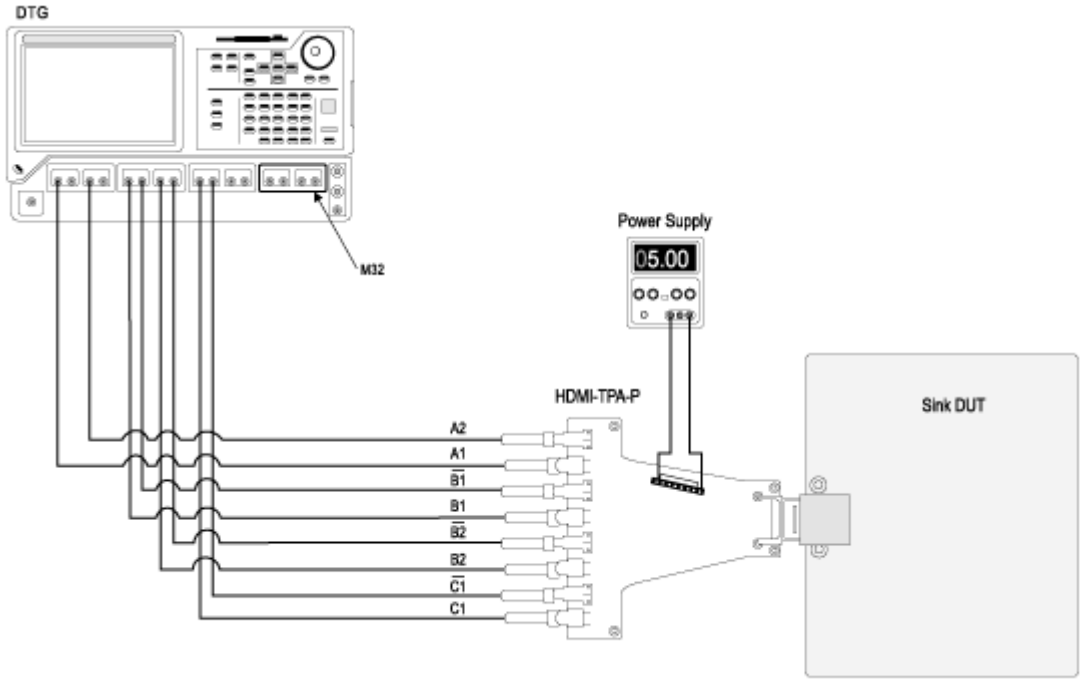
NOTE. *Using the Cable Emulator/Cable is not mandatory. You can connect a TPA-P-TDR fixture directly to the DUT. If you find this inconvenient, use the Cable Emulator/Cable to connect the DUT conveniently.*

1. Remove the TPA-R-DI test fixture from the Cable Emulator.
2. Connect the Sink DUT to the Cable Emulator.
3. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.

Method 2: Using Efficere test fixtures

Setup 1. To find intra-pair skew of the Sink DUT with the Efficere Test Fixture

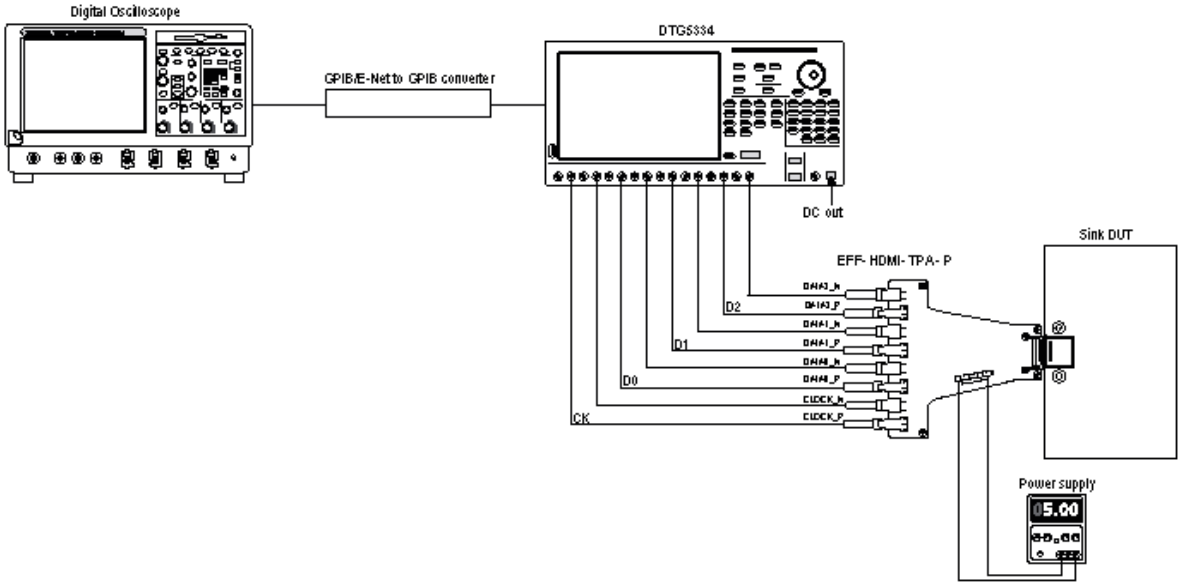
Make the connections as follows:



- Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the HDMI-TPA-P.
- Configure the DUT to receive the HDMI input signal.

For 4-Channel.

Make the connections as follows:

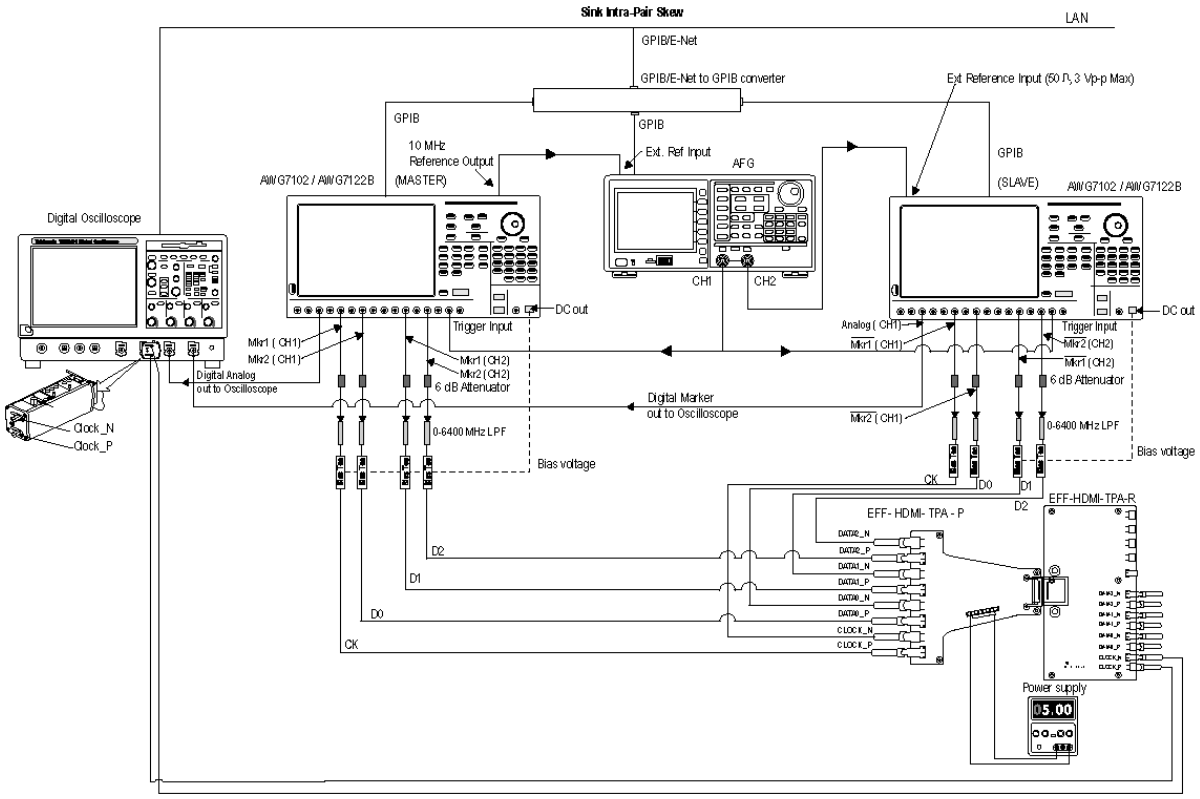


- Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the HDMI-TPA-P.
- Configure the DUT to receive the HDMI input signal.
- Run the Sink Intra-Pair skew test using TDSHT3 software to execute the 4-channel intra-pair skew measurement.
- Once the test completes, you can view the result.

For the DDS Method

Step 1: To measure Tbit

Make the connections as follows:



NOTE. *Terminate the lanes that are not connected with a 50 ohm terminator using a Bias-T which is pulled up to 3.3 V.*

1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Channel1+ output to oscilloscope Ch3 input
   - AWG2 Channel1+ output to oscilloscope Ch4 input
   - AWG1 Marker1 (Ch1) output to 6 dB attenuator

- 6 dB attenuator to 0-6400 MHz low pass filter
- 0-6400 MHz low pass filter output to Bias-Tee #1 signal input (RF)
- Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
- AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)

- AWG1 Marker2 (Ch1) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Marker1 (Ch2) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG1 Marker2 (Ch2) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 $\overline{\text{Marker1}}$ (Ch1) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #2 signal input (RF)
  - Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
  - AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)
- AWG2 $\overline{\text{Marker2}}$ (Ch1) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 $\overline{\text{Marker1}}$ (Ch2) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter

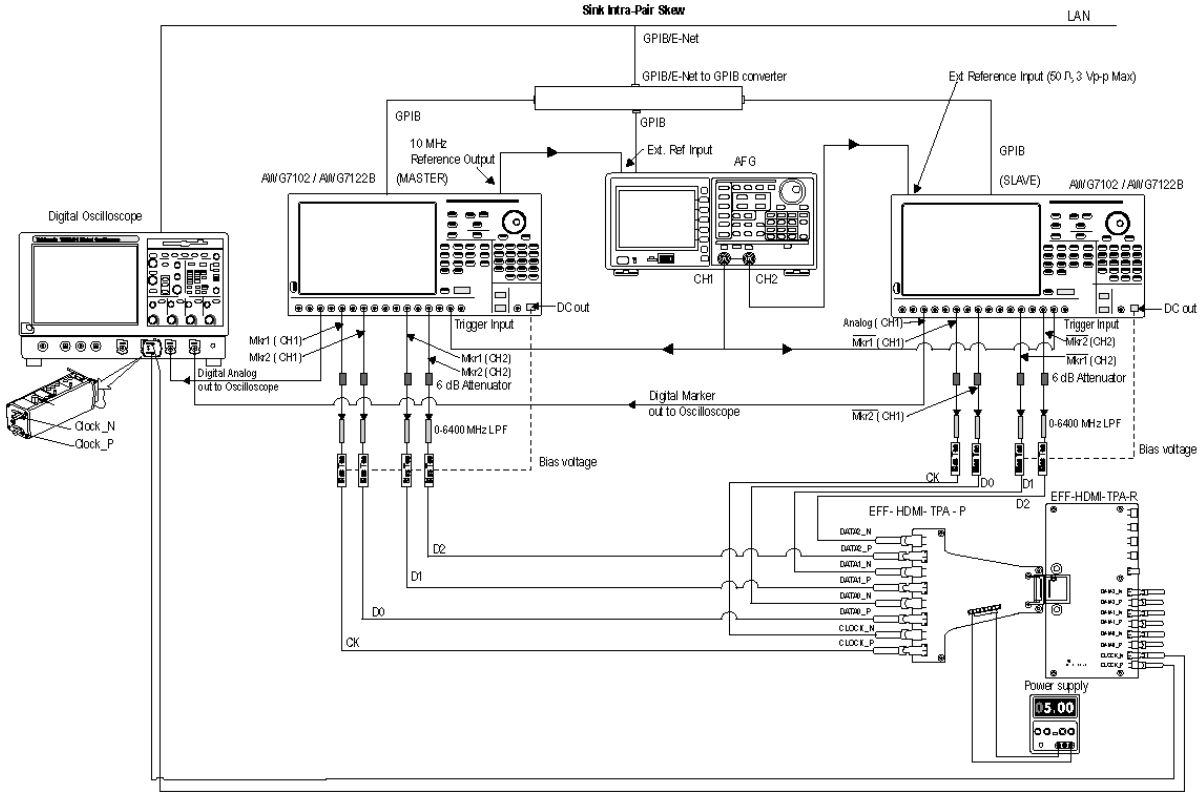
- 0-6400 MHz low pass filter output to Bias-Tee #6 signal input (RF)
- Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
- AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)

- AWG2 $\overline{\text{Marker2}}$ (Ch2) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to TPA-R.
5. Connect the Clock output of the TPA-R to the configured oscilloscope channel by using a differential probe.
6. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
7. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink Intra-Pair Skew Test.
   - Select the resolution of the DUT to be tested.
   - Run the measurement to calculate T-bit.
   - Determine the skew to be applied on the channels using the calculated T-bit.

Step 2: To perform Intra-Pair Skew test on the Sink DUT using skew on one channel

Make the connections as follows:



1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Channel1+ output to oscilloscope Ch3 input
   - AWG2 Channel1+ output to oscilloscope Ch4 input
   - AWG1 Marker1 (Ch1) output to 6 dB attenuator
     - 6 dB attenuator to 0-6400 MHz low pass filter
     - 0-6400 MHz low pass filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 $\overline{\text{Marker1}}$ (Ch1) output to 6 dB attenuator

- 6 dB attenuator to 0-6400 MHz low pass filter
- 0-6400 MHz low pass filter output to Bias-Tee #2 signal input (RF)
- Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
- AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Marker2 (Ch1) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 $\overline{\text{Marker2}}$ (Ch1) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG1 Marker1 (Ch2) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 $\overline{\text{Marker1}}$ (Ch2) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG1 Marker2 (Ch2) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG1 $\overline{\text{Marker2}}$ (Ch2) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter

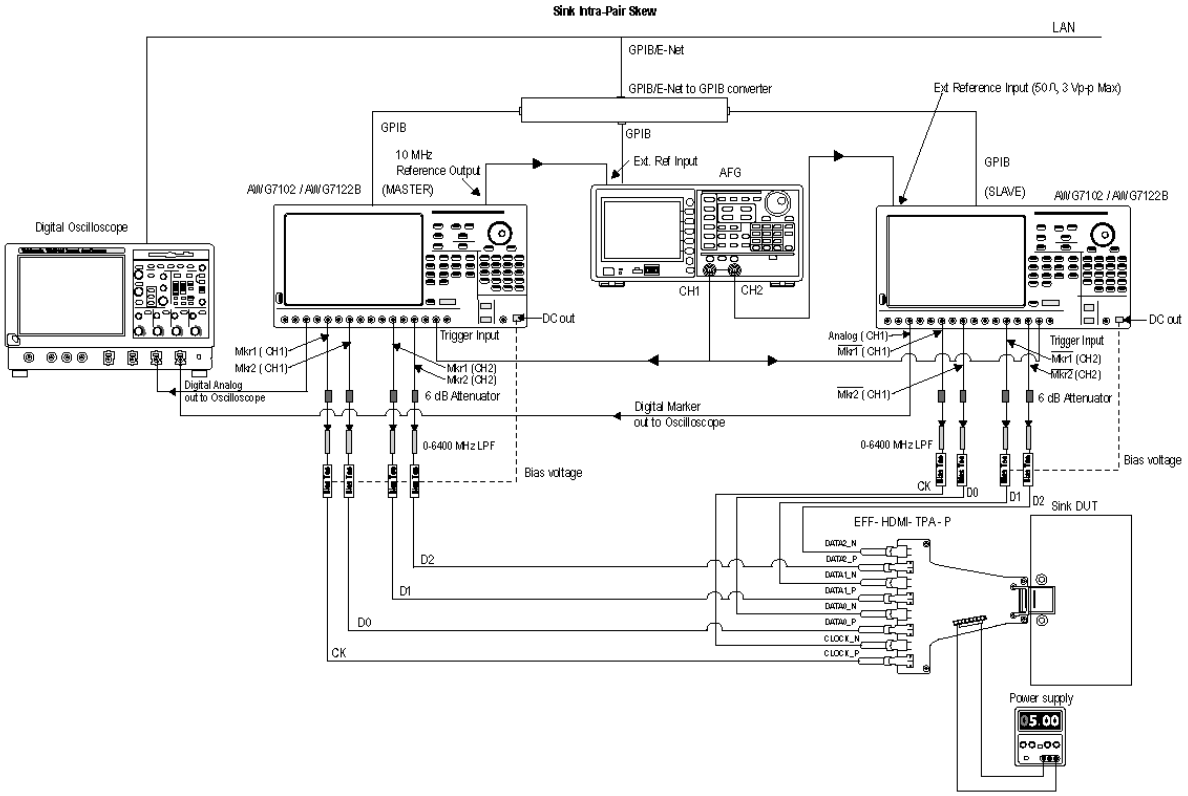
- 0-6400 MHz low pass filter output to Bias-Tee #8 signal input (RF)
- Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
- AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)

- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink Intra-Pair Skew Test.
   - Select the resolution of the DUT to be tested.
   - In the Signal Source dialog box, check the GPIB connection of the two AWGs and the AFG to ensure proper connection.
   - The TDSHT3 software will also change the skew in 0.1 TBit steps automatically, for example, 0.0TBIT, 0.1TBIT, until 0.6TBIT. In each step, you will be prompted to confirm if the DUT adequately supports the signal.
   - Once the test completes, you can view the result.

Step 3: To perform Intra-Pair Skew test on the Sink DUT using skew on all channels

Make the connections as follows:



1. Ensure that the Sink DUT port on which you perform the test is selected.
2. Connect the test equipment and DUT.
3. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Channel1+ output to oscilloscope Ch3 input
   - AWG2 Channel1+ output to oscilloscope Ch4 input
   - AWG1 Marker1 (Ch1) output to 6 dB attenuator
     - 6 dB attenuator to 0-6400 MHz low pass filter
     - 0-6400 MHz low pass filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)

- AWG1 Marker2 (Ch1) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Marker1 (Ch2) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG1 Marker2 (Ch2) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 $\overline{\text{Marker1}}$ (Ch1) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #2 signal input (RF)
  - Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
  - AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)
- AWG2 $\overline{\text{Marker2}}$ (Ch1) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 $\overline{\text{Marker1}}$ (Ch2) output to 6 dB attenuator
  - 6 dB attenuator to 0-6400 MHz low pass filter
  - 0-6400 MHz low pass filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 $\overline{\text{Marker2}}$ (Ch2) output to 6 dB attenuator

- 6 dB attenuator to 0-6400 MHz low pass filter
- 0-6400 MHz low pass filter output to Bias-Tee #8 signal input (RF)
- Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
- AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)

- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

4. Connect TPA-P to Sink DUT.
5. Connect and configure the DC power supply to drive +5 V between +5 V Power (P_5V) and DDC/CEC Ground (P_GND) on the TPA-R-TDR.
6. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Sink Intra-Pair Skew Test.
   - Select the resolution of the DUT to be tested.
   - In the Signal Source dialog box, check the GPIB connection of the two AWGs and the AFG to ensure proper connection.
   - The TDSHT3 software will also change the skew in 0.1 TBit steps automatically, for example, 0.0TBIT, 0.1TBIT, until 0.6TBIT. In each step, you will be prompted to confirm if the DUT adequately supports the signal.
   - Once the test completes, you can view the result.

Make Connections for Cable Eye Diagram (Passive and Active)

On the menu bar, click **Tests > Connect**.

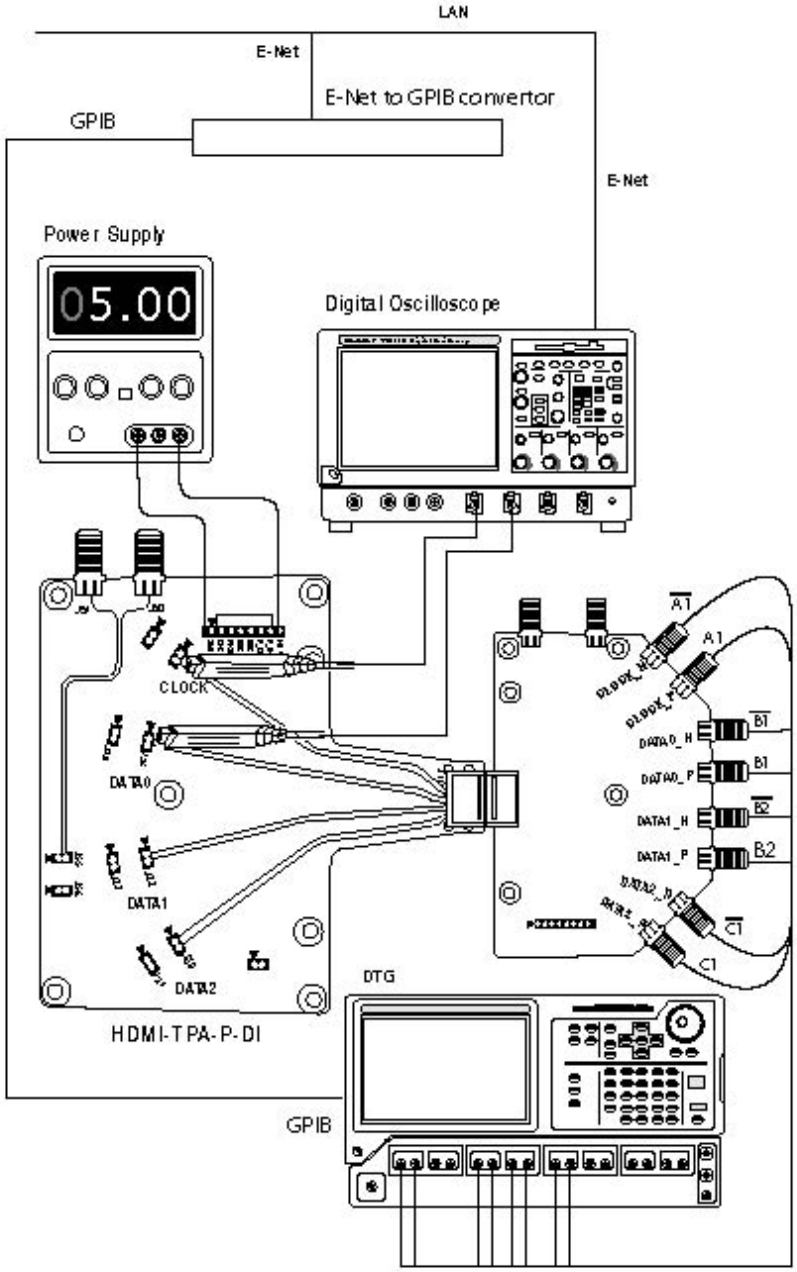
NOTE. *Passive and Active Cable Eye Diagram tests use the same connection, test, and waveform view procedures.*

For the DTG Method

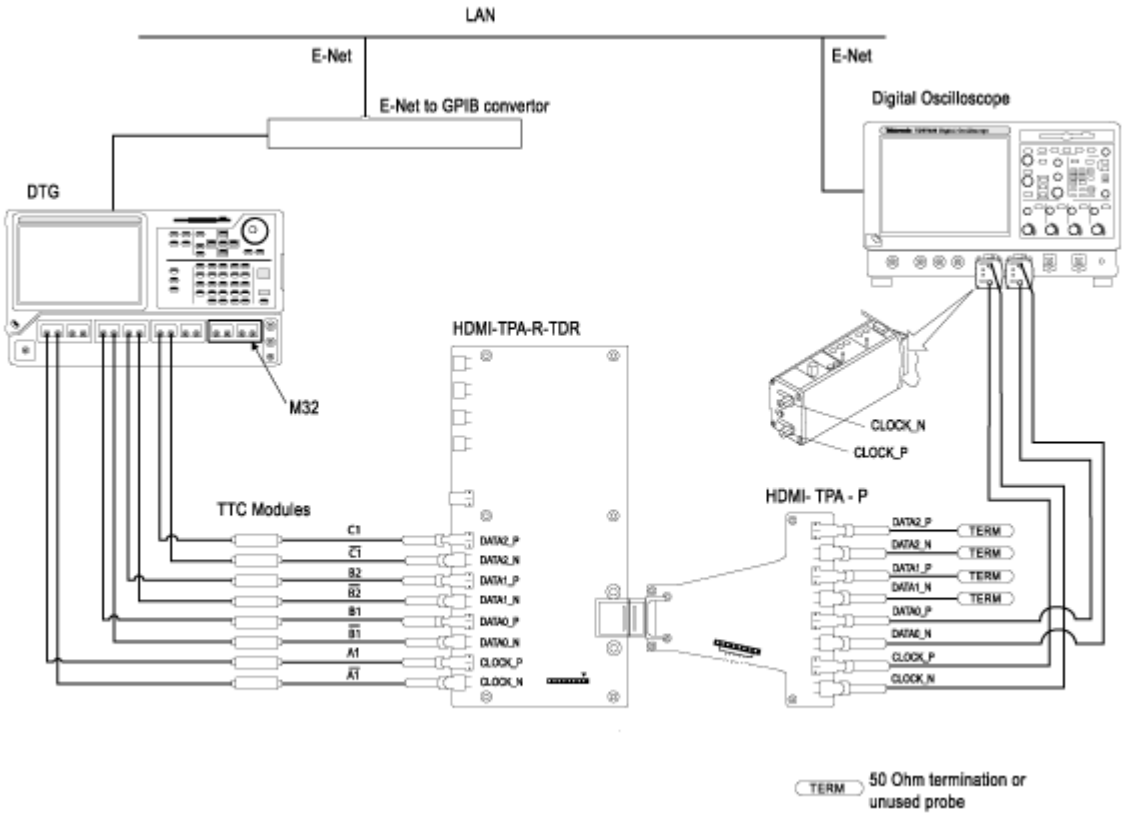
Setup diagram for TP1

Make the connections as follows:

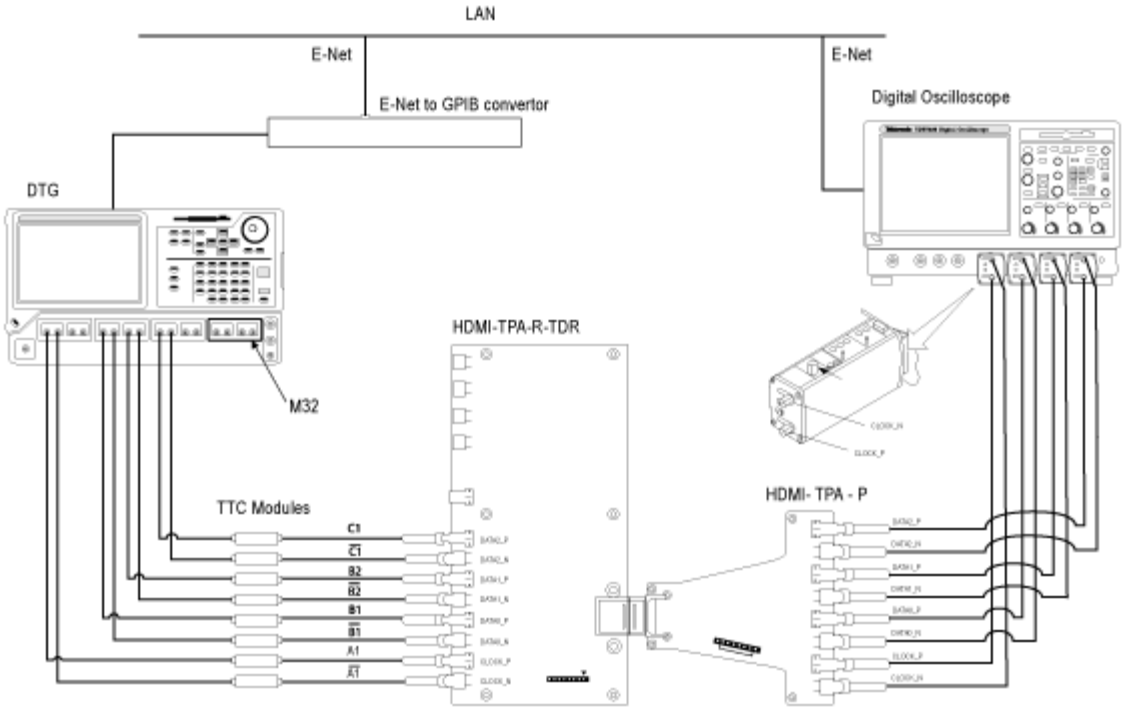
Method 1: Using HDMI 1.2 test fixtures



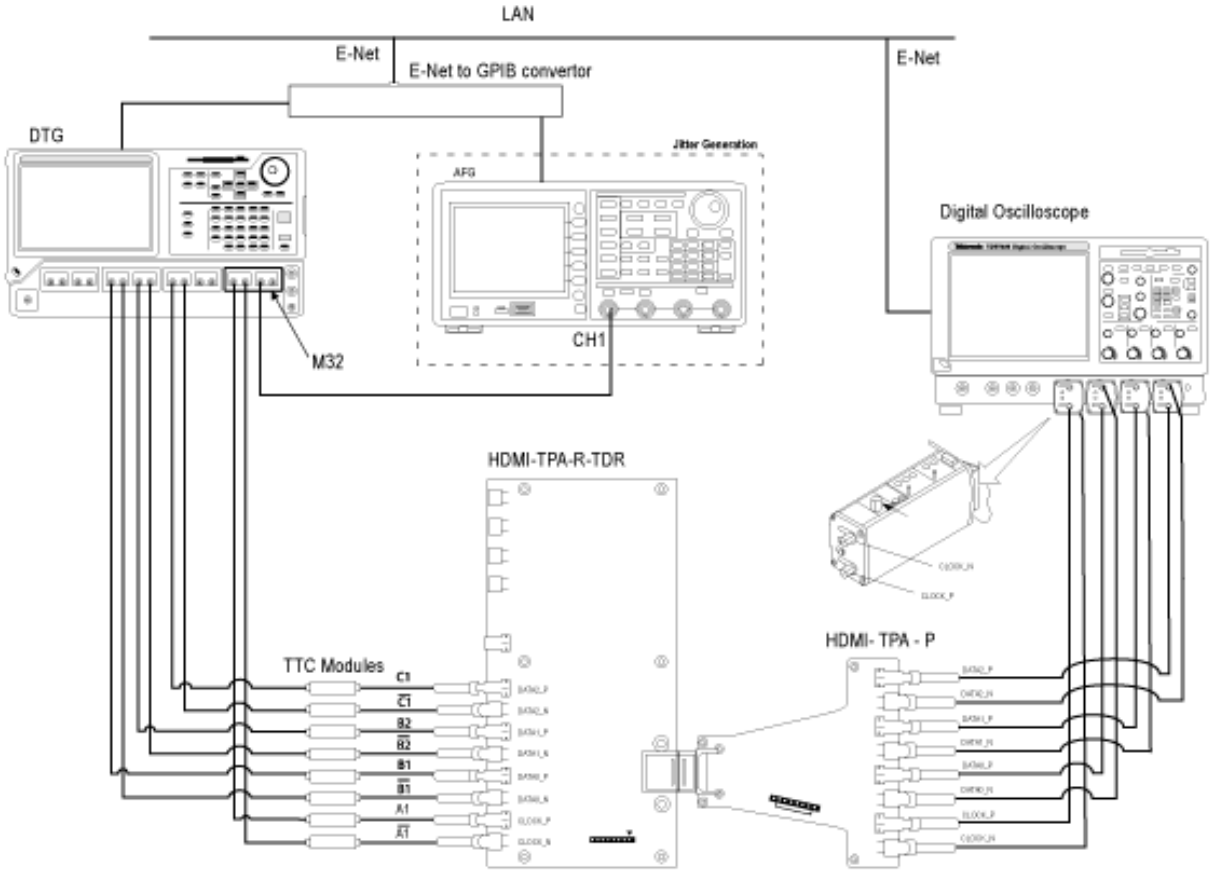
Method 2: Using Efficere test fixtures



For 4-Channel



For 4-Channel with AFG Jitter Insertion



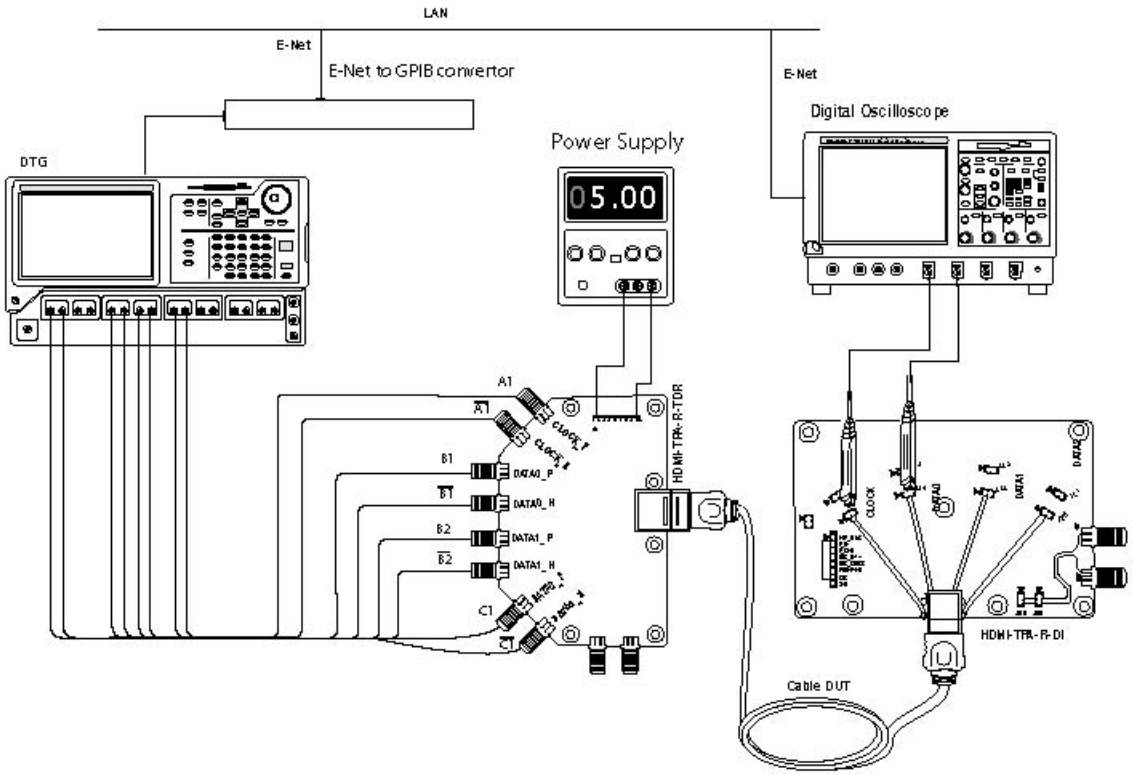
1. Connect the DTG to the “input” TPA-P-TDR/ET-TPA-P adapter by using eight one-meter (preferable) or one-and-a-half meter SMA cables:
   - Module A, Channel 1+, 1–: Connect to CLOCK_P and CLOCK_N
   - Module A, Channel 2+, 2–: No Connection
   - Module B, Channel 1+, 1–: Connect to DATA0_P and DATA0_N
   - Module B, Channel 2+, 2–: Connect to DATA1_P and DATA1_N
   - Module C, Channel 1+, 1–: Connect to DATA2_P and DATA2_N
   - Module C, Channel 2+, 2–: No Connection
2. Connect the oscilloscope to the “output” TPA-R-DI adapter by using two/four differential probes, and supply 3.3 V power.

3. Connect a TMDS Clock to the configured oscilloscope channel by using a differential probe.
4. Connect the TMDS Data pair(s) on which you will conduct the test to the configured oscilloscope channel by using a second differential probe(s).

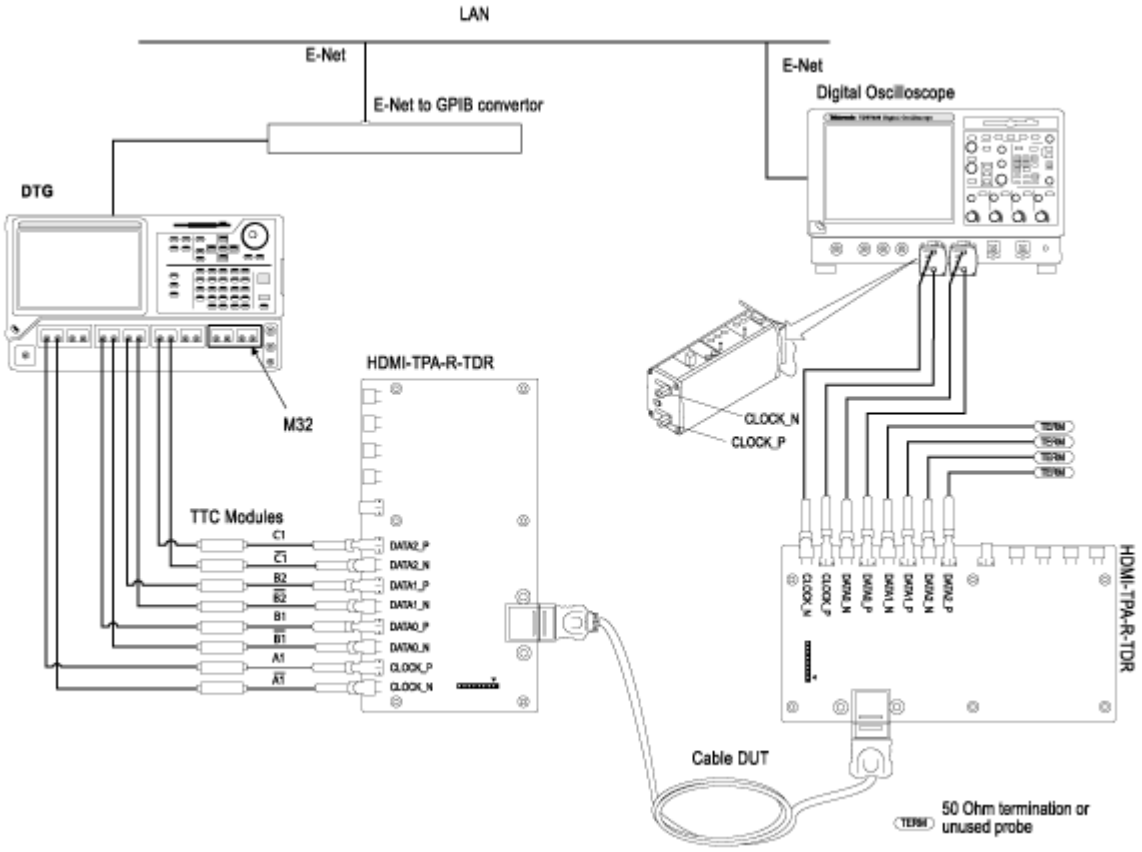
Setup diagram for TP2

Make the connections as follows:

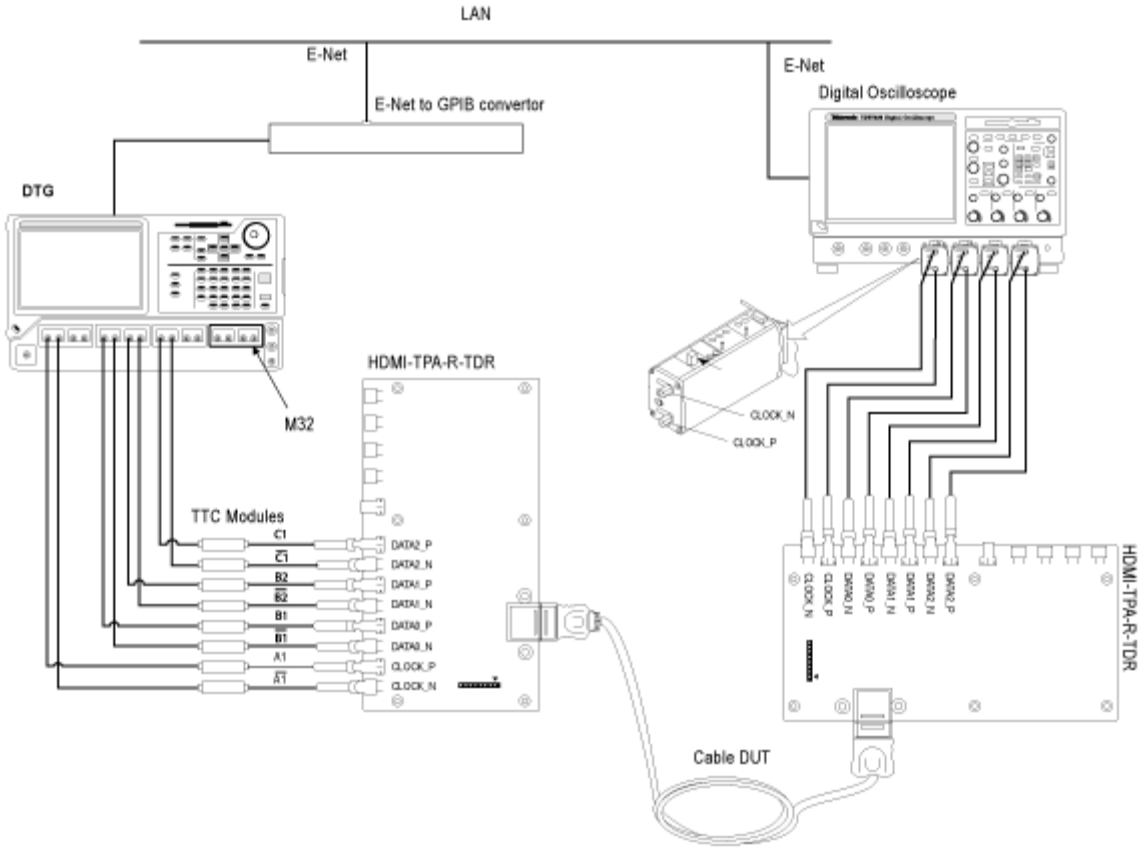
Method 1: Using HDMI 1.2 test fixtures



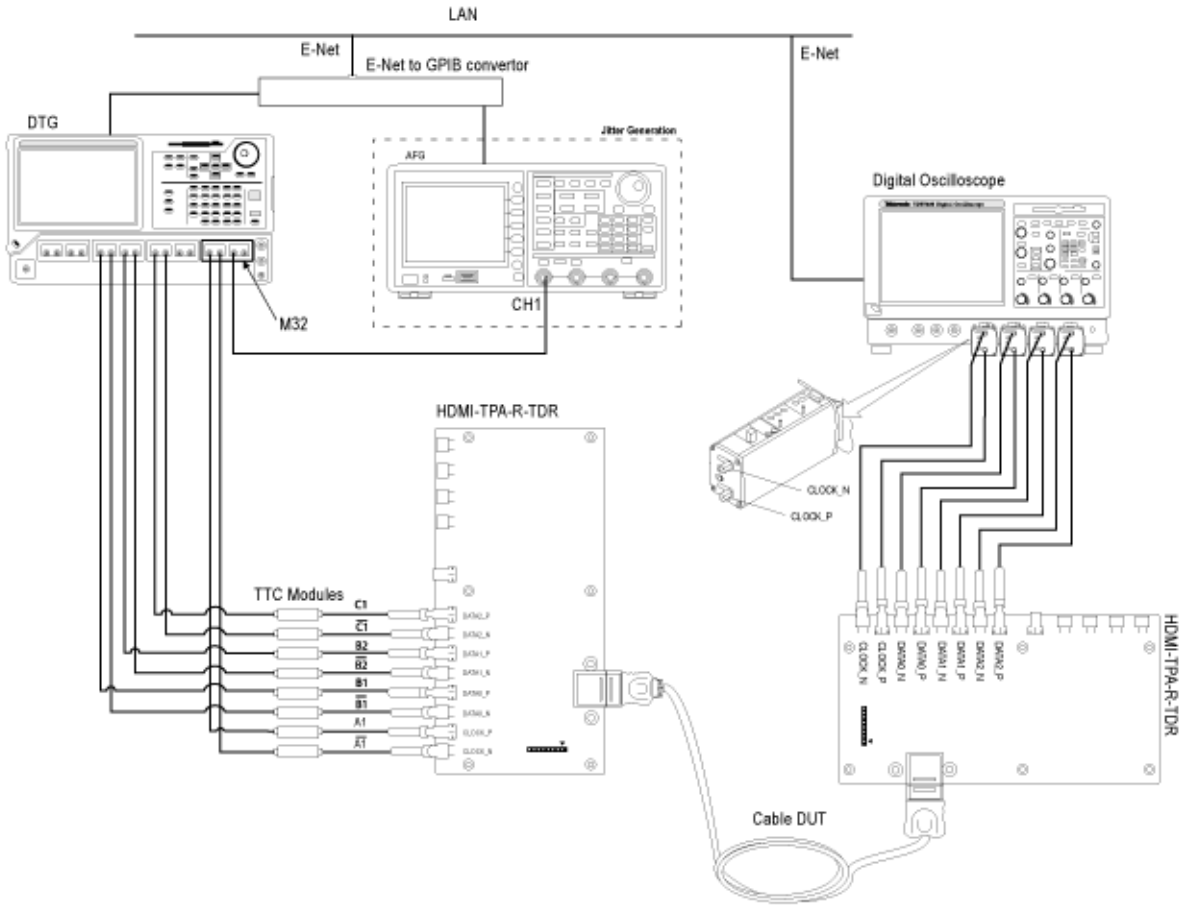
Method 2: Using Efficere test fixtures



For 4-Channel



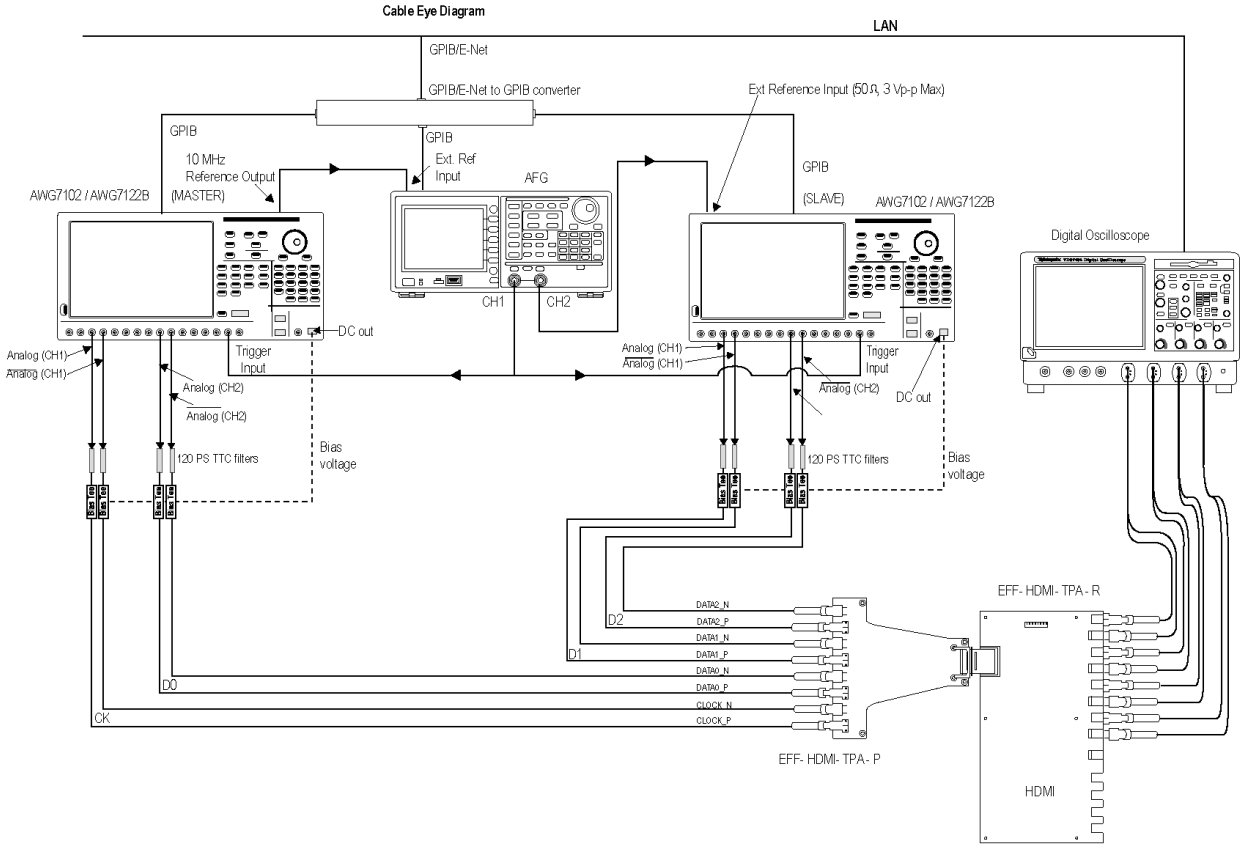
For 4-Channel with AFG Jitter Insertion



1. Remove the TPA-P-DI/ET-TPA-P test adapter.
2. Connect the Cable DUT.
3. Connect the TPA-R-DI test adapter.
4. Connect a TMDS Clock to the configured oscilloscope channel by using a differential probe.
5. Connect the TMDS Data pair(s) on which you will conduct the test to the configured oscilloscope channel by using a second differential probe(s).

For the DDS Method

Setup 1: To confirm worst case TP1 signal



Perform the following steps for each TMDS clock rate supported by the HDMI Cable DUT.

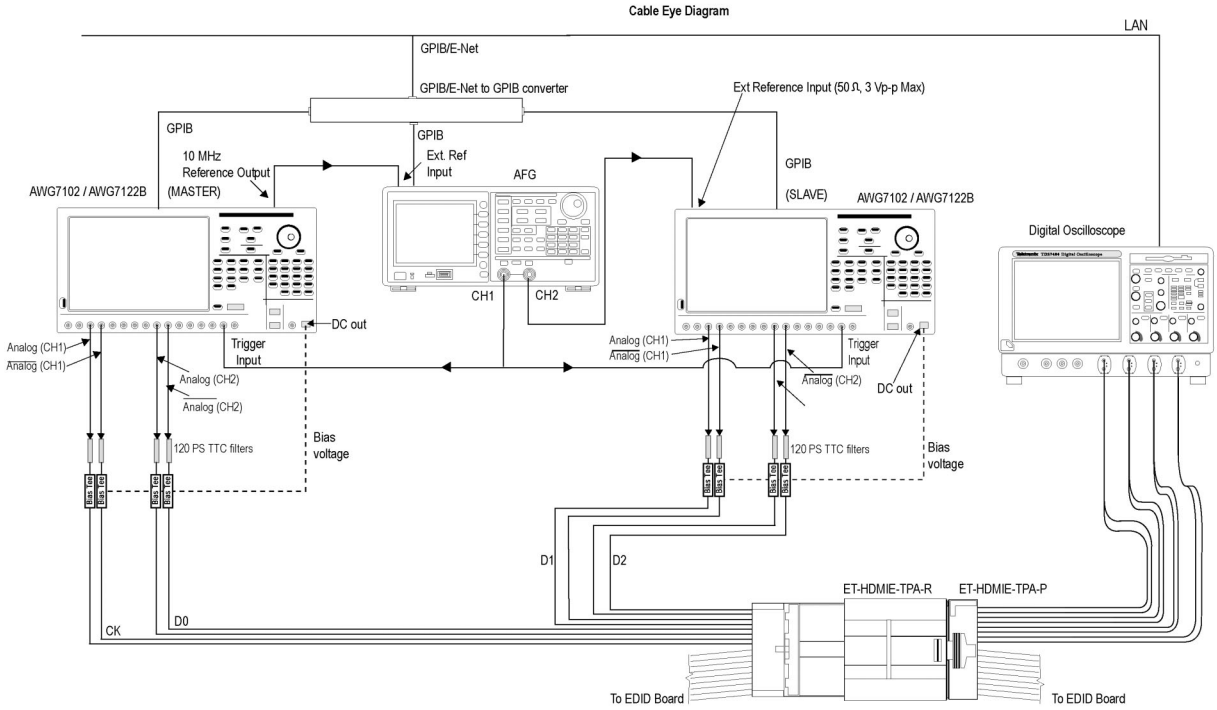
1. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, TPA-P, and TPA-R as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
     - Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
     - AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)

- AWG1 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
  - Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
  - AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

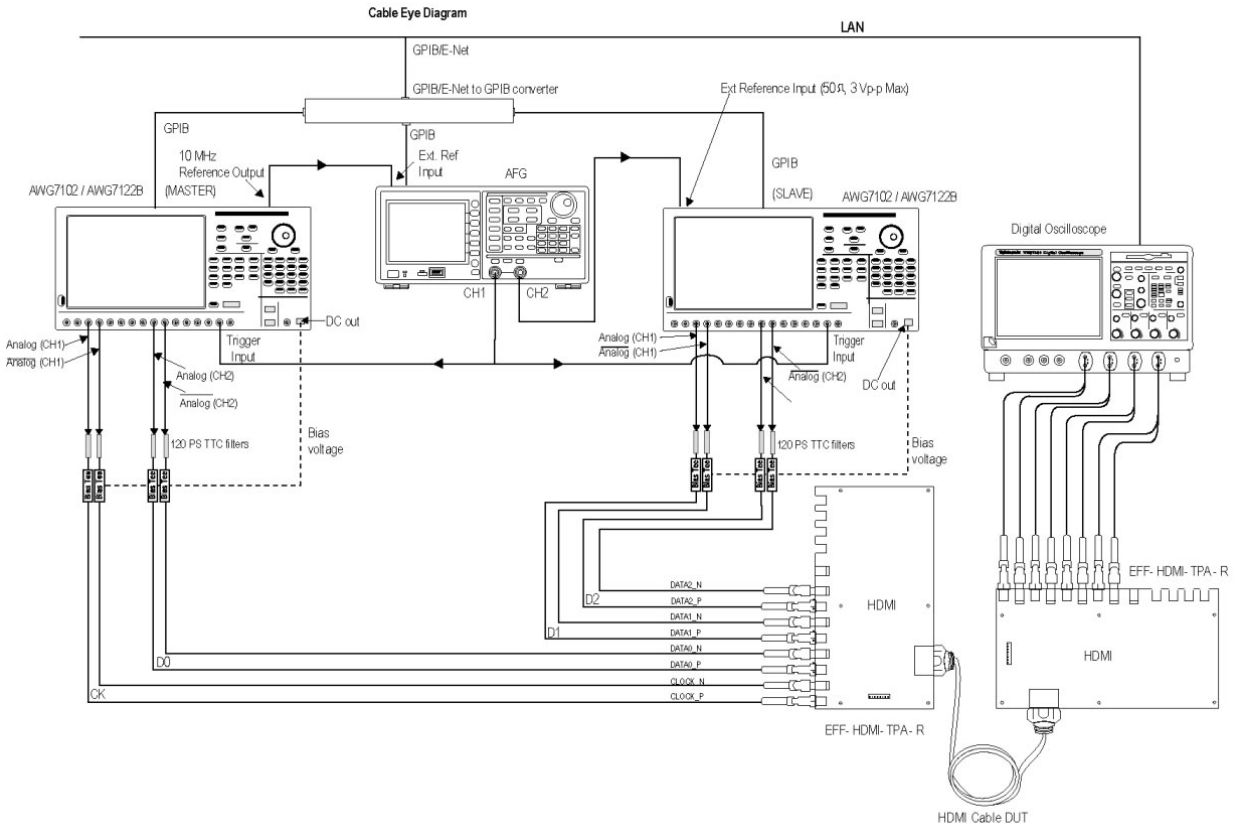
2. Connect TPA-P to TPA-R.

3. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Cable Eye Diagram Test.
   - Select the cable frequency based on the category of the cable (74 MHz, 165 MHz, 340 MHz, 74 MHz Type-E).
   - In the Signal Source dialog box, check the GPIB connection of the two AWGs and the AFG to ensure proper connection.
   - Once the test completes, you can verify the TP1/TP5 worst case eye diagram.

Setup 2: To confirm worst case TP1 signal using Type-E fixture



Setup 3: To test the Cable DUT

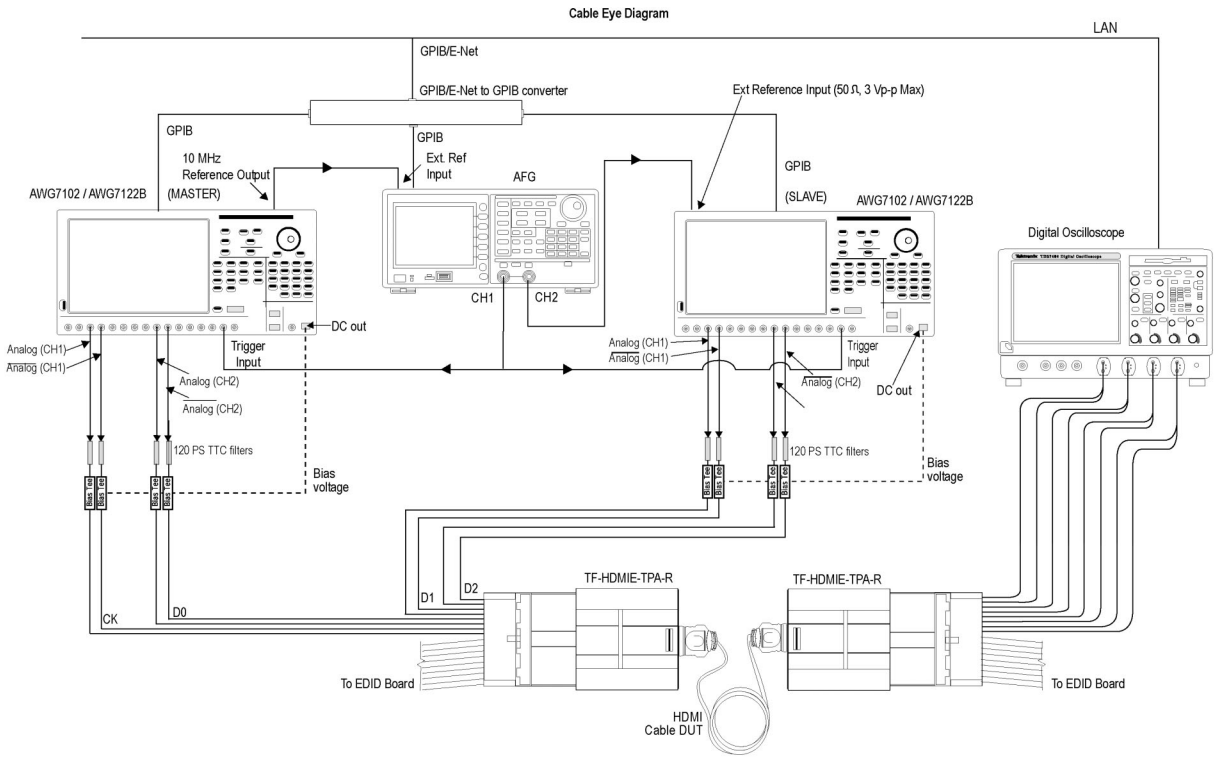


Perform the following steps for each TMDS clock rate supported by the HDMI Cable DUT.

1. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-Rs as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively). For connection details, refer to step 3 of the TP1 procedure.
2. Connect TPA-R to two ends of HDMI Cable DUT.
3. Configure the application as follows:
   a. Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   b. Select the DDS method in the configuration panel of the Cable Eye Diagram Test.
   c. Select the cable frequency based on the category of the cable (74 MHz, 165 MHz, 340 MHz, 74 MHz Type-E).
   d. In the Signal Source dialog box, check the GPIB connection of the two AWGs and the AFG to ensure proper connection.
   e. Once the test completes, you can view the result.

NOTE. *Passive and Active Cable Eye Diagram tests use the same connection, test, and waveform view procedures.*

Setup 4: To test the Cable DUT using Type-E fixture

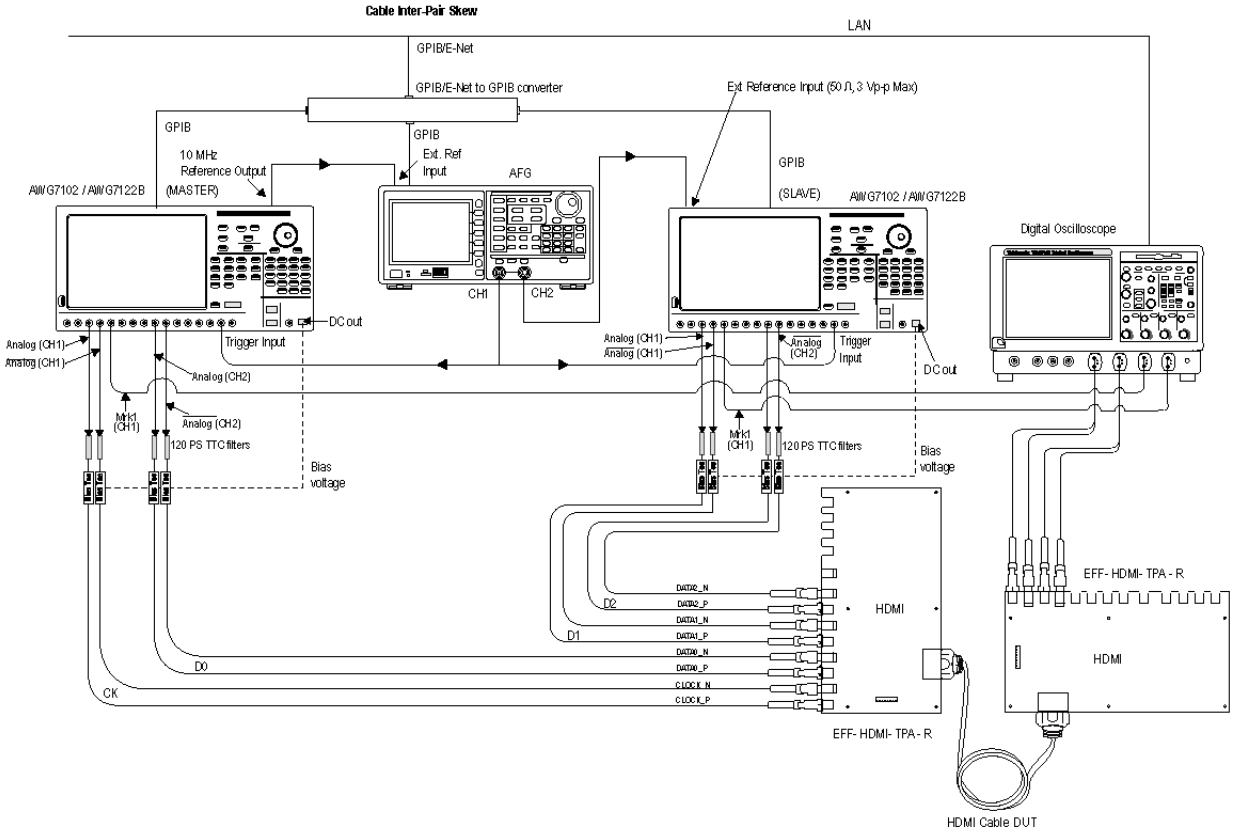


Make Connections for Cable Inter-Pair Skew

NOTE. *This Cable Inter-Pair Skew test is performed only for* ***repeater cable testing****.*

Setup 1: To synchronize both the AWGs

Make the connections as follows:



1. Connect the two AWGs, Bias-Tees, AFG, Digital Oscilloscope, and TPA-P as shown in the setup diagram. One AWG is used as the MASTER and the other AWG is used as the SLAVE (called AWG1 and AWG2 respectively).
   - AWG1 Marker1+ output to oscilloscope Ch3 input
   - AWG2 Marker1+ output to oscilloscope Ch4 input
   - AWG1 Ch1+ output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #1 signal input (RF)
     - Bias-Tee #1 signal output (RF and DC) to TMDS_CLOCK+
     - AWG1 DC_OUT (1) to Bias-Tee #1 DC-level input (DC)
   - AWG1 Ch1– output to 120 PS TTC filter
     - 120 PS TTC filter output to Bias-Tee #2 signal input (RF)
     - Bias-Tee #2 signal output (RF and DC) output to TMDS_CLOCK–
     - AWG1 DC_OUT (2) to Bias-Tee #2 DC-level input (DC)
   - AWG1 Ch2+ output to 120 PS TTC filter

- 120 PS TTC filter output to Bias-Tee #3 signal input (RF)
- Bias-Tee #3 signal output (RF and DC) to TMDS_DATA0+
- AWG1 DC_OUT (3) to Bias-Tee #3 DC-level input (DC)

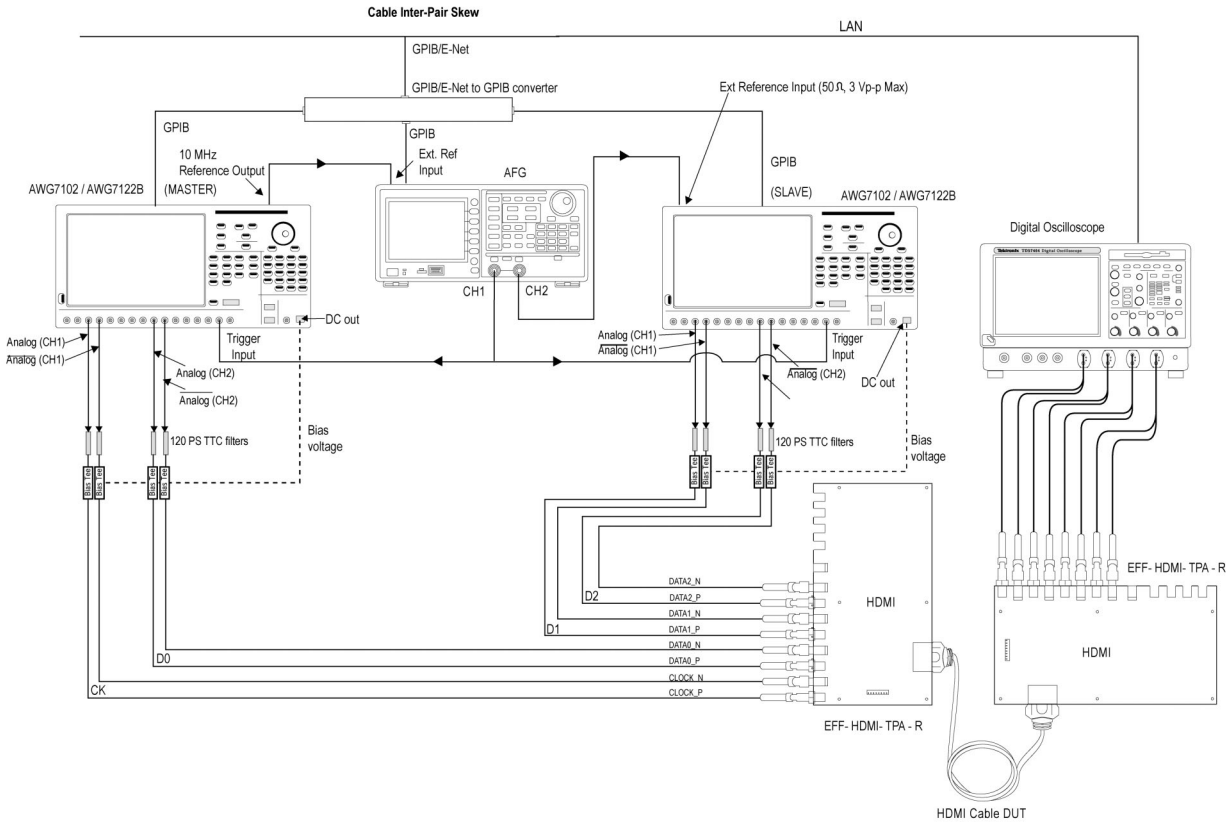
- AWG1 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #4 signal input (RF)
  - Bias-Tee #4 signal output (RF and DC) to TMDS_DATA0–
  - AWG1 DC_OUT (4) to Bias-Tee #4 DC-level input (DC)
- AWG2 Ch1+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #5 signal input (RF)
  - Bias-Tee #5 signal output (RF and DC) to TMDS_DATA1+
  - AWG2 DC_OUT (1) to Bias-Tee #5 DC-level input (DC)
- AWG2 Ch1– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #6 signal input (RF)
  - Bias-Tee #6 signal output (RF and DC) to TMDS_DATA1–
  - AWG2 DC_OUT (2) to Bias-Tee #6 DC-level input (DC)
- AWG2 Ch2+ output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #7 signal input (RF)
  - Bias-Tee #7 signal output (RF and DC) to TMDS_DATA2+
  - AWG2 DC_OUT (3) to Bias-Tee #7 DC-level input (DC)
- AWG2 Ch2– output to 120 PS TTC filter
  - 120 PS TTC filter output to Bias-Tee #8 signal input (RF)
  - Bias-Tee #8 signal output (RF and DC) to TMDS_DATA2–
  - AWG2 DC_OUT (4) to Bias-Tee #8 DC-level input (DC)
- AFG Ch1 using BNC-T adapter to trigger input of AWG1 and AWG2
- AFG Ch2 to be connected to Ext Ref input of AWG2
- AWG1 10 MHz Ref output to be connected to AFG Ext Ref input

2. Connect the Ch1 and Ch2 inputs of the oscilloscope to Clock and Data0 channels of the TPA-R.

3. Connect TPA-R to two ends of HDMI Cable DUT.
4. Configure the application as follows:
   - Run the TDSHT3 software (version with the Direct Synthesis capability) on the digital oscilloscope.
   - Select the DDS method in the configuration panel of the Cable Inter-Pair Skew Test.
   - Select the frequency of the cable to be tested.
   - In the Signal Source dialog box, check the GPIB connection of the two AWGs and the AFG to ensure proper connection.
   - Run the test to load the patterns on both the AWGs.
   - Once the synchronization of the two AWGs is complete, go to the setup 2 (see page 204).

Setup 2: To calculate inter-pair skew

Make the connections as follows:

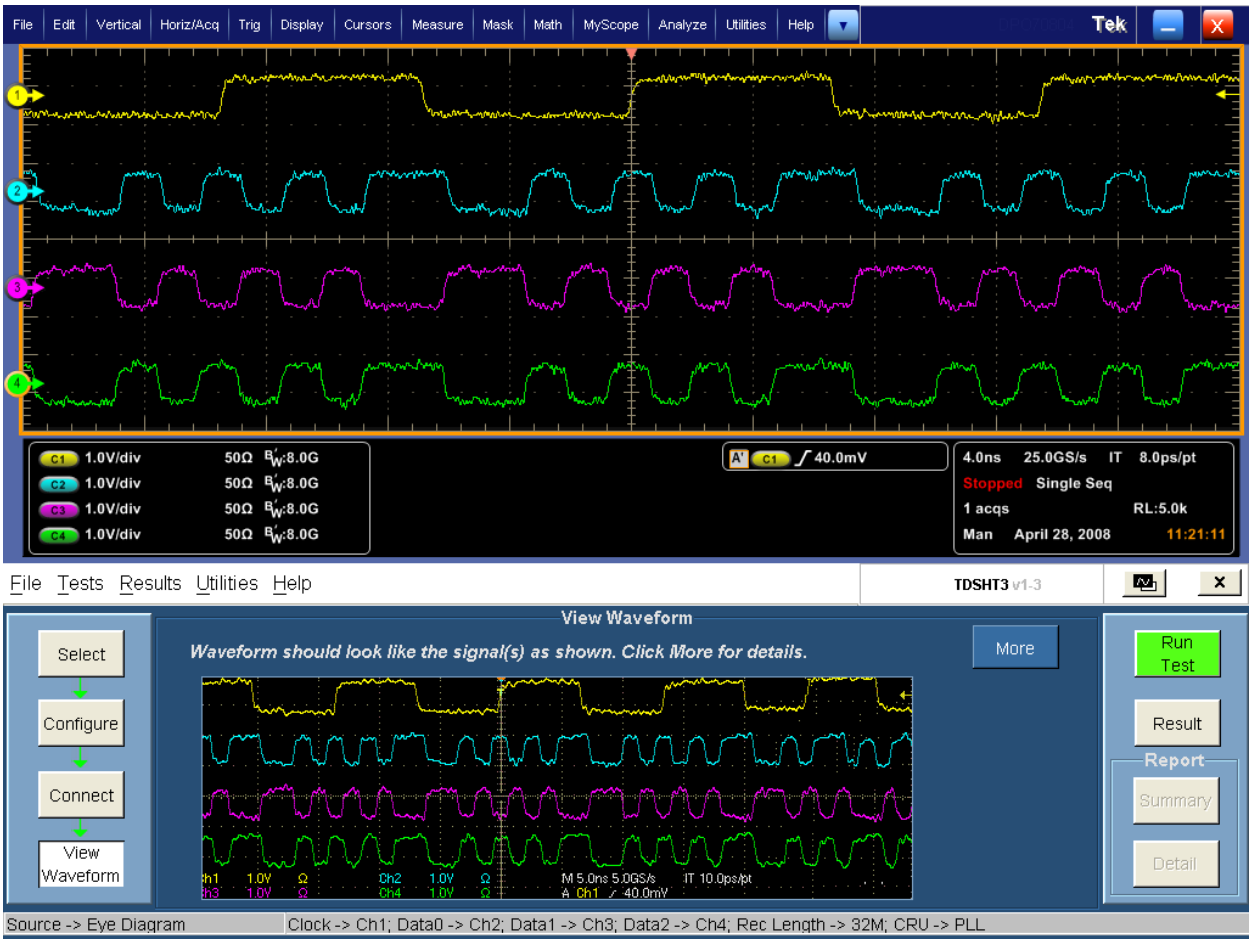


1. Remove the marker channel connections from the oscilloscope inputs.
2. Connect the Ch3 and Ch4 inputs of the oscilloscope to Data1 and Data2 channels of the TPA-R.

3. Run the test to measure the inter-pair skew.
4. Once the test completes, you can view the results.

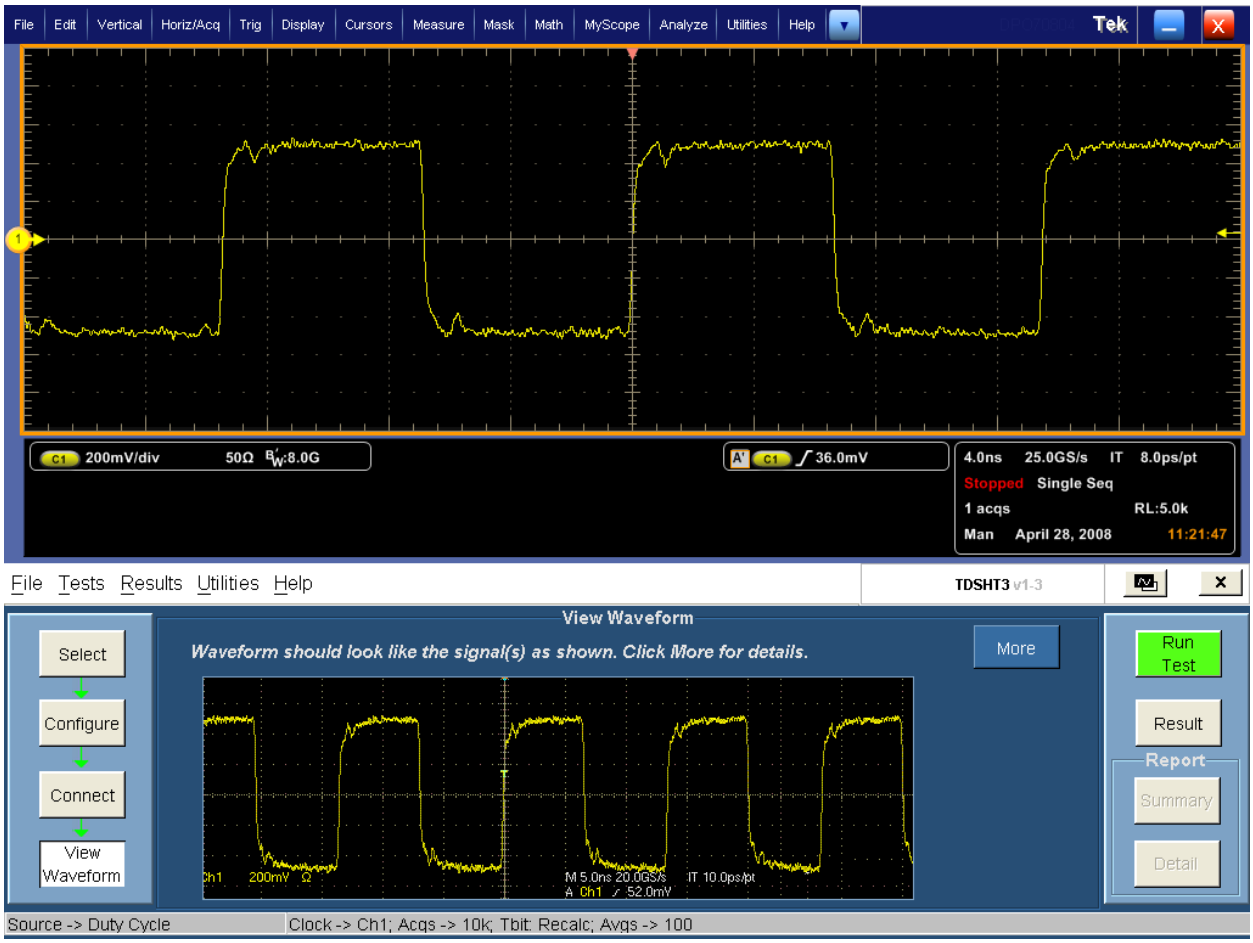
View the Source Eye Diagram Sample Waveform

Click **View Waveform** to display the input signals Clock and Data as follows:



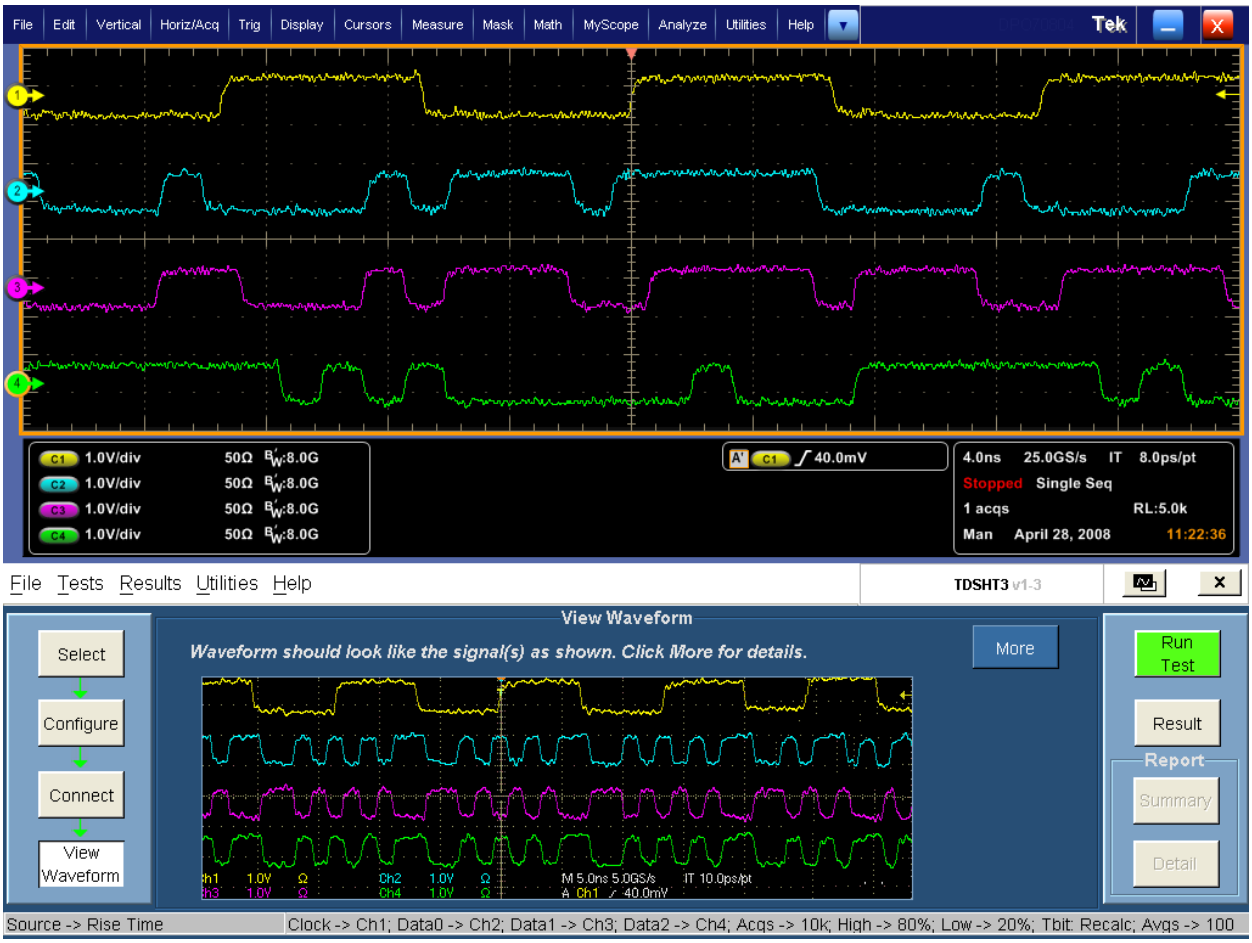
View the Duty Cycle Sample Waveform

Click **View Waveform** to display the Clock signal as follows:



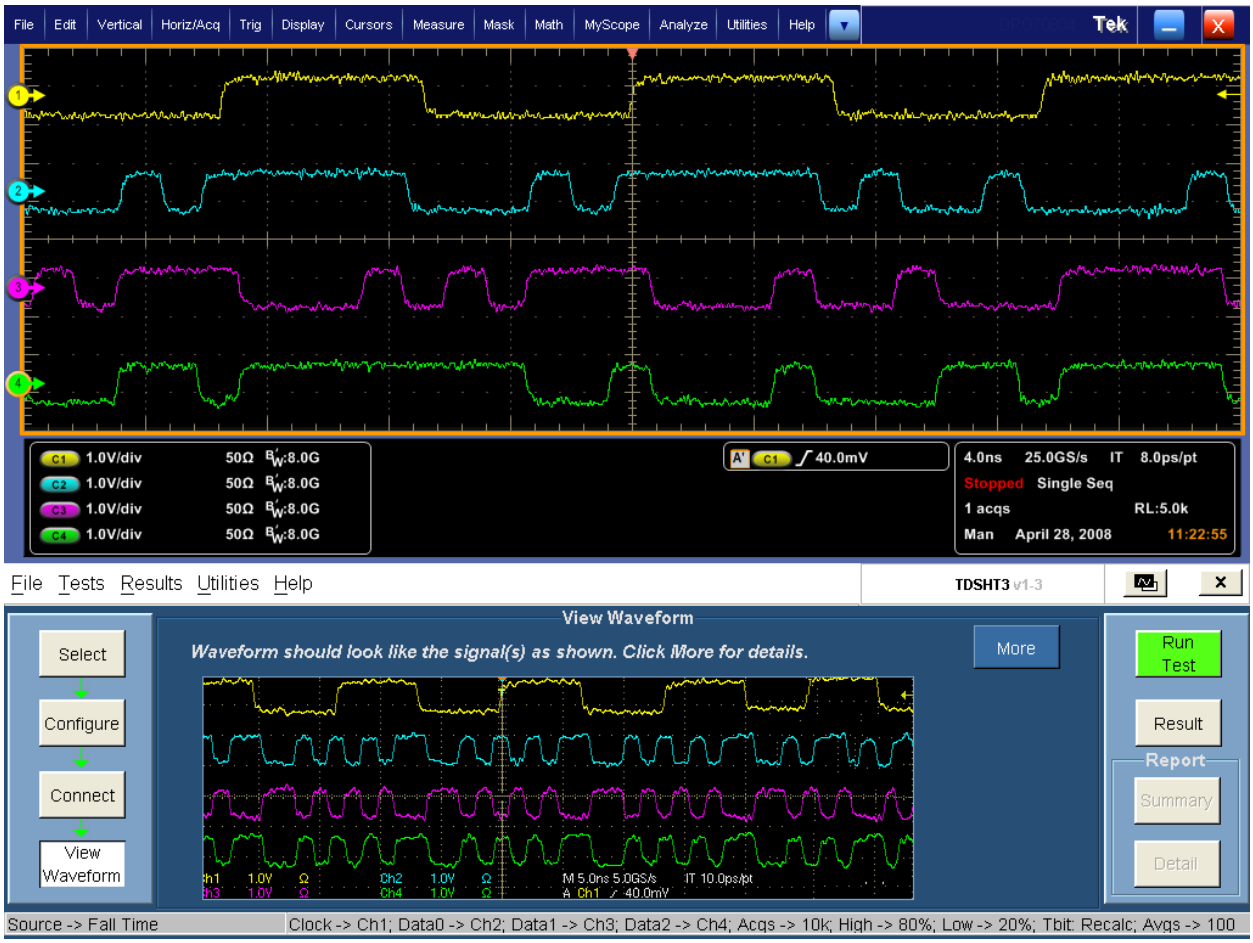
View the Rise Time Sample Waveform

Click **View Waveform** to display the input signals Clock or Data as follows:



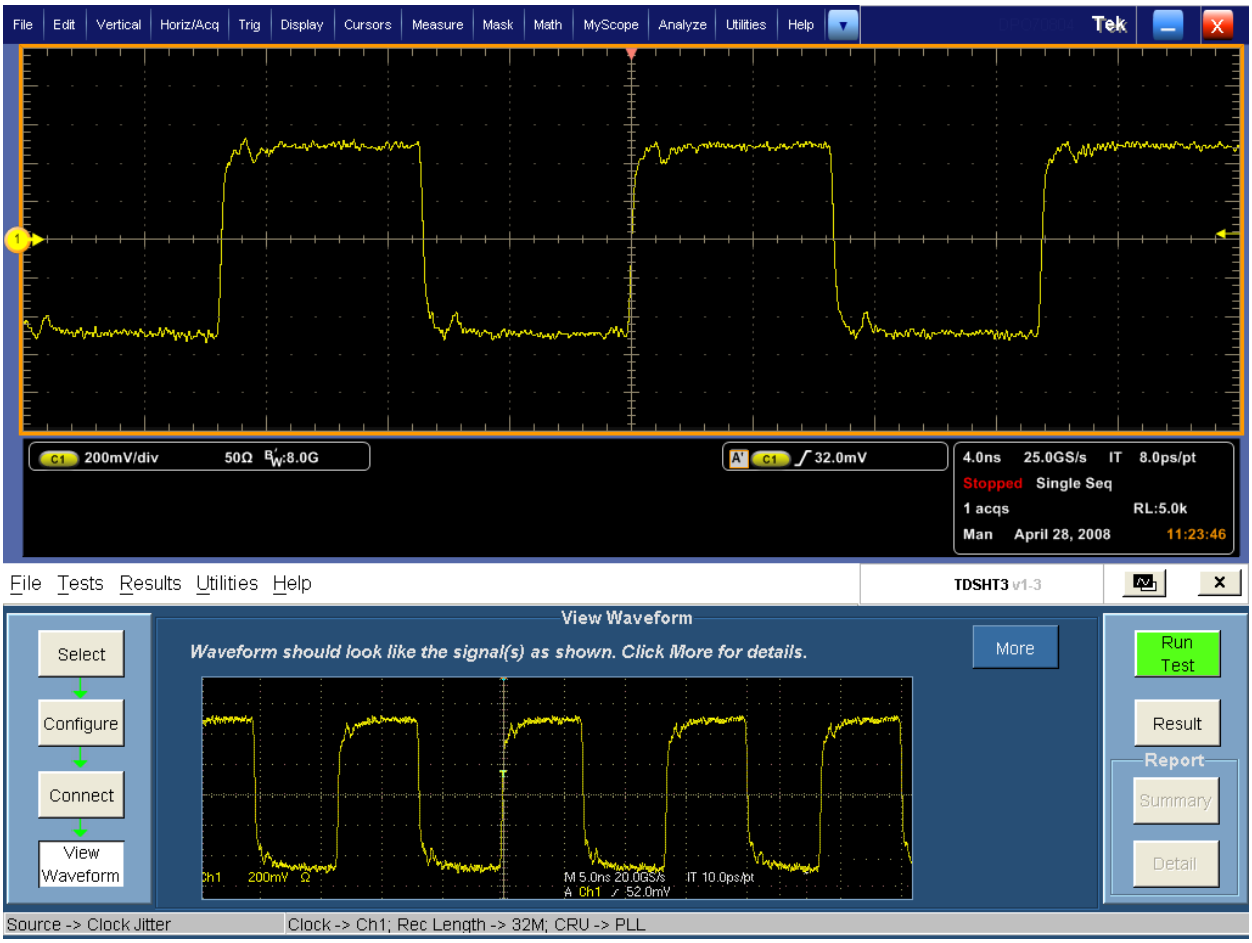
View the Fall Time Sample Waveform

Click **View Waveform** to display the input signals Clock or Data as follows:



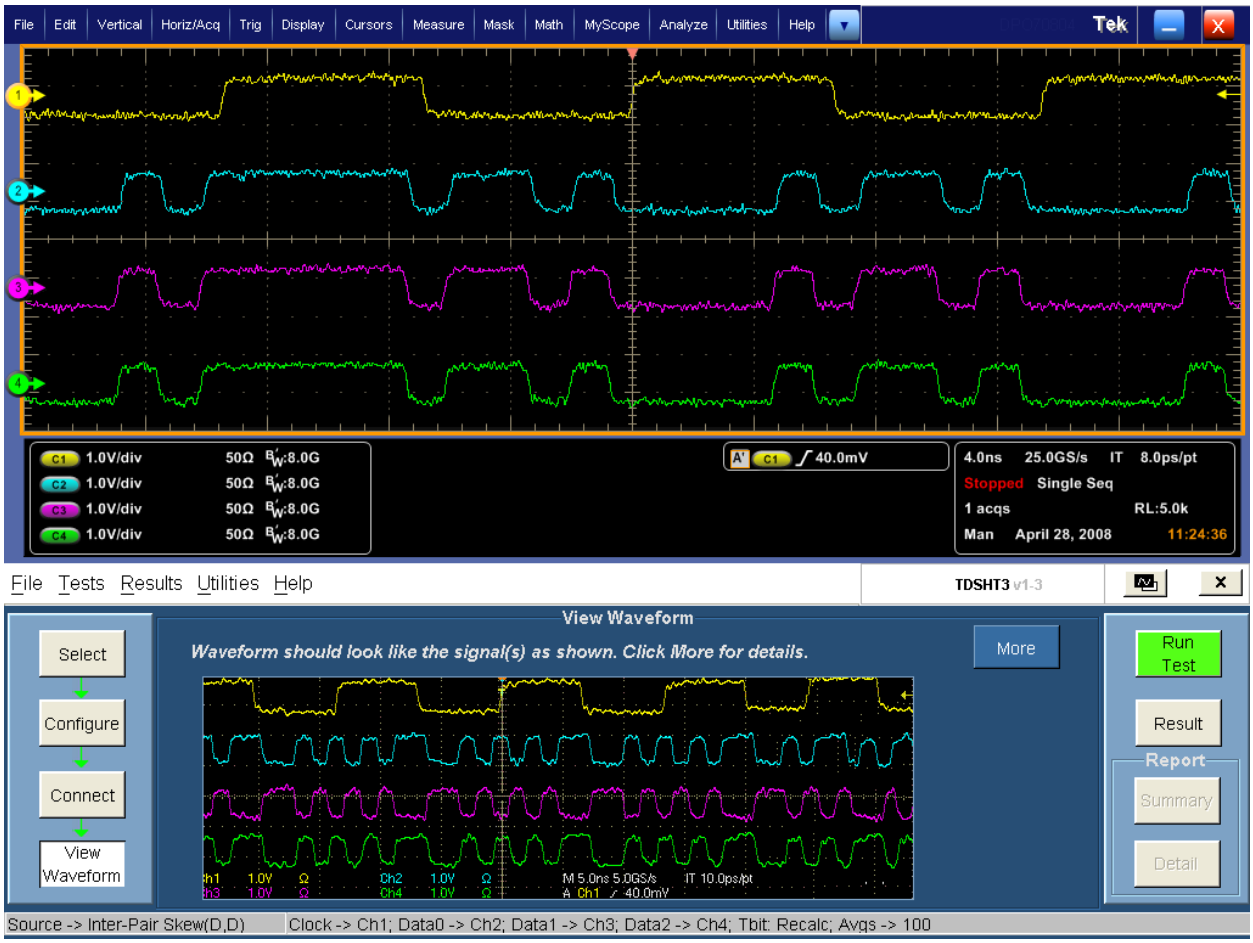
View the Clock Jitter Sample Waveform

Click **View Waveform** to display the Clock signal as follows:



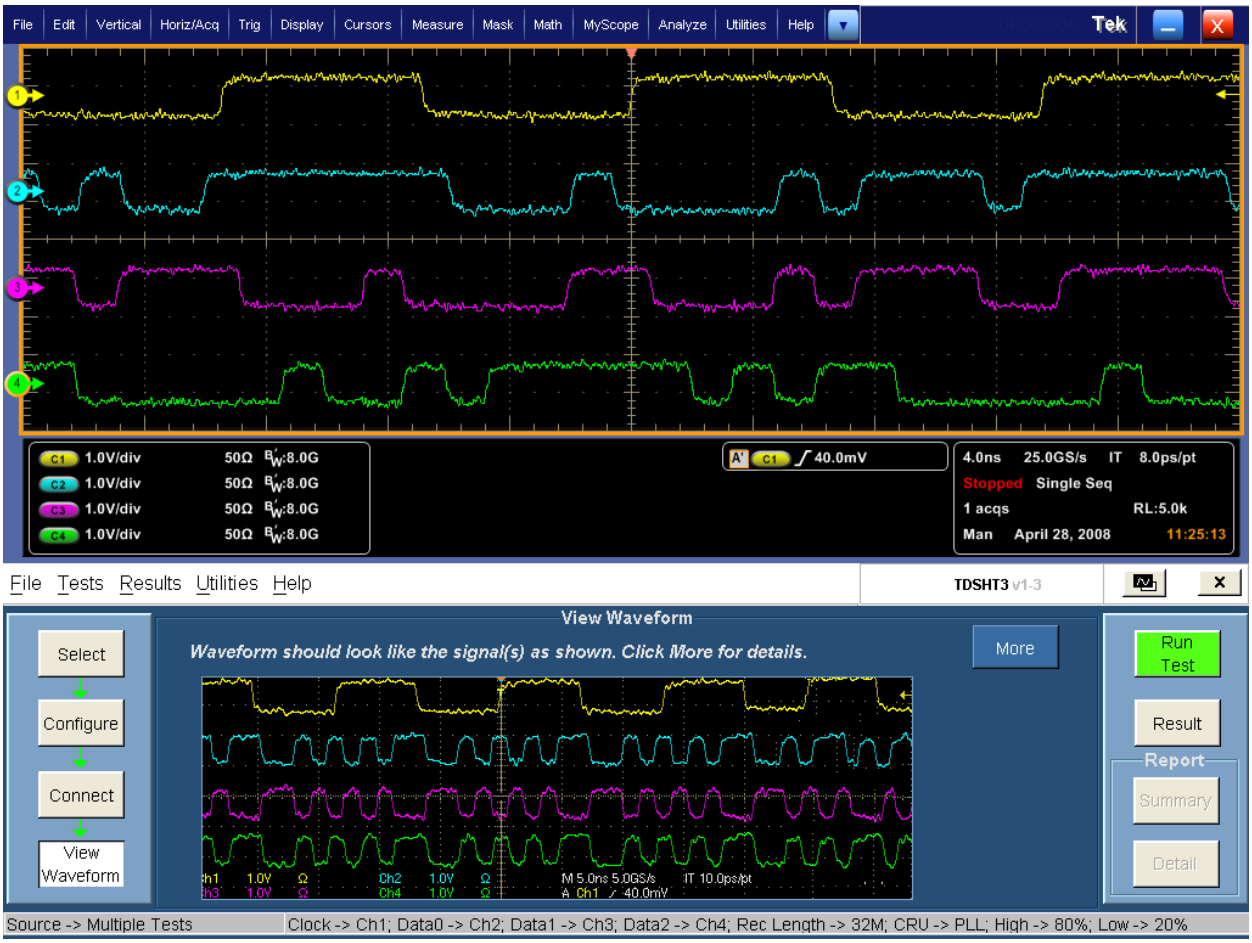
View the Source Inter-Pair Skew Sample Waveform

Click **View Waveform** to display the input signals Data+ and Data–, and Clock as follows:



View the Differential Tests Select All Sample Waveform

Click **View Waveform** to display the input signals Clock and Data as follows:



NOTE. *Similarly, click* ***View Waveform*** *to display a waveform for Single-Ended Tests Select All.*

View the Source Intra-Pair Skew Sample Waveform

Click **View Waveform** to display the input signals Data+ or Data–/Clock as follows:

View the Low Amplitude + Sample Waveform

Click **View Waveform** to display the input signals Data+ or Data–/Clock as follows:

View the Low Amplitude - Sample Waveform

Click **View Waveform** to display the input signals Data+ or Data–/Clock as follows:

View the Min/Max-Diff Swing Tolerance Sample Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Min/Max-Diff Swing Tolerance test.

View the Jitter Tolerance Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Jitter Tolerance test.

View the Deep Color Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Deep Color test.

View the Audio Clock Regeneration Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Audio Clock Regeneration test.

View the Audio Sample Packet Jitter Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Audio Sample Packet Jitter test.

View the Audio Formats Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Audio Formats test.

View the One Bit Audio Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the One Bit Audio test.

View the DVI Interoperability Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the DVI Interoperability test.

View the 3D Video Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the 3D Video test.

View the 4Kx2K Video Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the 4Kx2K Video test.

View the Extended Colors and Contents Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Extended Colors and Contents test.

View the Character Synchronization Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Character Synchronization test.

View the Pixel Encoding Requirements Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Pixel Encoding Requirements test.

View the Acceptance of All Valid Packets Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Acceptance of All Valid Packets test.

View the Video Format Timing Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Video Format Timing test.

View the Sink Intra-Pair Skew Sample Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Intra-Pair Skew test.

View the Cable Eye Diagram (Passive or Active) Sample Waveform

Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Eye Diagram tests (Active or Passive).

View the Cable Inter-Pair Skew Sample Waveform

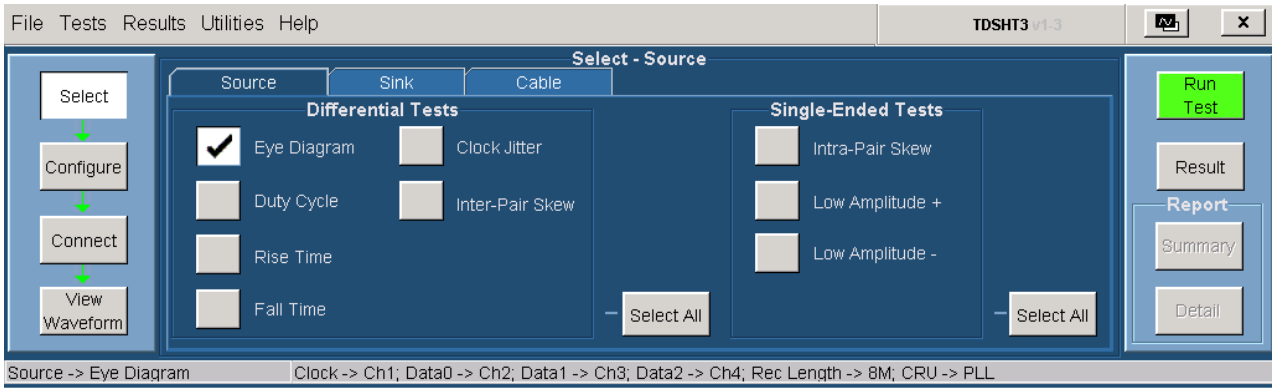
Because no signal is connected to the oscilloscope, you cannot view a sample waveform for the Cable Inter-Pair Skew test.

Test the Source Eye Diagram

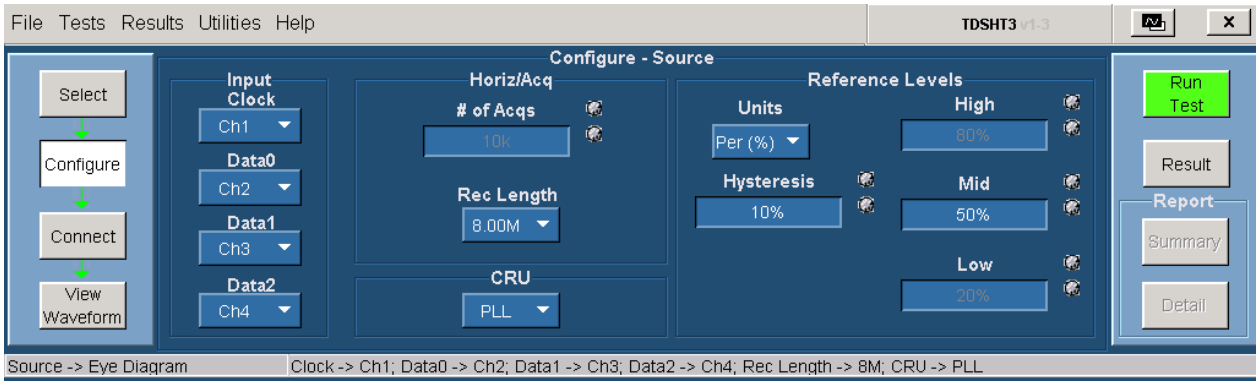
This test allows you to confirm that the differential signal on each TMDS differential data pair has an “eye opening” (region of valid data) which meets or exceeds the limits on eye opening in the specification.

You will need a Digital Oscilloscope, two/four differential probes, one DC power supply 3.3 V, one EDID emulator, and one TPA-P fixture. For DPO/DSA/MSO70000 series oscilloscopes, an external power supply is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

1. On the menu bar, click **Tests > Select > Source**.
2. In the differential tests pane, select the Eye Diagram check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



4. In the input pane, do the following:
   - Set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, Ch4, Ref1, Ref2, Ref3, and Ref4).
   - Set the Input Data0, Data1, and Data2 to the channel that you will use for the corresponding HDMI data inputs. Select from the available choices (Ch1, Ch2, Ch3, Ch4, Ref1, Ref2, Ref3, Ref4 and Not Conn).
5. In the horiz/acq pane, the required number of acquisitions are set for the test. The default value is 10 K.

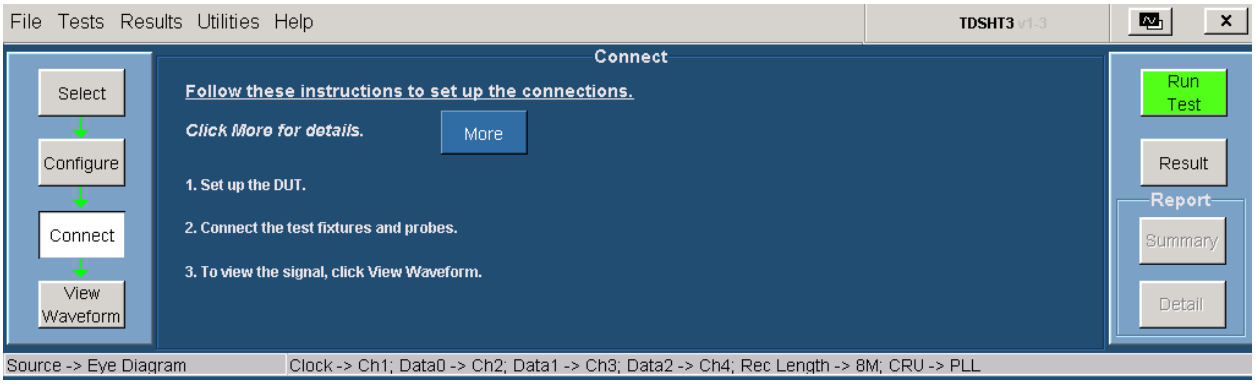
   Set the desired record length value for the eye tests in the Rec Length box. Select from the available choices (8.00k, 16.0k, 40.0k, 80.0k, 200k, 400k, 800k, 2.00M, 4.00M, 8.00M, 20.0M, 32.0M). The default value is 32.0M.

6. In the CRU pane, configure the Clock Recovery Unit. Select from the available choices (PLL, Raw, and Ideal). The default value is first order PLL and is used for compliance testing. Raw and Ideal are used for analysis.
7. In the reference levels pane, do the following:
   - Set the reference level units to either Per (%) or Abs.

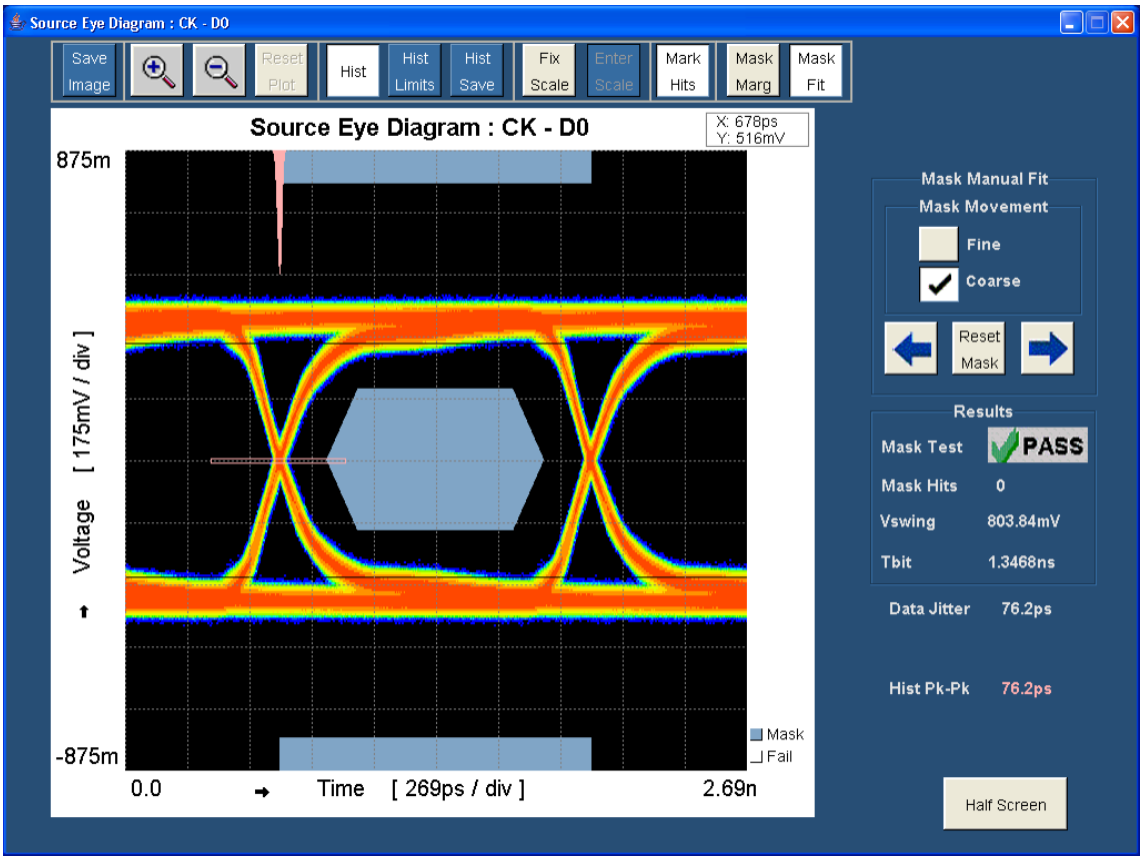
     Per (%) indicates that the reference levels are a percentage of the Vswing value.

     Abs indicates that the reference levels are absolute voltage values.

     The default selection is Per (%).
   - In the Hysteresis box, enter the desired hysteresis percent value. The range is from 0% to 25% and default is 10%.
   - In the High box, the required high reference voltage value is set for the test. The default value is 80%.
   - In the Mid box, enter the desired mid reference voltage value. The range is from 25% to 75% and default is 50%.
   - In the Low box, the required low reference voltage value is set for the test. The default value is 20%.
8. To connect the DUT, click **Tests > Connect**. Click here (see page 64) for information on how to make connections.



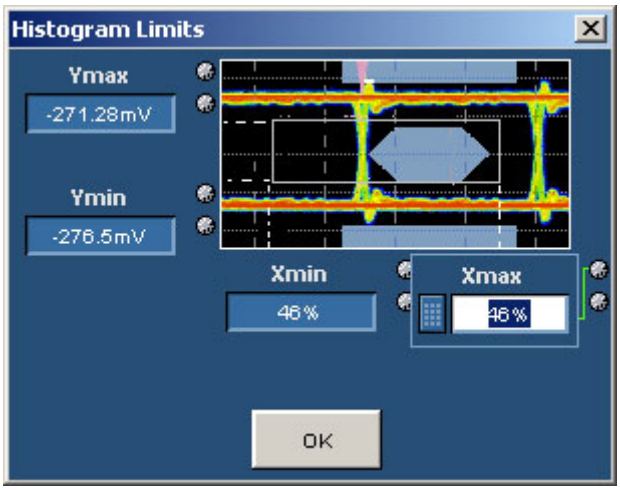
9. Ensure that your signal in the oscilloscope display is similar to the sample signal. Click View Waveform (see page 206) to display a sample of the expected signal. If the displays are not similar, go back and check your configuration and connections.
10. Click **Run Test** to perform the test. The TDSHT3 Software sets up the oscilloscope and the test runs, displaying a progress indicator.
11. If you have run the eye diagram test successfully, the software makes the results available automatically and displays the eye diagram plot.



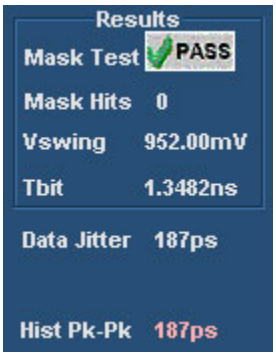
NOTE. *In the full screen mode, the histogram disappears if you click anywhere within the plot.*

Features on the Clock Jitter display include:

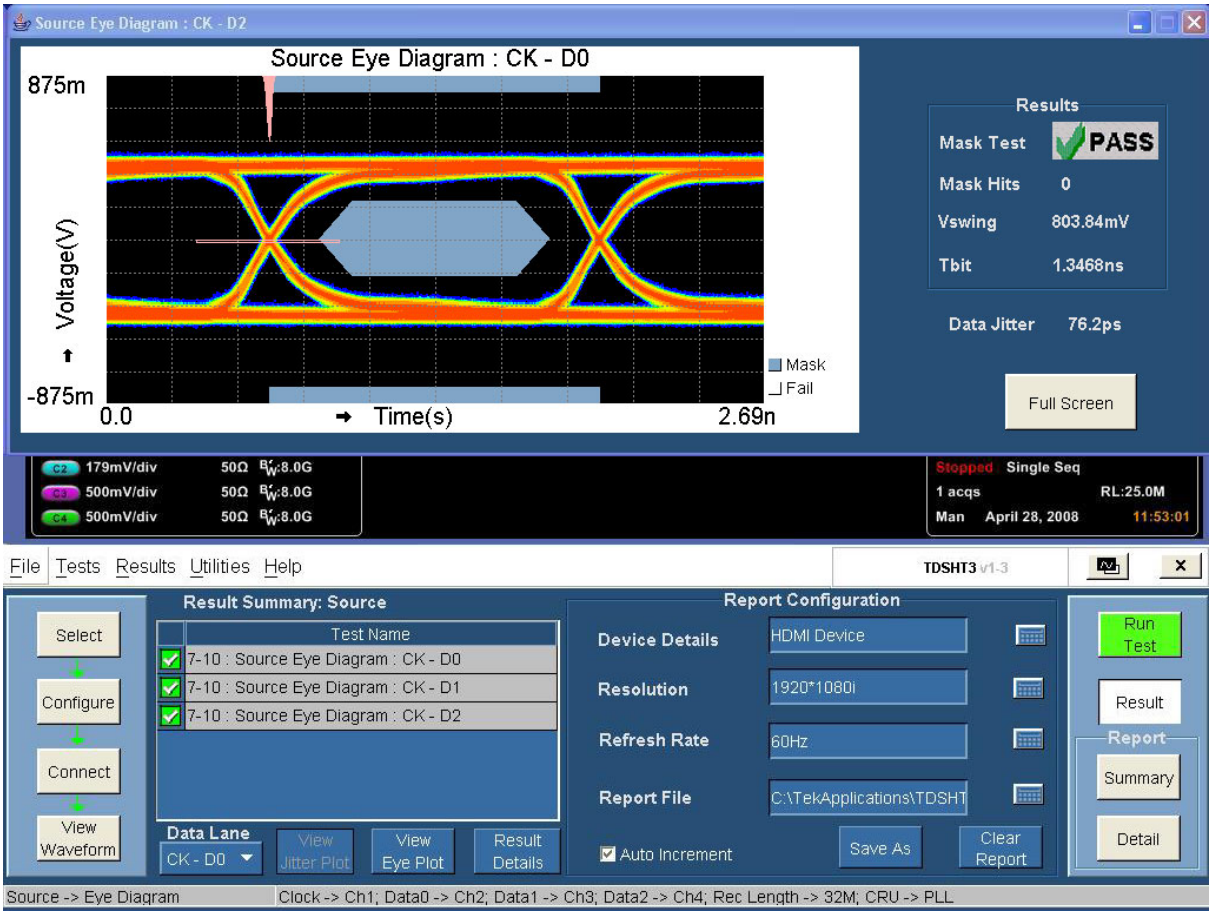
- Save: Click **Save Image** to save the eye diagram plot.
- Zoom: You can zoom in on an area of interest, up to five times the normal view. Either drag the mouse or click to define the area of interest.
- Reset Plot: Click **Reset Plot** to reset the plot.
- Histogram: Click **Hist** to draw the histogram on the eye diagram plot. Click **Hist Limits** to draw the histogram box, and **Hist Save** to save the histogram. Double-click the buttons next to the Ymax, Ymin, Xmin, and Xmax labels to type the X and Y histogram limits.



- Scale: Click **Fix Scale** to type in a new scale value, or click **Enter Scale** to type in a new vertical scale value.
- Mark Hits: Click **Mark Hits** to mark the hits in the eye diagram plot.
- Mask: Click **Mask Marg** to display the margins on the eye diagram plot. Click **Mask Fit** to enable to move the mask either in the left or the right direction. Mask Marg and Mask Fit are mutually exclusive of each other.
- Mask Manual Fit pane: Use this pane to move the mask either in the left or the right direction. Select either a fine or a coarse movement.
- Results display: The results pane displays the result of the mask test result (pass or fail), mask hits (number of mask hits), Vswing value (voltage swing of the signal), and the Tbit value (time period of each bit). The Data Jitter and the Hist Pk-Pk values are also shown near the results pane. If there is no value for data jitter, it implies the absence of data points in the histogram window. In this case, increase the record length value and run the test again.



12. Click **Half Screen** to view the eye diagram plot in half screen. You can also view both the result summary of the test and the report configuration in the result pane as shown in the following figure.

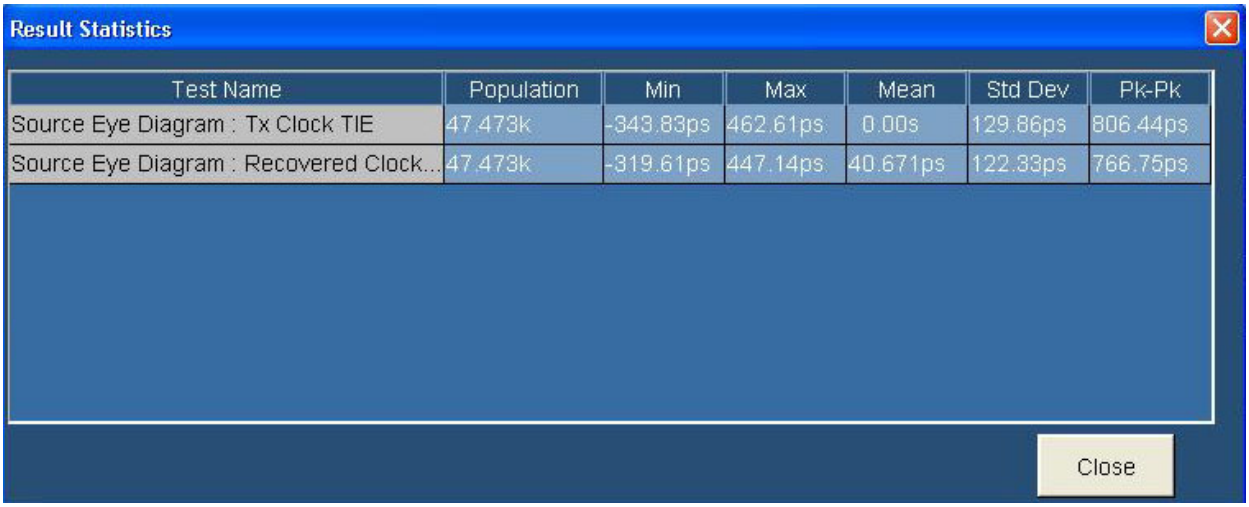


The result pane displays the result summary pane and the report configuration pane.

The result summary pane displays the test results. Click here (see page 48) for more information.

Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

13. In the result summary pane, click **Result Details** to display the details of the result. Click here (see page 50) for more information.
14. In the Result Details dialog box, click **Result Statistics** to display statistics based on the tests. Click here (see page 50) for more information.



Test Method

This sequence explains the actions that the software takes while it performs an eye diagram test. For the procedure on how to make this test, see eye diagram test procedure (see page 218).

1. Refer to Eye Diagram (see page 64) for information on how to make connections for Source Eye Diagram test.
2. Set up the oscilloscope as follows:
   - Set the memory length to at least 25 M points.
   - Set the single-shot trigger at the rising edge of TMDS Clock (50 percent).
   - Set the sample rate to ≥ 10 GS/s based on the oscilloscope.
   - Adjust the vertical scale to accommodate the waveform in six vertical divisions.
3. Capture the waveforms on the oscilloscope.

NOTE. *Do not transfer the waveforms.*

4. Perform software clock recovery as follows:
   - Find V_H and V_L of both clock and data.
   - Find 50 percent reference level of the clock.
   - Calculate the Software CRU filter as follows.

     $H(s) = 1/(1+s\tau)$, where $\tau = 40$ nsec.
   - Pass the TIE values through the filter (FFT and IFFT) $H(s) = 1/(1+s\tau)$, where $\tau = 40$ nsec.
   - Reconstruct the clock, and then create a bit clock (x10 clock) by using even up sampling.

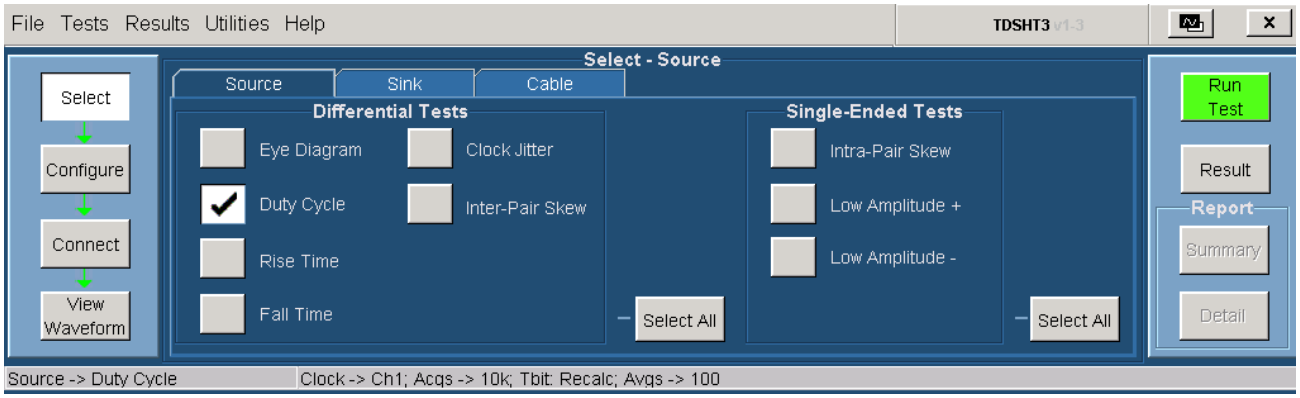
5. Draw the eye diagram.
   - x10 clock is used for slicing.
   - Draw the eye diagram with ½ UI+UI+½ UI method. This ensures that all UIs are overlapped.
6. Create eye mask.
   - Calculate V_{SWING} by using V_H and V_L of the data.
   - Construct the mask co-ordinate by using T_{BIT} and V_{SWING}.
7. Position the mask in such a way that one of its left corners just touches the waveform.
8. If any other part of the waveform either touches or crosses the data eye, it implies Fail.
9. Calculate the data jitter by using the histogram technique. The histogram co-ordinates are V_C+/-5 mV.
10. If data jitter is more than (0.3*T_{BIT}), it implies Fail.
11. Repeat the test for all the remaining TMDS_DATA pairs.
12. Repeat the test for all supported pixel clock rates. Only one video format is required per pixel clock rate.

Test the Duty Cycle

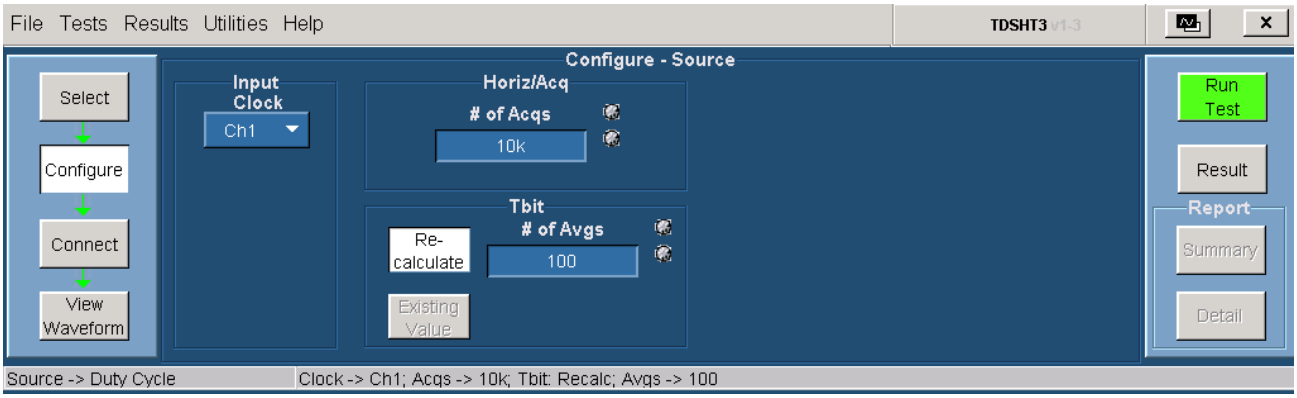
This test allows you to confirm that the duty cycle of the differential TMDS clock does not exceed the limits allowed by the specification.

You will need a Digital Oscilloscope, one differential probe, one DC power supply 3.3 V, one EDID emulator, and one TPA-P fixture. For DPO/DSA/MSO70000 series oscilloscopes, an external power supply is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

1. On the menu bar, click **Tests > Select > Source**.
2. In the differential tests pane, select the Duty Cycle check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



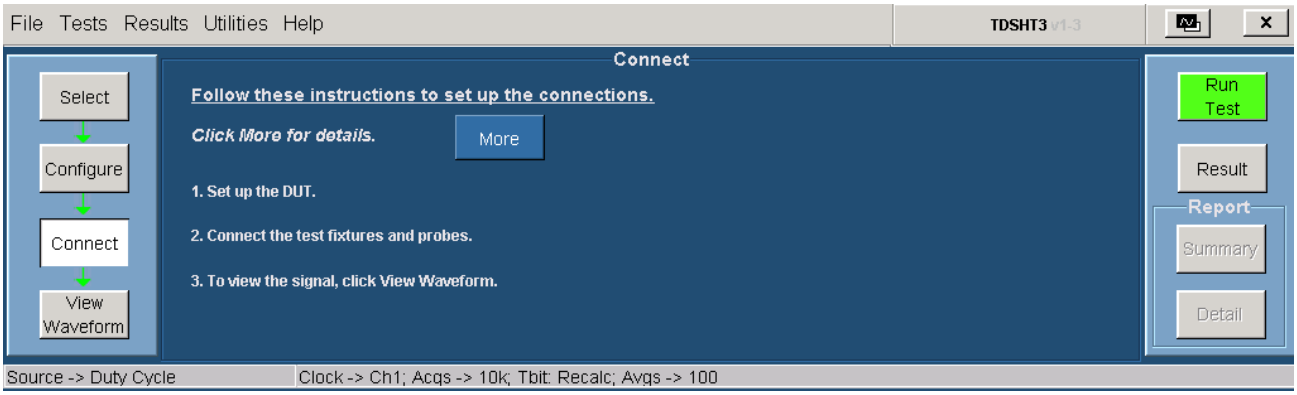
4. In the input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

5. In the horiz/acq pane, enter the desired number of acquisitions that are required for the test. The range is from 10 K to 1 M and default is 10 K.

6. In the tbit pane, do the following:

   - Enter the desired number of periods that are considered to calculate Tbit. The range is from 2 to 1 K and default is 100.
   - Click **Re-calculate** to recalculate the Tbit value.
   - If you want to use the previously calculated Tbit value, click **Existing Value**.

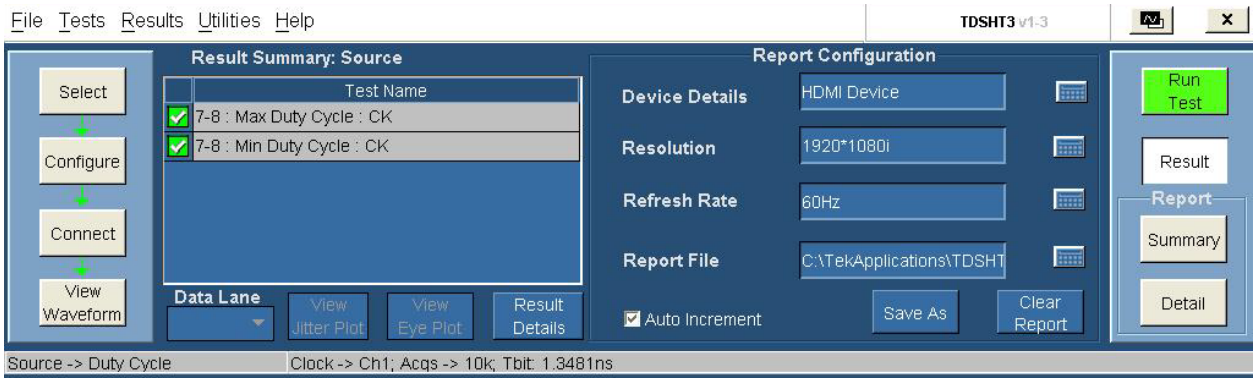
7. To connect the DUT, click **Tests > Connect**. Click here (see page 67) for information on how to make connections.



8. Ensure that your signal in the oscilloscope display is similar to the sample signal. Click View Waveform (see page 207) to display a sample of the expected signal. If the displays are not similar, go back and check your configuration and connections.

9. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and the test runs, displaying a progress indicator.

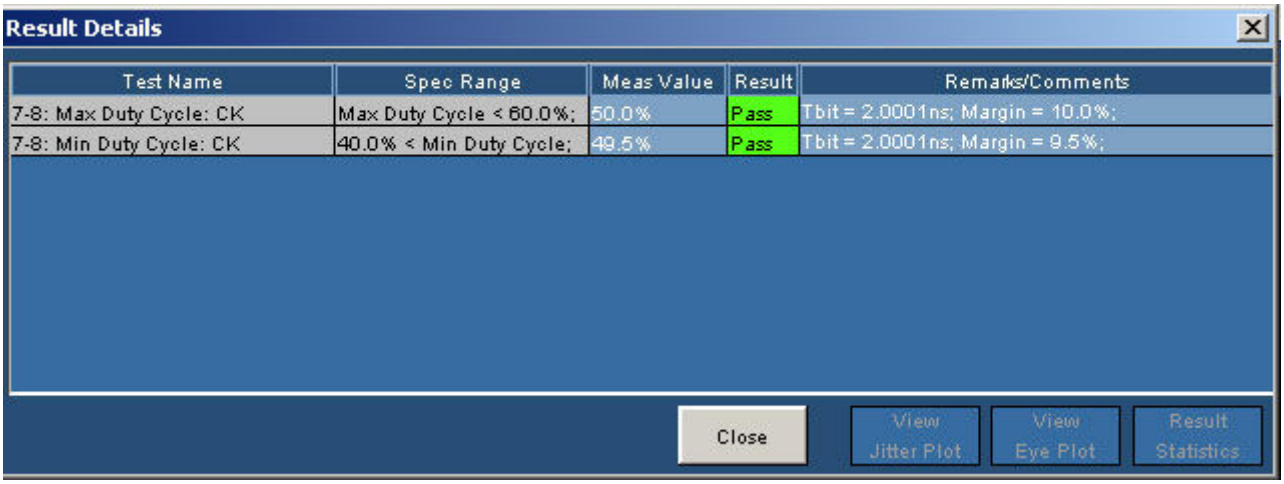
10. The software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and their status (pass, fail, or error). To view the details of the results, click **Results Details**.

11. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

12. In the result summary pane, click **Result Details**. The result details pane displays the following fields.

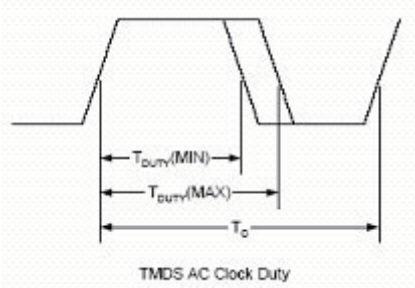


- Test Name (displays the test id, test name, and lane)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the measured value)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the relevant details, such as Tbit and Margin). If the test could not be run, the field displays an error code (see page 397).

Test Method

This sequence explains the actions that the software takes while it performs a duty cycle test. For the procedure on how to make this test, see duty cycle test procedure (see page 225).

1. Refer to Duty Cycle (see page 67) for information on how to make connections for Duty Cycle test.
2. Display the waveform of one clock period.
3. Set up the oscilloscope as follows:
   - Adjust the vertical scale to accommodate the waveform in six vertical divisions
   - Trigger: Edge trigger
   - Acquire at least 10,000 waveforms in FastAcq
4. Find the minimum and maximum duty cycle by using the following method:



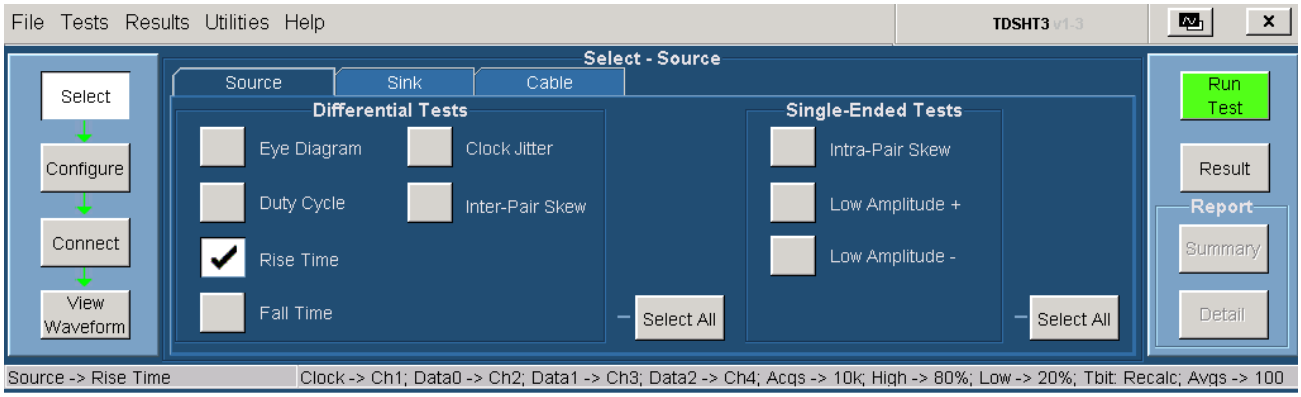
5. Compare with the limit value.
   - If minimum duty cycle is more than 40 percent, it implies Pass.
   - If maximum duty cycle is less than 60 percent, it implies Pass.

Test the Rise Time

This test allows you to confirm that the rise times on the TMDS differential signals fall within the limits of the specification.

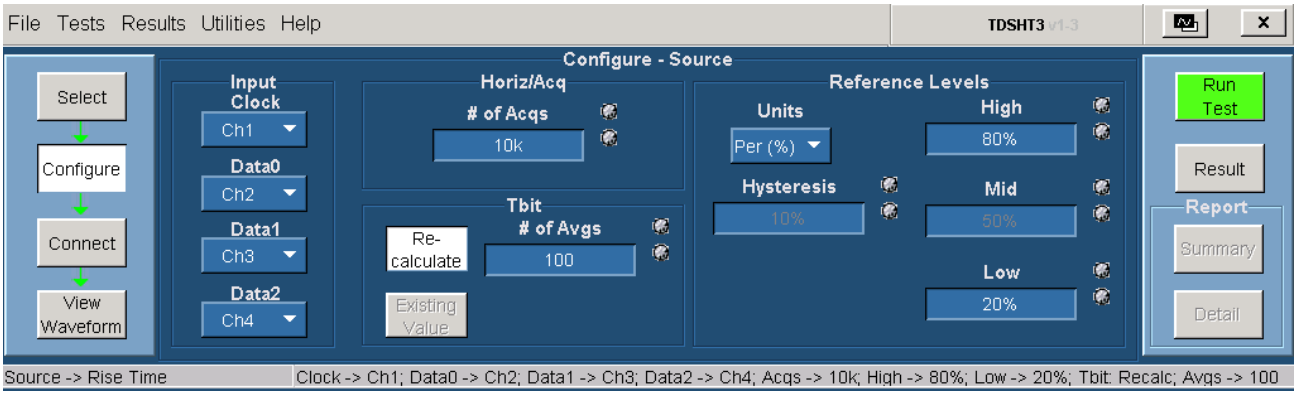
You will need a Digital Oscilloscope, one differential probe, one DC power supply 3.3 V, one EDID emulator, and one TPA-P fixture. For DPO/DSA/MSO70000 series oscilloscopes, an external power supply is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

1. On the menu bar, click **Tests > Select > Source**.
2. In the differential tests pane, select the Rise Time check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is

recommended that you save the configuration settings before you choose to select Recall Default or close the application.



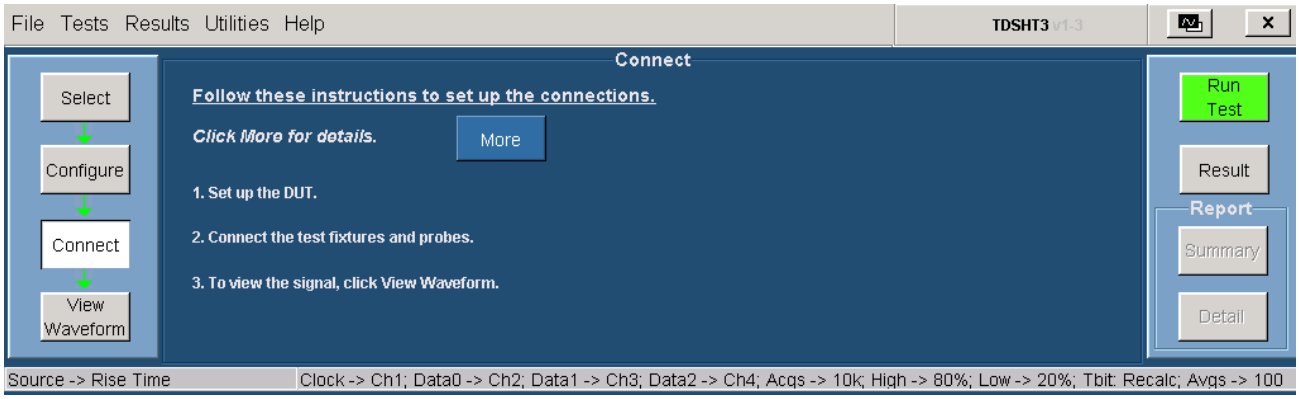
4. In the input pane, do the following:
   - Set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, Ch4, and Not Conn).
   - Set the Input Data0, Data1, and Data2 to the channel that you will use for the corresponding HDMI data inputs. Select from the available choices (Ch1, Ch2, Ch3, Ch4, and Not Conn).
5. In the horiz/acq pane, enter the desired number of acquisitions that are required for the test. The range is from 10 K to 1 M and default is 10 K.
6. In the tbit pane, do the following:
   - Enter the desired number of averages (periods) that are considered to calculate Tbit. The range is from 2 to 1 K and default is 100.
   - Click **Re-calculate** to recalculate the Tbit value.
   - Click **Existing Value** to use the previously calculated Tbit value.
7. In the reference levels pane, do the following:
   - Set the reference level units to either Per (%) or Abs.

     Per (%) indicates that the reference levels are a percentage of the Vswing value.

     Abs indicates that the reference levels are absolute voltage values.

     The default setting is Per (%).
   - In the Hysteresis box, the required hysteresis value is set for the test. The default value is 10%.
   - In the High box, enter the desired high reference voltage value. The range is from 50% to 100% and the default is 80%.
   - In the Mid box, the required mid reference voltage value is set. The default value is 50%.
   - In the Low box, enter the desired low reference voltage value. The range is from 1% to 50% and the default is 20%.

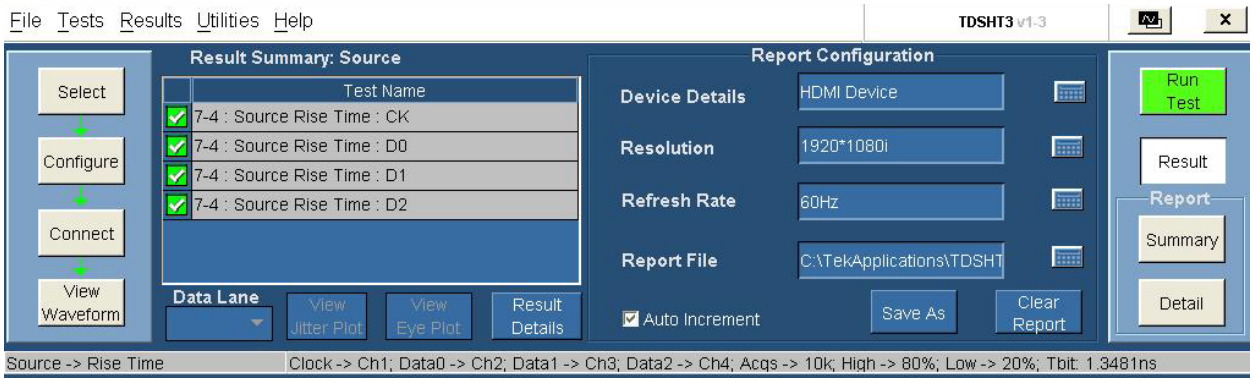
8. To connect the DUT, click **Tests > Connect**. Click here (see page 70) for information on how to make connections.



9. Ensure that your signal in the oscilloscope display is similar to the sample signal. Click View Waveform (see page 208) to display a sample of the expected signal. If the displays are not similar, go back and check your configuration and connections.

10. Click **Run Test** to perform the test. The TDSHT3 Software sets up the oscilloscope and the test runs, displaying a progress indicator.

11. The software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



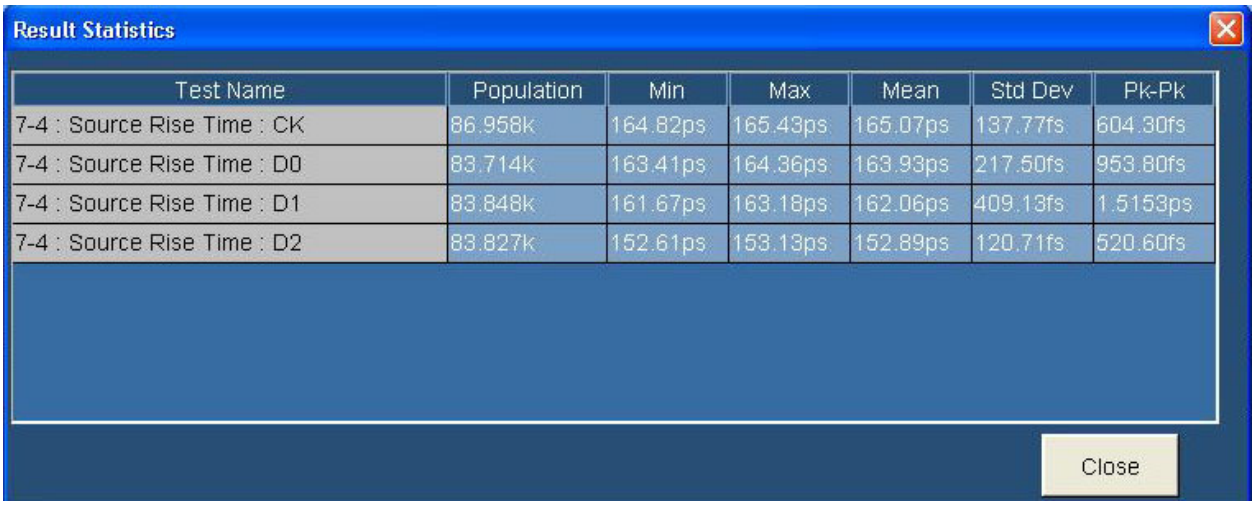
The results summary lists the test name and their status (pass, fail, or error). To view the details of the results, click **Results Details**.

12. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

13. In the result summary pane, click **Result Details**. The result details pane displays the following fields.

- Test Name (displays the test id, test name, and selected lanes)
- Spec Range (displays the lower limit and upper limit of the rise time test)
- Meas Value (displays the measured value)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the relevant details, such as Tbit, Vswing, Upper Margin, and Lower Margin). If the test could not be run, the field displays an error code (see page 397).
- Result Statistics (displays statistics based on the tests)

14. In the Result Details dialog box, click **Result Statistics** to display statistics based on the tests. Click here (see page 50) for more information.



Test Method

This sequence explains the actions that the software takes while it performs a rise time test. For the procedure on how to make this test, see rise time test procedure (see page 229).

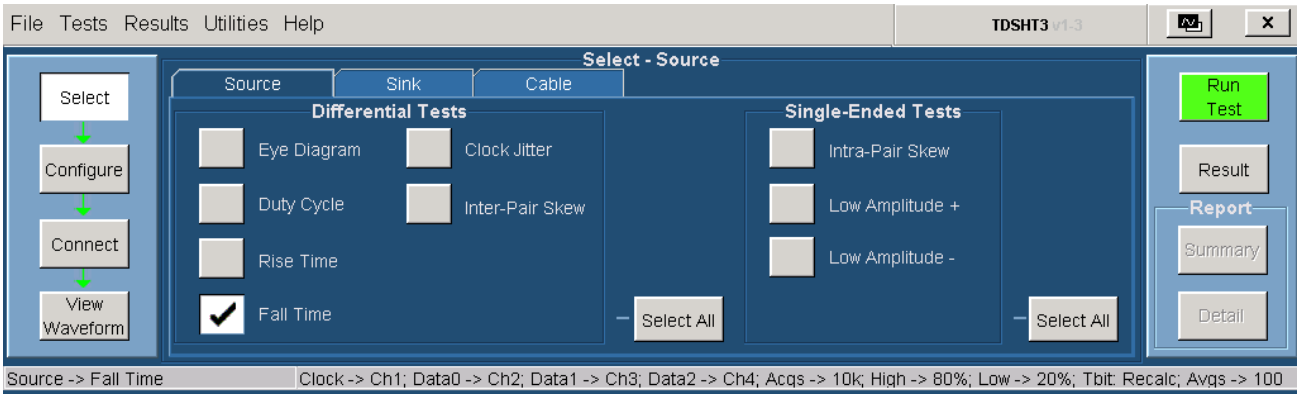
1. Refer to Rise Time (see page 70) for information on how to make connections for Rise Time test.
2. Set the trigger position at the center of the screen.
3. Set up the oscilloscope as follows:
   - Calculate T_{BIT} by using differential clock.
   - Set the vertical scale to accommodate the waveform in at least six divisions.
   - Set the horizontal scale to more than $2*T_{BIT}$.
   - If pulse width trigger is selected, Trigger with pulse width trigger with ($4*T_{BIT}$) pulse or trigger with edge trigger.
4. Accumulate at least 10,000 triggered waveforms by acquiring the waveform in FastAcq mode of acquisition.
5. Calculate V_{SWING} of the signal ($V_{SWING} = V_H – V_L$), and then find the 20 percent and 80 percent of the level.
6. Measure the rise time and fall time.
   - Enable the oscilloscope rise time measurement. Set the reference level to 20 percent and 80 percent.
   - Acquire at least 10 K waveforms (RUN and STOP).
   - Calculate the rise time.
   - Set the trigger to negative pulse.
   - Enable the oscilloscope rise time measurement.
   - Acquire at least 10 K waveforms (RUN and STOP).
   - Calculate the fall time.
7. Compare with the limit.
   - If T_{RISE} is less than 75 ps or T_{RISE} is more than ($0.4*T_{BIT}$), it implies Fail.
   - If T_{FALL} is less than 75 ps or T_{FALL} is more than ($0.4*T_{BIT}$), it implies Fail.
8. Repeat the test for all the remaining TMDS clock and data pairs.

Test the Fall Time

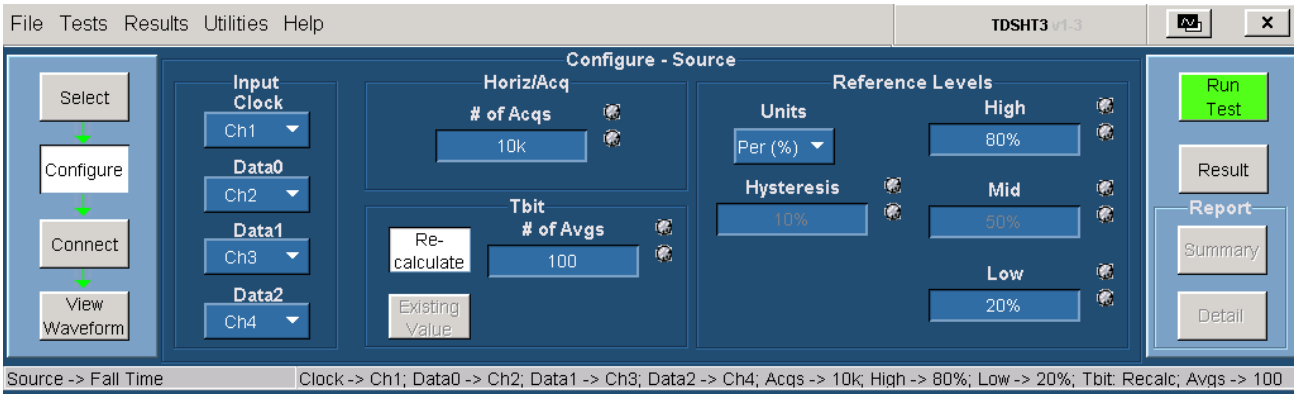
This test allows you to confirm that the fall times on the TMDS differential signals fall within the limits of the specification.

You will need a Digital Oscilloscope, one differential probe, one DC power supply 3.3 V, one EDID emulator, and one TPA-P fixture. For DPO/DSA/MSO70000 series oscilloscopes, an external power supply is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

1. On the menu bar, click **Tests > Select > Source**.
2. In the differential tests pane, select the Fall Time check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



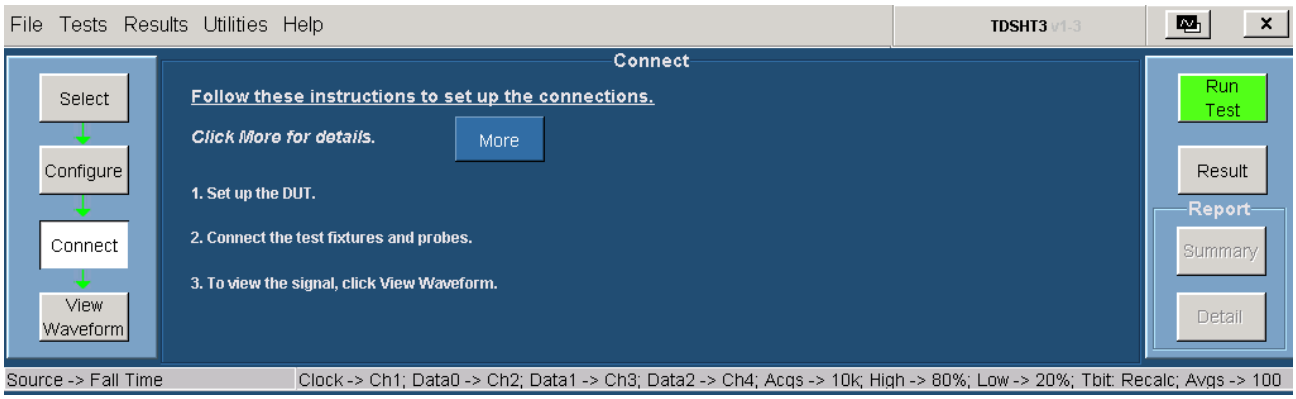
4. In the input pane, you have the following options:
   - Set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, Ch4, and Not Conn).
   - Set the Input Data0, Data1, and Data2 to the channel that you will use for the corresponding HDMI data inputs. Select from the available choices (Ch1, Ch2, Ch3, Ch4, and Not Conn).
5. In the horiz/acq pane, enter the desired number of acquisitions that are required for the test. The range is from 10 K to 1 M and default is 10 K.

6. In the tbit pane, do the following:
   - Enter the desired number of averages (periods) that are considered to calculate Tbit. The range is from 2 to 1 K. The default value is 100.
   - Click **Re-calculate** to recalculate the Tbit value.
   - Click **Existing Value** to use the previously calculated Tbit value.
7. In the reference levels pane, do the following:
   - Set the reference level units to either Per (%) or Abs.

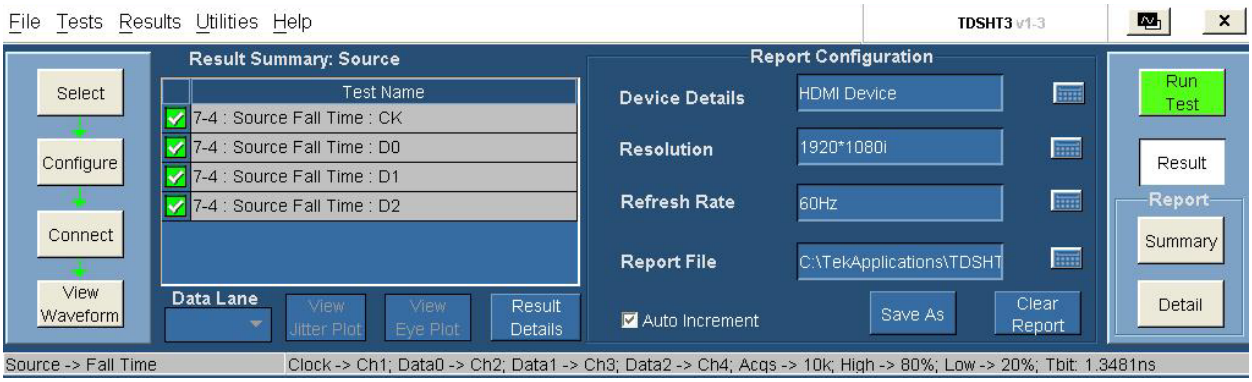
     Per (%) indicates that the reference levels are a percentage of the Vswing value.

     Abs indicates that the reference levels are absolute voltage values.

     The default setting is Per (%).
   - In the Hysteresis box, the required hysteresis value is set for the test. The default value is 10%.
   - In the High box, enter the desired high reference voltage value. The range is from 50% to 100% and the default is 80%.
   - In the Mid box, the required mid reference voltage value is set. The default value is 50%.
   - In the Low box, enter the desired low reference voltage value. The range is from 1% to 50% and the default is 20%.
8. To connect the DUT, click **Tests > Connect**. Click here (see page 73) for information on how to make connections.



9. Ensure that your signal in the oscilloscope display is similar to the sample signal. Click View Waveform (see page 209) to display a sample of the expected signal. If the displays are not similar, go back and check your configuration and connections.
10. Click **Run Test** to perform the test. The TDSHT3 Software sets up the oscilloscope and the test runs, displaying a progress indicator.
11. The software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



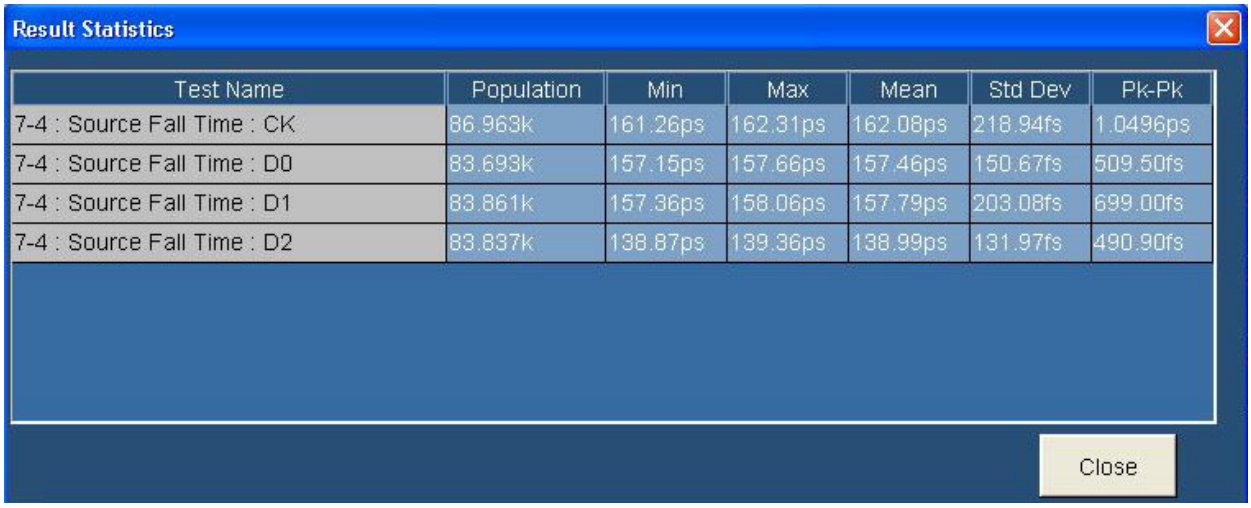
The results summary lists the test name and their status (pass, fail, or error). To view the details of the results, click **Results Details**.

12. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

13. In the result summary pane, click **Result Details**. The result details pane displays the following fields.

- Test Name (displays the test id, test name, and selected lanes)
- Spec Range (displays the lower limit and upper limit of the rise time test)
- Meas Value (displays the measured value)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the relevant details, such as Tbit, Vswing, Upper Margin, and Lower Margin). If the test could not be run, the field displays an error code (see page 397).
- Result Statistics (displays statistics based on the tests)

14. In the Result Details dialog box, click **Result Statistics** to display statistics based on the tests. Click here (see page 50) for more information.



Test Method

This sequence explains the actions that the software takes while it performs a fall time test. For the procedure on how to make this test, see fall time test procedure (see page 233).

1. Refer to Fall Time (see page 73) for information on how to make connections for Fall Time test.
2. Set the trigger position at the center of the screen.
3. Set up the oscilloscope as follows:
   - Calculate T_{BIT} by using differential clock.
   - Set the vertical scale to accommodate the waveform in at least six divisions.
   - Set the horizontal scale to more than $2*T_{BIT}$.
   - If pulse width trigger is selected, Trigger with pulse width trigger with $(4*T_{BIT})$ pulse or trigger with edge trigger.
4. Accumulate at least 10,000 triggered waveforms by acquiring the waveform in FastAcq mode of acquisition.
5. Calculate V_{SWING} of the signal ($V_{SWING} = V_H – V_L$), and then find the 20 percent and 80 percent of the level.

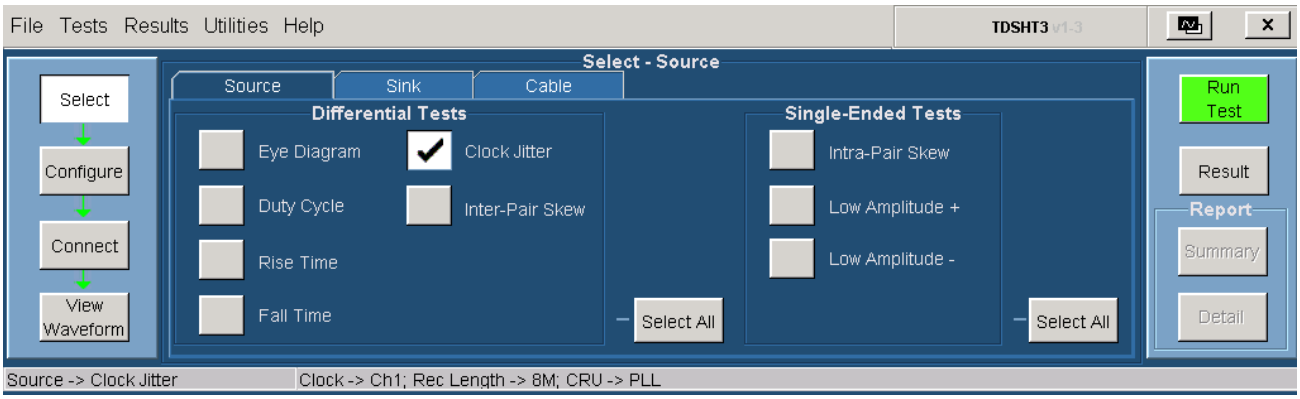
6. Measure the rise time and fall time.
   - Enable the oscilloscope rise time measurement. Set the reference level to 20 percent and 80 percent.
   - Acquire at least 10 K waveforms (RUN and STOP).
   - Calculate the rise time.
   - Set the trigger to negative pulse.
   - Enable the oscilloscope rise time measurement.
   - Acquire at least 10 K waveforms (RUN and STOP).
   - Calculate the fall time.
7. Compare with the limit.
   - If T_{RISE} is less than 75 ps or T_{RISE} is more than (0.4*T_{BIT}), it implies Fail.
   - If T_{FALL} is less than 75 ps or T_{FALL} is more than (0.4*T_{BIT}), it implies Fail.
8. Repeat the test for all the remaining TMDS clock and data pairs.

Test the Clock Jitter

This test allows you to confirm that the TMDS clock does not carry excessive jitter.

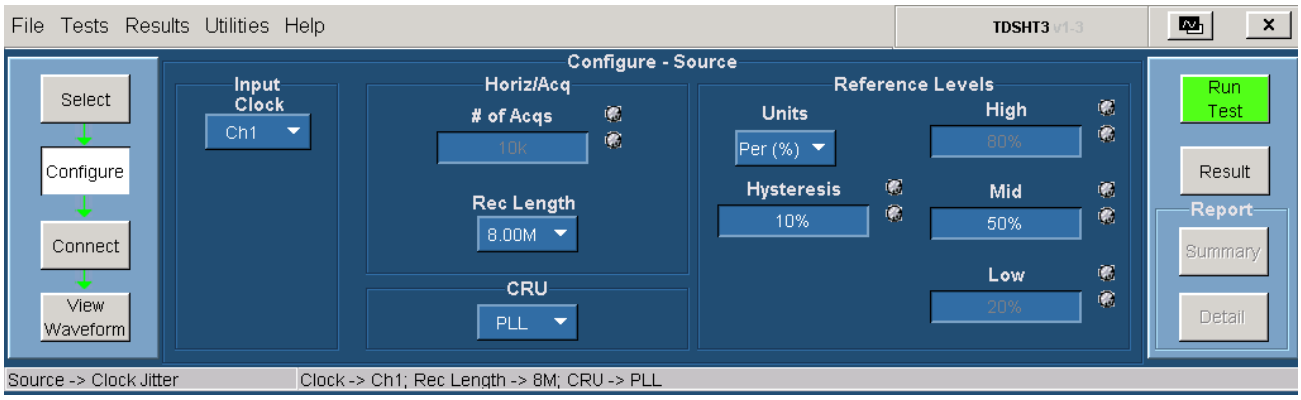
You will need a Digital Oscilloscope, one differential probe, one DC power supply 3.3 V, one EDID emulator, and one TPA-P fixture. For DPO/DSA/MSO70000 series oscilloscopes, an external power supply is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

1. On the menu bar, click **Tests > Select > Source**.
2. In the differential tests pane, select the Clock Jitter check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26)

or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



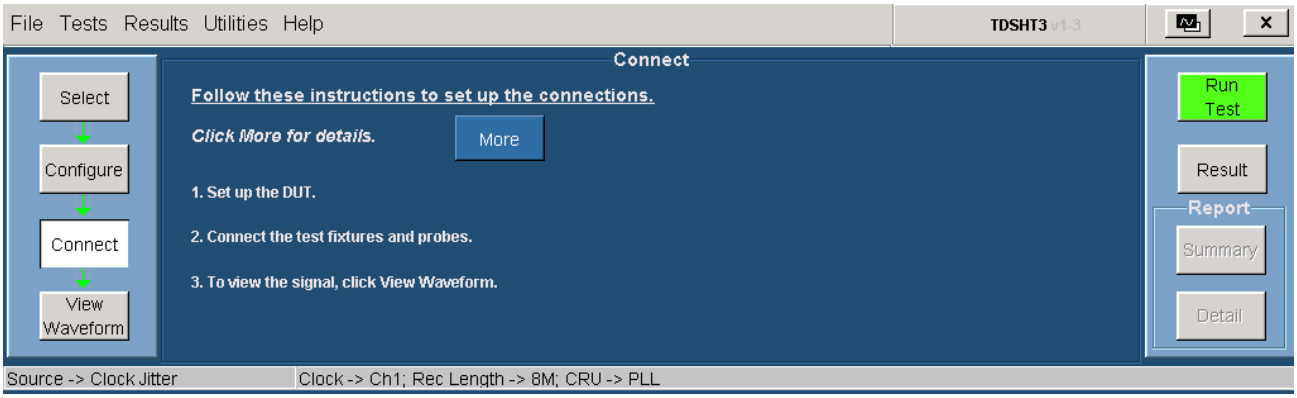
4. In the input pane, set the Input Clock to the channel that you will use for the HDMI clock input.
5. In the horiz/acq pane, the required number of acquisitions are set for the test. The default value is 10 K.

   Set the desired record length value for the clock jitter tests in the Rec Length box. Select from the available choices (8.00k, 16.0k, 40.0k, 80.0k, 200k, 400k, 800k, 2.00M, 4.00M, 8.00M, 20.0M, 32.0M). The default value is 32.0M.
6. In the CRU pane, configure the Clock Recovery Unit. The available choices are PLL, Raw, and Ideal. The default value is first order PLL and is used for compliance testing. Raw and Ideal are used for analysis.
7. In the reference levels pane, do the following:
   - Set the reference level units to either Per (%) or Abs.

     Per (%) indicates that the reference levels are a percentage of the Vswing value.

     Abs indicates that the reference levels are absolute voltage values.

     The default setting is Per (%).
   - In the Hysteresis box, enter the desired hysteresis percent value. The range is from 0% to 25% and default is 10%.
   - In the High box, the required high reference voltage value is set for the test. The default value is 80%.
   - In the Mid box, enter the desired mid reference voltage value. The range is from 25% to 75% and default is 50%.
   - In the Low box, the required low reference voltage value is set for the test. The default value is 20%.
8. To connect the DUT, click **Tests > Connect**. Click here (see page 77) for information on how to make connections.

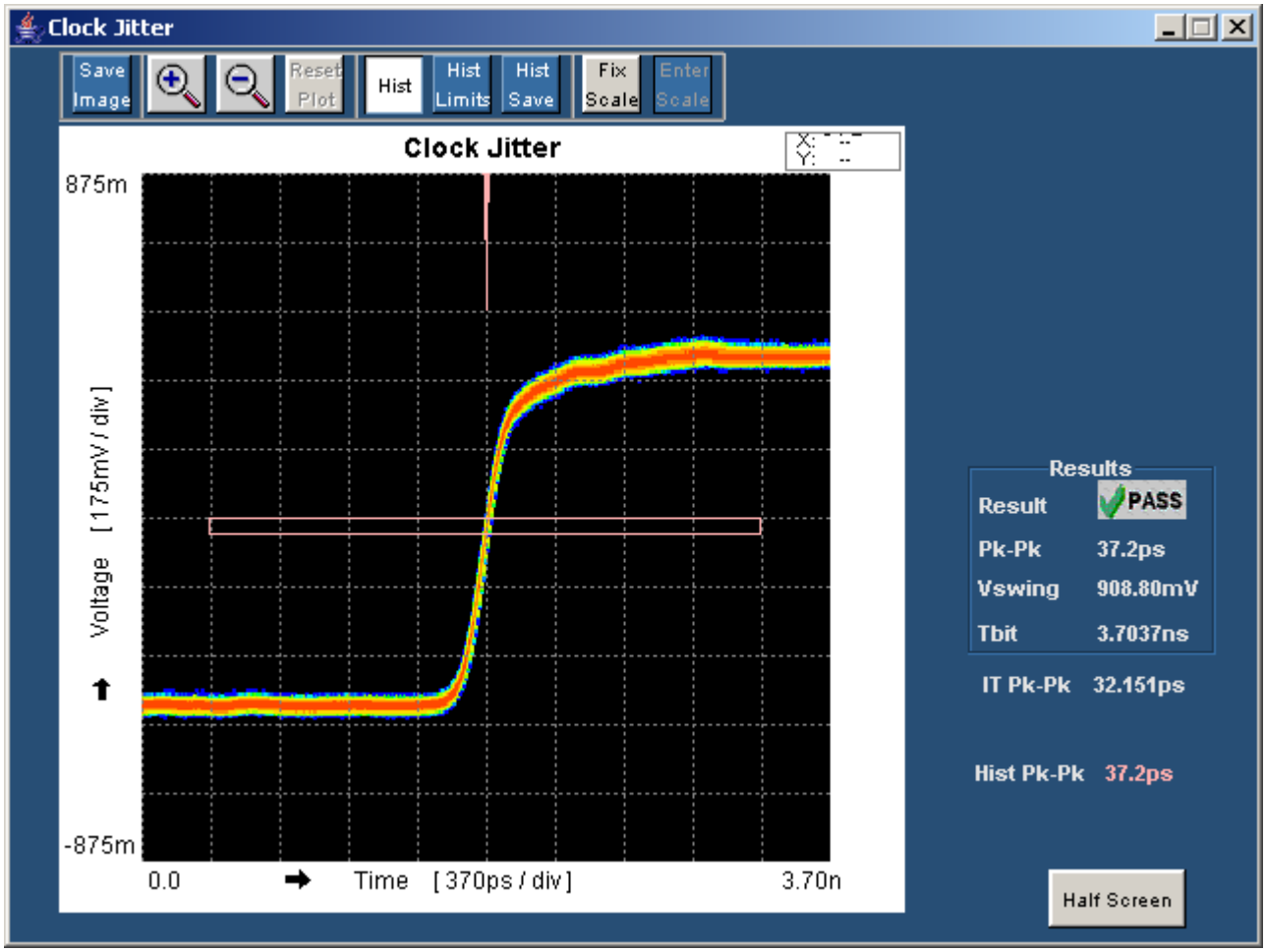


9. Ensure that your signal in the oscilloscope display is similar to the sample signal. Click View Waveform (see page 210) to display a sample of the expected signal. If the displays are not similar, go back and check your configuration and connections.

10. Click **Run Test** to perform the test. The TDSHT3 Software sets up the oscilloscope and the test runs, displaying a progress indicator.

11. If you have run the clock jitter test successfully, the software makes the results available automatically and displays the clock jitter plot.

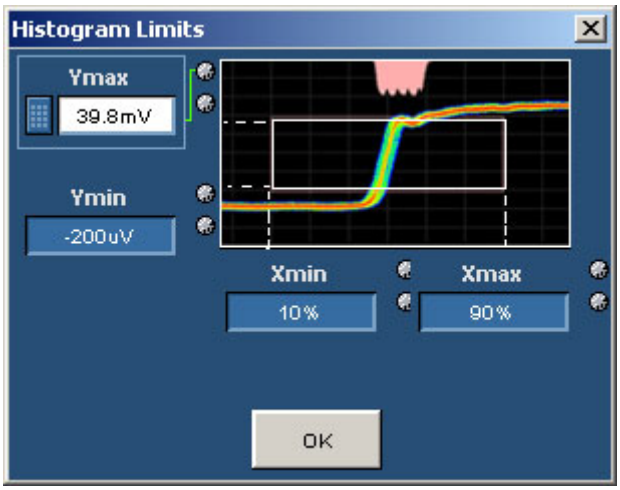
    The clock jitter plot is as follows:



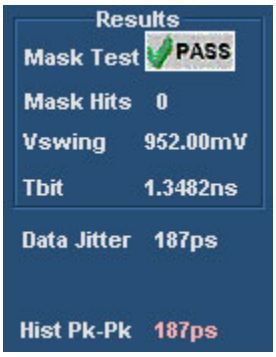
NOTE. *In the full screen mode, the histogram disappears if you click anywhere within the plot.*

Features on the Clock Jitter display include:

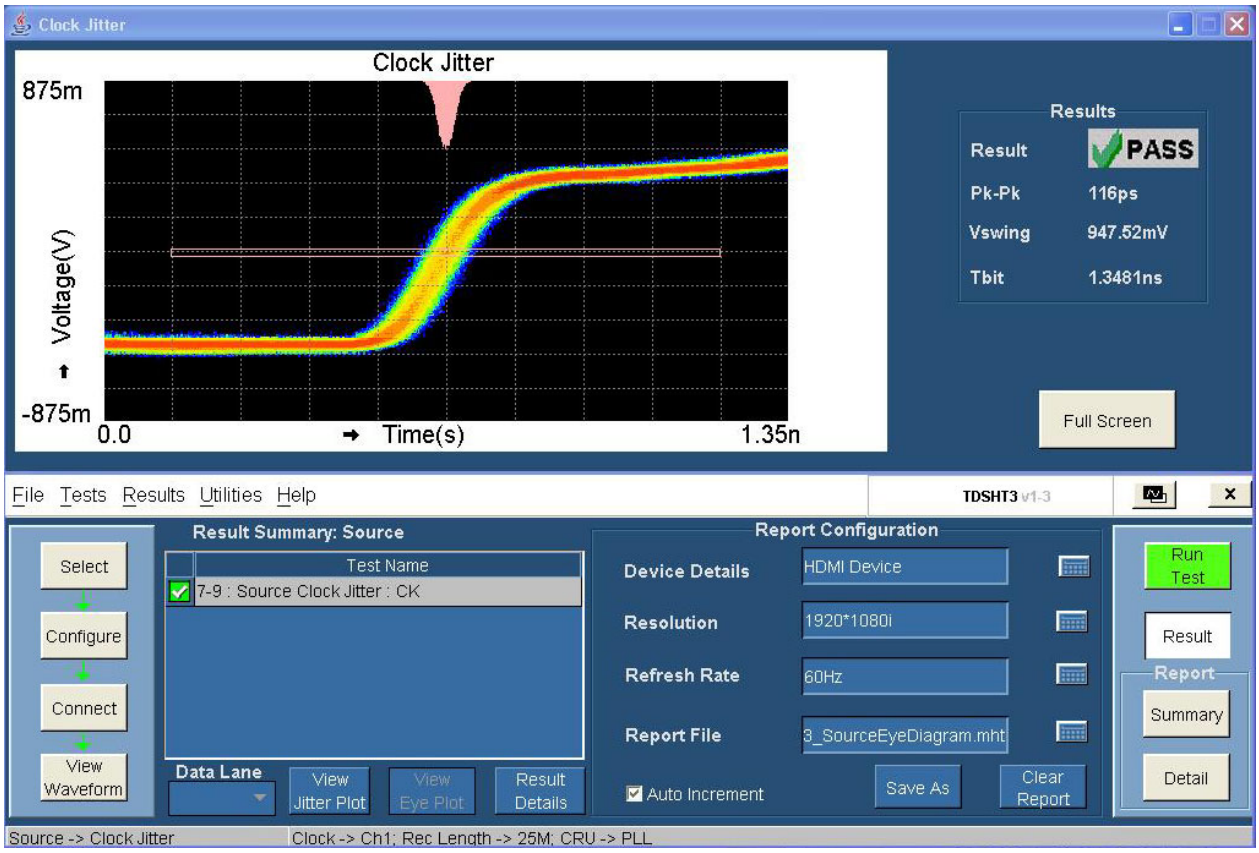
- Save: Click **Save Image** to save the clock jitter plot.
- Zoom: You can zoom in on an area of interest, up to five times the normal view. Either drag the mouse or click to define the area of interest.
- Reset Plot: Click **Reset Plot** to reset the plot.
- Histogram: Click **Hist** to draw the histogram on the eye diagram plot. Click **Hist Limits** to draw the histogram box, and **Hist Save** to save the histogram. Double-click the buttons next to the Ymax, Ymin, Xmin, and Xmax labels to type the X and Y histogram limits.



- Scale: Click **Fix Scale** to type in a new scale value, or click **Enter Scale** to type in a new vertical scale value.
- Results display: The results pane displays the result of the mask test result (pass or fail), mask hits (number of mask hits), Vswing value (voltage swing of the signal), and the Tbit value (time period of each bit). The IT Pk-Pk and the Hist Pk-Pk values are also shown near the results pane. If there is no value for IT Pk-Pk, it implies the absence of data points in the histogram window. In this case, increase the record length value and run the test again.

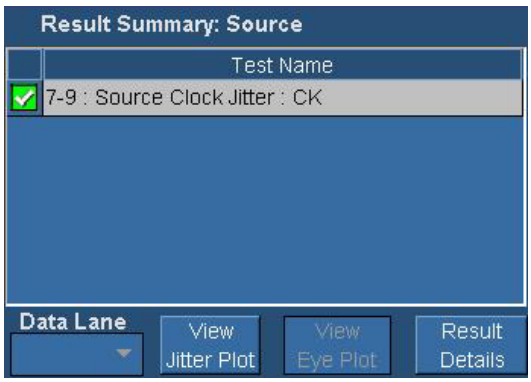


12. Click **Half Screen** to view the clock jitter plot in half screen. You can also view both the result summary of the test and the report configuration in the result pane as shown in the following figure.



The result pane displays the result summary pane and the report configuration pane.

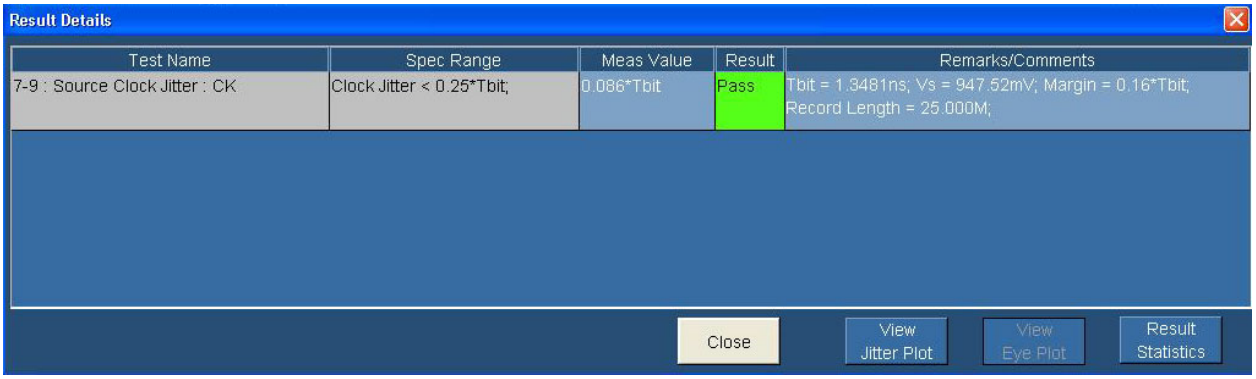
The result summary pane displays the test results. It lists the test name, status of the test (pass, fail or error), and jitter plot. To view the details of the results, click **Results Details**.



NOTE. *The View Jitter Plot option is available if you have successfully run the clock jitter test.*

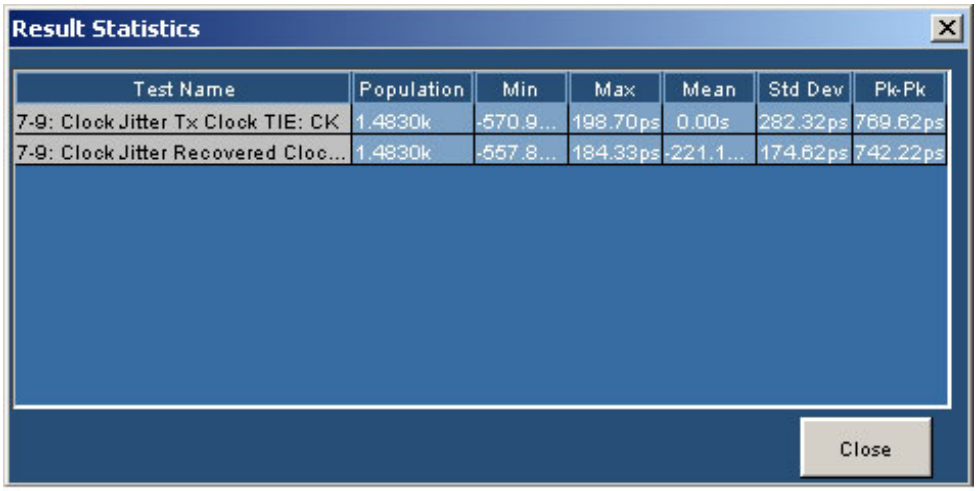
Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

13. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected lanes)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the measured value)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the results of Tbit, Vswing, and Margin). If the test could not be run, this field displays an error code (see page 397).

14. In the Result Details dialog box, click **Result Statistics** to display statistics based on the tests. Click here (see page 50) for more information.



Test Method

This sequence explains the actions that the software takes while it performs a clock jitter test. For the procedure on how to make this test, see clock jitter test procedure (see page 238).

1. Refer to Clock Jitter (see page 77) for information on how to make connections for Clock Jitter test.
2. Set up the oscilloscope as follows:
   - Adjust the vertical scale to accommodate the waveform in six vertical divisions
   - Set the record length to 25 M
   - Set the sample rate to ≥ 10 GS/s based on the oscilloscope
   - Trigger with the rising edge of the clock (50 percent level)
3. Capture the waveforms on the oscilloscope.

NOTE. *Do not transfer the waveforms.*

4. Perform software clock recovery as follows:
   - Set the reference level to 50 percent of the clock and hysteresis to 10 percent of V_{SWING}.
   - Calculate the Software CRU filter as follows.

     $H(s) = 1/(1+s\tau)$, where $\tau = 40$ nsec.
5. Draw the TMDS waveform with positive edge trigger.
6. Measure the clock jitter as follows:
   - Calculate V_{SWING} by using V_H and V_L of the clock.
   - Calculate the center voltage as follows:
     - $V_C = (V_H+V_L)/2$
   - Draw the histogram at V_C+ /-20 mV.
   - Calculate Pk-Pk jitter and 'Interpolated' Pk-pk jitter.
7. If clock jitter exceeds ($0.25*T_{BIT}$), it implies Fail.

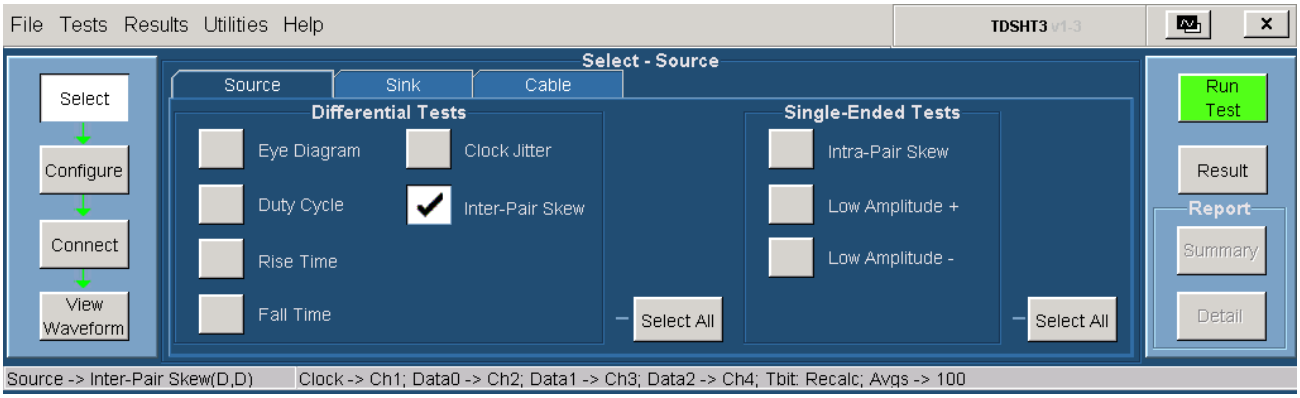
Test the Source Inter-Pair Skew

This test allows you to confirm that any skew between the differential pairs in the TMDS portion of the HDMI link does not exceed the limits in the specification.

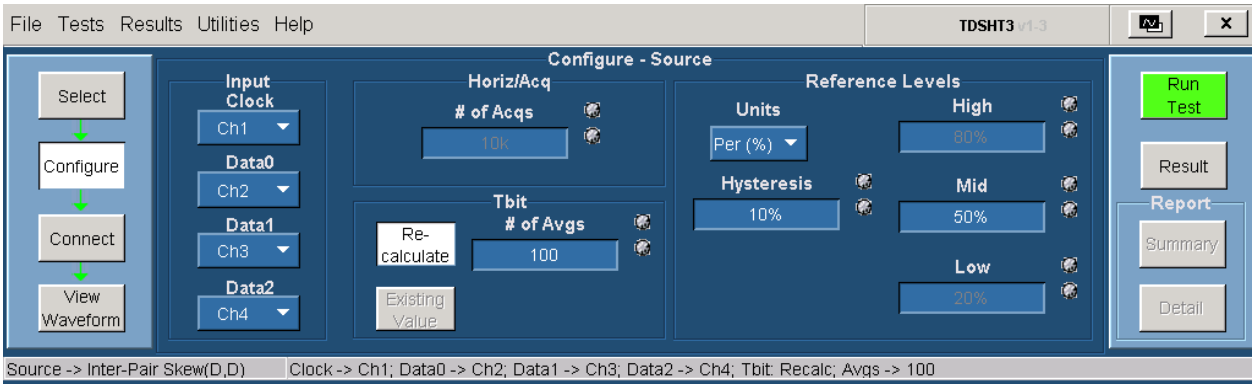
You will need a Digital Oscilloscope, two/four differential probes, one DC power supply 3.3 V, one EDID emulator, and one TPA-P fixture. For DPO/DSA/MSO70000 series oscilloscopes, an external power supply is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

NOTE. *Deskew (see page 45) is recommended before you conduct any skew test.*

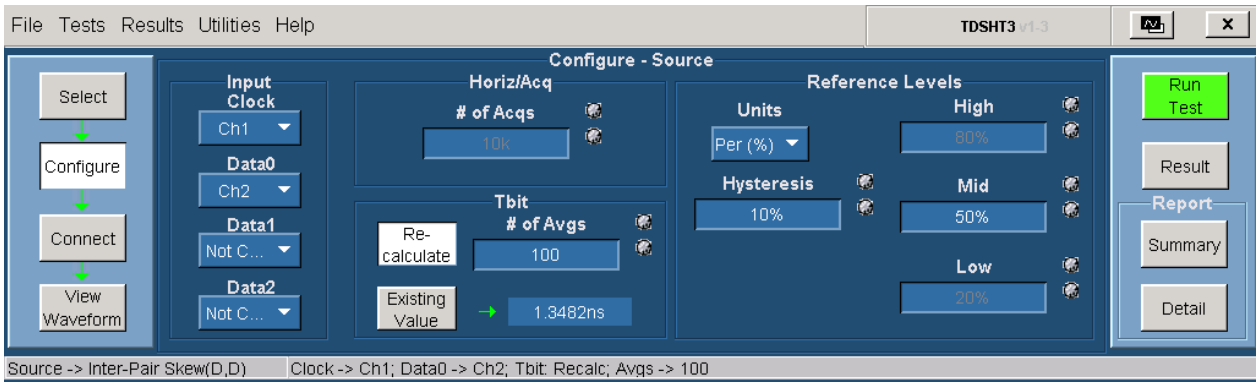
1. On the menu bar, click **Tests > Select > Source**.
2. In the differential tests pane, select the Inter-Pair Skew check box.

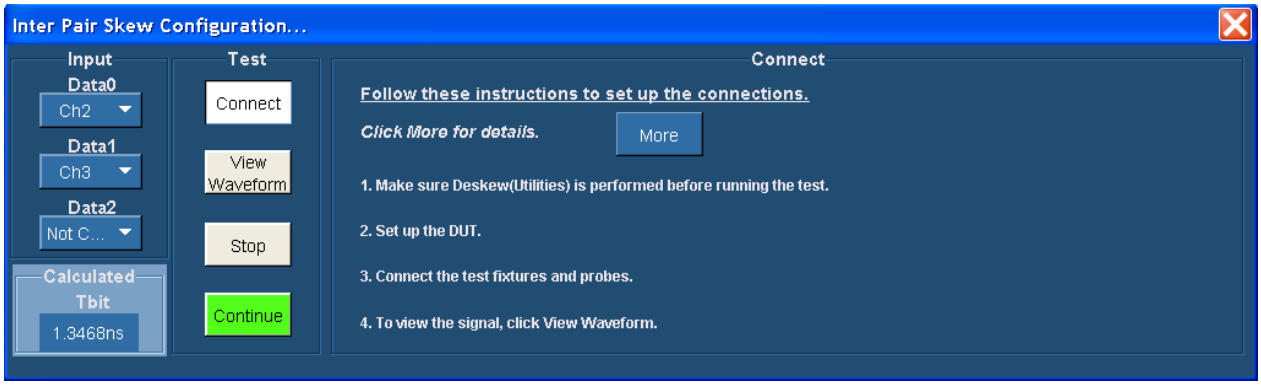


3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



For 2-Channel setup, the configuration is as follows:





Remove the clock signal connection and connect the data pair between which you want to calculate the skew.

4. In the input pane, do the following:
   - Set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
   - Set the Input Data0, Data1, and Data2 to the channel that you will use for the corresponding HDMI data inputs. Select from the available choices (Ch1, Ch2, Ch3, Ch4, and Not Conn).
5. In the tbit pane, do the following:
   - Enter the desired number of averages (periods) that are considered to calculate Tbit. The range is from 2 to 1 K and default is 100.
   - Click **Re-calculate** to recalculate the Tbit value.
   - Click **Existing Value** to use the previously calculated Tbit value.
6. In the reference levels pane, do the following:
   - Set the reference level units to either Per (%) or Abs.

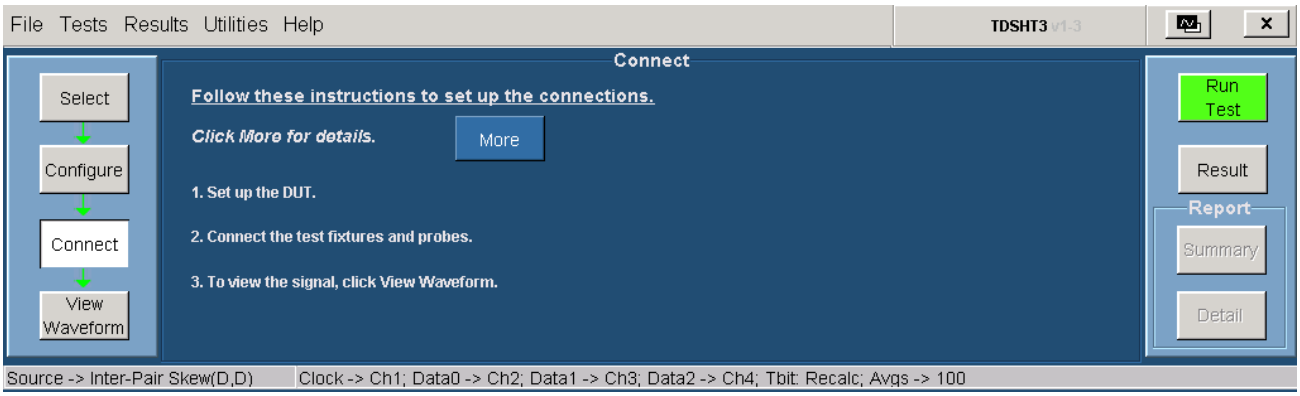
     Per (%) indicates that the reference levels are a percentage of the Vswing value.

     Abs indicates that the reference levels are absolute voltage values.

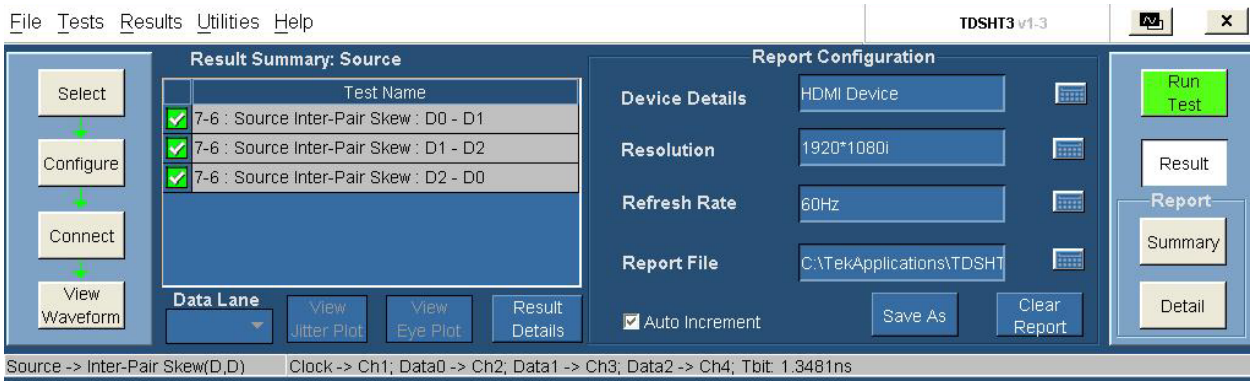
The default setting is Per (%).

- In the Hysteresis box, enter the desired hysteresis percent value. The range is from 0% to 25% and default is 10%.
- In the High box, the required high reference voltage value is set for the test. The default value is 80%.
- In the Mid box, enter the desired mid reference voltage value. The range is from 25% to 75% and default is 50%.
- In the Low box, the required low reference voltage value is set for the test. The default value is 20%.

7. To connect the DUT, click **Tests > Connect**. Click here (see page 80) for information on how to make connections.



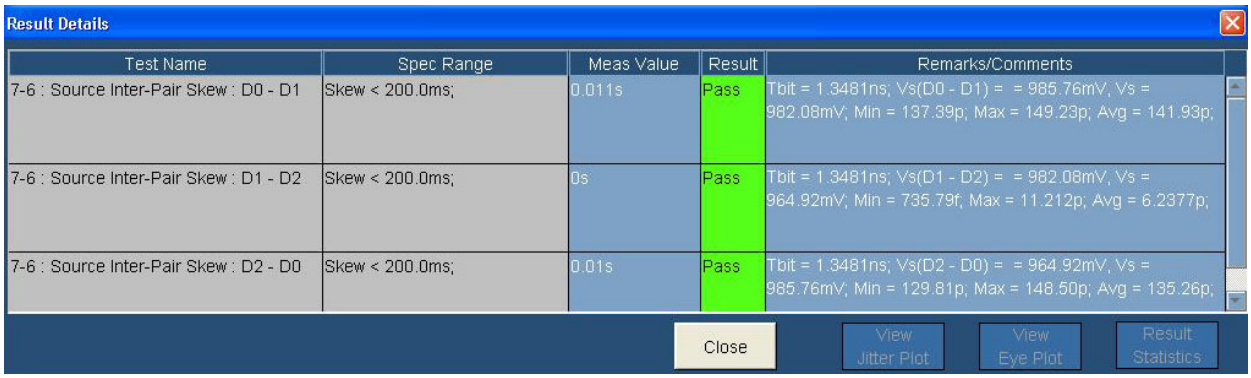
8. Ensure that your signal in the oscilloscope display is similar to the sample signal. Click View Waveform (see page 211) to display a sample of the expected signal. If the displays are not similar, go back and check your configuration and connections. The waveform shown here is for the re-calculate Tbit option. Click **Run Test** to run the test. The Confirm dialog box appears. Click **Continue** to continue to run the test. Go to step 10.
9. If you have selected existing the Tbit value, click **View Waveform** to get a different waveform on your display. Ensure that your signal in the oscilloscope display is similar to the sample signal.
10. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and the test runs, displaying a progress indicator.
11. The software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name, status of the test (pass, fail or error), and jitter plot. To view the details of the results, click **Results Details**.

12. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

13. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected lanes)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the measured value)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the relevant details, such as Tbit, Vswing, and Margin. If the test could not be run, this field displays an error code (see page 397).

Test Method

This sequence explains the actions that the software takes while it performs an inter-pair skew test. For the procedure on how to make this test, see inter-pair skew test procedure (see page 245).

1. Refer to Inter-Pair Skew (see page 80) for information on how to make connections for Clock Jitter test.
2. Set up the oscilloscope and acquire the waveform.
   - Adjust the vertical scale to accommodate the waveform in six vertical divisions.
   - Calculate T_{BIT} by using differential clock
   - Set the sample rate to ≥ 10 GS/s based on the oscilloscope
   - Set the bit rate based on the T_{BIT} value
   - Acquire the waveform in real-time single shot
3. Calculate the inter-pair skew as follows:
   - Find the CTL pattern in Data<X>
   - Find the CTL pattern in Data<Y>
   - Find the skew between the two channels in each transition
   - Calculate the average skew
4. If T_{SKEW} is greater than $(0.2*T_{PIXEL})$, it implies Fail.
5. Repeat the test for the remaining combinations of TMDS pairs.

CTL Patterns

Use the following patterns to perform the inter-pair skew measurement:

NOTE. *The patterns vary based on the HDMI data lane input.*

10-bit pattern.

0010101011 for Data0, Data1, Data2

1101010100 for Data0, Data1, Data2

0010101010 for Data0

1101010101 for Data0

20–bit pattern.

00101010110011001101 for Data0

11010101010011001101 for Data0

11010101001100110010 for Data1

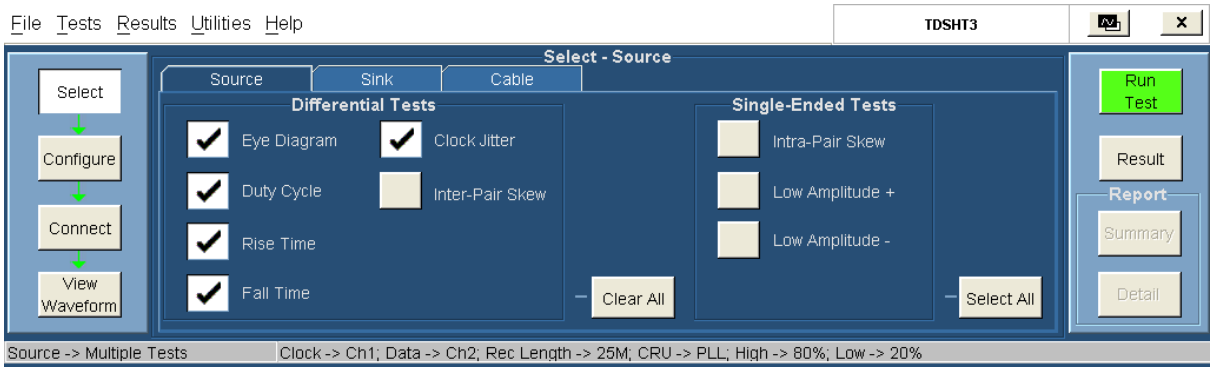
00101010110011001101 for Data2

Test the Differential Tests Select All

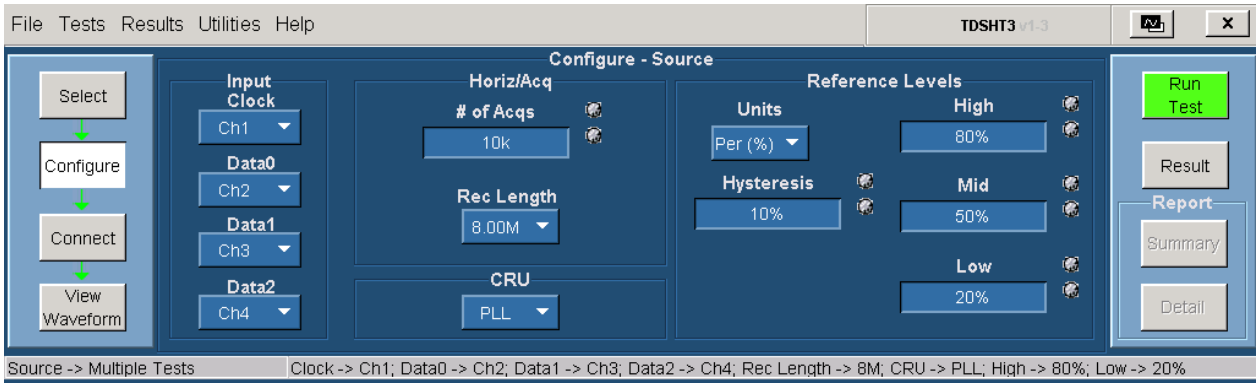
This option enables you to run the eye diagram, duty cycle, rise time, fall time, and clock jitter test simultaneously.

You will need a Digital Oscilloscope, two/four differential probes, one DC power supply 3.3 V, one EDID emulator, and one TPA-P fixture. For DPO/DSA/MSO70000 series oscilloscopes, an external power supply is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

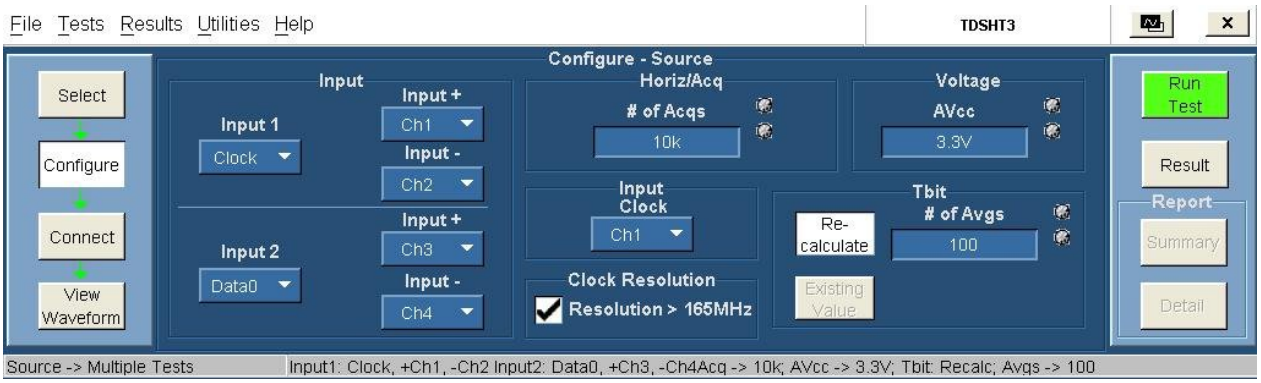
1. On the menu bar, click **Tests > Select > Source**.
2. In the differential tests pane, click **Select All**.

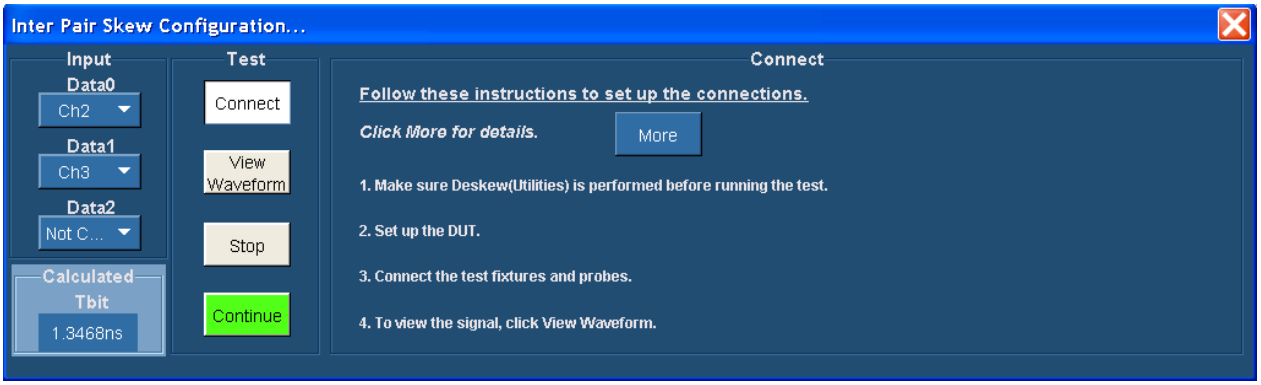


3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



For 2-Channel setup, the configuration is as follows:





Remove the clock signal connection and connect the data pair between which you want to calculate the skew.

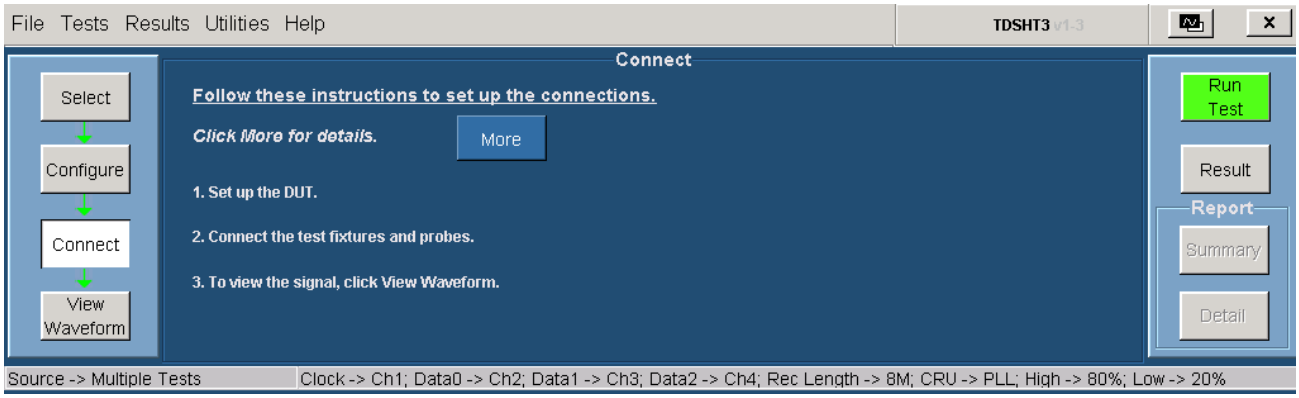
4. In the input pane, do the following:
   - Set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
   - Set the Input Data0, Data1, and Data2 to the channel that you will use for the corresponding HDMI data inputs. Select from the available choices (Ch1, Ch2, Ch3, Ch4, and Not Conn).
5. In the horiz/acq pane, do the following:
   - In the horiz/acq pane, enter the desired number of acquisitions that are required for the test. The range is from 10 K to 1 M and default is 10 K.
   - In the Rec Length box, set the desired record length value for all the selected tests in the Rec Length box. Select from the available choices (8.00k, 16.0k, 40.0k, 80.0k, 200k, 400k, 800k, 2.00M, 4.00M, 8.00M, 20.0M, 32.0M). The default value is 32.0M.

6. In the CRU pane, do the following:
   - Configure the Clock Recovery Unit. The available choices are PLL, Raw, and Ideal. The default value is first order PLL and is used for compliance testing. Raw and Ideal are used for analysis.
7. In the reference levels pane, do the following:
   - Set the reference level units to either Per (%) or Abs.

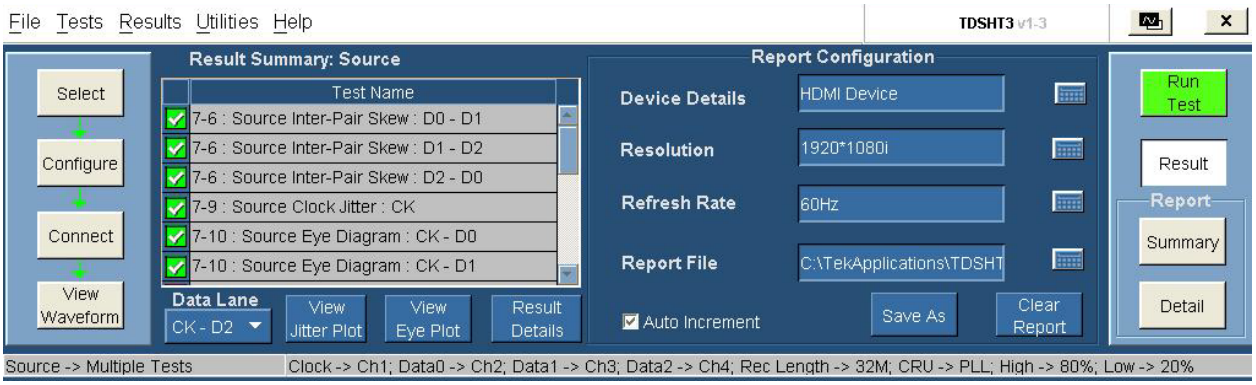
     Per (%) indicates that the reference levels are a percentage of the Vswing value.

     Abs indicates that the reference levels are absolute voltage values.

     The default setting is Per (%).
   - In the Hysteresis box, enter the desired hysteresis percent value. The range is from 0% to 25% and default is 10%.
   - In the High box, enter the desired high reference voltage value. The range is from 50% to 100% and default is 80%.
   - In the Mid box, enter the desired mid reference voltage value. The range is from 25% to 75% and default is 50%.
   - In the Low box, enter the desired low reference voltage value. The range is from 1% to 50% and default is 20%.
8. To connect the DUT, click **Tests > Connect**. Click here (see page 87) for information on how to make connections.



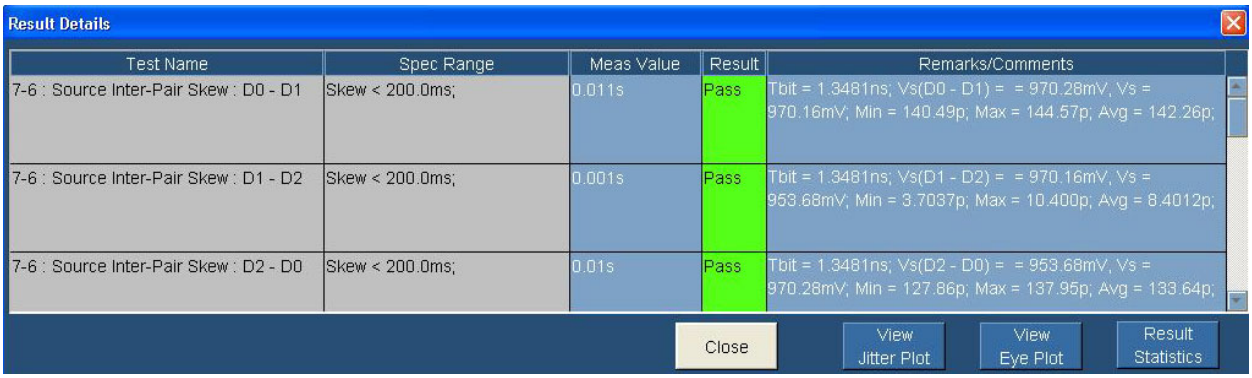
9. Ensure that your signal in the oscilloscope display is similar to the sample signal. Click View Waveform (see page 212) to display a sample of the expected signal. If the displays are not similar, go back and check your configuration and connections.
10. Click **Run Test** to perform the test. The TDSHT3 Software sets up the oscilloscope and the test runs, displaying a progress indicator.
11. If you have run the tests successfully, the software makes the results available automatically and displays the eye diagram plot and the clock jitter plot. For more information on the plots, refer to the section on the eye diagram and the clock jitter tests. You can also view both the result summary of the test and the report configuration in the result pane as shown in the following figure:



The results summary lists the test name, status of the test (pass, fail or error), jitter plot for the clock jitter test, and eye plot for the eye diagram test. To view the details of the results, click **Results Details**.

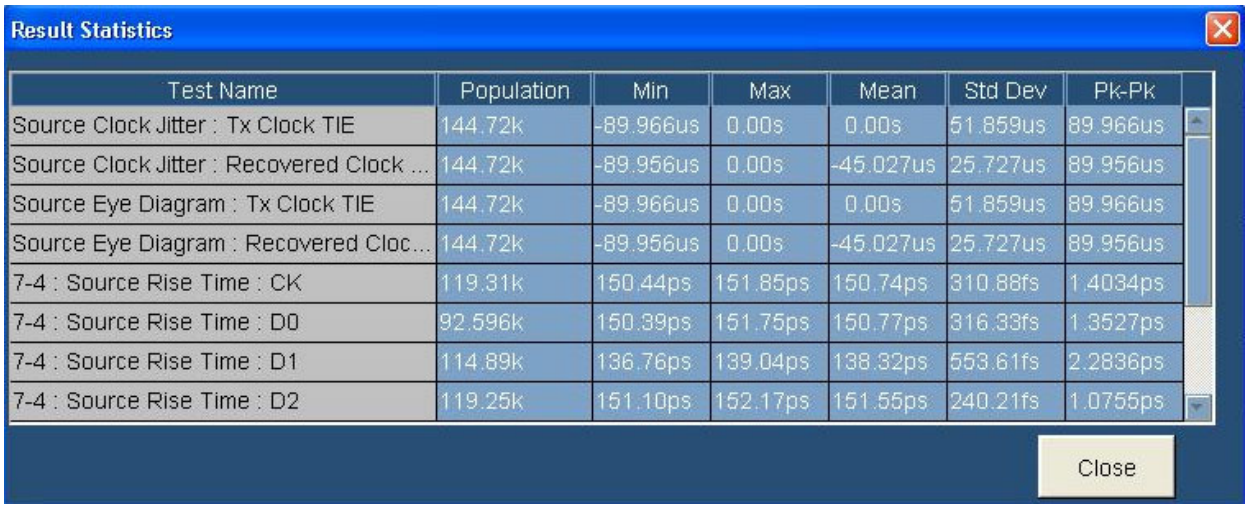
12. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

13. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected lanes)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the results of Tbit, Vswing, and Margin). If the test could not be run, this field displays an error code (see page 397).
- View Jitter Plot (displays the jitter plot for the clock jitter test)
- View Eye Plot (displays the eye plot for the eye diagram test)
- Result Statistics (displays statistics based on the tests)

14. In the Result Details dialog box, click **Result Statistics** to display statistics based on the tests. Click here (see page 50) for more information.



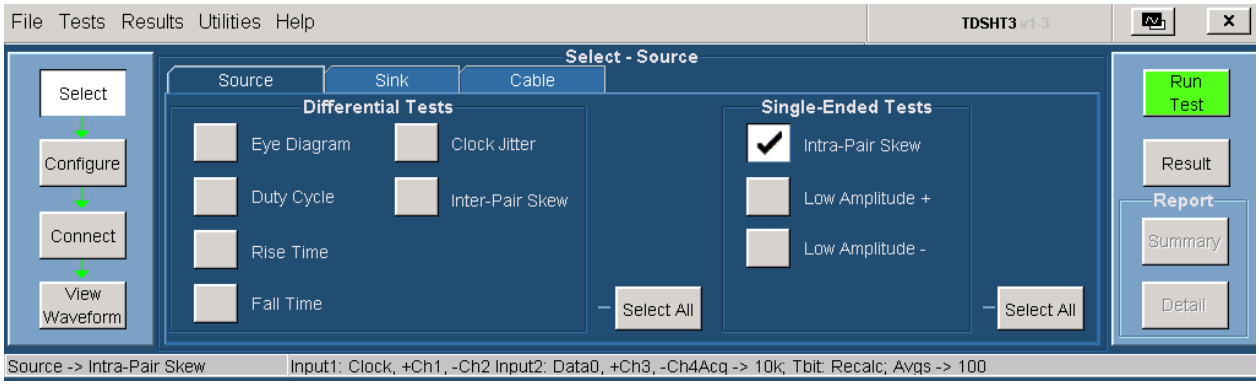
NOTE. *Perform similar steps as mentioned in this procedure to test Single-Ended Select All.*

Test the Source Intra-Pair Skew

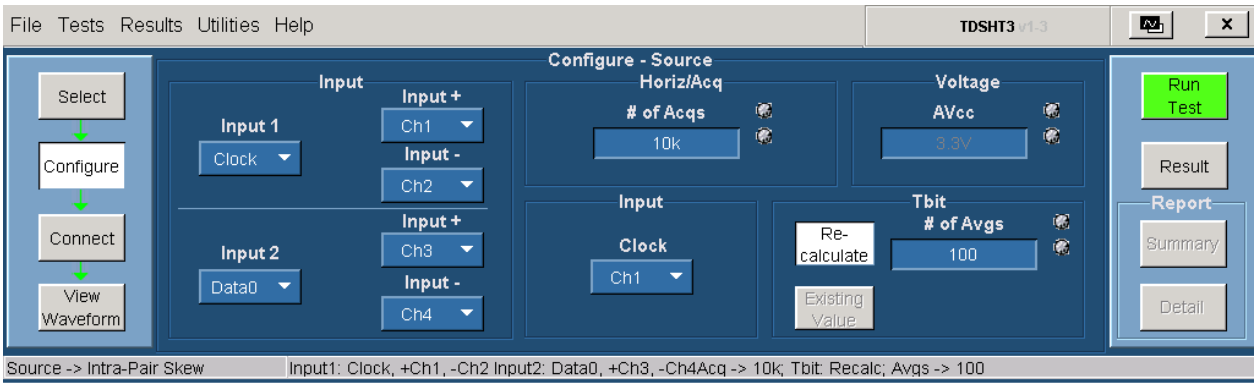
This test allows you to confirm that any skew within any one differential pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.

You will need a Digital Oscilloscope, two single-ended probes, one DC power supply 3.3 V, one EDID emulator, and one TPA-P fixture. For DPO/DSA/MSO70000 series oscilloscopes, an external power supply is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

1. On the menu bar, click **Tests > Select > Source**.
2. In the single-ended tests pane, select the Intra-Pair Skew check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



4. In the input pane, do the following:

   - Set the Input1, Input+, and Input– to the channel that you will use for the HDMI inputs.

     Input1 indicates the source channel to which you will connect the HDMI input. Select from the available choices (Clock, Data0, Data1, and Data2).

     Input+ indicates the source channel to which you will connect the positive input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

     Input– indicates the source channel to which you will connect the negative input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

   - Set the Input2, Input+, and Input– to the channel that you will use for the HDMI inputs.

     Input2 indicates the source channel to which you will connect the HDMI input. Select from the available choices (Clock, Data0, Data1, Data2, and Not Conn).

     Input+ indicates the source channel to which you will connect the positive input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

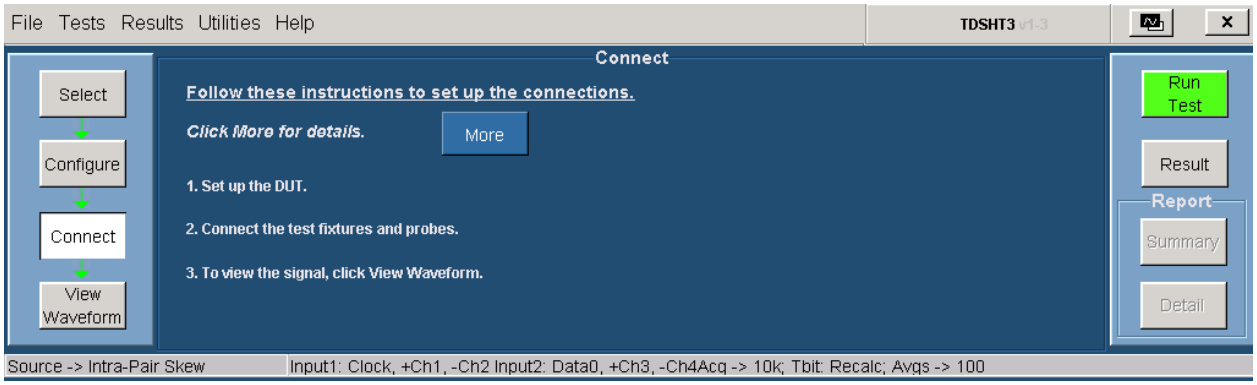
     Input– indicates the source channel to which you will connect the negative input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

5. In the horiz/acq pane, enter the desired number of acquisitions that are required for the test. The range is from 10 K to 1 M and default is 10 K.

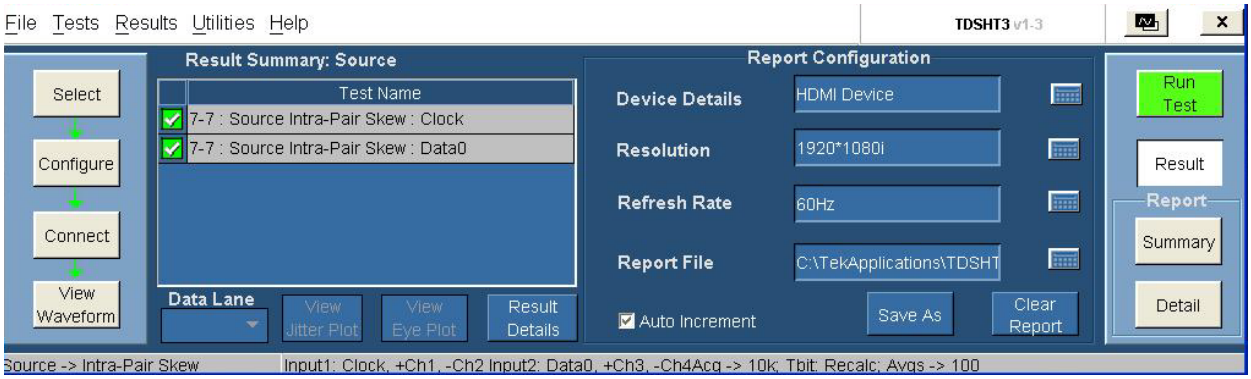
6. In the input pane, set the Clock channel that you want to use. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

7. In the voltage pane, the required voltage value is set for the test. The default value is 3.3 V.

8. In the tbit pane, do the following:
   - Enter the desired number of averages (periods) that are considered to calculate Tbit. The range is from 2 to 1 K and default is 100.
   - Click **Re-calculate** to recalculate the Tbit value.
   - Click **Existing Value** to use the previously calculated Tbit value.
9. To connect the DUT, click **Tests > Connect**. Click here (see page 91) for information on how to make connections.



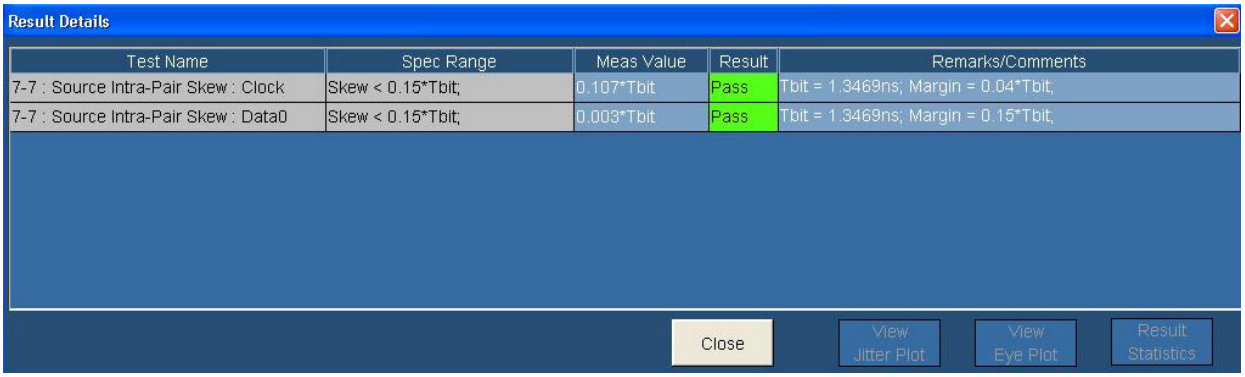
10. Ensure that your signal in the oscilloscope display is similar to the sample signal. Click View Waveform (see page 213) to display a sample of the expected signal. If the displays are not similar, go back and check your configuration and connections. The waveform shown here is for the re-calculate Tbit option. Click **Run Test** to run the test. The Confirm dialog box appears. Click **Continue** to continue to run the test. Go to step 13.
11. If you have selected existing the Tbit value, click **View Waveform** to get a different waveform on your display. Ensure that your signal in the oscilloscope display is similar to the sample signal.
12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and the test runs, displaying a progress indicator.
13. The software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and their status (pass, fail, or error). To view the details of the results, click **Results Details**.

14. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

15. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected lanes)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the measured value)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the relevant details, such as Tbit, Vswing, and Margin). If the test could not be run, this field displays an error code (see page 397).

Test Method

This sequence explains the actions that the software takes while it performs an intra-pair skew test. For the procedure on how to make this test, see intra-pair skew test procedure (see page 255).

1. Refer to Intra-Pair Skew (see page 91) for information on how to make connections for Intra-Pair Skew test.
2. Set up the oscilloscope as follows:
   - Calculate T_{BIT} by using differential clock.
   - Adjust the vertical scale to accommodate the waveform in six vertical divisions.
   - Set the horizontal scale to ($2*T_{BIT}$).
   - Trigger with edge trigger of Data+ (Rising edge with 50 percent level).
3. Display the waveform of TMDS_DATA0+ and DATA0-. Accumulate at least 10,000 triggers by acquiring the waveform in FastAcq mode.
4. Determine the most common TMDS_DATA0- 50 percent point by using the histogram method.

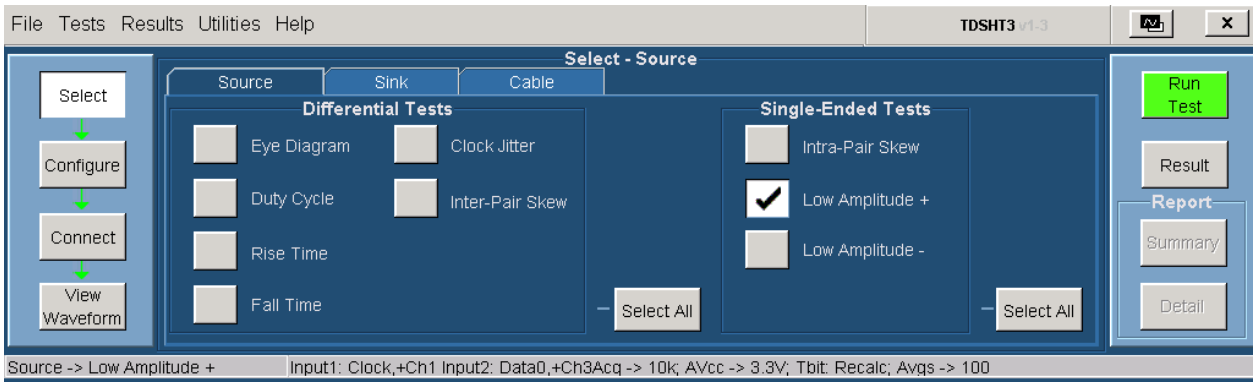
5. Measure skew from most common TMDS_DATA0+ point to 50 percent point of first edge of TMDS_DATA0-.
6. If skew is greater than ($0.15*T_{BIT}$), it implies Fail.
7. Repeat the test for all the remaining TMDS differential pairs.

Test the Low Amplitude +

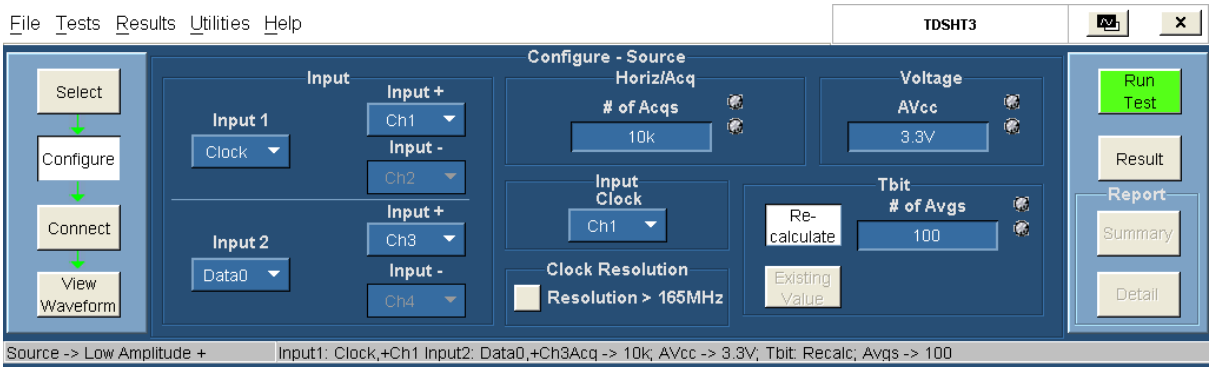
This test allows you to confirm that DC voltage levels on the HDMI link are within specified limits for each TMDS signal.

You will need a Digital Oscilloscope, one single-ended probe, one DC power supply 3.3 V, one EDID emulator, and one TPA-P fixture. For DPO/DSA/MSO70000 series oscilloscopes, an external power supply is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

1. On the menu bar, click **Tests > Select > Source**.
2. In the single-ended tests pane, select the Low Amplitude + check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



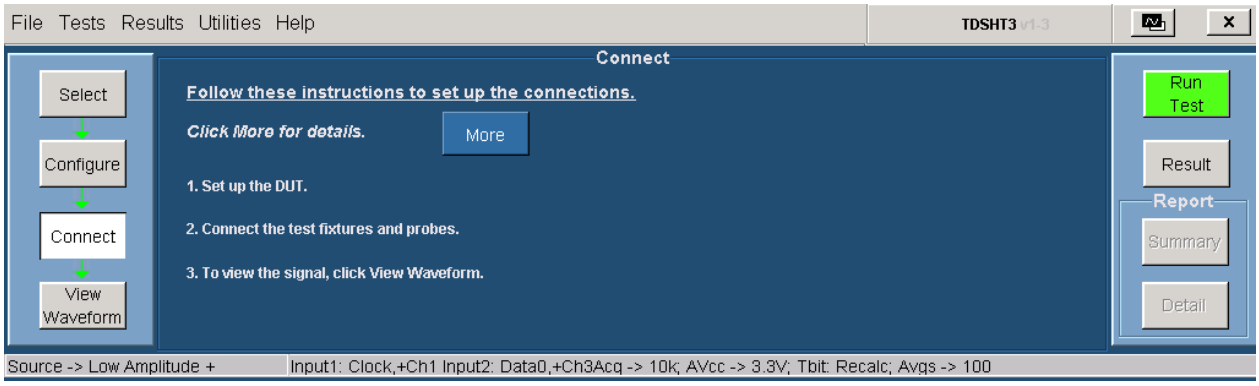
4. In the input pane, you have the following options:
   - Set the Input1 and Input+ to the channel that you will use for the HDMI inputs.

     Input1 indicates the source channel to which you will connect the HDMI input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

     Input+ indicates the source channel to which you will connect the positive input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
   - Set the Input2 and Input+ to the channel that you will use for the HDMI inputs.

     Input2 indicates the source channel to which you will connect the HDMI input. Select from the available choices (Ch1, Ch2, Ch3, Ch4, and Not Conn).

     Input+ indicates the source channel to which you will connect the positive input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
5. In the horiz/acq pane, enter the desired number of acquisitions that are required for the test. The range is from 10 K to 1 M and default is 10 K.
6. In the input clock pane, set the Clock channel that you want to use. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
7. In the clock resolution pane, select "Clock Resolution > 165MHz " when the DUT connected to Sink supports greater than 165 MHz resolution. Based on this selection, the software performs the test for both Lower (≤165 MHz) and Higher resolution (>165 MHz) as per CTS.
8. In the voltage pane, enter the desired voltage value. The range is from 1 V to 5 V and default is 3.3 V.
9. In the tbit pane, do the following:
   - Enter the desired number of averages (periods) that are considered to calculate Tbit. The range is from 2 to 1 K and default is 100.
   - Click **Re-calculate** to recalculate the Tbit value.
   - Click **Existing Value** to use the previously calculated Tbit value.
10. To connect the DUT, click **Tests > Connect**. Click here (see page 97) for information on how to make connections.

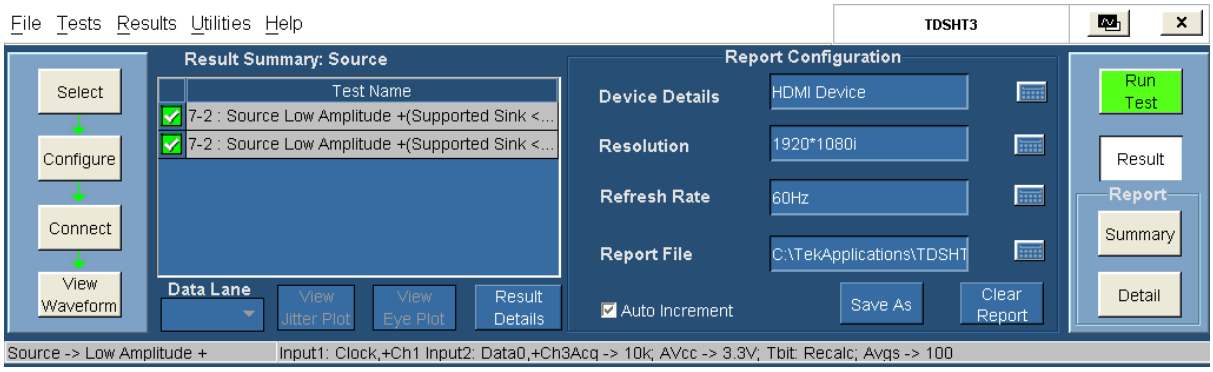


11. Ensure that your signal in the oscilloscope display is similar to the sample signal. Click View Waveform (see page 214) to display a sample of the expected signal. If the displays are not similar, go back and check your configuration and connections. The waveform shown here is for the re-calculate Tbit option. Click **Run Test** to run the test. The Confirm dialog box appears. Click **Continue** to continue to run the test. Go to step 11.

12. If you have selected existing the Tbit value, click **View Waveform** to get a different waveform on your display. Ensure that your signal in the oscilloscope display is similar to the sample signal.

13. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and the test runs, displaying a progress indicator.

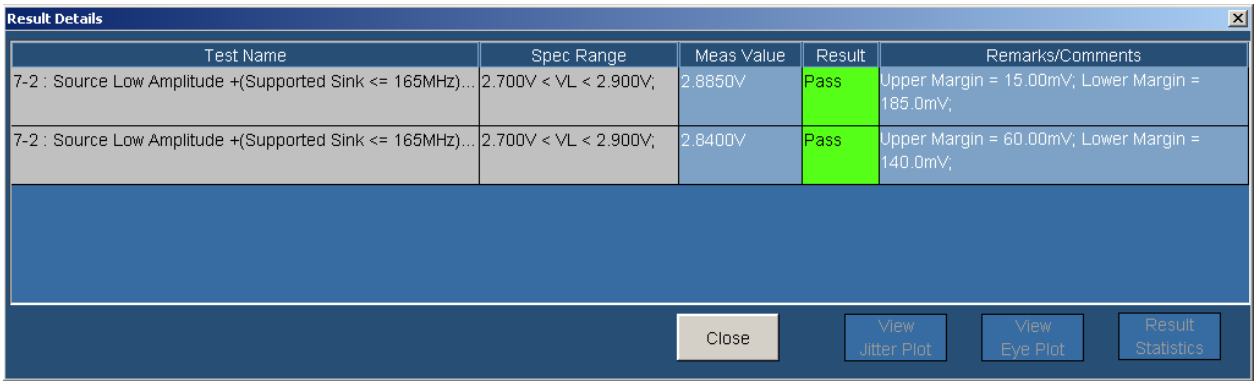
14. The software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and their status (pass, fail, or error). To view the details of the results, click **Results Details**.

15. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

16. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



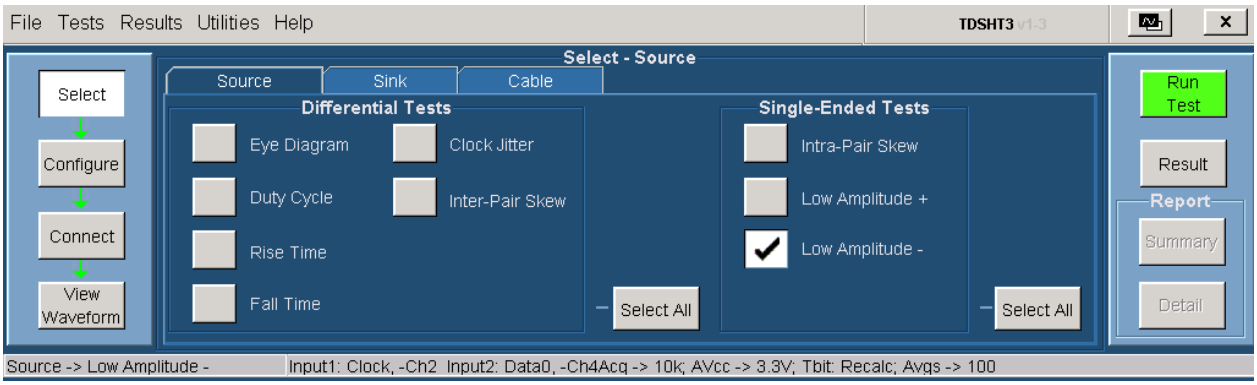
- Test Name (displays the test id, test name, and selected lanes)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the measured value in volts)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the relevant details of Tbit, Vswing, Upper Margin, and Lower Margin). If the test could not be run, this field displays an error code (see page 397).

Test the Low Amplitude -

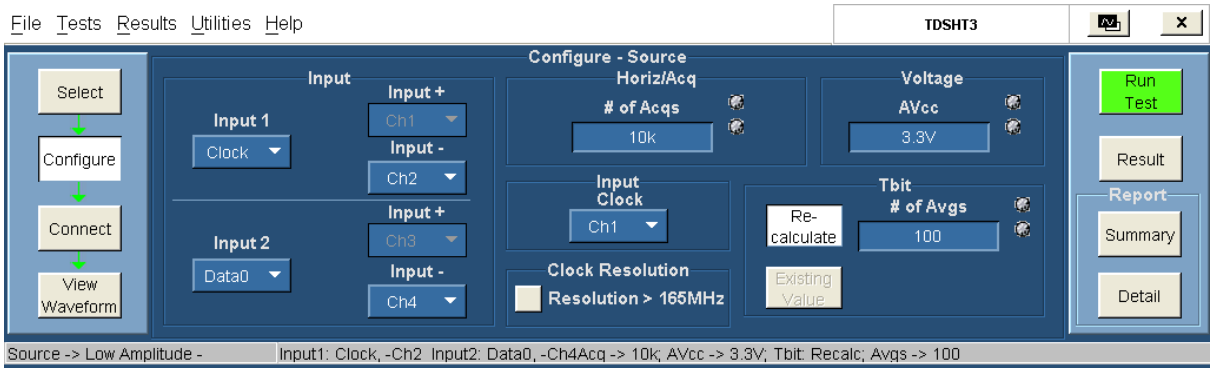
This test allows you to confirm that DC voltage levels on the HDMI link are within specified limits for each TMDS signal.

You will need a Digital Oscilloscope, one single-ended probe, one DC power supply 3.3 V, one EDID emulator, and one TPA-P fixture. For DPO/DSA/MSO70000 series oscilloscopes, an external power supply is not required if the internal power supply is used. See the Preferences (see page 24) menu for details.

1. On the menu bar, click **Tests > Select > Source**.
2. In the single-ended tests pane, select the Low Amplitude - check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



4. In the input pane, you have the following options:

   - Set the Input1 and Input– to the channel that you will use for the HDMI inputs.

     Input1 indicates the source channel to which you will connect the HDMI input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

     Input– indicates the source channel to which you will connect the negative input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

   - Set the Input2 and Input– to the channel that you will use for the HDMI inputs.

     Input2 indicates the source channel to which you will connect the HDMI input. Select from the available choices (Ch1, Ch2, Ch3, Ch4, and Not Conn).

     Input– indicates the source channel to which you will connect the input. Select from the available choices (Ch1, Ch2, Ch3, Ch4, and Not Conn).

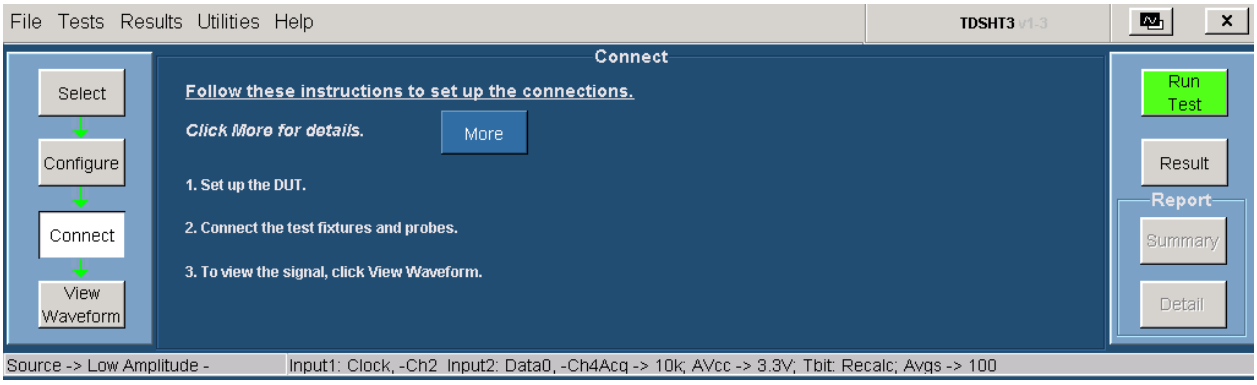
5. In the horiz/acq pane, enter the desired number of acquisitions that are required for the test. The range is from 10 K to 1 M and default is 10 K.

6. In the input clock pane, set the Clock channel that you want to use. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

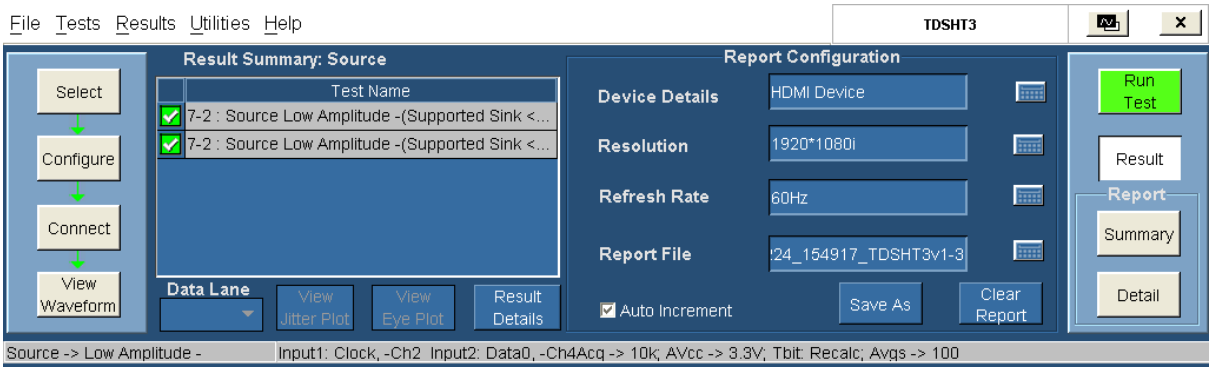
7. In the clock resolution pane, select "Clock Resolution > 165MHz " when the DUT connected to Sink supports greater than 165 MHz resolution. Based on this selection, the software performs the test for both Lower (≤165 MHz) and Higher resolution (>165 MHz) as per CTS.

8. In the voltage pane, enter the desired voltage value. The range is from 1 V to 5 V and default is 3.3 V.

9. In the tbit pane, do the following:
   - Enter the desired number of averages (periods) that are considered to calculate Tbit. The range is from 2 to 1 K and default is 100.
   - Click **Re-calculate** to recalculate the Tbit value.
   - Click **Existing Value** to use the previously calculated Tbit value.
10. To connect the DUT, click **Tests > Connect**. Click here (see page 103) for information on how to make connections.

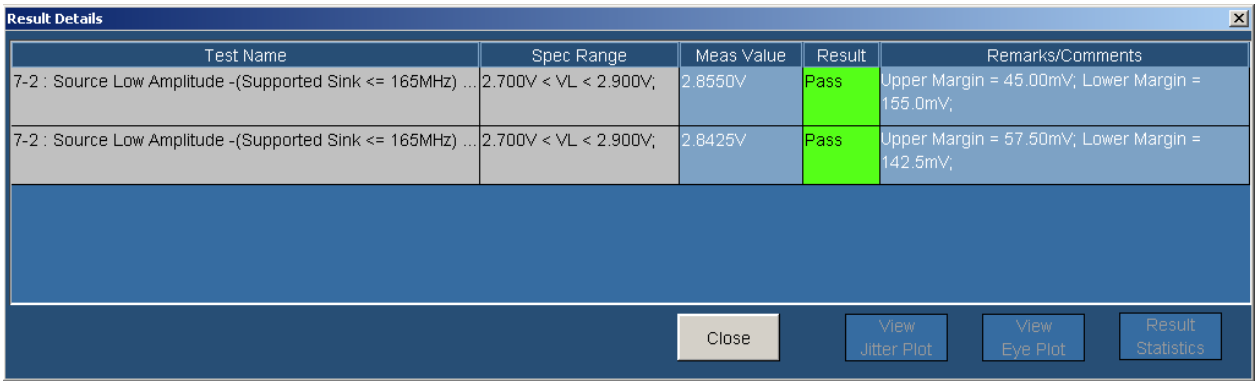


11. Ensure that your signal in the oscilloscope display is similar to the sample signal. Click View Waveform (see page 215) to display a sample of the expected signal. If the displays are not similar, go back and check your configuration and connections. The waveform shown here is for the re-calculate Tbit option. Click **Run Test** to run the test. The Confirm dialog box appears. Click **Continue** to continue to run the test. Go to step 13.
12. If you have selected existing the Tbit value, click **View Waveform** to get a different waveform on your display. Ensure that your signal in the oscilloscope display is similar to the sample signal.
13. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and the test runs, displaying a progress indicator.
14. The software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and their status (pass, fail, or error). To view the details of the results, click **Results Details**.

15. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected lanes)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the measured value in volts)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the relevant details of Tbit, Vswing, Upper Margin, and Lower Margin). If the test could not be run, this field displays an error code (see page 397).

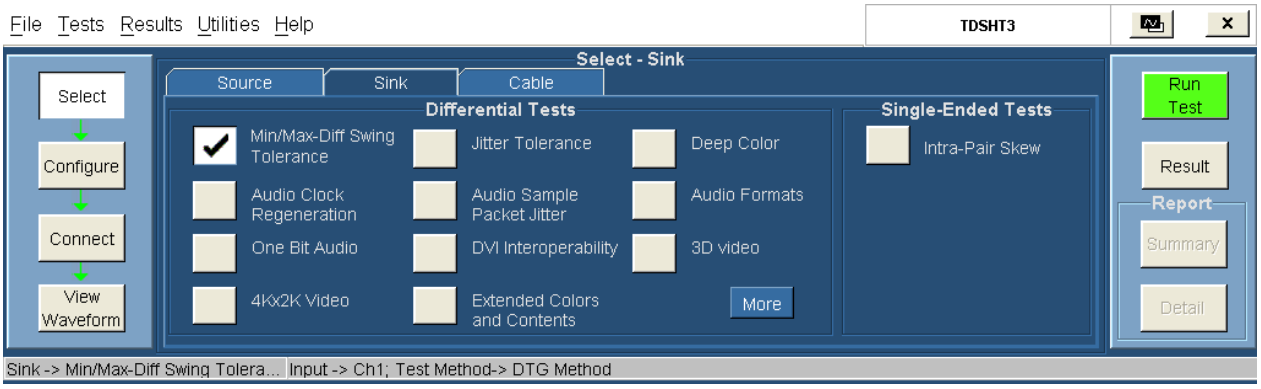
Test the Min/Max-Diff Swing Tolerance

This test allows you to confirm that the Sink correctly supports TMDS differential voltages at minimum levels.

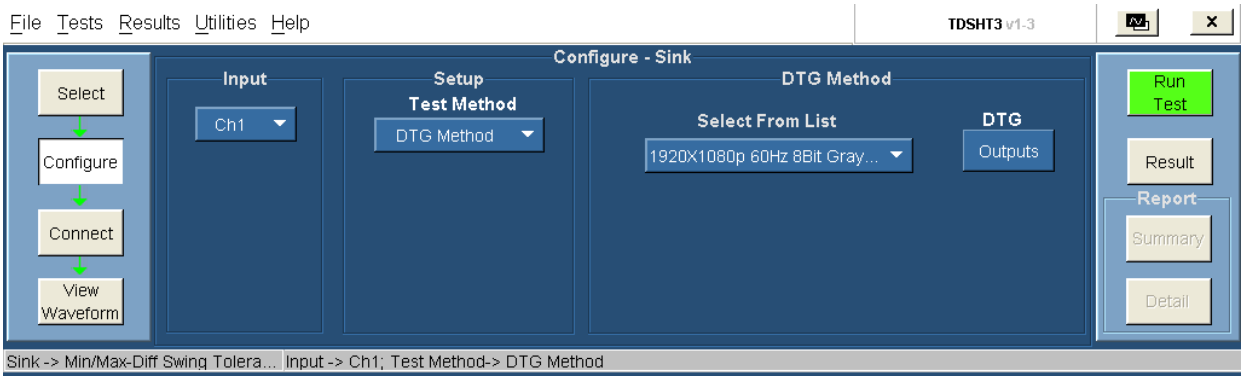
To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

To use the DDS test method, you will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the Min/Max-Diff Swing Tolerance check box.

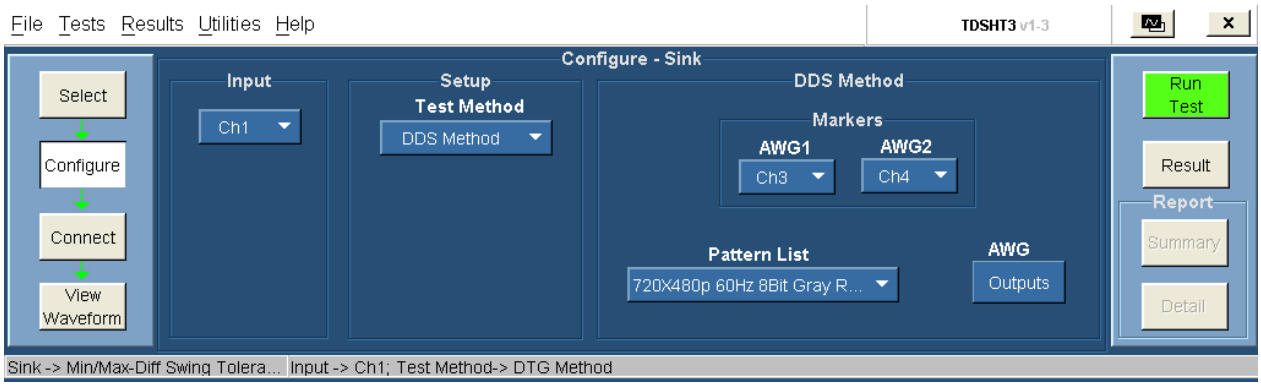


3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



4. In the Input pane, set the channel that you will use for the HDMI input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).
6. If the selected test method is DTG, do the following:
   - Select the DTG pattern file from the drop-down list.
   - Click **Outputs** to display a dialog box where you can set unique Clock, Data0, Data1, and Data2 outputs.

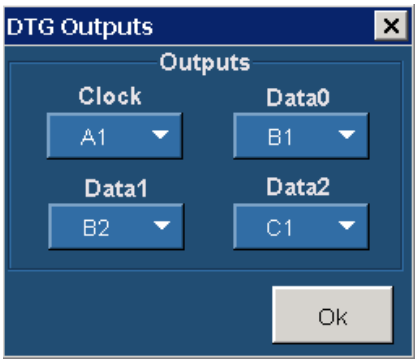
   If the selected test method is DDS, do the following:



- In the Markers pane:
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
- Select the DDS pattern file from the drop-down list for the selected DUT frequency.
- Click **Outputs** to display the AWG Output dialog box.

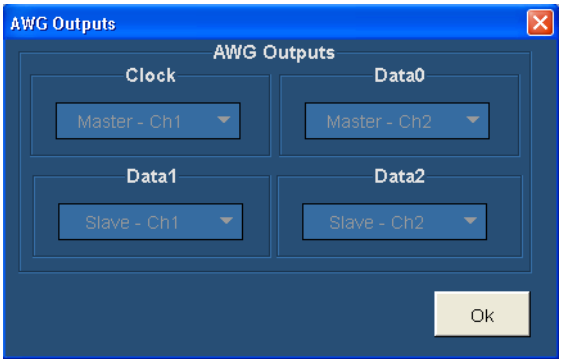
NOTE. *You cannot configure the AWG Outputs dialog box.*

7. The DTG Outputs dialog box has the following options:



- Clock (allows you to configure the Clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
- Data0, Data1, and Data2 (allows you to configure the corresponding data output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

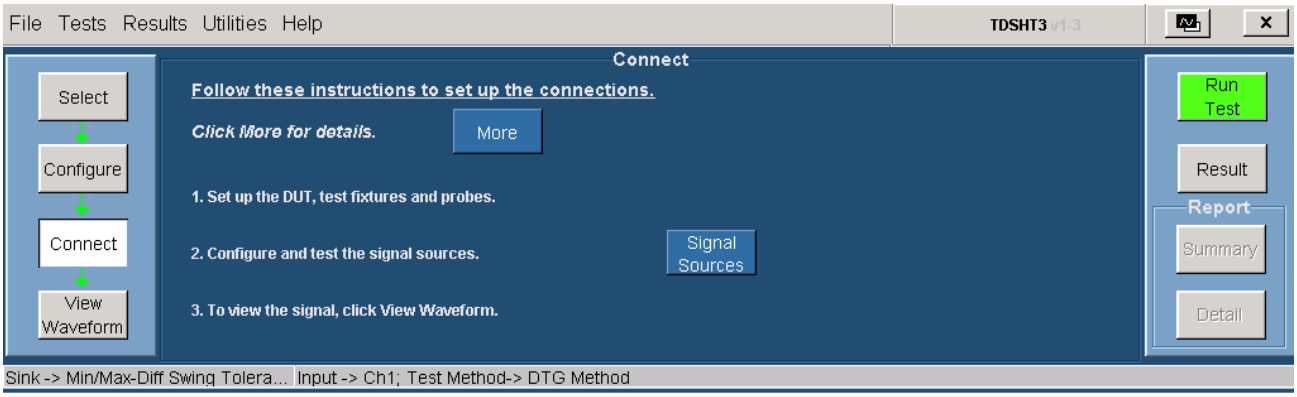
The AWG Outputs dialog box for the DDS method has following configurations:



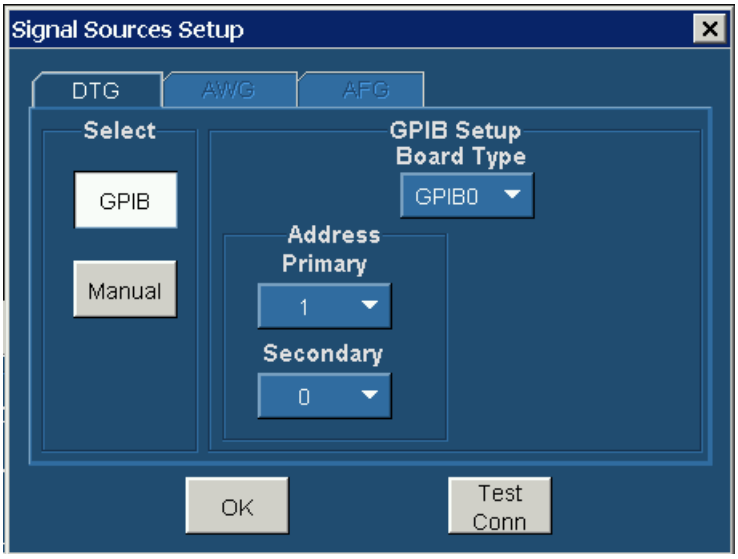
NOTE. *You cannot configure the AWG Outputs dialog box.*

NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

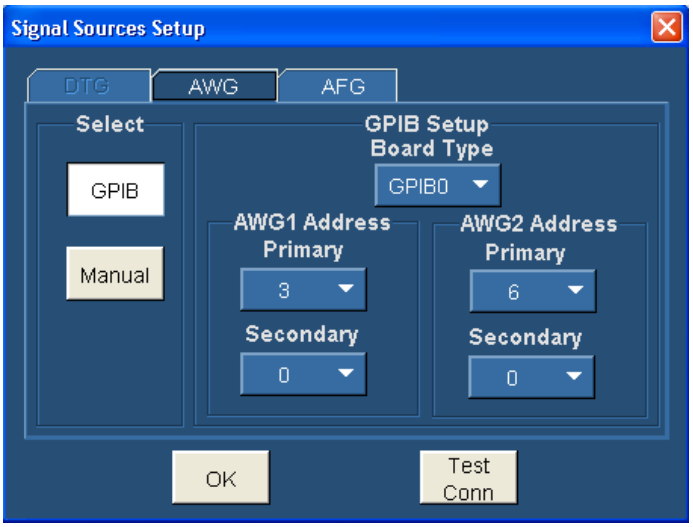
8. To connect the DUT, click **Tests > Connect**. Click here (see page 109) for information on how to make connections.



9. To configure and test the GPIB connection to the DTG, click **Signal Sources**. The Signal Sources Setup dialog box appears.



If you have selected the DDS test method, the AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

10. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.

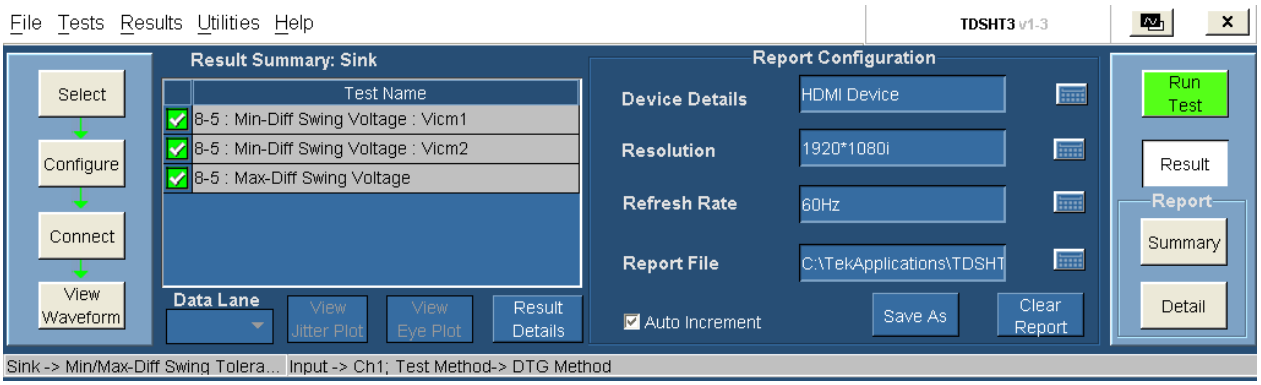
11. To test both the connection and the DTG GPIB configuration, click **Test Conn**.

12. Because no signal is connected to the oscilloscope, you cannot view the waveform for the min-diff sensitivity test.

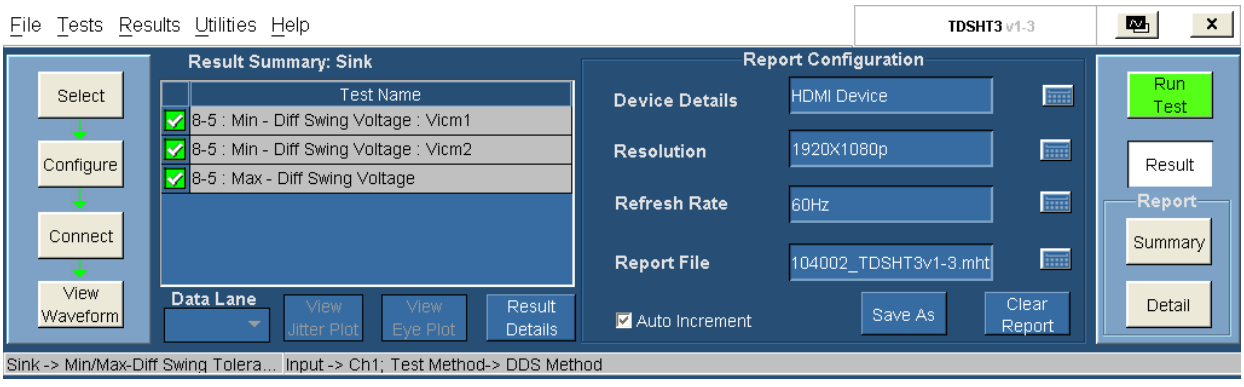
NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration. For more details,* *click here (see page 38)**.*

13. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test. Follow the instructions in the dialog box. Depending on your answer, a series of dialog boxes may prompt you for your input.

14. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



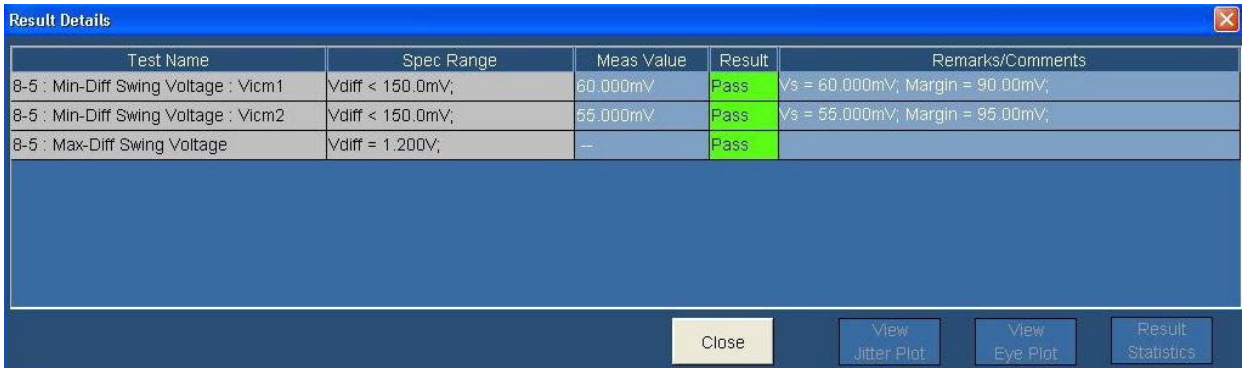
The result summary for the DDS test method is as follows:



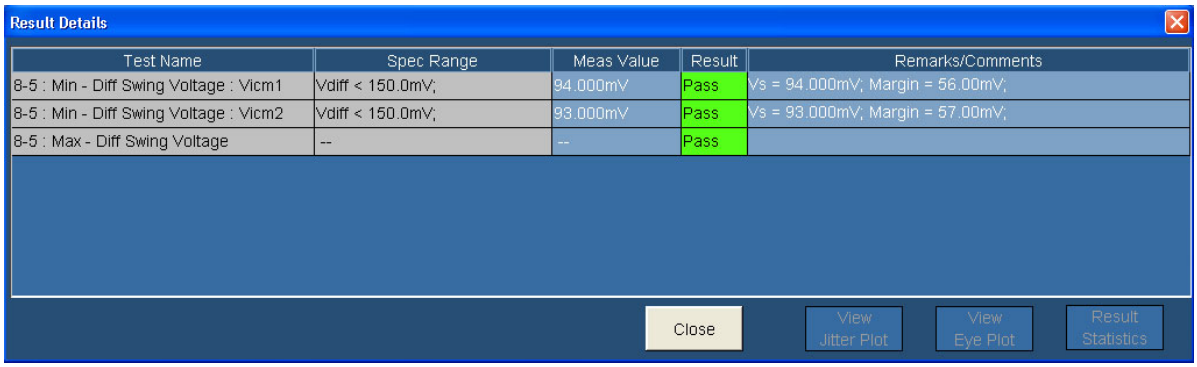
The results summary lists the test name and their status (pass, fail, or error). To view the details of the results, click **Results Details**.

15. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

16. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



The result details for the DDS test method are as follows:



- Test Name (displays the test id, test name, VIcm, and lane)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the measured value in mV)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the relevant details, such as Vswing and Margin). If the test could not be run, this field displays an error code (see page 397).

Test Method

This sequence explains the actions that the software takes while it performs a min/max-diff swing tolerance test. For the procedure on how to make this test, refer to the min/max-diff swing tolerance test procedure (see page 265).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Search for and record the minimum differential swing voltage that the Sink DUT supports without error at V_{ICM} = 2.9 V (Frequency > 165 MHz) and 3.0 V (Frequency < 165 MHz).
   - Set V_{ICM1} = 3.0/2.9 V.
   - Set V_{DIFF} = 170 mV on all TMDS differential pairs. (Note that "Amplitude and Offset" mode in the DTG "Level" window should be chosen. In this mode, set "Amplitude" to 0.085 Vpp to correspond to a 170 mV differential swing.)
   - If the test passes at 170 mV, reduce V_{DIFF} in 10 mV steps (corresponding to 0.01 Vpp steps in the "Amplitude" setting) on all pairs until the Sink DUT outputs errors or V_{DIFF} of 90 mV is reached.
   - If the test fails at 170 mV, increase V_{DIFF} in 10 mV steps on all pairs until the Sink DUT outputs pass or V_{DIFF} of 250 mV is reached.
   - Record V_{DIFF} {minimum} at first voltage level where no error appears.
3. Repeat the test for V_{ICM2} = 3.3 V.
4. Set V_{DIFF} = 1.2 V on all TMDS differential pairs. (Note that "Amplitude and Offset" mode in the DTG "Level" window should be chosen. In this mode, "Amplitude" should be set to 0.6 Vpp to correspond to a 1.2 V differential swing.)
5. Verify that the DUT continues to support the signal without errors.
6. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

1. Operate the Sink DUT to support the HDMI input signal.
2. For the procedure on how to make this test, refer to the min/max-diff swing tolerance test procedure (see page 265).
3. Refer to the make connections for sink min-max differential swing test (see page 115) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate patterns with differential voltage of 170 mV. The software prompts you to confirm the gray bars on the DUT.
6. If the gray bar does not appear, the differential voltage is increased to 250 mV in steps of 10 mV. You are prompted to confirm for the gray bars on the DUT for each step.

7. If the gray bar appears, the differential voltage is decreased to 90 mV in steps of 10 mV as per the CTS. You are prompted to confirm for the gray bars on the DUT for each step.
8. You are promoted to connect the Clock channel to the oscilloscope to measure the voltage.
9. Once the test completes, the appropriate test results are generated.

NOTE. *Using a manual DDS test method is not recommended because the software performs the Min/Max-Diff Swing Tolerance test automatically and effectively.*

Test the Jitter Tolerance

This test allows you to confirm that the maximum allowed TMDS clock jitter is supported by the Sink DUT.

The signal degradation of typical passive copper cables increases with the frequency and the length of the cable. To recover data from such cables, the TDSHT3 software applies the reference cable equalizer (as specified in the HDMI specifications 1.4a) automatically to the jitter tolerance measurement when the clock frequency is more than 165 MHz.

To use the DTG test method, you will need a supported oscilloscope (which also acts as a GPIB Controller), two differential probes, one digital timing generator (DTG), one arbitrary waveform generator (AWG), one DC power supply, 12 SMA cables, two bias-tees, cable emulators, one TPA-R-DI, one TPA-R-TDR, and TTC modules.

To use the DDS test method, you will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, and two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter). For Type-E cable emulator, use the Type-E fixtures (one TF-HDMIE-TPA-P and one TF-HDMIE-TPA-R) in place of Type-A and Type-C fixtures.

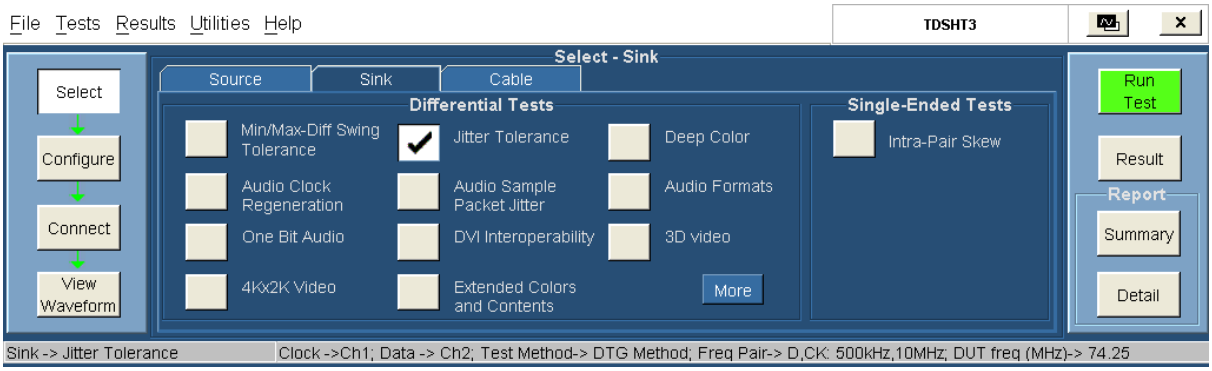
Jitter Calibration Steps.

To calibrate the jitter values of the Direct Synthesis signal, do the following:

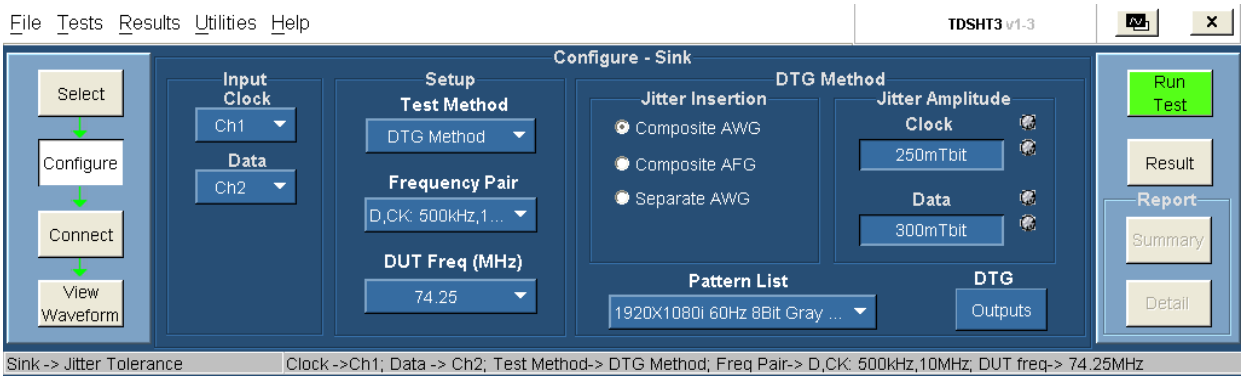
- Connect a TPA-R fixture to the TPA-P fixture.
- Connect the Clock and Data0 output of the TPA-R fixture to the oscilloscope using two P7313SMA probes.
- The software measures the jitter values using two P7313SMA probes. If the measured values are not within ±2.5% of the range specified in the CTS, the software regenerates the patterns.

  This sequence is repeated until the measured values are within the specified range in the CTS.

1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the Jitter Tolerance check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



4. In the Input pane, do the following:

- Set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
- Set the Input Data to the channel that you will use for the HDMI data input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

NOTE. *For the DTG method, this connection is required only if you perform jitter calibration by selecting* ***Jitter Tolerance (No calibration)*** *in the Preferences (see page 24) menu.*

5. In the Setup pane, do the following:
   - In the Test Method pane, select the appropriate test method from the available choices (DTG Method and DDS Method).
   - In the Frequency Pair list, click the desired value for the jitter tolerance tests. Select from the available choices (D, Ck: 500 KHz, 10 MHz and D, Ck: 1 MHz, 7 MHz, and Both). If you select Both, the test is run for both the frequency pairs.
   - In the DUT Freq (MHz) list, select the frequency to be tested for the DUT. The available choices depend upon the selected test method.

     For the DTG method, the available choices are 27.175, 27, 74.25, 148.5, 222.75, and 297.

     For the DDS method, the available choices are 27, 74.25, 148.5, 222.75, 27 Type-E, and 74.25 Type-E.
6. If the selected test method is DTG, do the following:
   - In the Jitter Insertion pane:
     - Select AWG to insert composite jitter using an AWG.

       NOTE. *In the composite jitter, both clock and data jitter frequency components are added to the clock signal.*

     - Select AFG to insert composite jitter using an AFG.

       NOTE. *In the composite jitter, both clock and data jitter frequency components are added to the clock signal.*

     - Select AWG to insert separate jitter.

       NOTE. *In separate jitter insertion, clock jitter is added to the clock signal and data jitter is added to the data signal.*

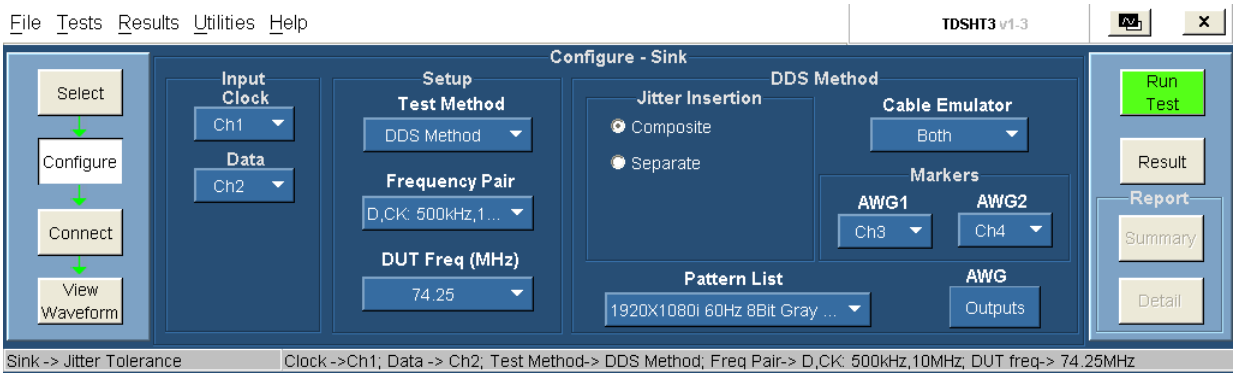
   - In the Jitter Amplitude pane:
     - Set the amplitude of the clock jitter. By default, the value is set to the value specified in the HDMI standards (CTS 1.4a).

       The minimum and maximum value of clock are 150 mTbit and 500 mTbit respectively.
     - Set the amplitude of the data jitter. By default, the value is set to the value specified in the HDMI standards. Set the amplitude of the data jitter. By default the value is set to the value specified in the HDMI standards.

The minimum and maximum value of data are 150 mTbit and 500 mTbit respectively.

- Select the DTG pattern file from the drop-down list for the selected DUT frequency.
- In the DTG field, click **Outputs** to display a dialog box where you can set unique Clock, Data0, Data1, and Data2 outputs.

If the selected test method is DDS, do the following:



- In the Jitter Insertion pane, select the composite jitter insertion technique to add jitter. In the composite jitter insertion technique, clock jitter and data jitter are added to the clock signal.

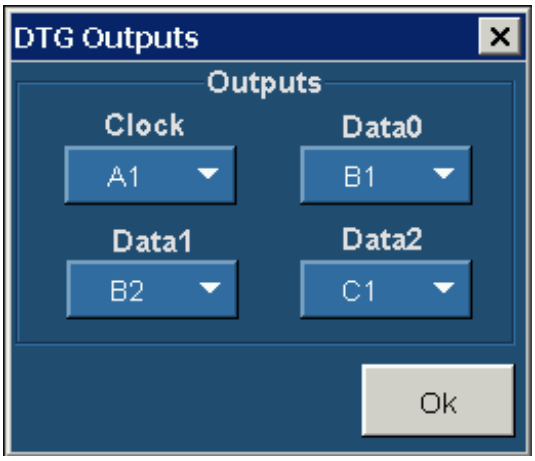
NOTE. *The Separate Jitter Insertion technique is not supported for the DDS method.*

- Select the cable emulator type to use. The available choices are: 1st Cable Emulator, 2nd Cable Emulator, and Both. The default is Both.

  If you have selected 27 Type-E or 74.25 Type-E in the DUT Freq (MHz) list, only one cable emulator type (Type-E Cable Emulator) is available.

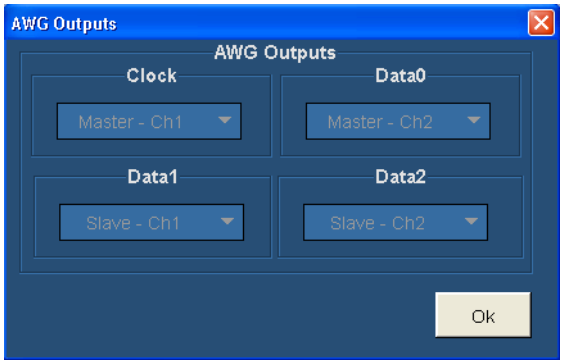
- In the Markers pane:
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
- Select the DDS pattern file from the drop-down list for the selected DUT frequency.
- In the AWG field, click **Outputs** to display a dialog box.

7. The DTG Outputs dialog box for the DTG method has the following options:



- Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
- Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

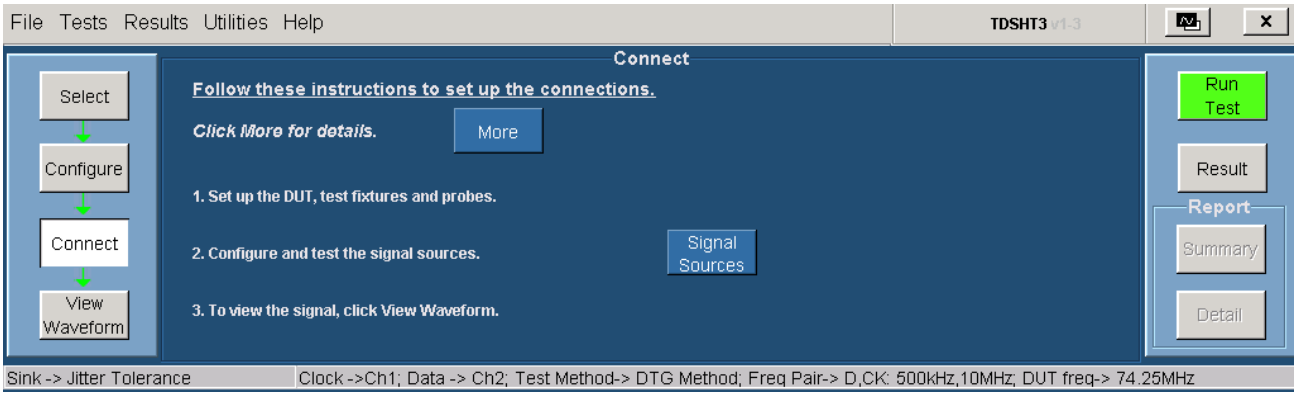
  The AWG Outputs dialog box for the DDS method has following configurations:



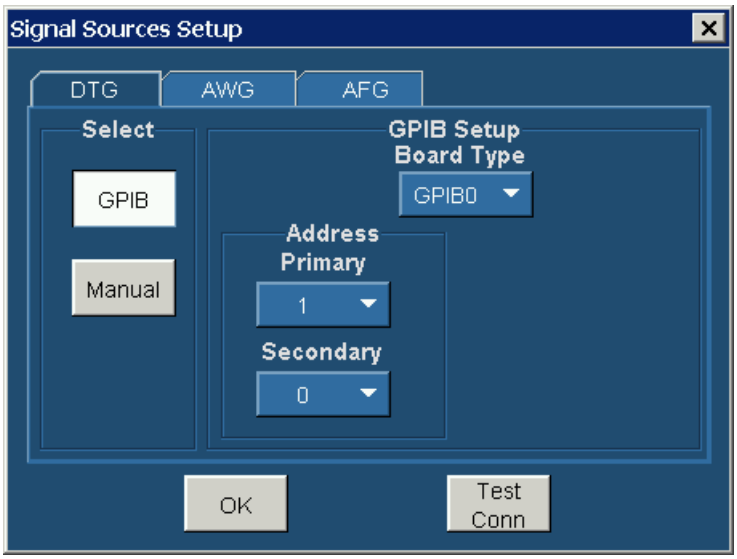
NOTE. *You cannot configure the AWG Outputs dialog box.*

NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

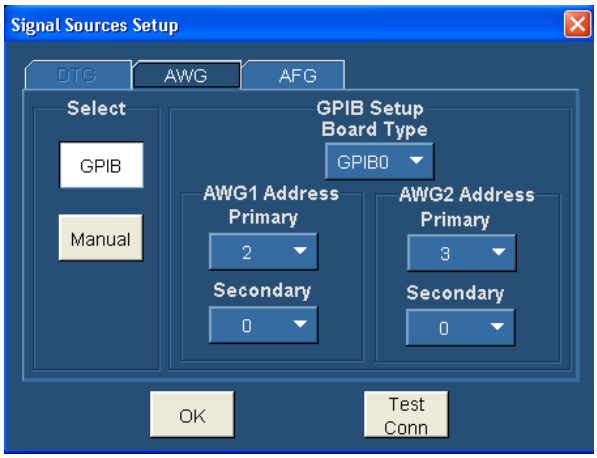
8. To connect the DUT, click **Tests > Connect**. Click here (see page 119) for information on how to make connections.



9. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears. The Signal Sources parameters are populated based on the selected test method: DTG or DDS.



If you have selected the DDS test method, the AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



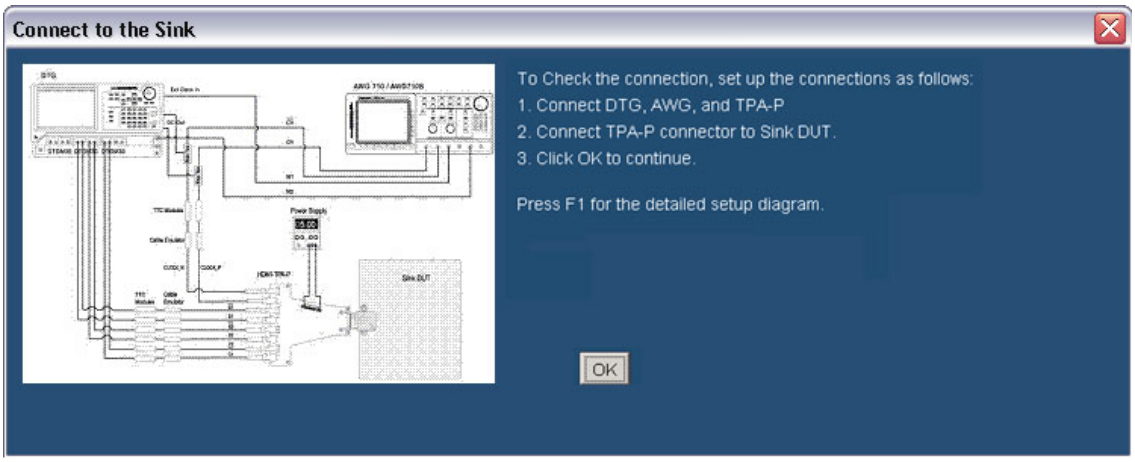
NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

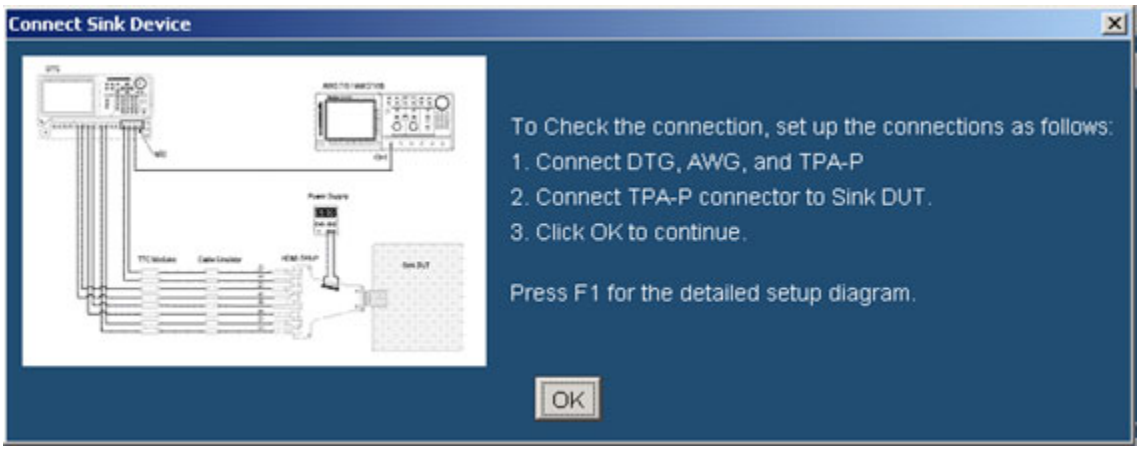
10. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.
11. To test the connection and the GPIB configuration, click **Test Conn**.
12. Because no signal is connected to the oscilloscope, you cannot view the waveform for the jitter tolerance test.

NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

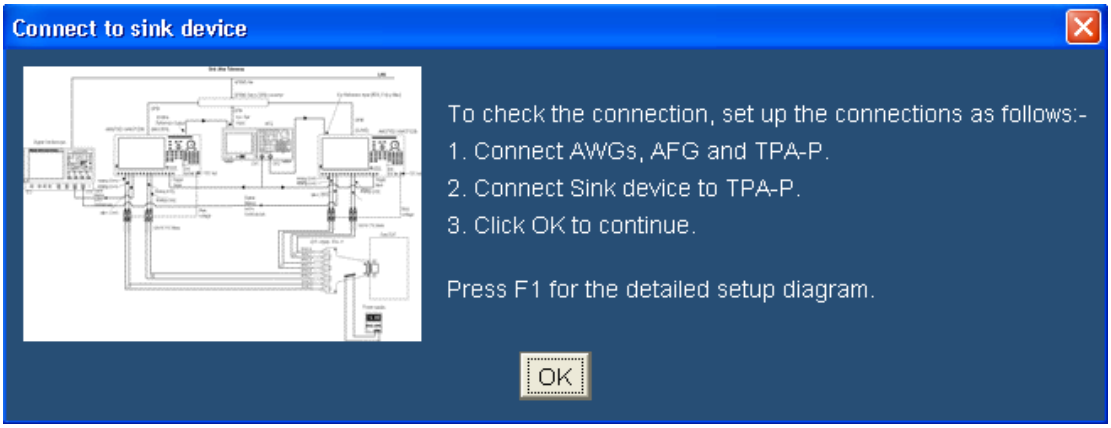
13. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.
14. Follow the instructions in the Sink Jitter Tolerance dialog box. Click **OK**. The Connect Sink Device dialog box for low frequency appears as follows.



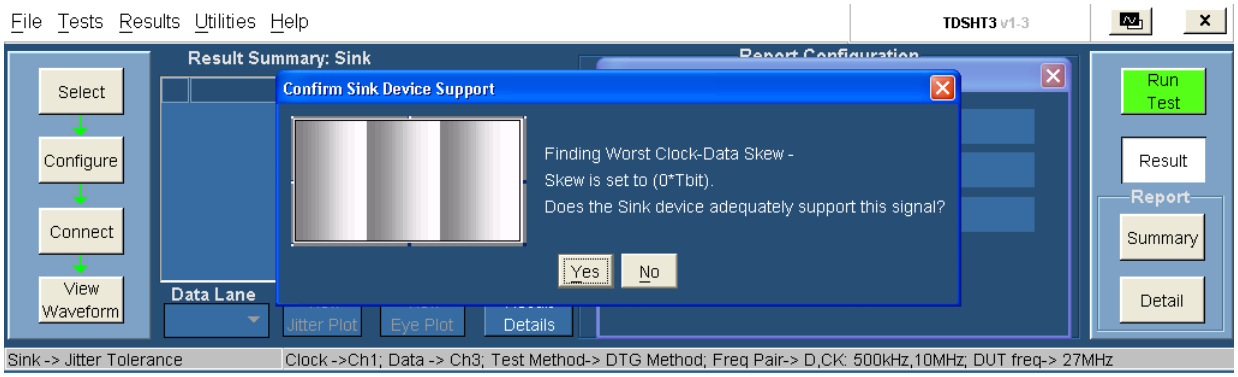
The Connect Sink Device dialog box for high frequency appears as follows.



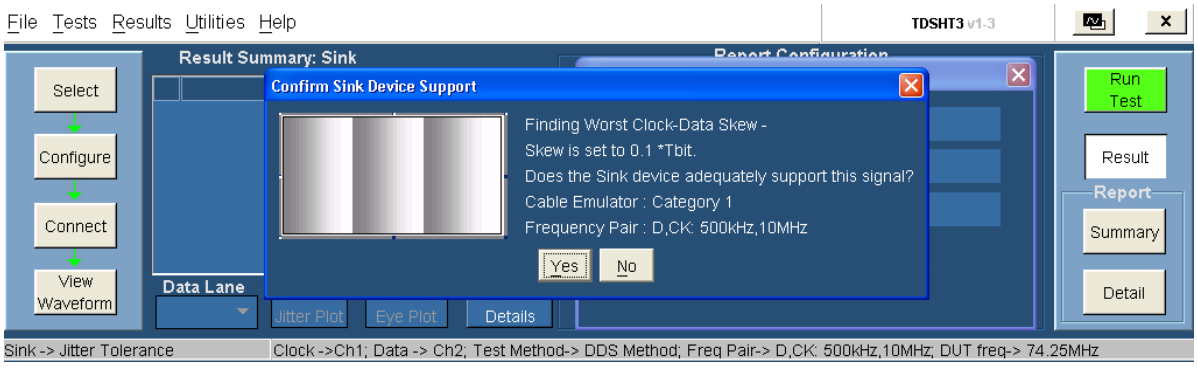
If you select the DDS test method, the Connect Sink Device dialog box appears as follows:



15. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.

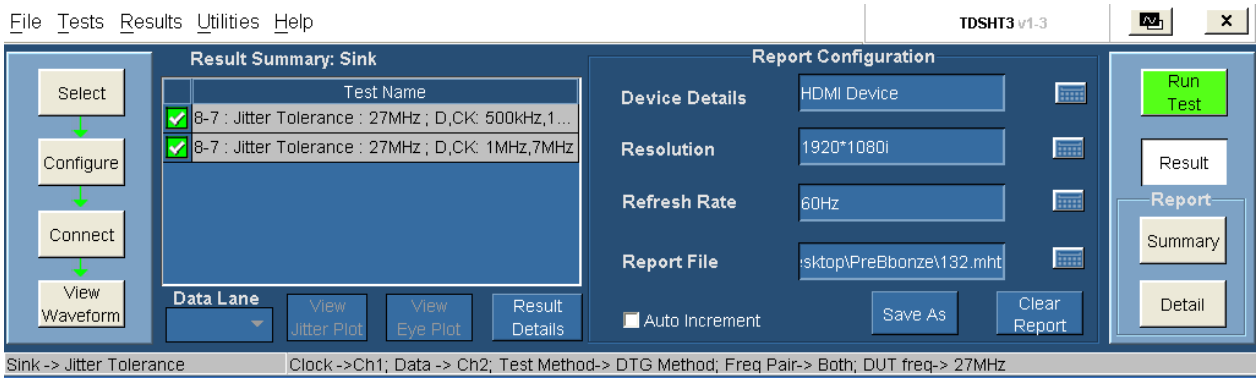


If you select the DDS test method, the Confirm Sink Device Support dialog box appears as follows:

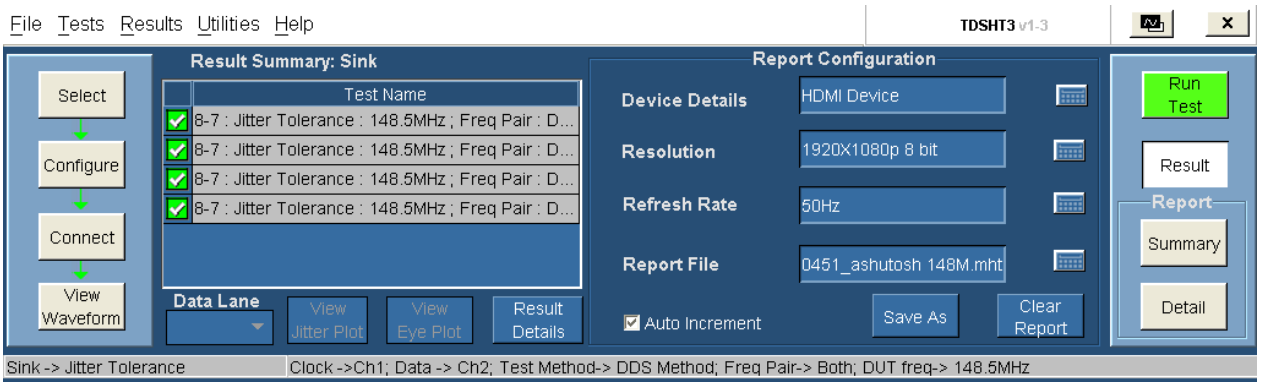


16. Follow the instructions in the dialog box. Depending on your answer, a series of dialog boxes may prompt you for your input.

17. If you successfully run the test, the software calculates the jitter values and displays the results. The software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The result summary for the DDS test method is as follows:

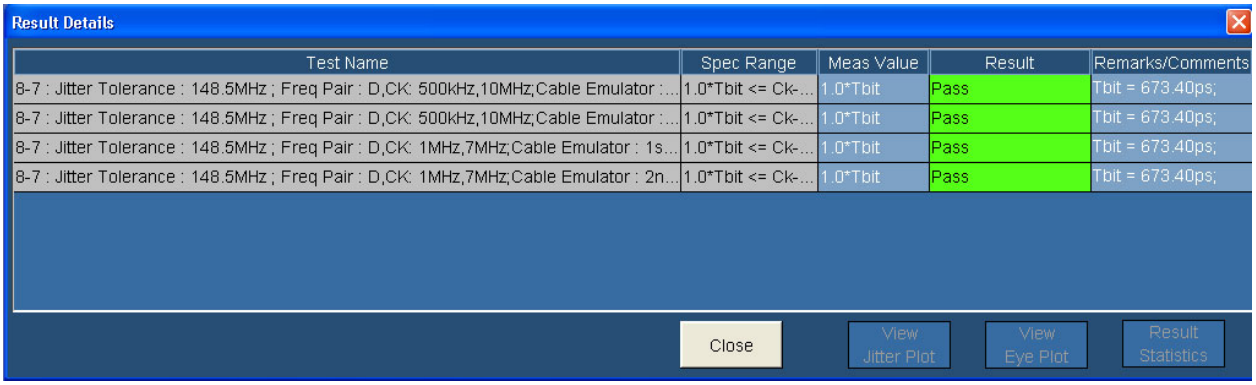


The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

18. Set the report details to identify and generate the report automatically. Click here (see page 49) for more information.

19. In the result summary pane, click **Result Details**. The result details pane displays the following fields.

The result details for the DDS test method are as follows:



- Test Name (displays the test id, test name, and selected lanes)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the measured value in mV)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the relevant details, such as Vswing and Margin. If the test could not be run, this field displays an error code (see page 397).

Test Method

This sequence explains the actions that the software takes while it performs a jitter tolerance test. For the procedure on how to make this test, refer jitter tolerance test procedure (see page 273).

For the DTG Method

1. Operate the Sink DUT to support the HDMI input signal.
2. Configure the DTG as follows:
   - Load the appropriate no-jitter pattern in the DTG
   - Set the signal outputs to 3.0 V average
3. Configure the AWG as follows:
   - In the “Vertical” menu, set the following:
     - Filter-through
     - Amplitude
     - Offset = 0 V
     - Marker 1 = 0.00 V to 1.00 V
     - Marker 2 = 0.00 V to 2.00 V
   - No jitter on output initially, with ability to add two simultaneous jitter components.
4. Connect the test fixture to the oscilloscope for jitter calibration. The oscilloscope calculates data and clock jitter inserted due to the cables and the test fixtures along with the known amount of jitter.
5. Use the appropriate TTC module based on the recommended resolution.

6. Measure jitter tolerance while verifying adequate support by sink.
   - For each of the two test cases:
     - D_JITTER = 500 kHz, C_JITTER = 10 MHz
     - D_JITTER = 1 MHz, C_JITTER = 7 MHz
7. Increase the skew (Differential timing offset) in steps of 0.1 Tbit from 0.0 Tbit to 1.0 Tbit. The test fails if the sink outputs errors at any time.

For the DDS Method

The DDS method does not require a DTG. The setup includes two AWGs to create synthesized patterns for HDMI Sink Jitter Tolerance testing. It does not need different TTC filters for each resolution and cable emulators because their effects are emulated by the software.

1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer jitter tolerance test procedure (see page 273).
3. Refer to the sink jitter tolerance test connection (see page 129) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate patterns with no-jitter waveforms. The software prompts you to confirm the gray bars on the DUT. Once this is confirmed, the software loads the TP1 waveforms with jitter insertion as per the CTS.

   If you have not selected **Jitter Tolerance (No calibration)** in the Preferences (see page 24) menu, the software will measure the jitter values. If the measured values are not within ±2.5% of the value specified in the CTS, the software will regenerate the patterns to match the specified jitter values.
6. Confirm the gray bars on the DUT for TP1. Upon confirmation, the software loads the TP2 waveforms with appropriate cable emulator and jitter insertion as per the CTS.

   If you have not selected **Jitter Tolerance (No calibration)** in the Preferences (see page 24) menu, the software will measure the jitter values. If the measured values are not within ±2.5% of the value specified in the CTS, the software will regenerate the patterns to match the specified jitter values.
7. Confirm the gray bars on the DUT for TP2. Upon confirmation, the software loads the skew patterns in steps of 0.1 Tbit from 0.0 Tbit to 1.0 Tbit. The test fails if the sink outputs errors at any time.

NOTE. *Using a manual DDS test method is not recommended because the software performs the Sink Jitter Tolerance test automatically and effectively.*

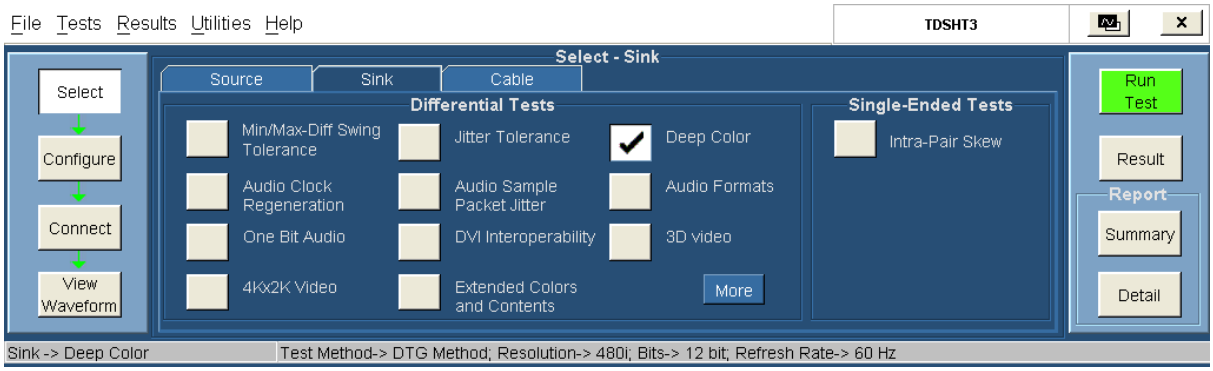
Test the Deep Color

This test allows you to confirm that a particular resolution and color depth (bits) is supported by the Sink DUT.

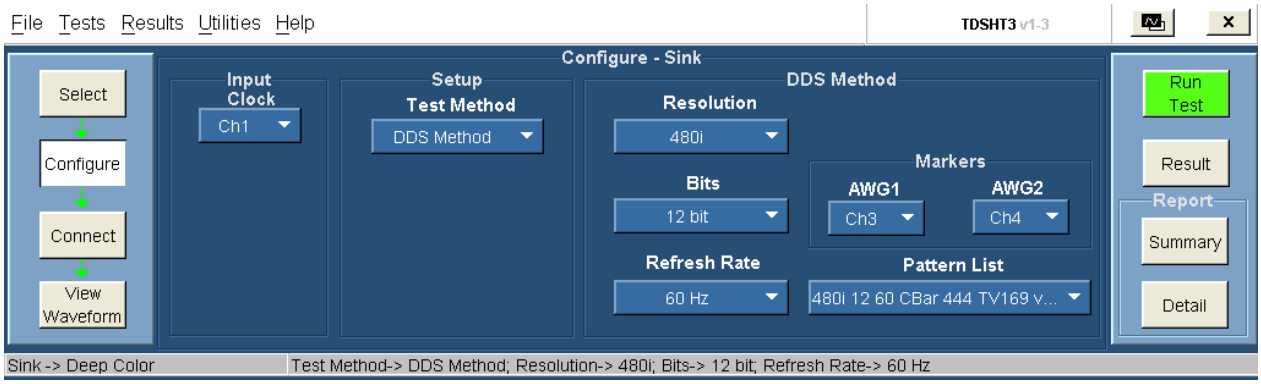
To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

To use the DDS test method, you will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the Deep Color check box.

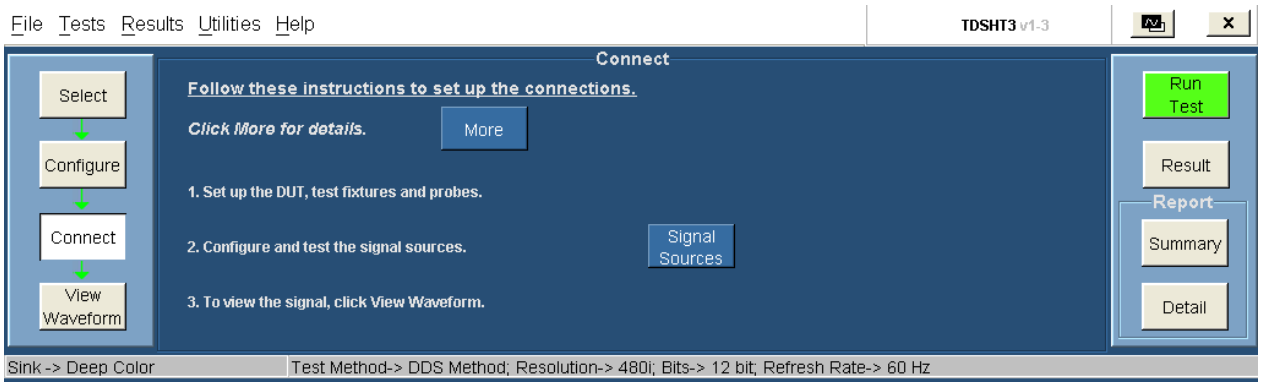


3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



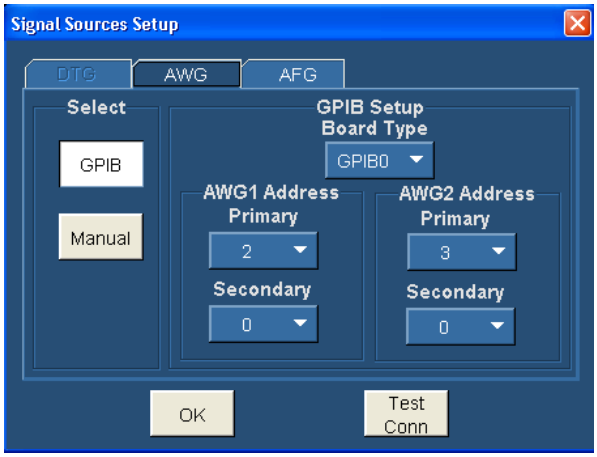
4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).
6. In the DTG Method pane, do the following:
   - Select the resolution of the pattern to be loaded on the AWG. Select from the available choices (480i, 480p, 480px640, 576i, 576p, 720p, 1080i, 1080p, and VGA). The default value is 480i.
   - Select the color depth (Bits) of the deep color pattern. Select from the available choices (10 Bit, 12 Bit, and 16 Bit).
   - Select the refresh rate of the patterns. Select from the available choices (50 Hz and 60 Hz). The default value is 60 Hz.
   - Select the pattern(s) from the available list for the selected resolution, refresh rate, and the bits.

   In the DDS Method pane, do the following:
   - Select the resolution of the pattern to be loaded on the AWG. Select from the available choices (480i, 480p, 480px640, 576i, 576p, 720p, 1080i, 1080p, and VGA). The default value is 480i.
   - Select the color depth (Bits) of the deep color pattern. Select from the available choices (10 Bit, 12 Bit, and 16 Bit).
   - Select the refresh rate of the patterns. Select from the available choices (50 Hz and 60 Hz). The default value is 60 Hz.
   - In the Markers pane:
     - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
     - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
   - Select the pattern(s) from the available list for the selected resolution, refresh rate, and the bits.
7. To connect the DUT, click **Tests > Connect**. Click here (see page 165) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

   The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

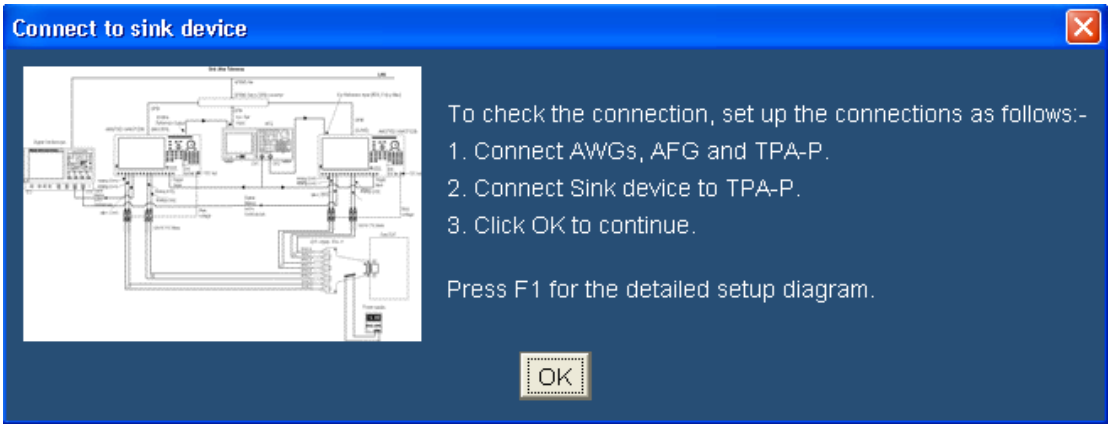
NOTE. *The Manual test option is not available for the DDS method.*

9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.
10. To test the connection and the GPIB configuration, click **Test Conn**.
11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the jitter tolerance test.

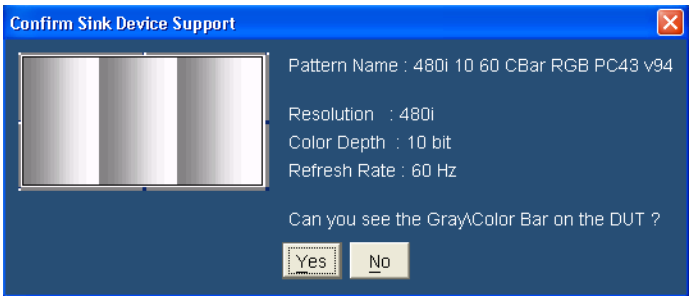
NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.

13. Follow the instructions in the Sink Deep Color dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:

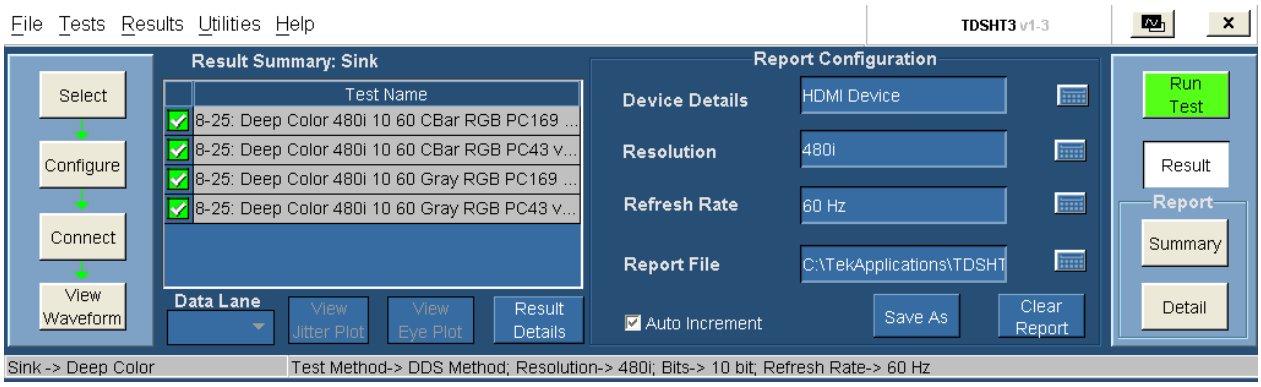


14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.



15. Follow the instructions in the dialog box.

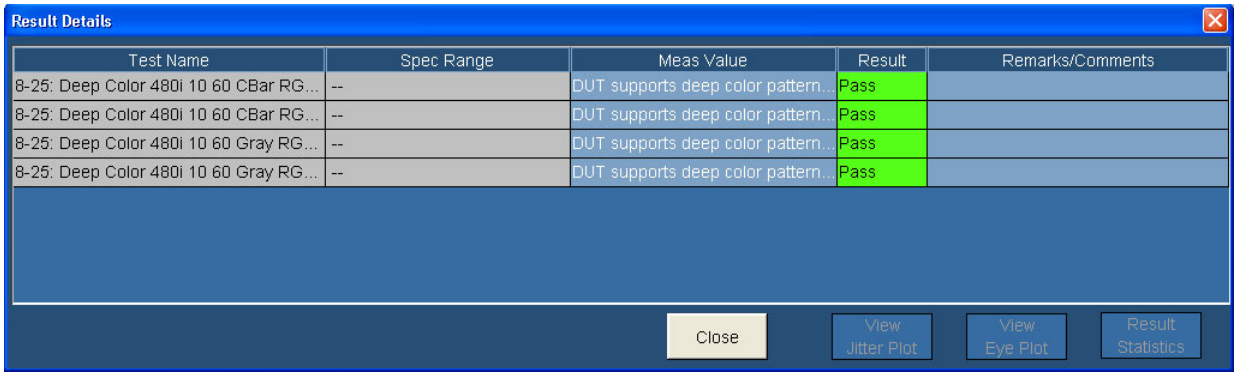
16. If you successfully run the test, the software loads the deep color pattern(s). The software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected lanes)
- Meas Value (displays the deep color pattern supported by the DUT)
- Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs a deep color test. For the procedure on how to make this test, refer deep color test procedure (see page 285).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs to create synthesized patterns for HDMI Sink Deep Color testing.

1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer deep color test procedure (see page 285).
3. Refer to the make connections for deep color (see page 165) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

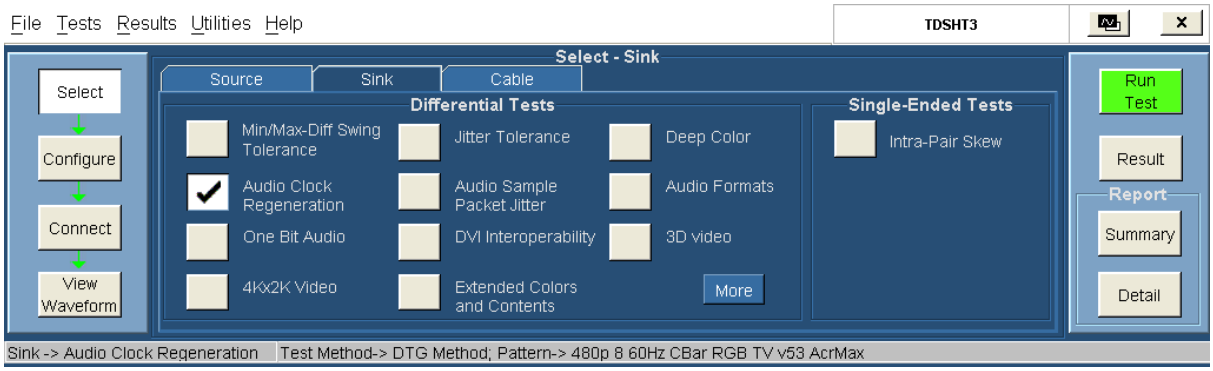
NOTE. *Using a manual DDS test method is not recommended because the software performs the Sink Deep Color test automatically and effectively.*

Test the Audio Clock Regeneration

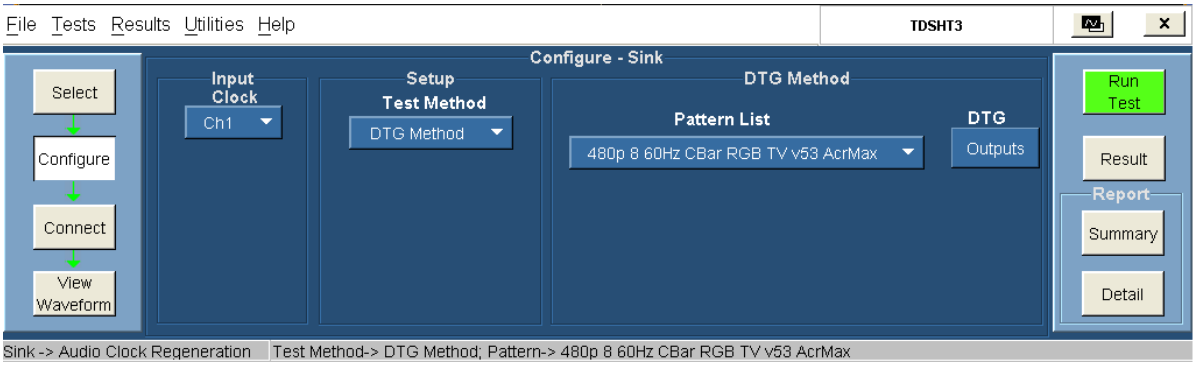
To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

To use the DDS test method, you will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

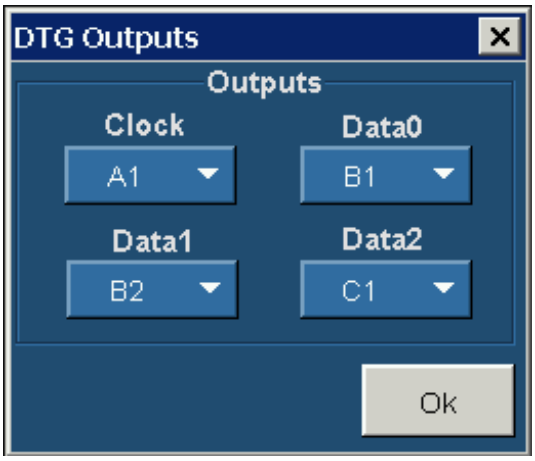
1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the Audio Clock Regeneration check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.
4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).
6. In the DTG Method pane, select the pattern(s) from the available list.



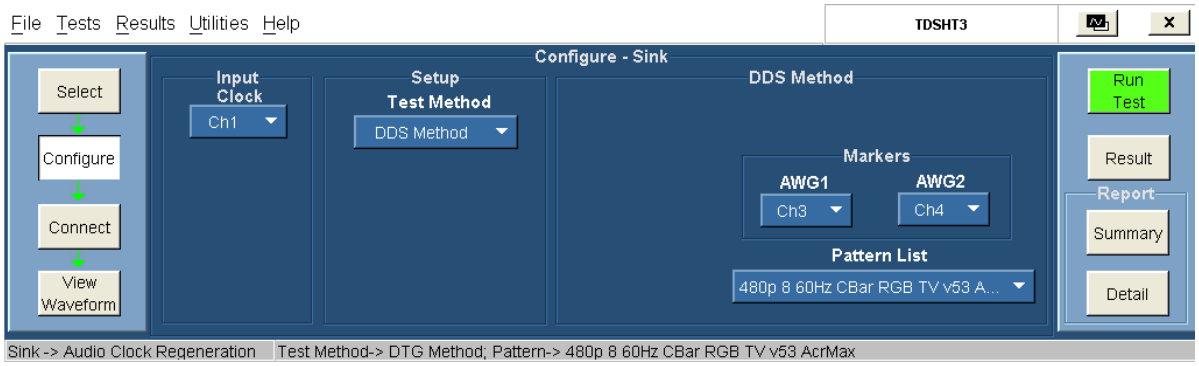
The DTG Outputs dialog box for the DTG method has the following options:



- Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
- Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

In the DDS Method pane, do the following:

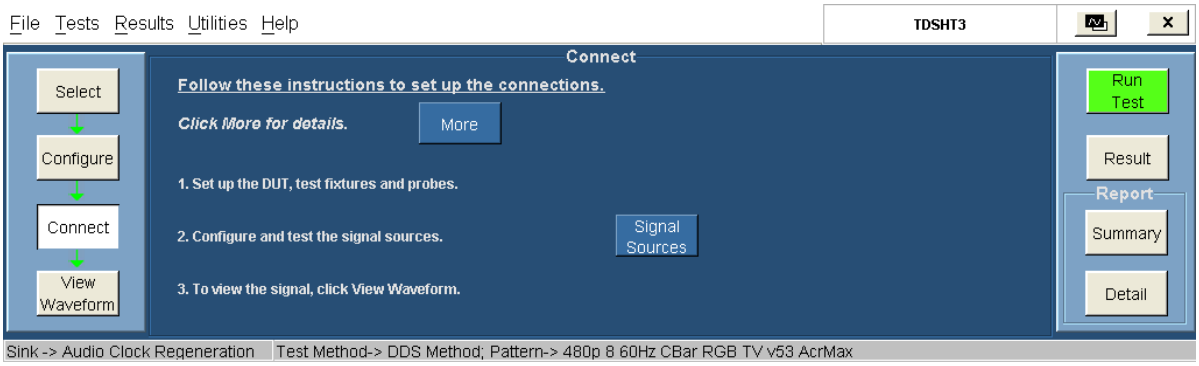


- Select the pattern(s) from the available list.

  In the Markers pane:

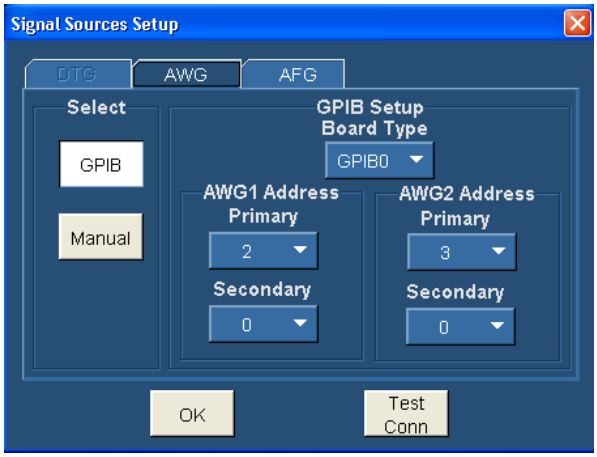
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.

7. To connect the DUT, click **Tests > Connect**. Click here (see page 138) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

   The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

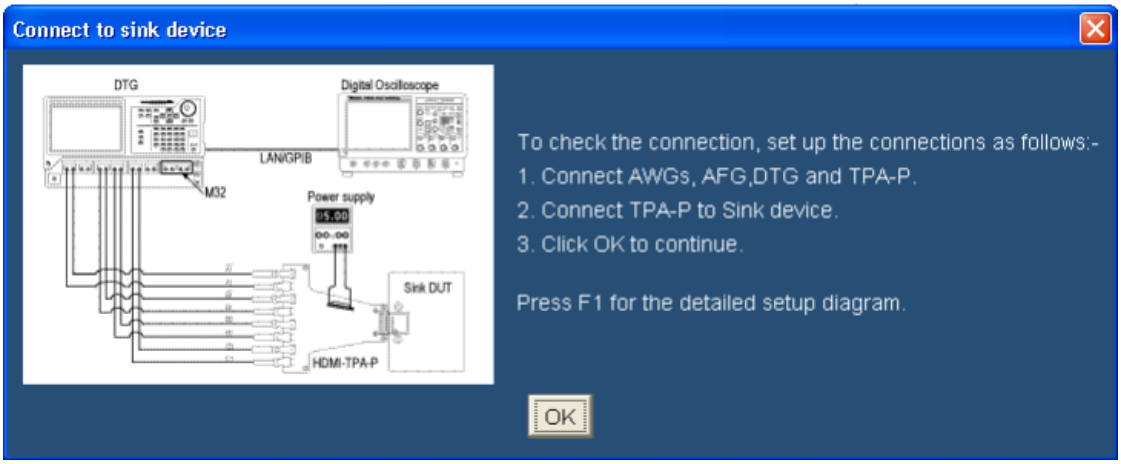
NOTE. *The Manual test option is not available for the DDS method.*

9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.
10. To test the connection and the GPIB configuration, click **Test Conn**.
11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the audio clock regeneration test.

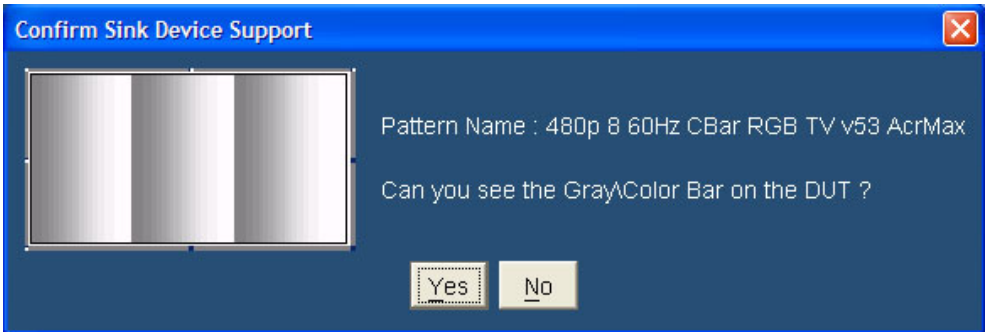
NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.

13. Follow the instructions in the Sink dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:

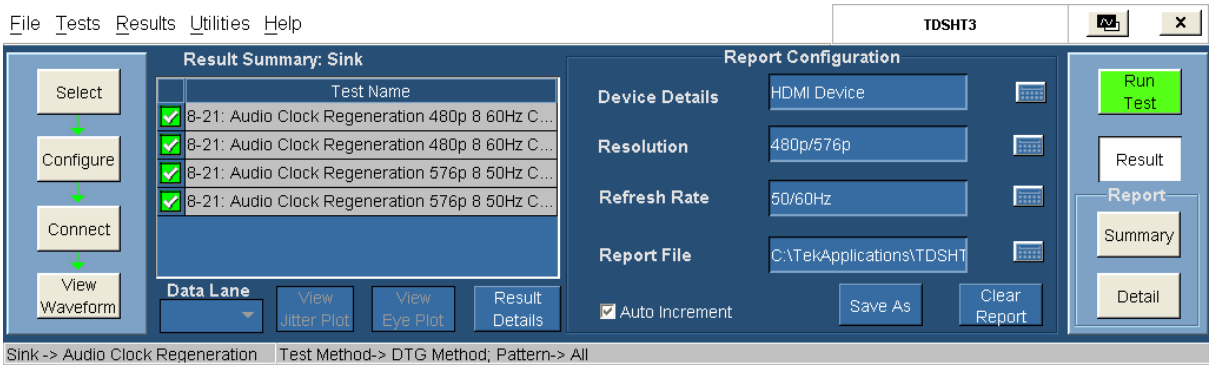


14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.



15. Follow the instructions in the dialog box.

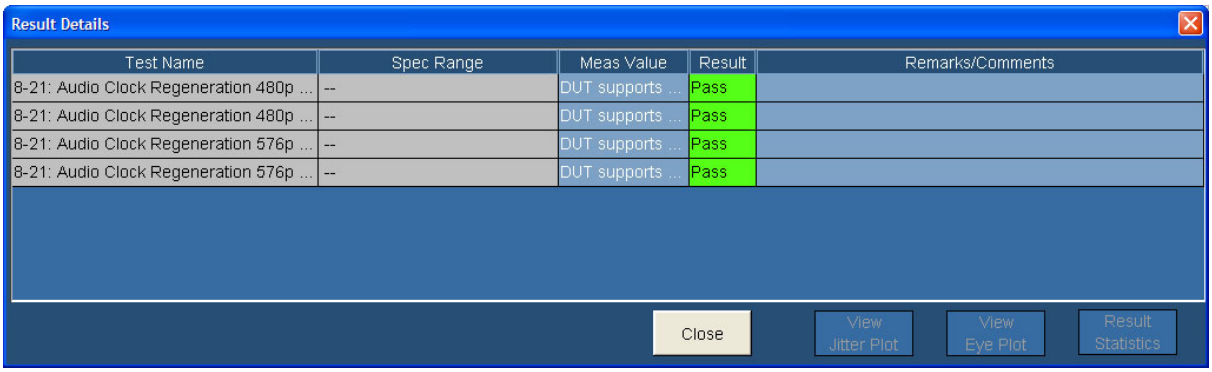
16. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected pattern)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the pattern supported by the DUT)
- Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs an audio clock regeneration test. For the procedure on how to make this test, refer to the audio clock regeneration test procedure (see page 290).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs.

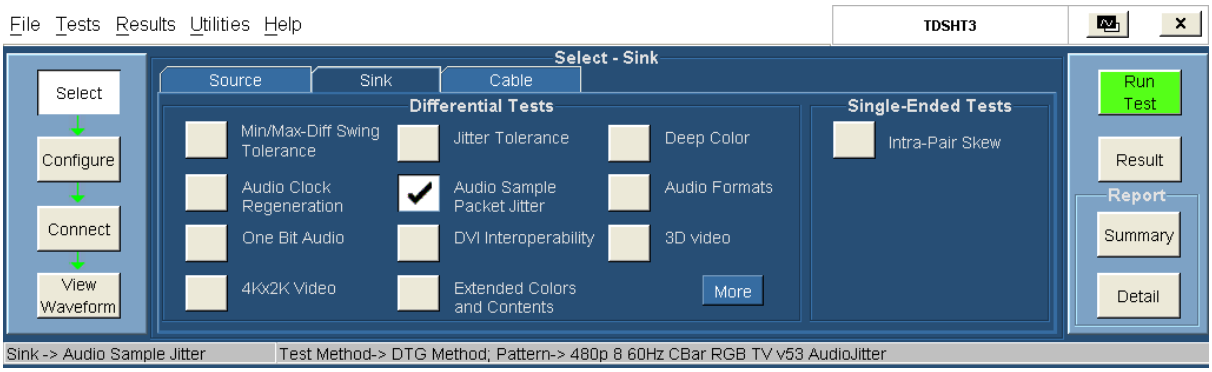
1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer audio clock regeneration test procedure (see page 290).
3. Refer to make connections for audio clock regeneration (see page 138) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

Test the Audio Sample Packet Jitter

To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

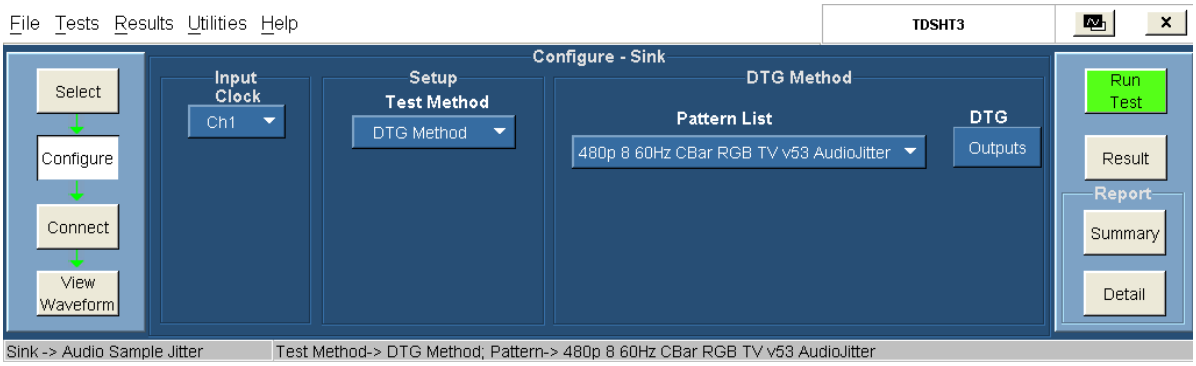
To use the DDS test method, you will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the Audio Sample Packet Jitter check box.

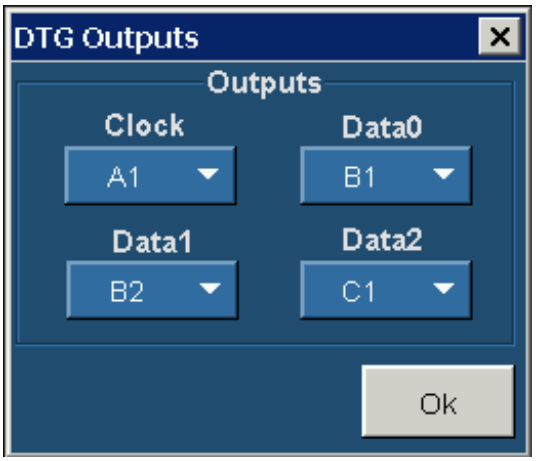


3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.

4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).
6. In the DTG Method pane, select the pattern(s) from the available list.



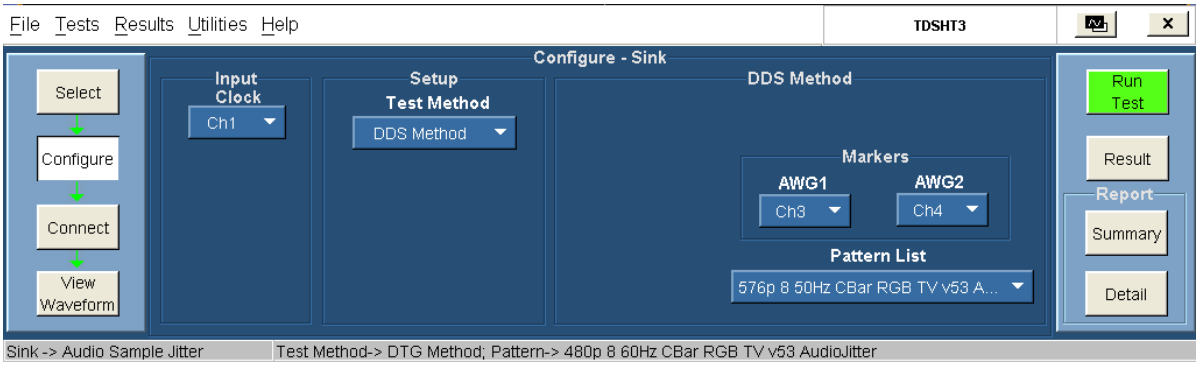
The DTG Outputs dialog box for the DTG method has the following options:



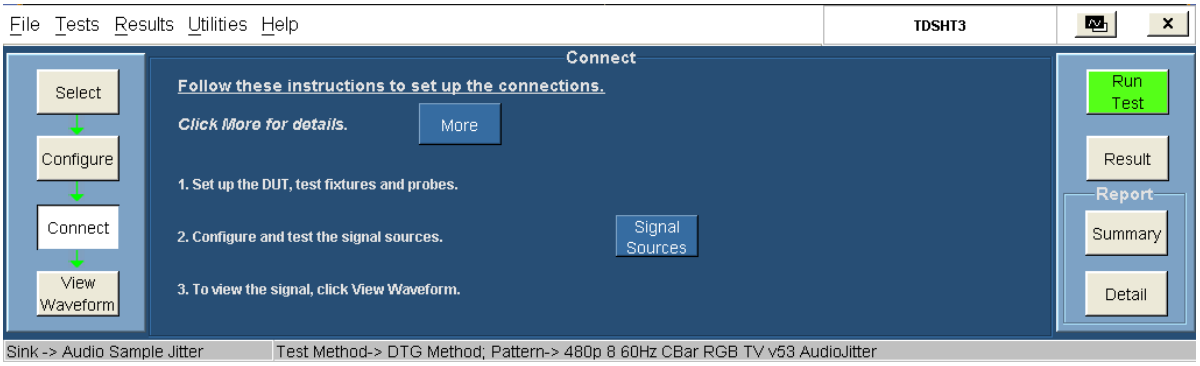
- Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
- Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

In the DDS Method pane, select the pattern(s) from the available list.

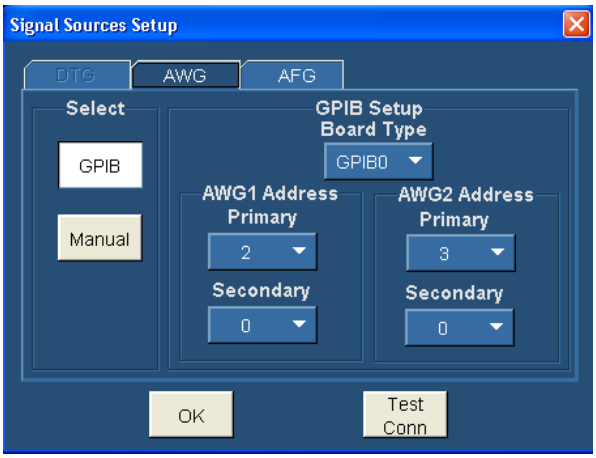


7. To connect the DUT, click **Tests > Connect**. Click here (see page 141) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



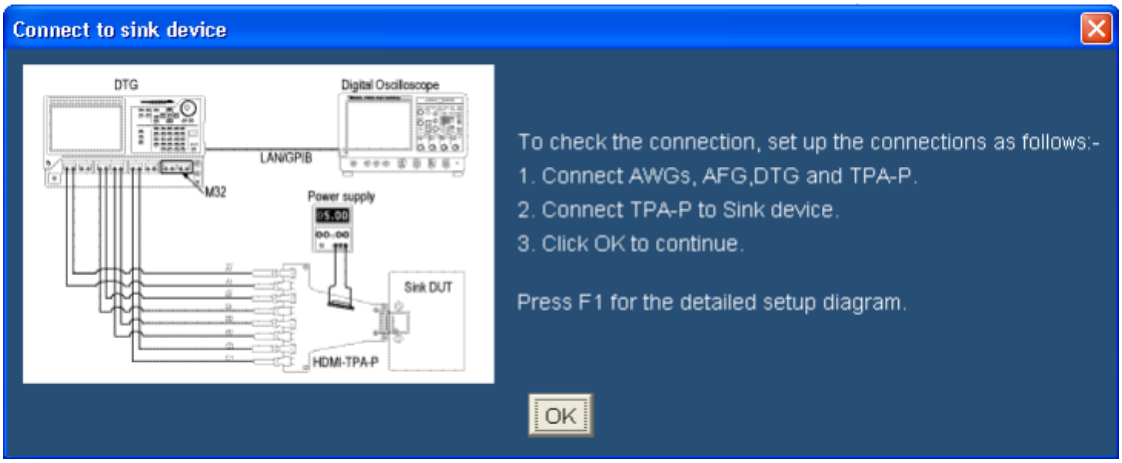
NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

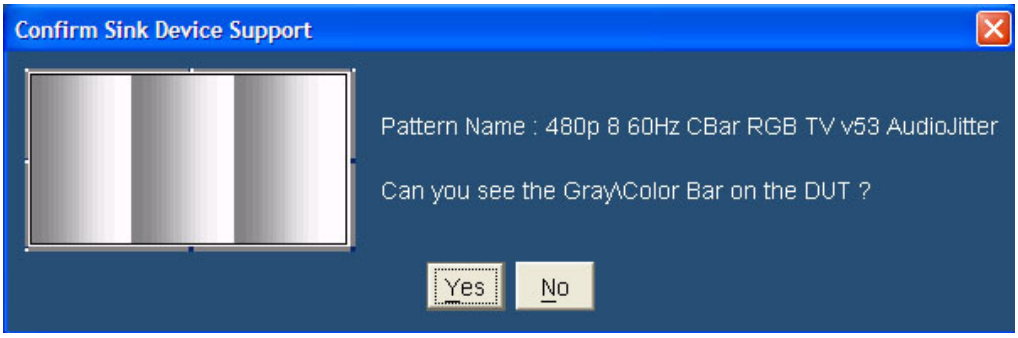
9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.
10. To test the connection and the GPIB configuration, click **Test Conn**.
11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the audio sample packet jitter test.

NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.
13. Follow the instructions in the Sink dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:

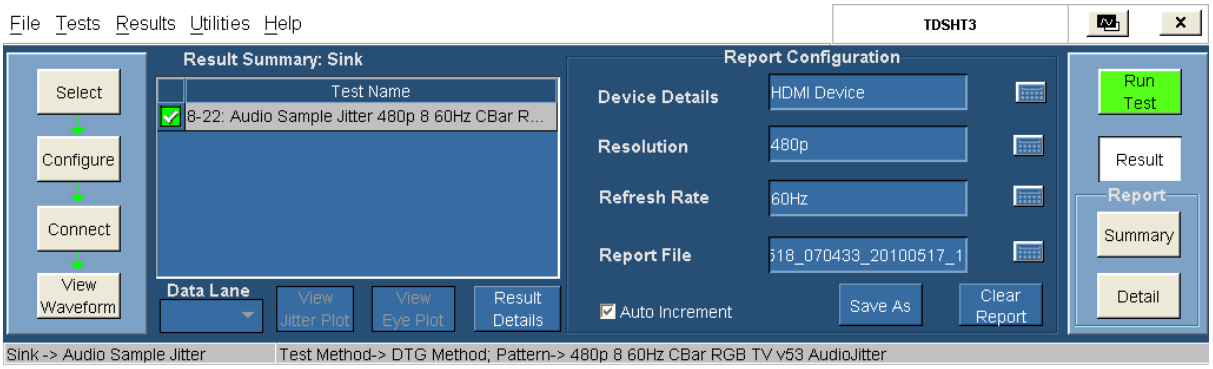


14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.



15. Follow the instructions in the dialog box.

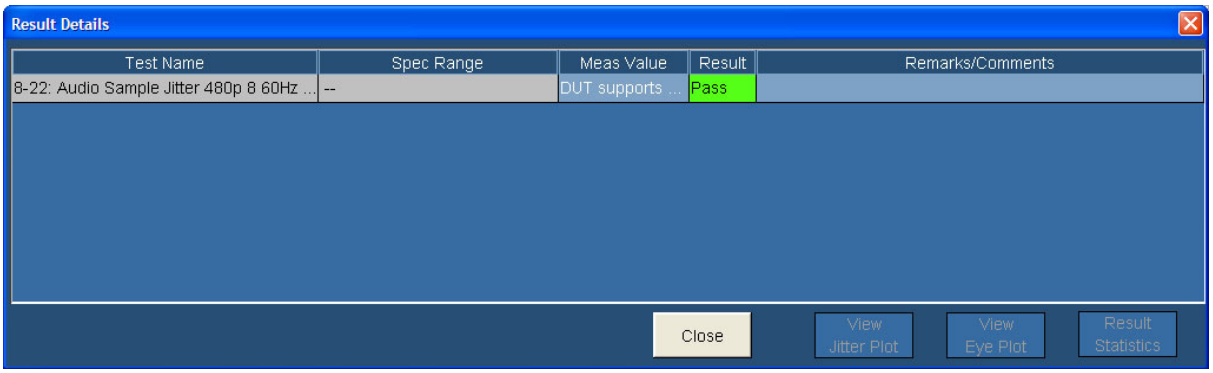
16. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected lanes)
- Meas Value (displays the deep color pattern supported by the DUT)
- Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs a deep color test. For the procedure on how to make this test, refer audio sample packet jitter test procedure (see page 296).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs.

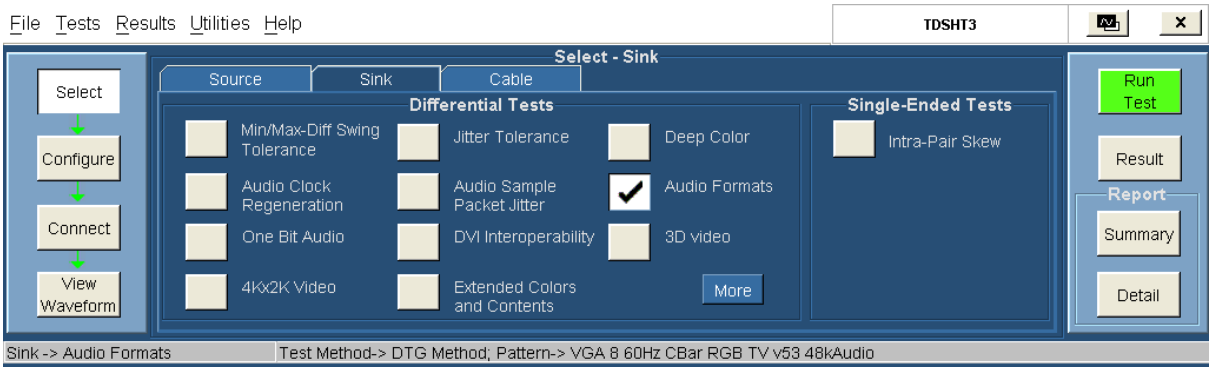
1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer audio sample packet jitter test procedure (see page 296).
3. Refer to make connections for audio sample packet jitter (see page 141) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

Test the Audio Formats

To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

To use the DDS test method, you will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the Audio Formats check box.

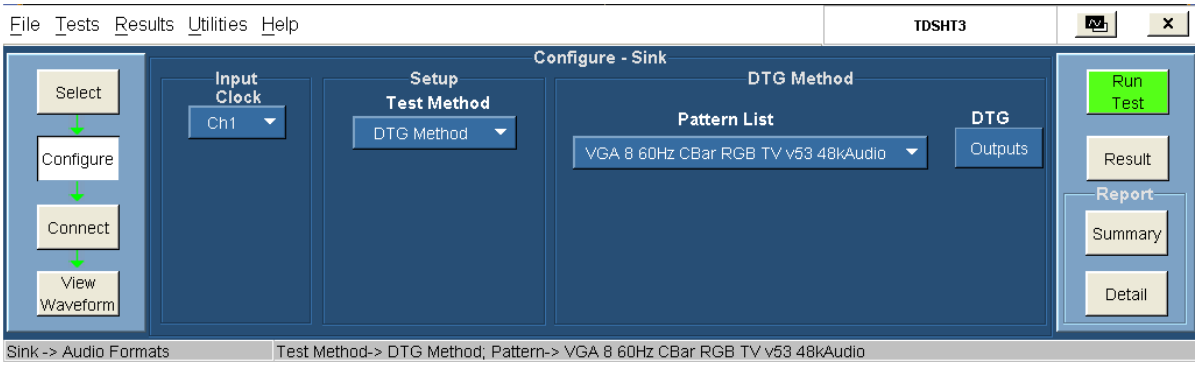


3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.

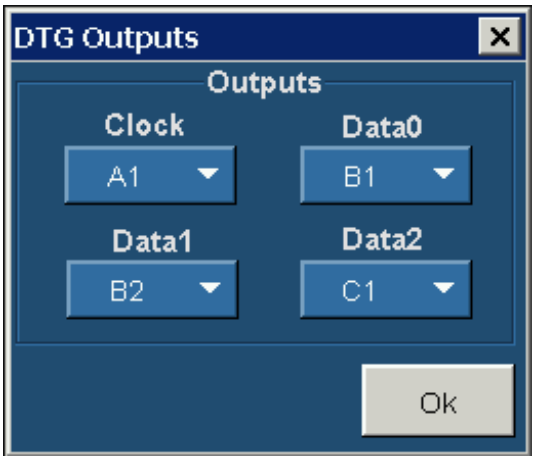
4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).

6. In the DTG Method pane, select the pattern(s) from the available list.



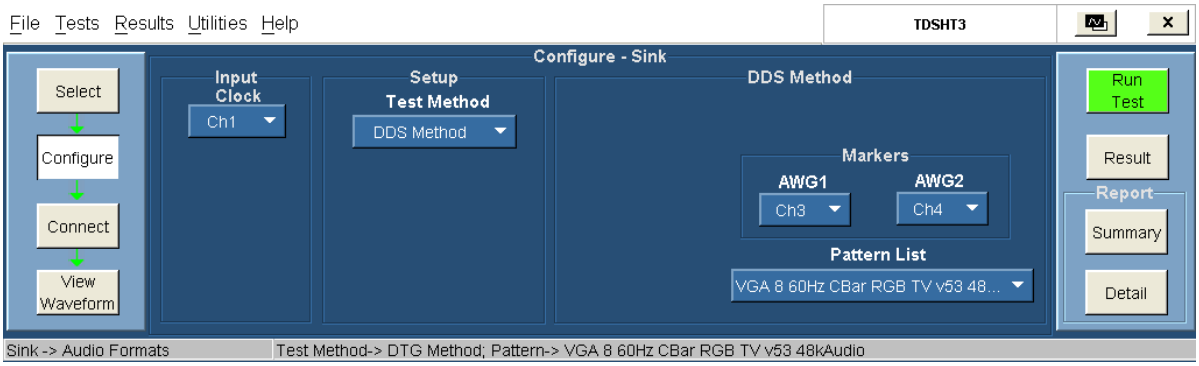
The DTG Outputs dialog box for the DTG method has the following options:



- Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
- Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

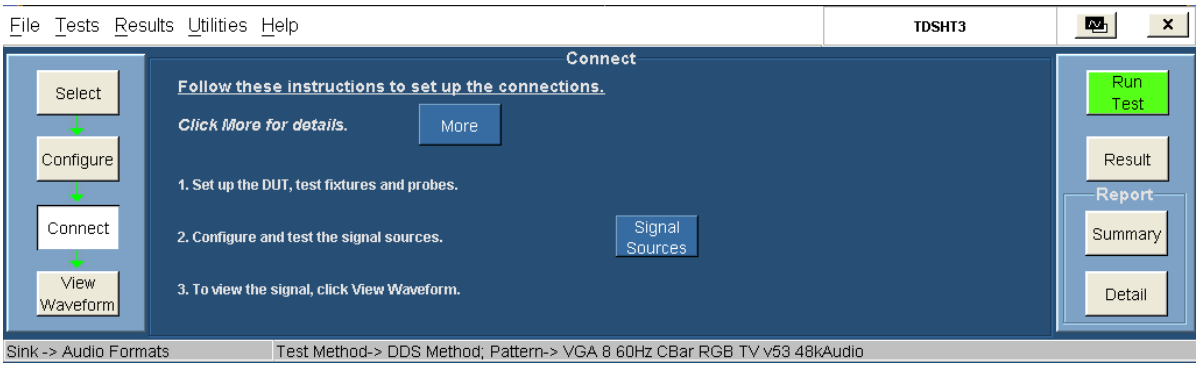
NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

In the DDS Method pane, do the following:



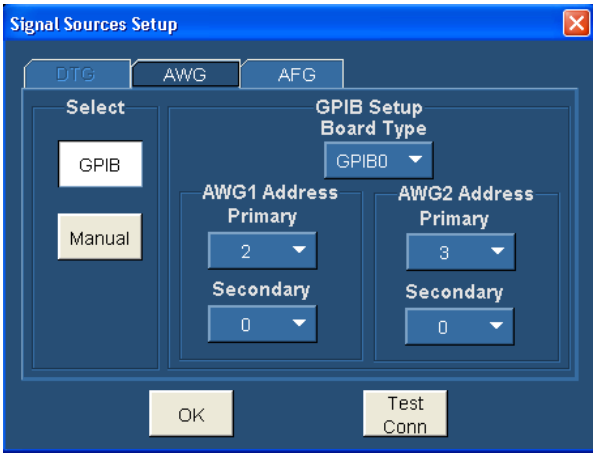
- In the Markers pane:
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
- Select the pattern(s) from the available list.

7. To connect the DUT, click **Tests > Connect**. Click here (see page 144) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.

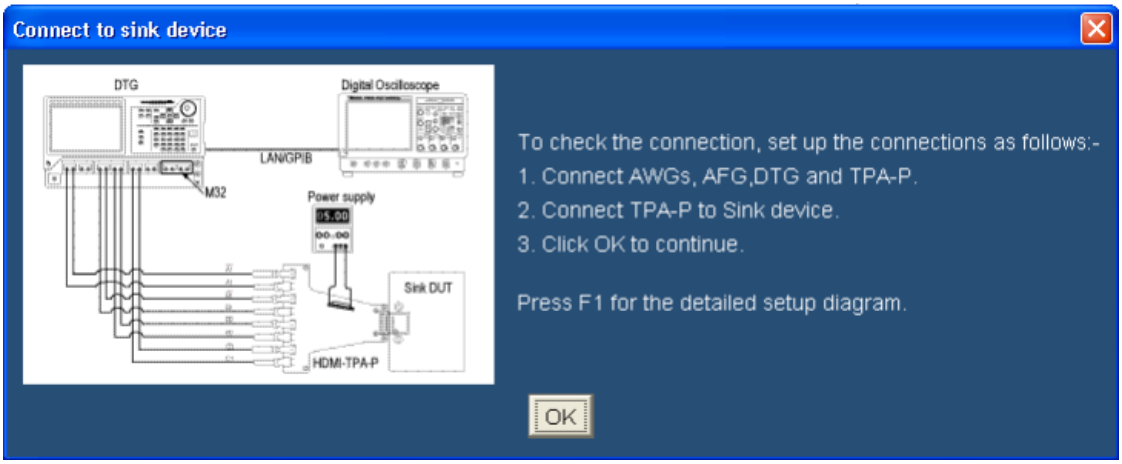
10. To test the connection and the GPIB configuration, click **Test Conn**.

11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the audio formats test.

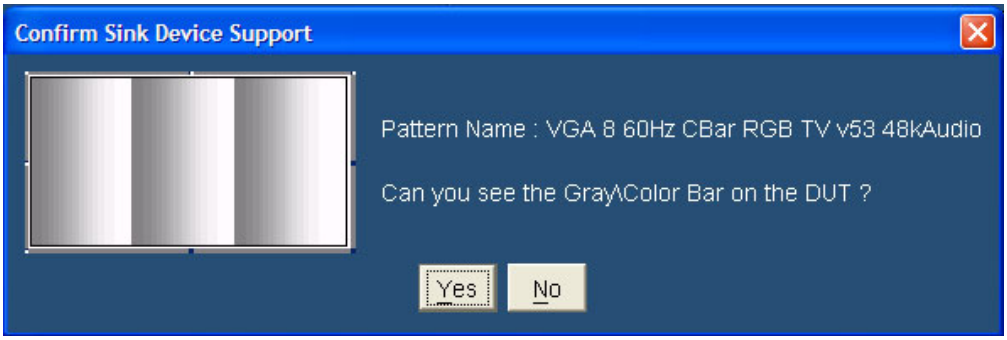
NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.

13. Follow the instructions in the Sink dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:

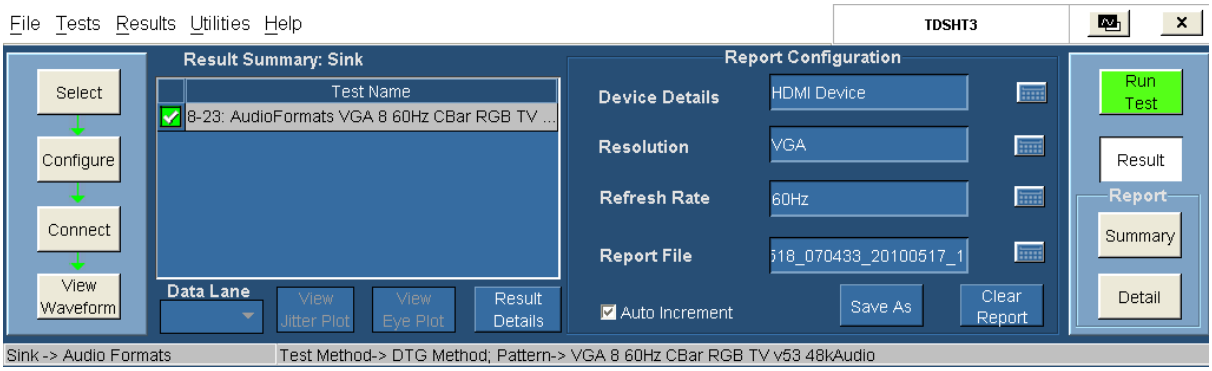


14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.



15. Follow the instructions in the dialog box.

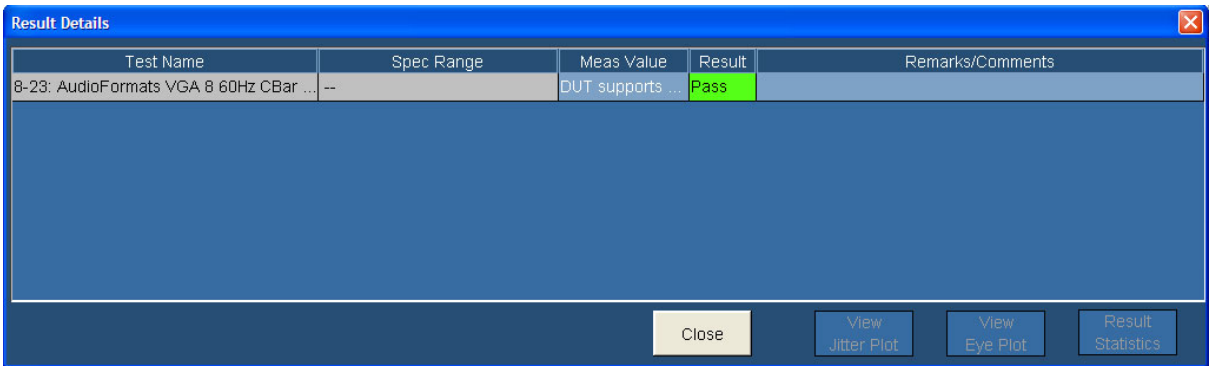
16. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected patterns)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the pattern supported by the DUT)
- Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs an audio formats test. For the procedure on how to make this test, refer to audio formats test procedure (see page 301).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs.

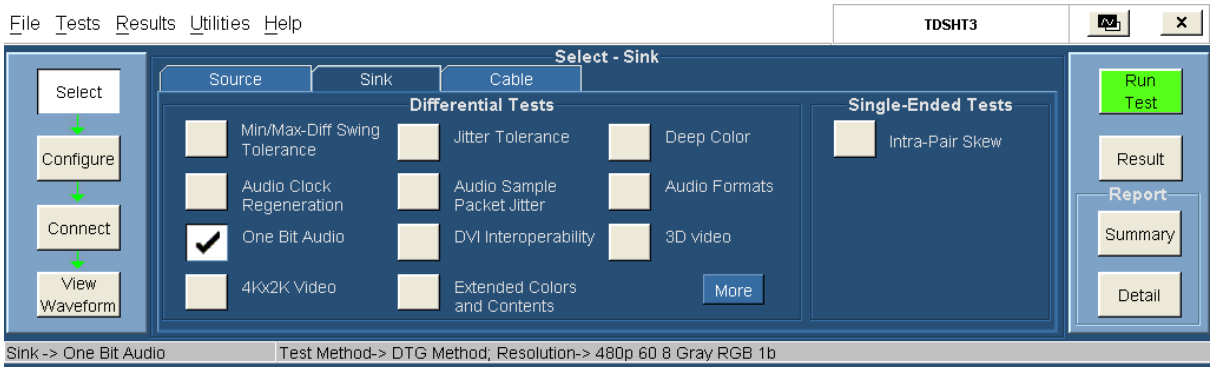
1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer audio formats test procedure (see page 301).
3. Refer to make connections for audio formats (see page 144) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

Test the One Bit Audio

To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

To use the DDS test method, you will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

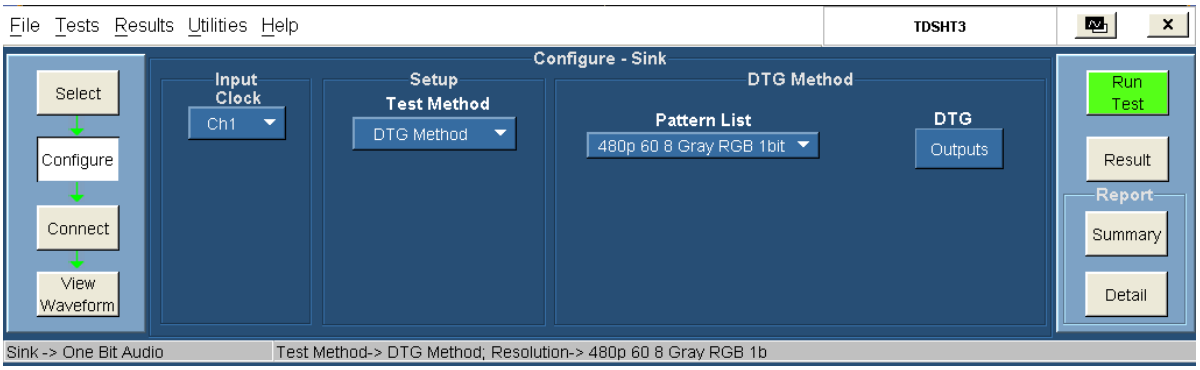
1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the One Bit Audio check box.



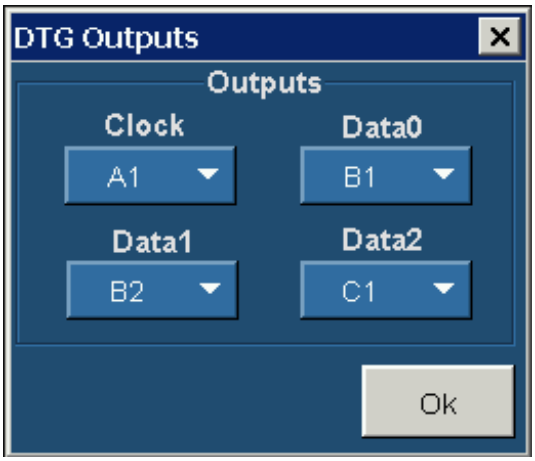
3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.
4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).

6. In the DTG Method pane, select the pattern(s) from the available list.



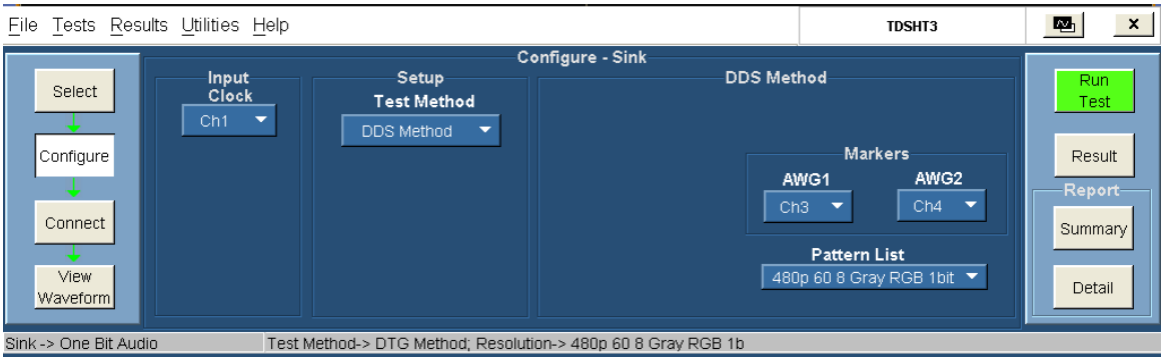
The DTG Outputs dialog box for the DTG method has the following options:



- Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
- Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

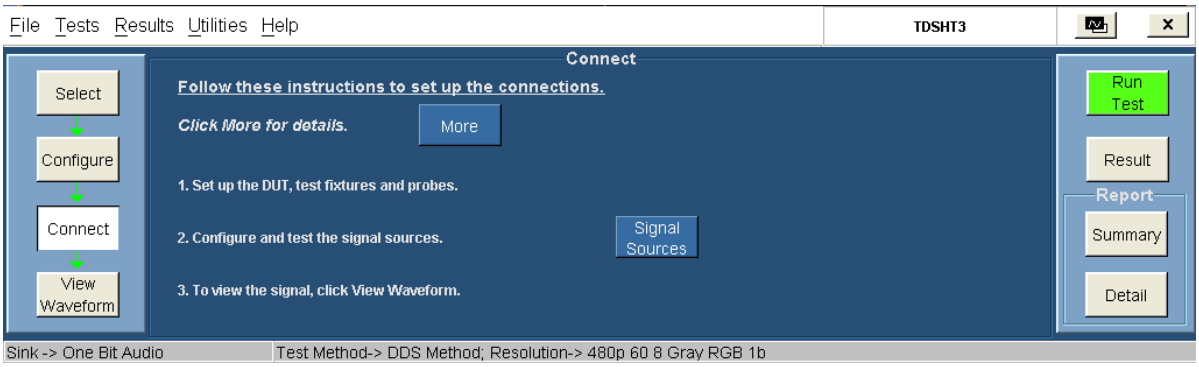
NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

In the DDS Method pane, do the following:



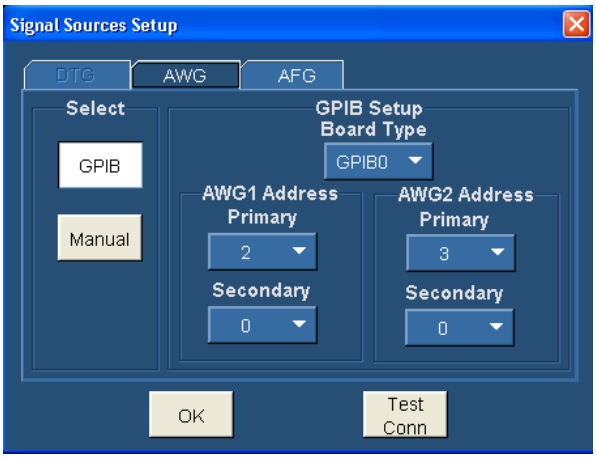
- In the Markers pane:
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
- Select the pattern(s) from the available list.

7. To connect the DUT, click **Tests > Connect**. Click here (see page 147) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

   The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.

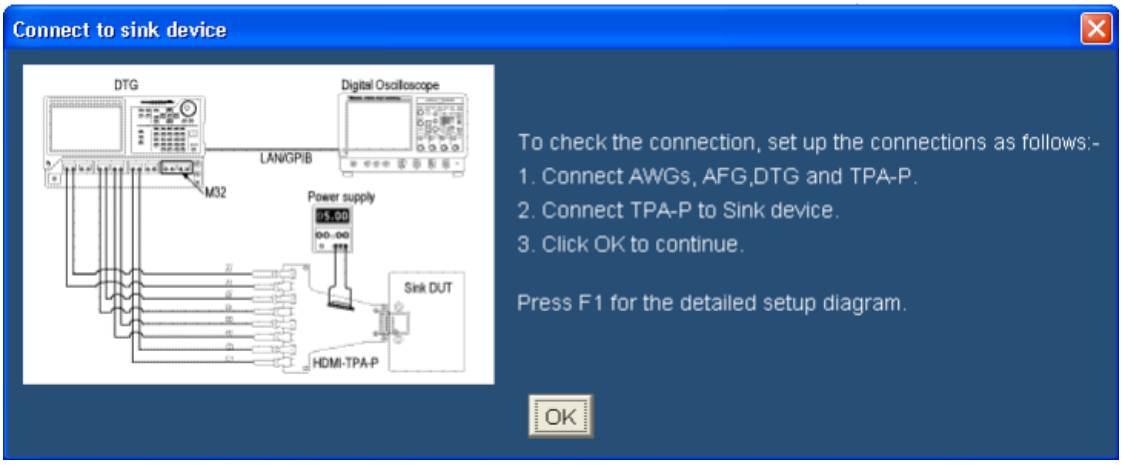
10. To test the connection and the GPIB configuration, click **Test Conn**.

11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the one bit audio test.

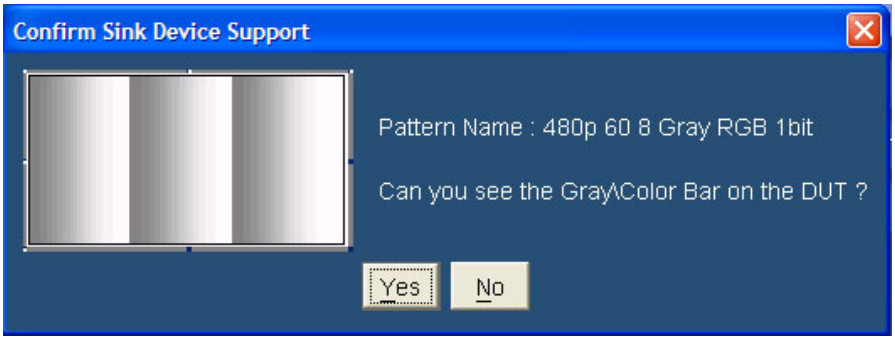
NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.

13. Follow the instructions in the Sink dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:

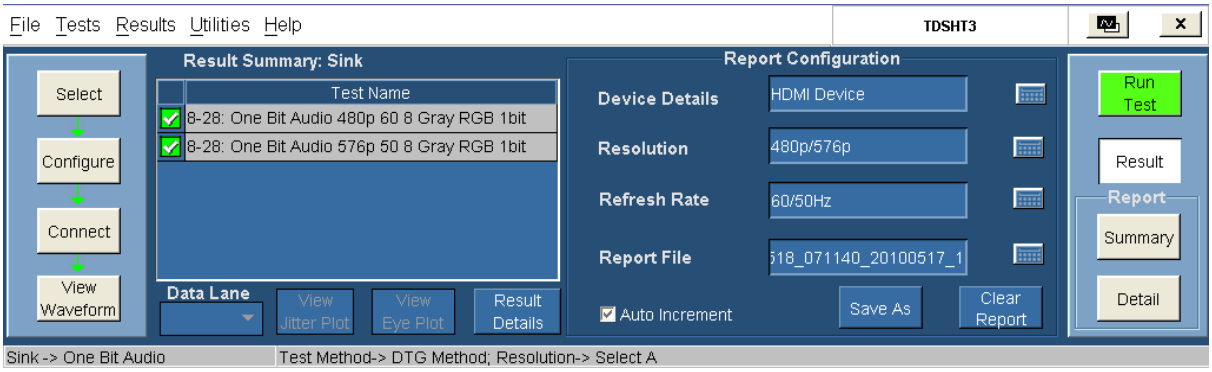


14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.



15. Follow the instructions in the dialog box.

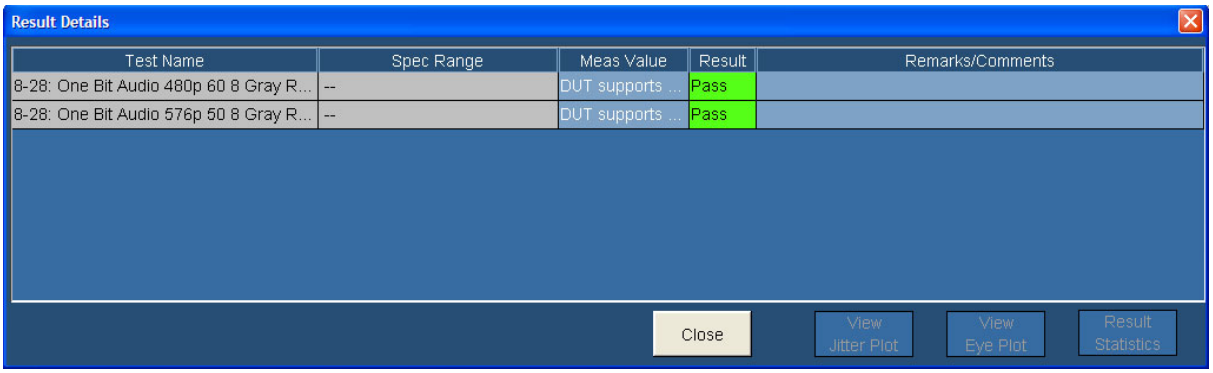
16. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected patterns)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the patterns supported by the DUT)
- Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs a one bit audio test. For the procedure on how to make this test, refer one bit audio test procedure (see page 307).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs.

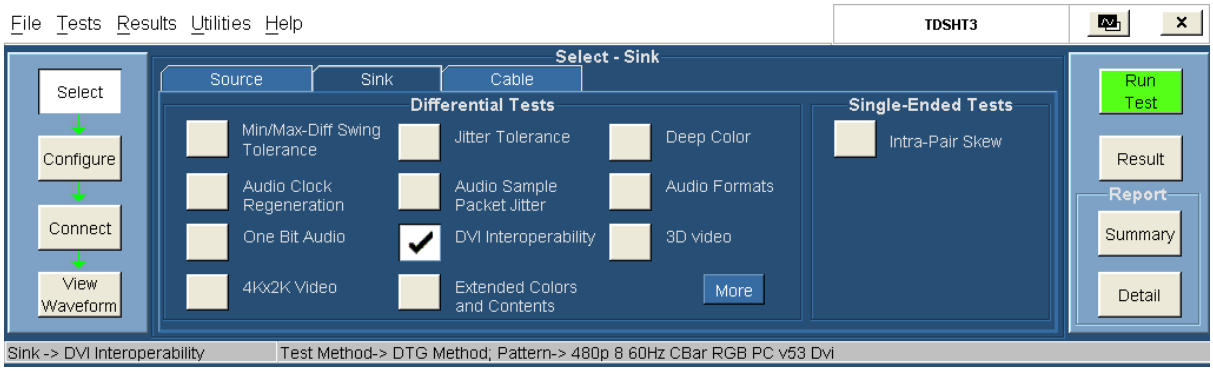
1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer one bit audio test procedure (see page 330).
3. Refer to make connections for one bit audio (see page 147) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

Test the DVI Interoperability

To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

To use the DDS test method, you will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

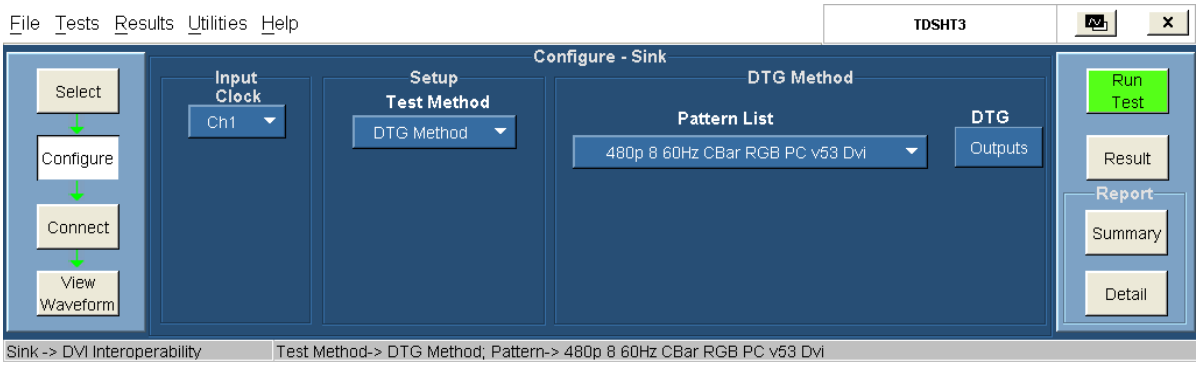
1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the DVI Interoperability check box.



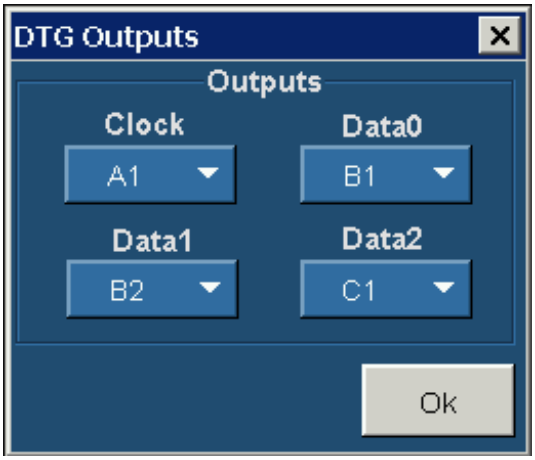
3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.
4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).

6. In the DTG Method pane, select the pattern(s) from the available list.



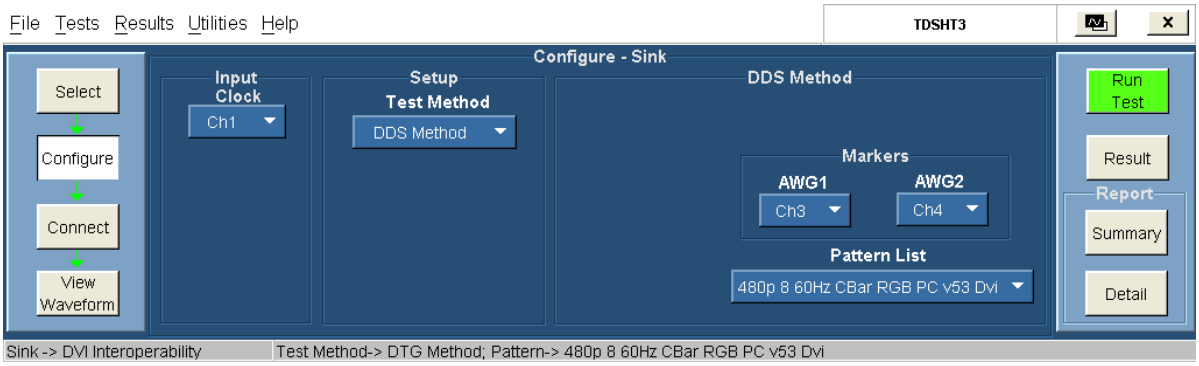
The DTG Outputs dialog box for the DTG method has the following options:



- Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
- Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

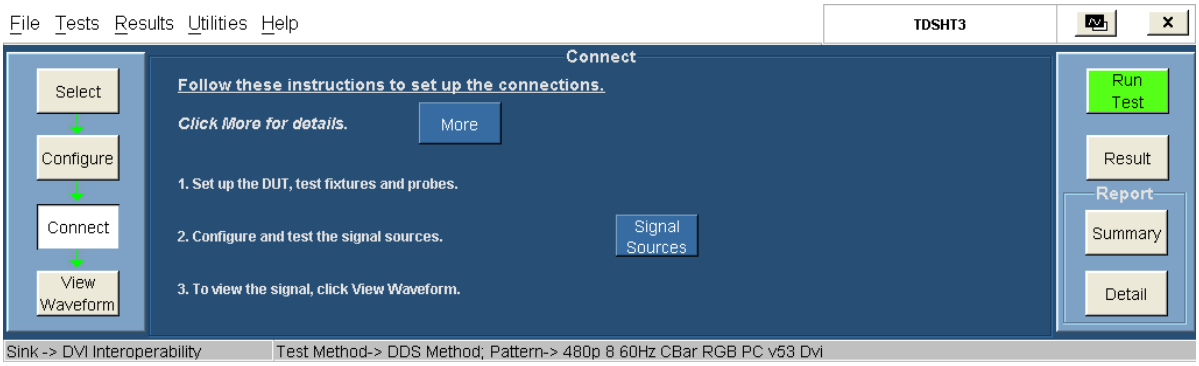
NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

In the DDS Method pane, do the following:



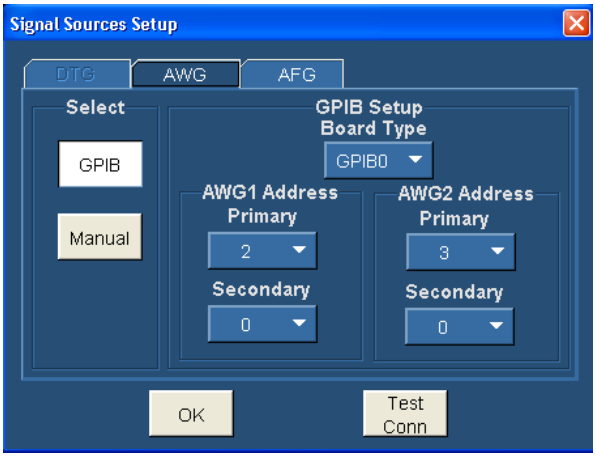
- In the Markers pane:
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
- Select the pattern(s) from the available list.

7. To connect the DUT, click **Tests > Connect**. Click here (see page 150) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

   The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



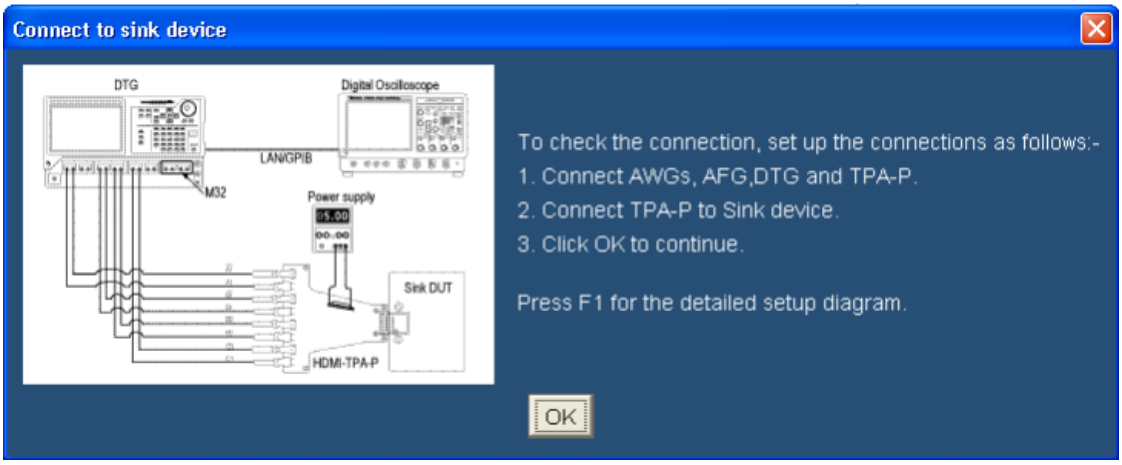
NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

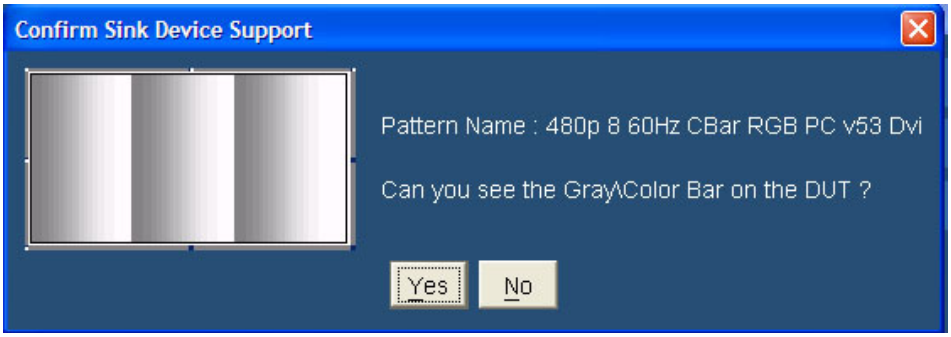
9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.
10. To test the connection and the GPIB configuration, click **Test Conn**.
11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the DVI interoperability test.

NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.
13. Follow the instructions in the Sink dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:

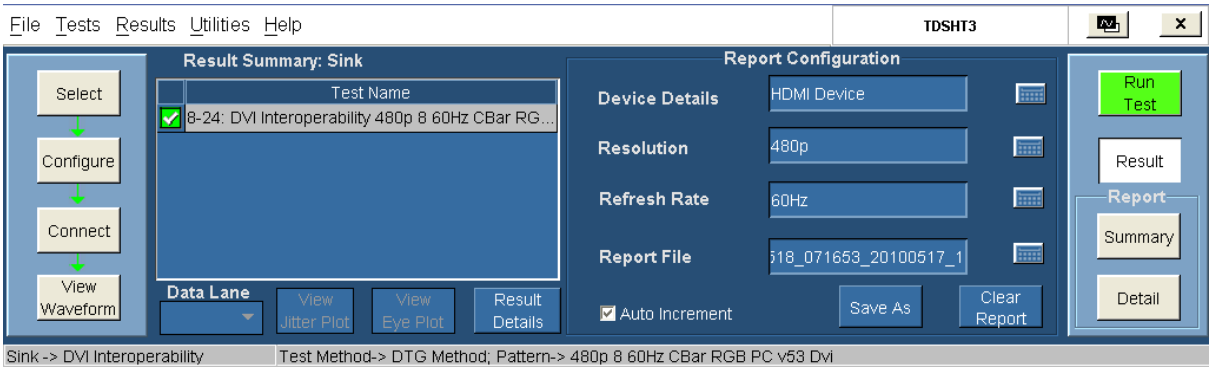


14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.



15. Follow the instructions in the dialog box.

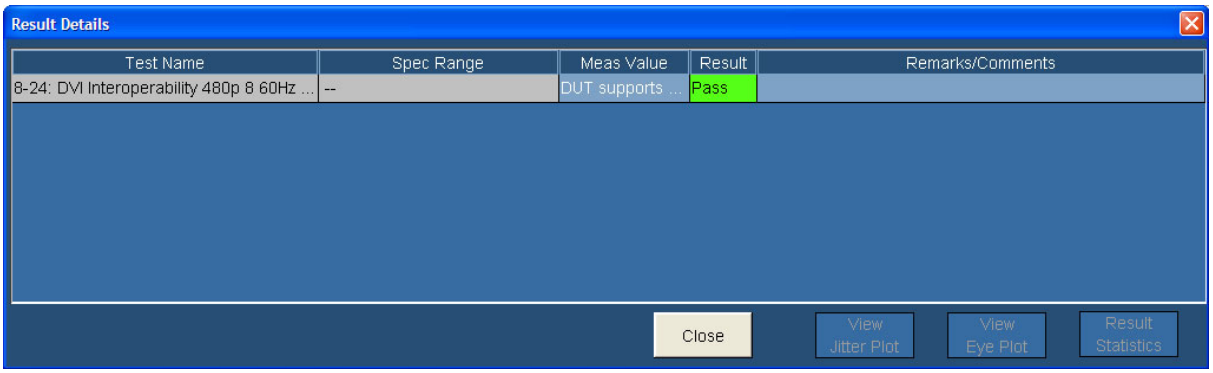
16. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected pattern)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the pattern supported by the DUT)
- Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs a DVI Interoperability test. For the procedure on how to make this test, refer DVI interoperability test procedure (see page 330).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs.

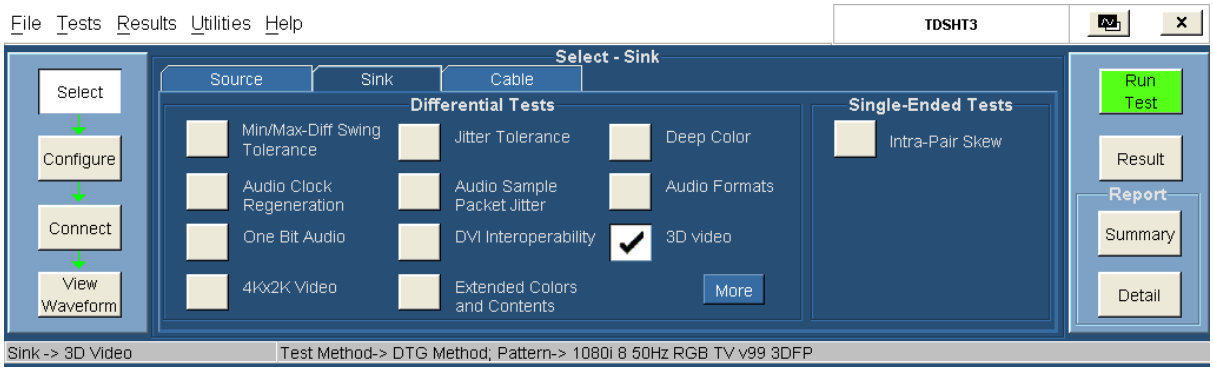
1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer DVI interoperability test procedure (see page 330).
3. Refer to make connections for DVI interoperability (see page 150) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

Test the 3D Video

To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

To use the DDS test method, You will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

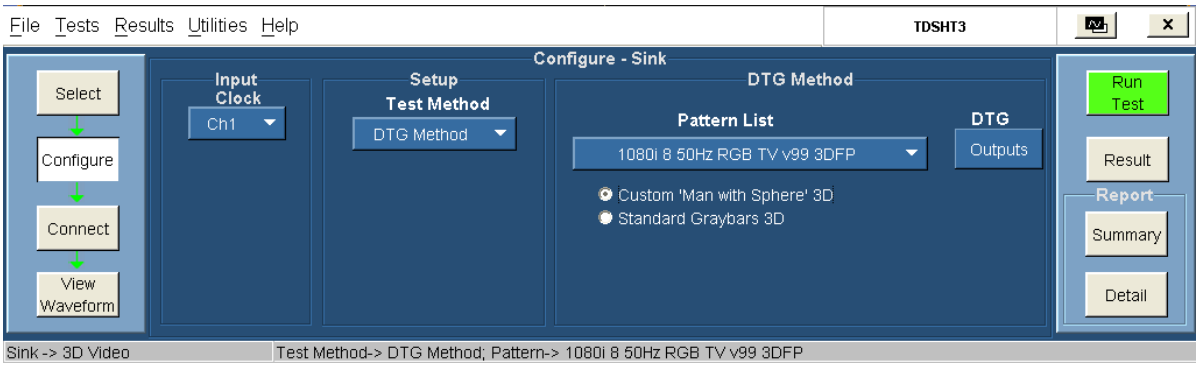
1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the 3D Video check box.



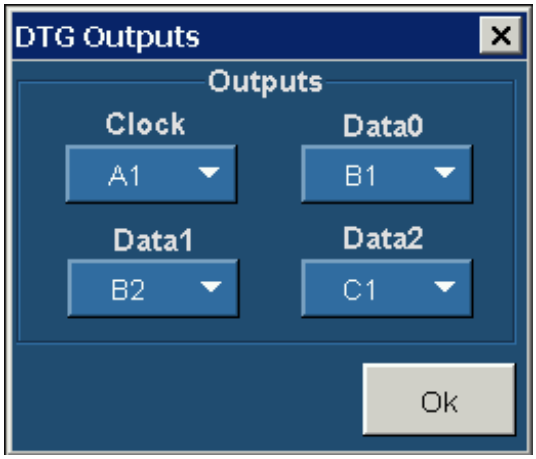
3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.
4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).

5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).

6. In the DTG Method pane, do the following:



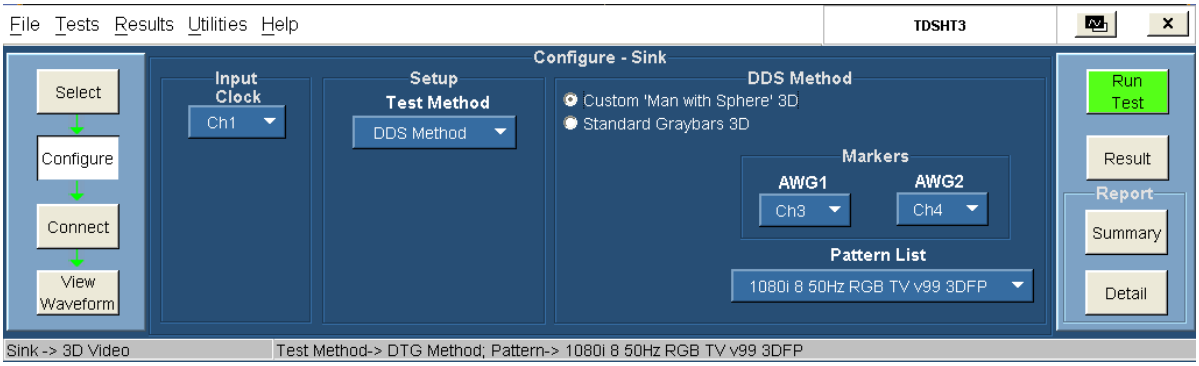
- Select the pattern(s) from the available list.
- Select one of the two: Custom 'Man with Sphere' 3D, or Standard Graybars 3D.
- The DTG Outputs dialog box for the DTG method has the following options:



  - Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
  - Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

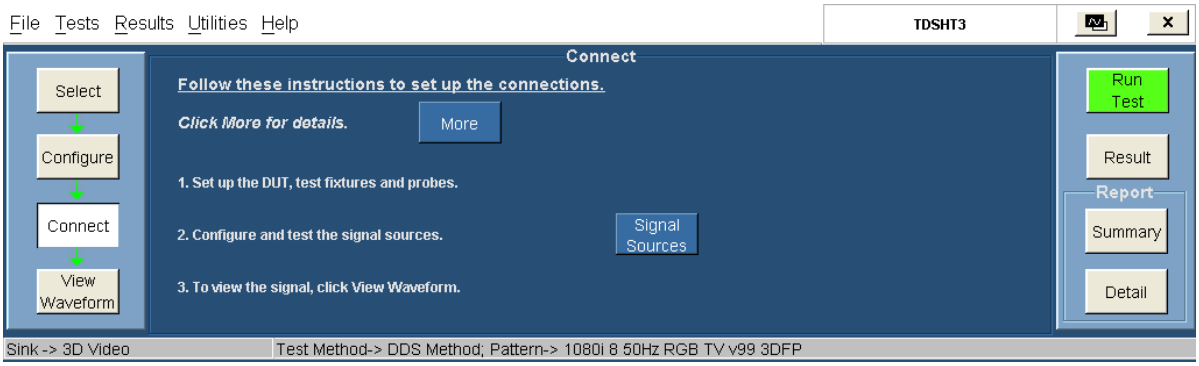
NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

In the DDS Method pane, do the following:



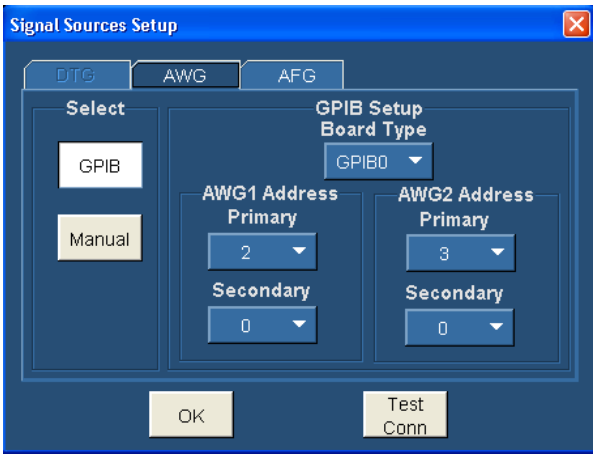
- Select one of the two: Custom 'Man with Sphere' 3D, or Standard Graybars 3D.
- In the Markers pane:
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
- Select the pattern(s) from the available list.

7. To connect the DUT, click **Tests > Connect**. Click here (see page 153) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

   The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



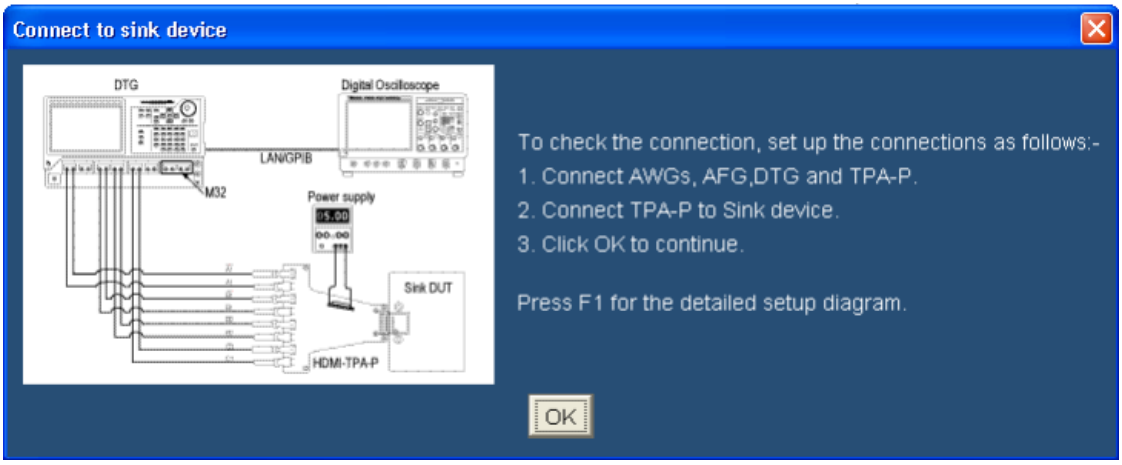
NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

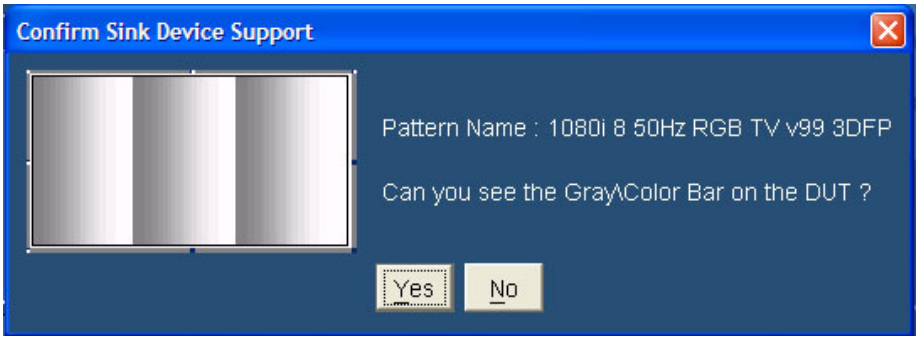
9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.
10. To test the connection and the GPIB configuration, click **Test Conn**.
11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the jitter tolerance test.

NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.
13. Follow the instructions in the Sink dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:

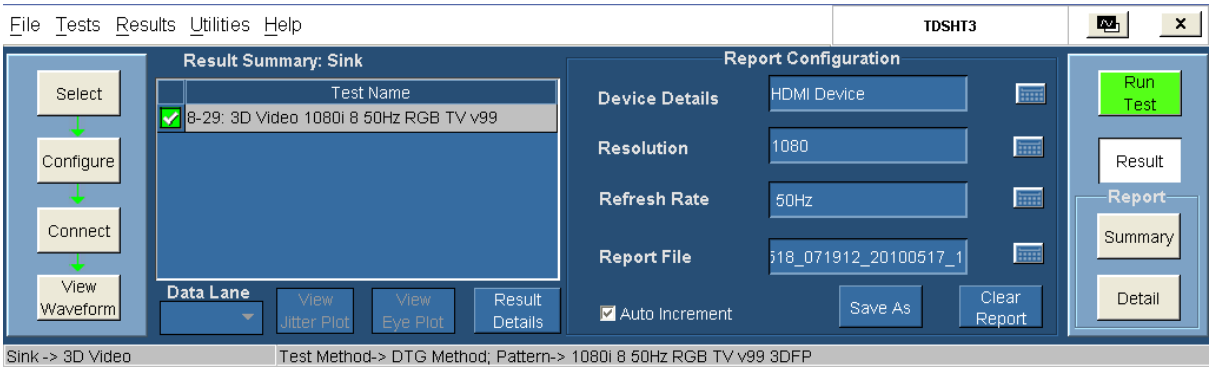


14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.



15. Follow the instructions in the dialog box.

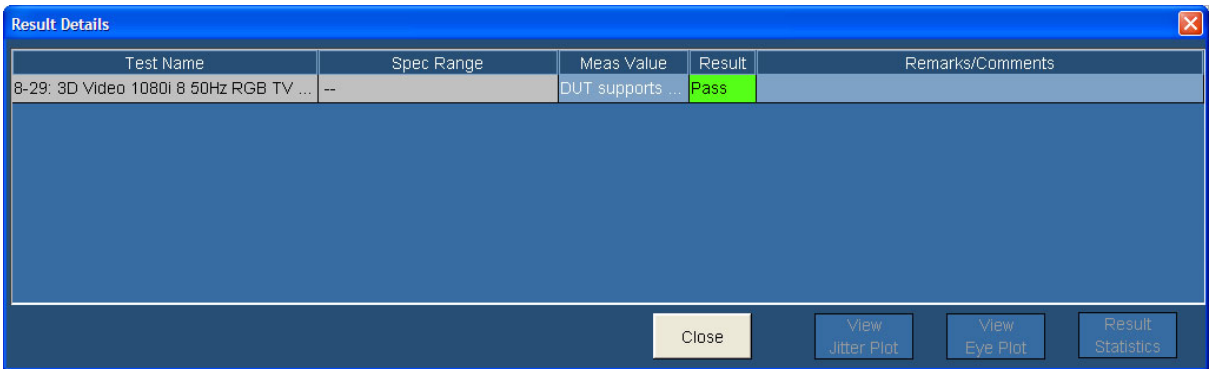
16. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected patterns)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the patterns supported by the DUT)
- Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs a 3D Video test. For the procedure on how to make this test, refer 3D Video test procedure (see page 330).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs.

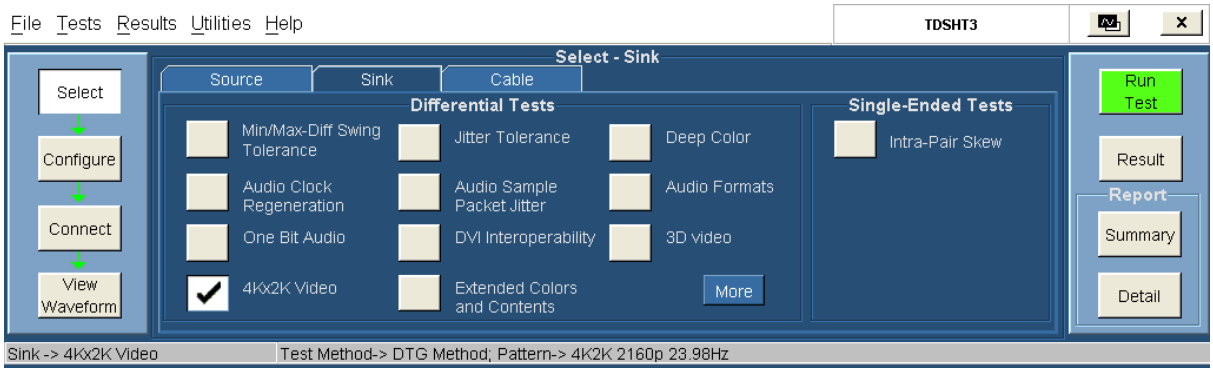
1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer 3D Video test procedure (see page 330).
3. Refer to make connections for 3D Video (see page 153) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

Test the 4Kx2K Video

To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

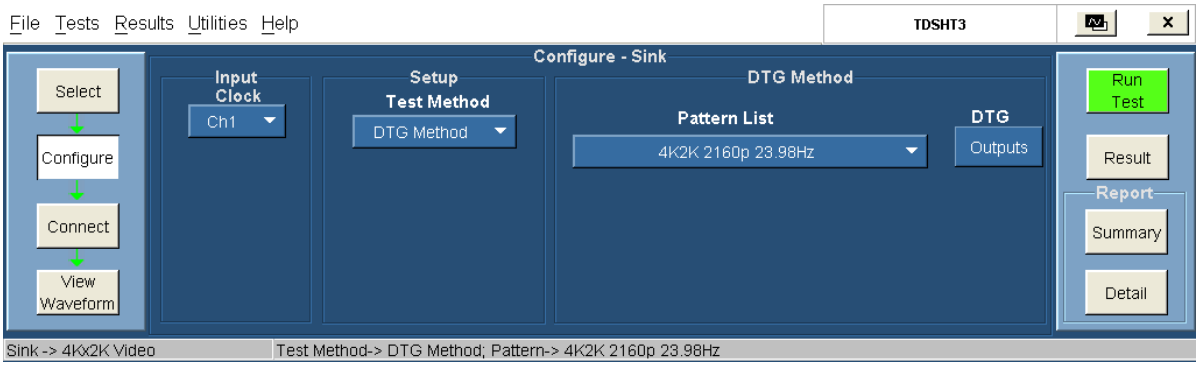
To use the DDS test method, you will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the 4Kx2K Video check box.

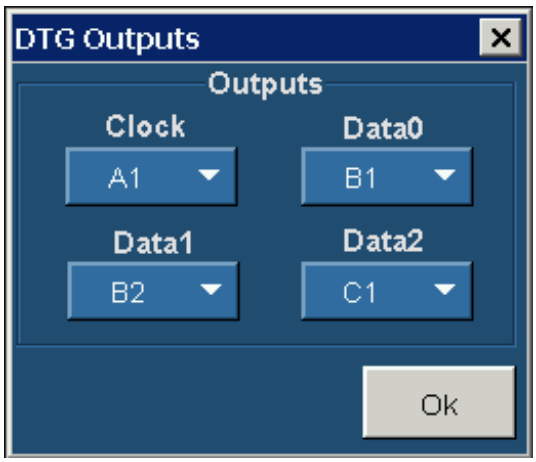


3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.
4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).

6. In the DTG Method pane, do the following:



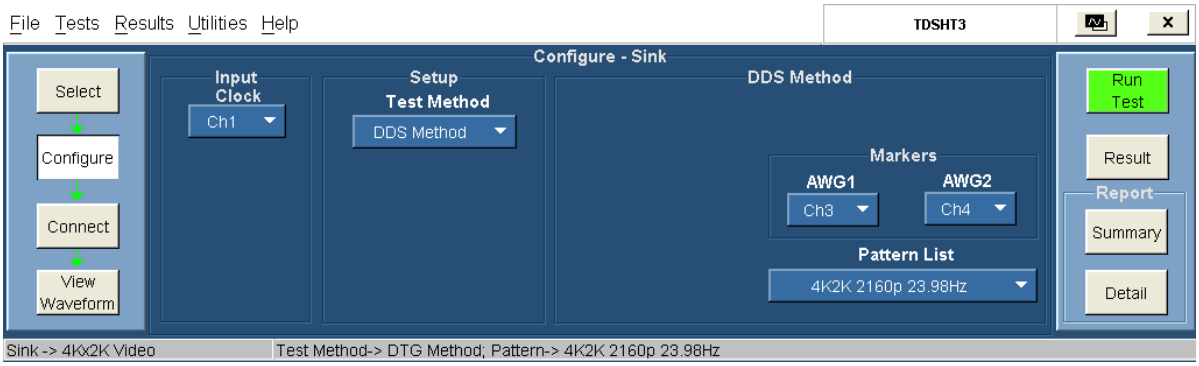
- Select the pattern(s) from the available list.
- The DTG Outputs dialog box for the DTG method has the following options:



  - Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
  - Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

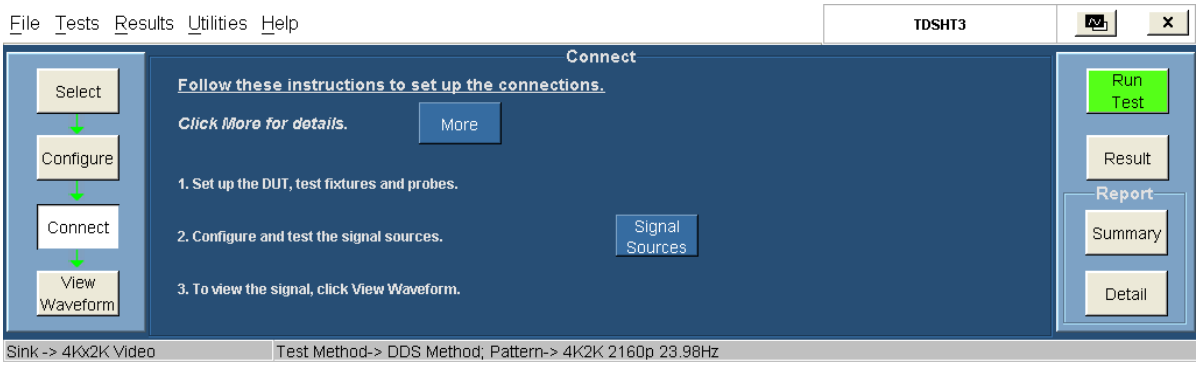
NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

In the DDS Method pane, do the following:



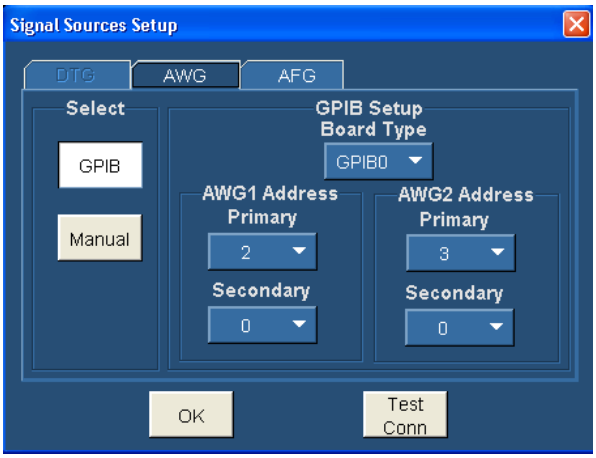
- In the Markers pane:
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
- Select the pattern(s) from the available list.

7. To connect the DUT, click **Tests > Connect**. Click here (see page 156) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

   The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



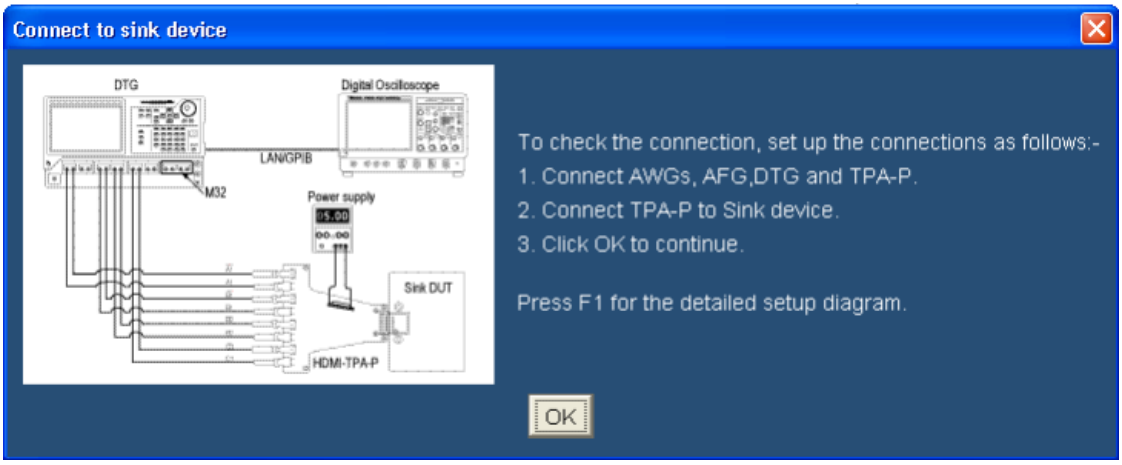
NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

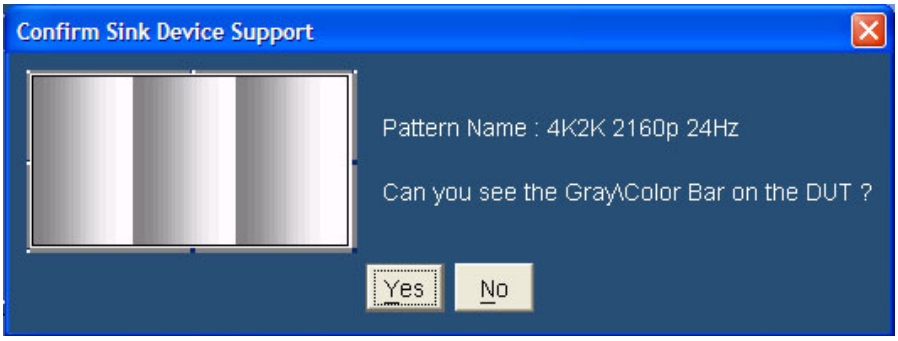
9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.
10. To test the connection and the GPIB configuration, click **Test Conn**.
11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the 4Kx2K video test.

NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.
13. Follow the instructions in the Sink dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:



14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.



15. Follow the instructions in the dialog box.

16. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.

    The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.

    - Test Name (displays the test id, test name, and selected patterns)
    - Spec Range
    - Meas Value (displays the patterns supported by the DUT)
    - Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs a 4Kx2K Video test. For the procedure on how to make this test, refer 4Kx2K Video test procedure (see page 330).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs.

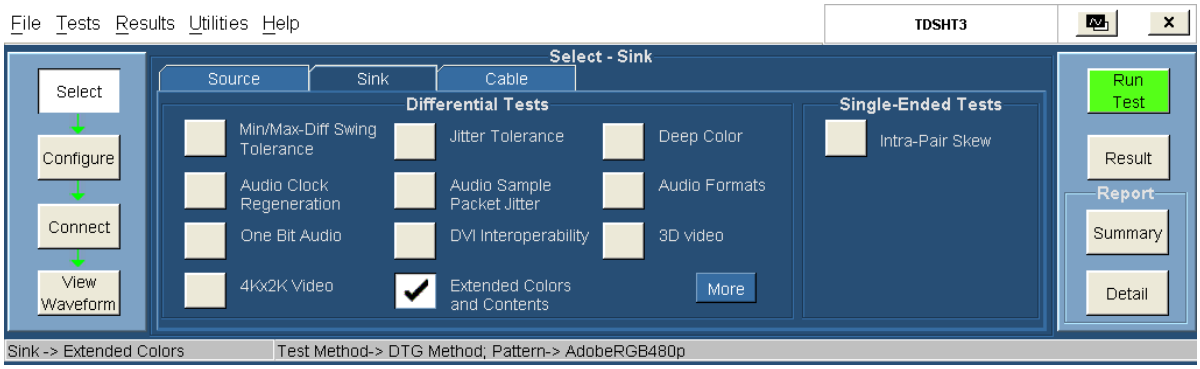
1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer 4Kx2K Video test procedure (see page 330).
3. Refer to make connections for 4Kx2K Video (see page 156) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

Test the Extended Colors and Contents

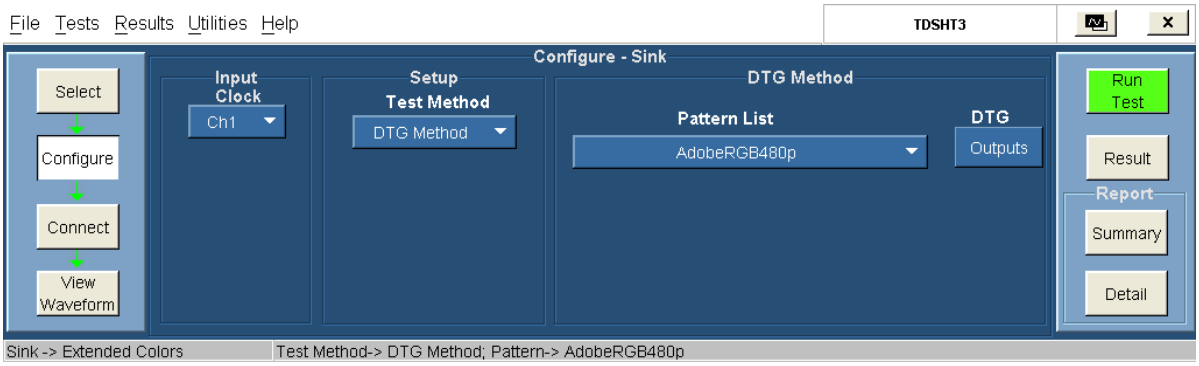
To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

To use the DDS test method, You will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

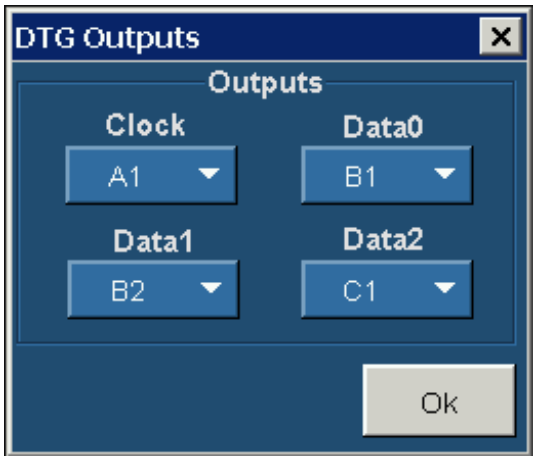
1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the Extended Colors and Contents check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.
4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).
6. In the DTG Method pane, do the following:



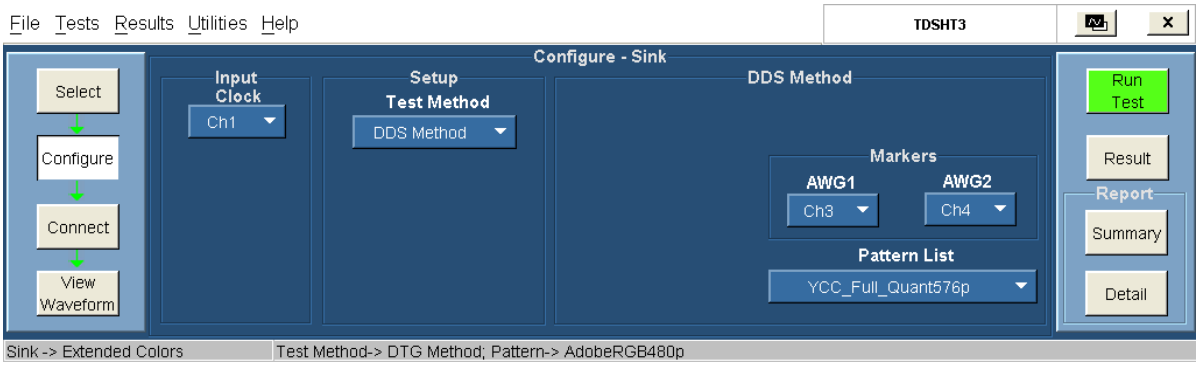
- Select the pattern(s) from the available list.
- The DTG Outputs dialog box for the DTG method has the following options:



- Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
- Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

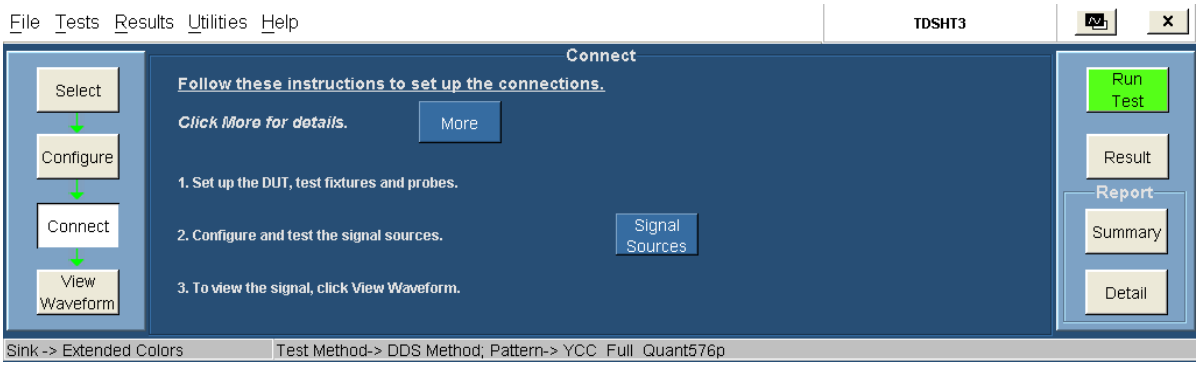
NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

In the DDS Method pane, do the following:



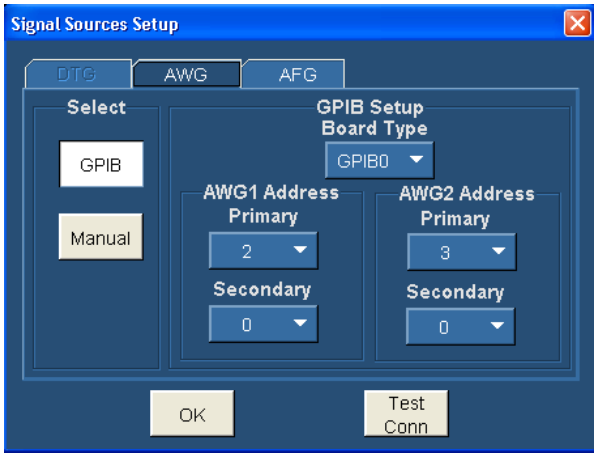
- In the Markers pane:
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
- Select the pattern(s) from the available list.

7. To connect the DUT, click **Tests > Connect**. Click here (see page 159) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.

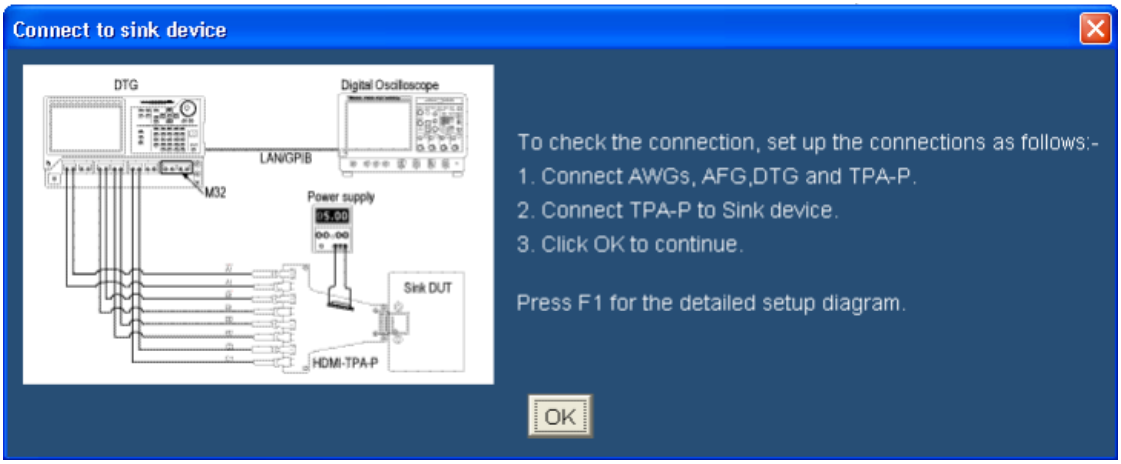
10. To test the connection and the GPIB configuration, click **Test Conn**.

11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the extended colors and contents test.

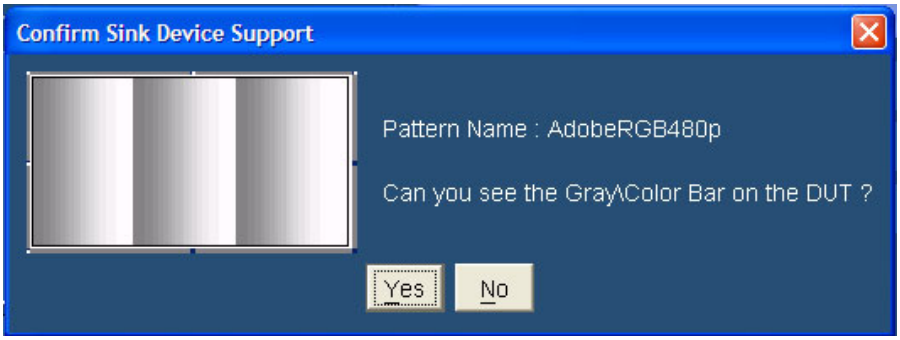
NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.

13. Follow the instructions in the Sink dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:

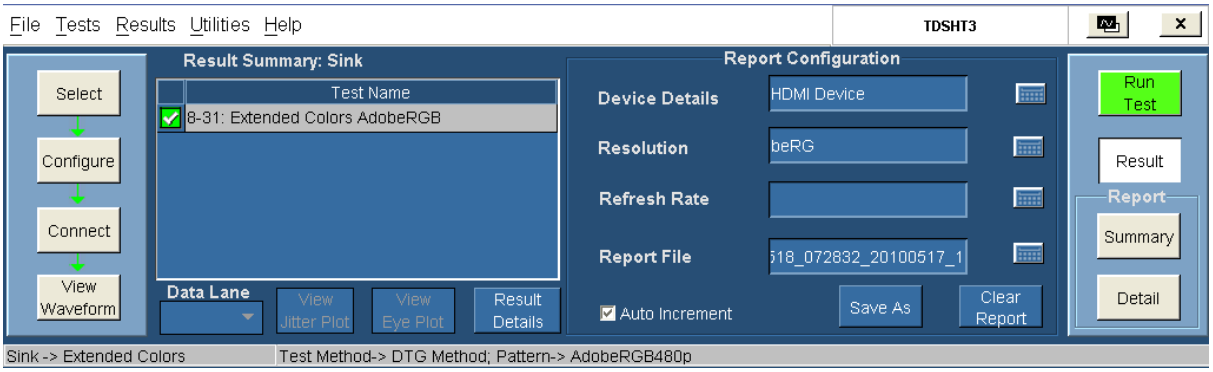


14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.



15. Follow the instructions in the dialog box.

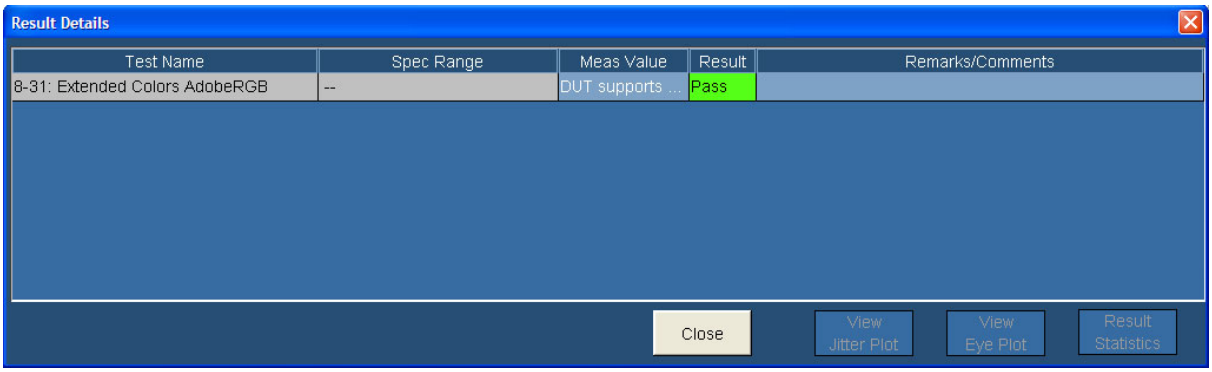
16. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected patterns)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the pattern supported by the DUT)
- Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs a Extended Colors and Contents test. For the procedure on how to make this test, refer Extended Colors and Contents test procedure (see page 330).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs.

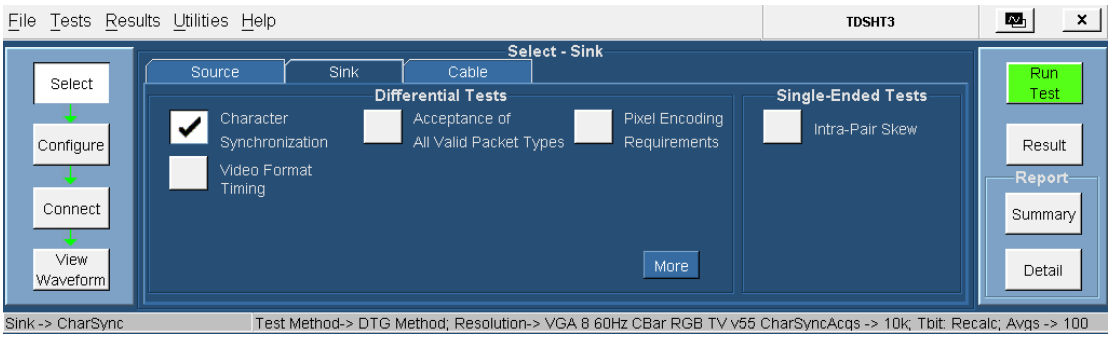
1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer Extended Colors and Contents test procedure (see page 330).
3. Refer to Extended Colors and Contents test procedure (see page 330) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

Test the Character Synchronization

To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

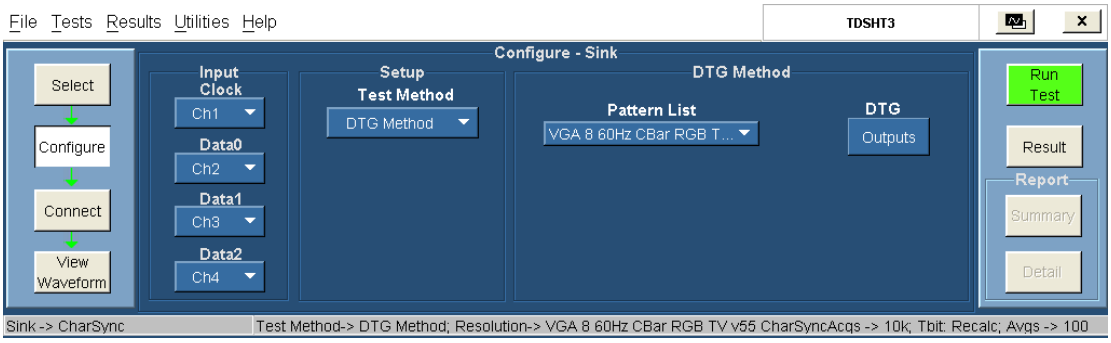
To use the DDS test method, You will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, click **More** and select the Character Synchronization check box.

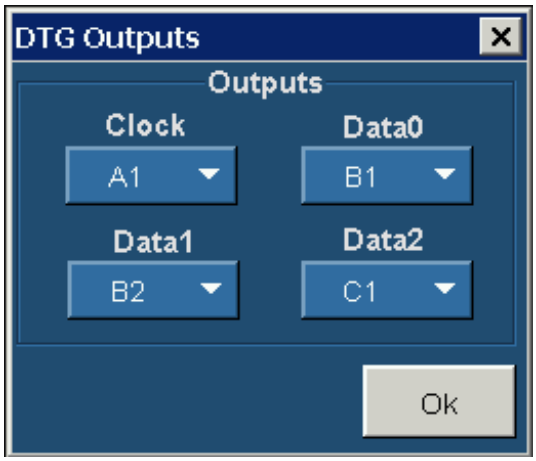


3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.

4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).
6. In the DTG Method pane, do the following:



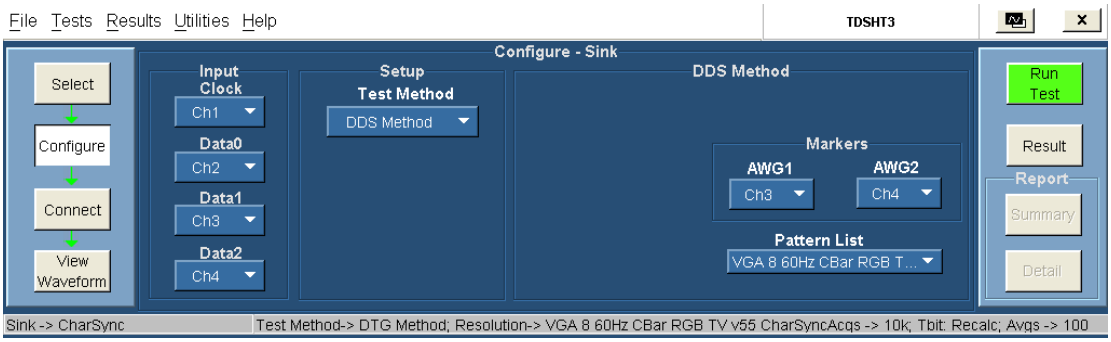
- Select the pattern(s) from the available list.
- The DTG Outputs dialog box for the DTG method has the following options:



- Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
- Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

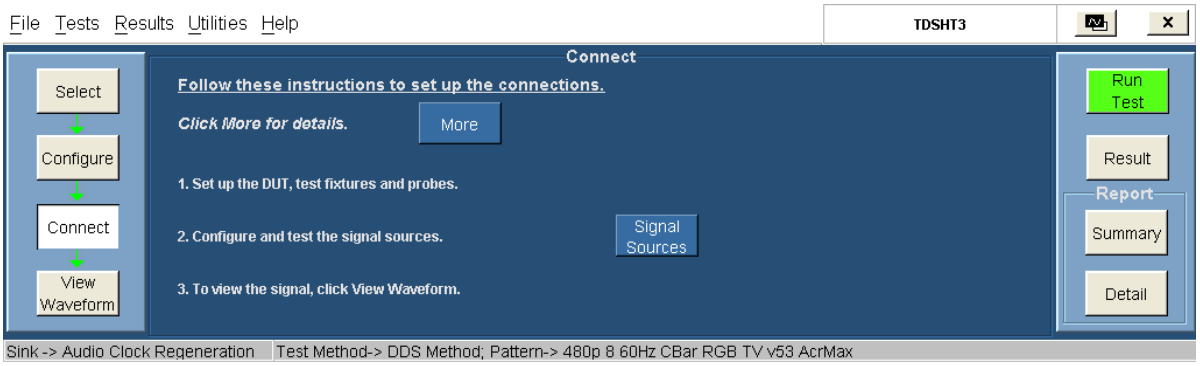
NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

In the DDS Method pane, do the following:



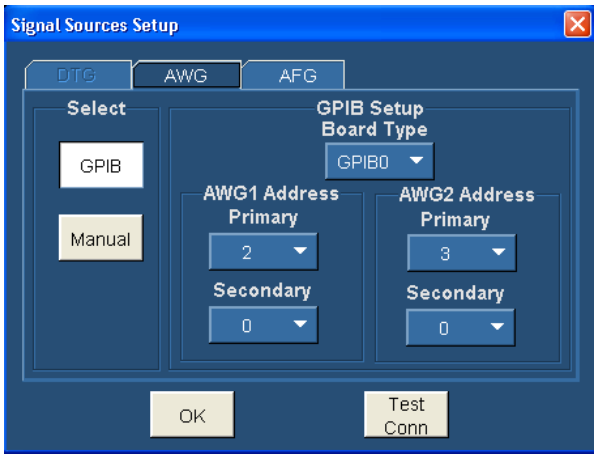
- In the Markers pane:
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
- Select the pattern(s) from the available list.

7. To connect the DUT, click **Tests > Connect**. Click here (see page 162) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



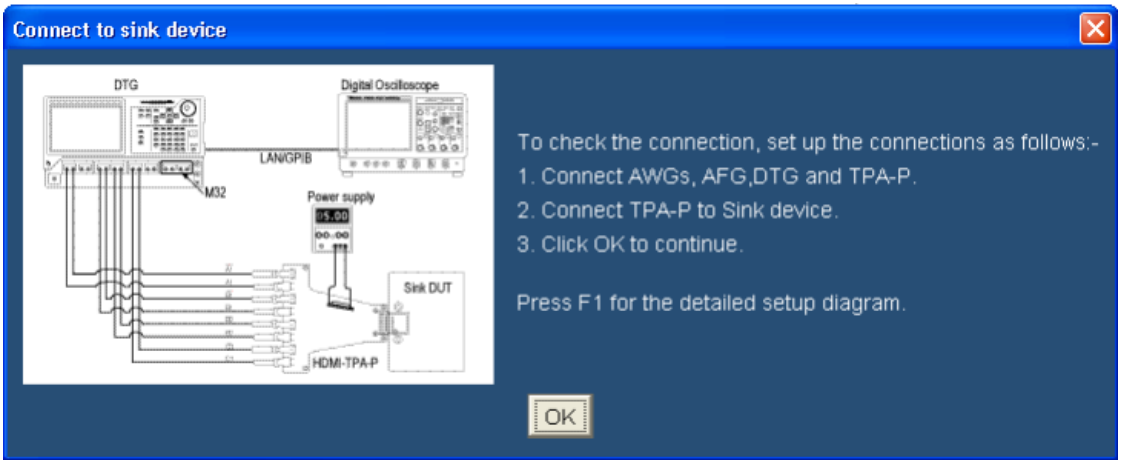
NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

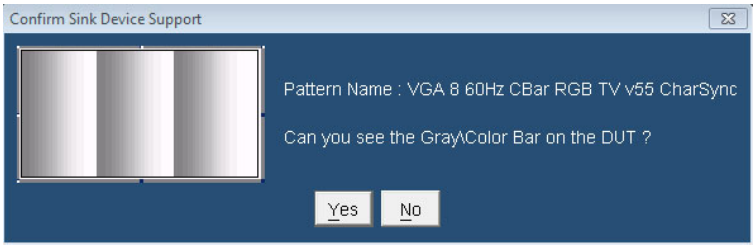
9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.
10. To test the connection and the GPIB configuration, click **Test Conn**.
11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the jitter tolerance test.

NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.
13. Follow the instructions in the Sink dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:

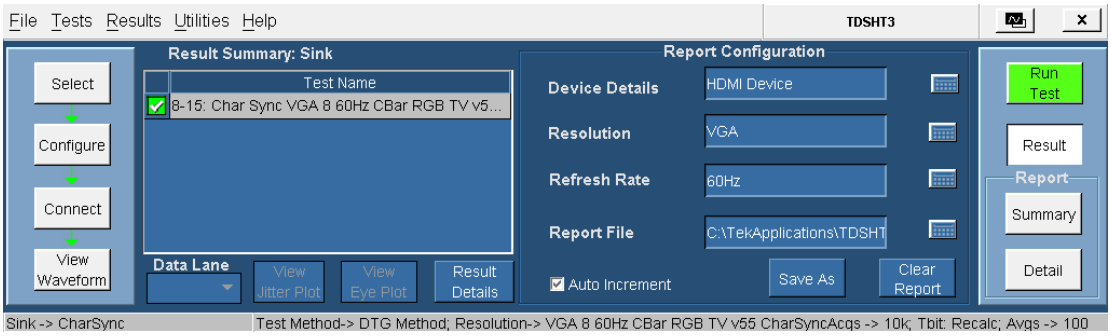


14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.



15. Follow the instructions in the dialog box.

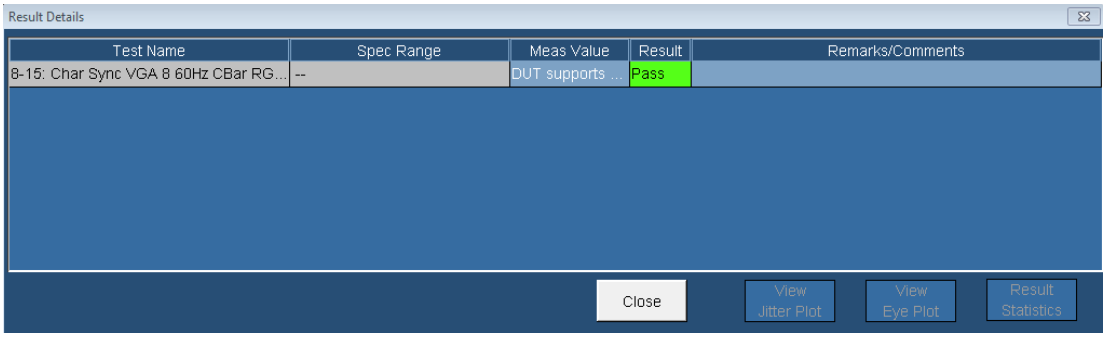
16. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected patterns)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the patterns supported by the DUT)
- Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs a Configuration Synchronization test. For the procedure on how to make this test, refer to the character synchronization test procedure (see page 336).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs.

1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer character synchronization test procedure (see page 336).
3. Refer to make connections for character synchronization (see page 162) for information on how to make connections.

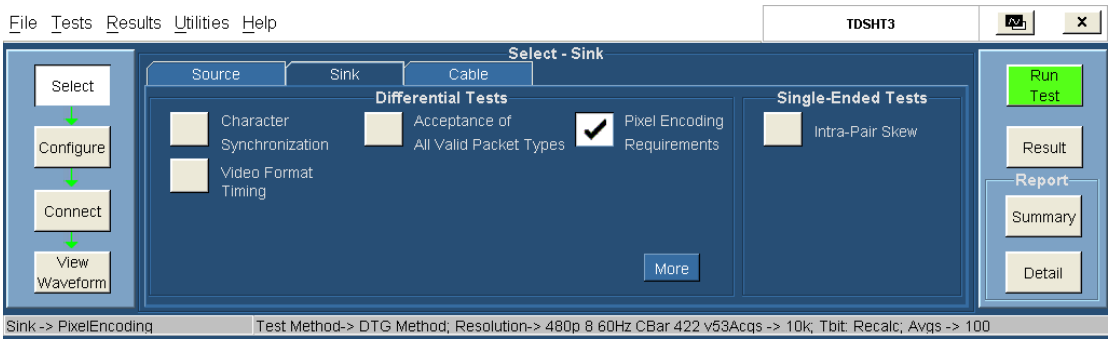
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

Test the Pixel Encoding Requirements

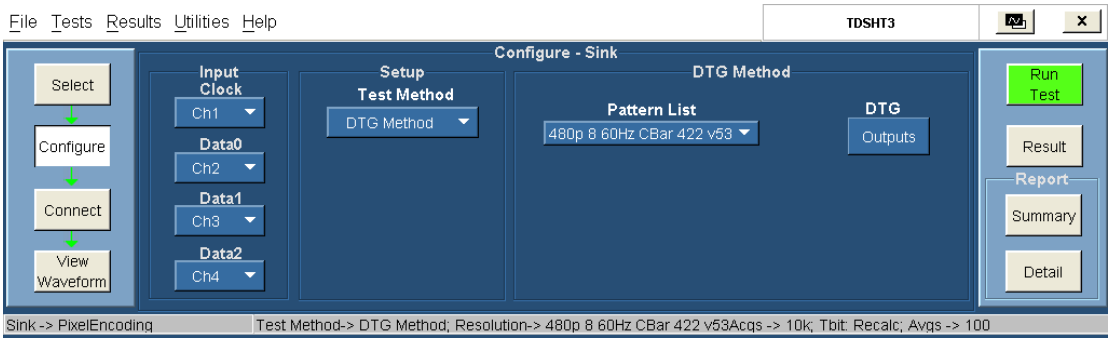
To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

To use the DDS test method, You will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

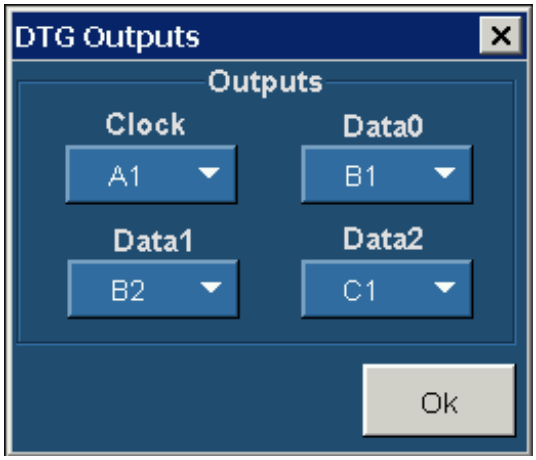
1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the Pixel Encoding Requirements check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.
4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).
6. In the DTG Method pane, do the following:



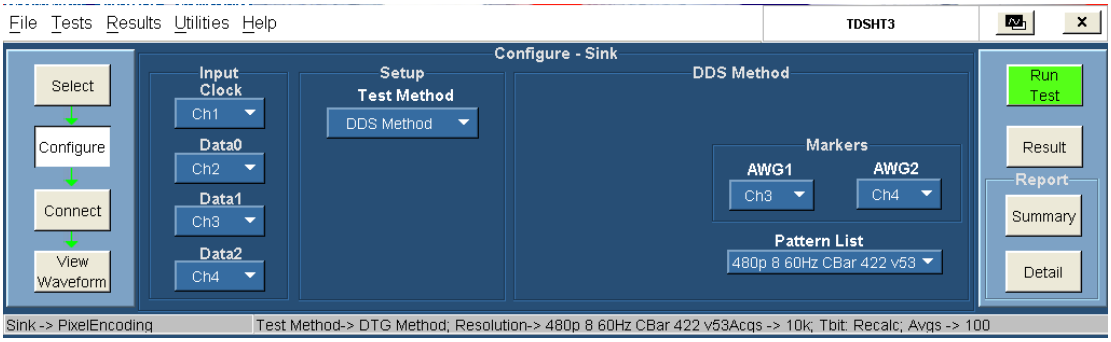
- Select the pattern(s) from the available list.
- The DTG Outputs dialog box for the DTG method has the following options:



  - Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
  - Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

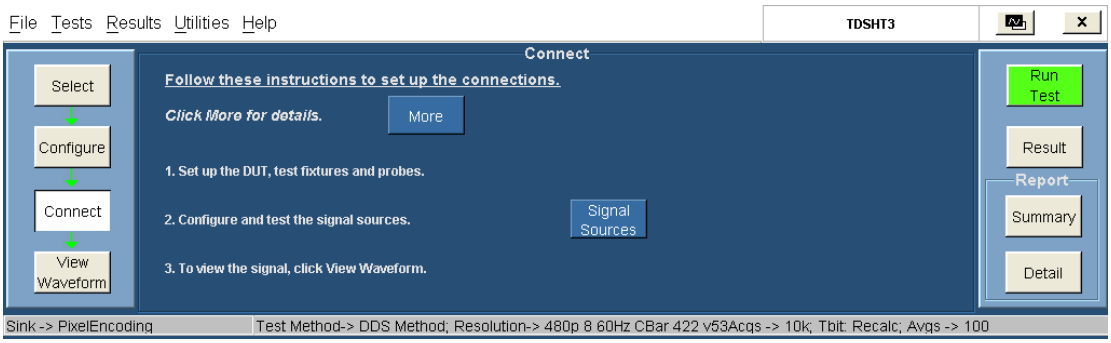
NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

In the DDS Method pane, do the following:



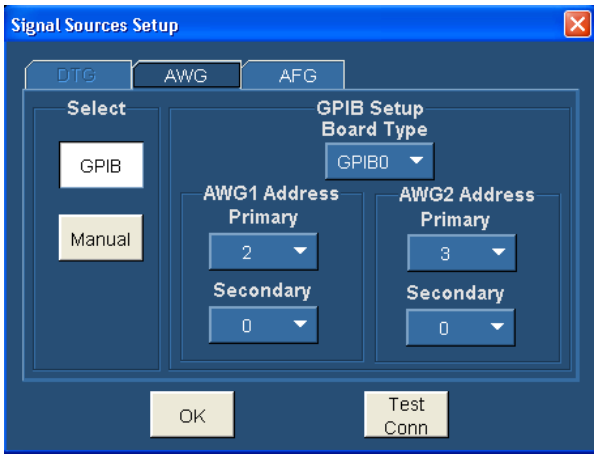
- Select one of the two: Custom 'Man with Sphere' 3D, or Standard Graybars 3D.
- In the Markers pane:
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
- Select the pattern(s) from the available list.

7. To connect the DUT, click **Tests > Connect**. Click here (see page 162) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

   The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



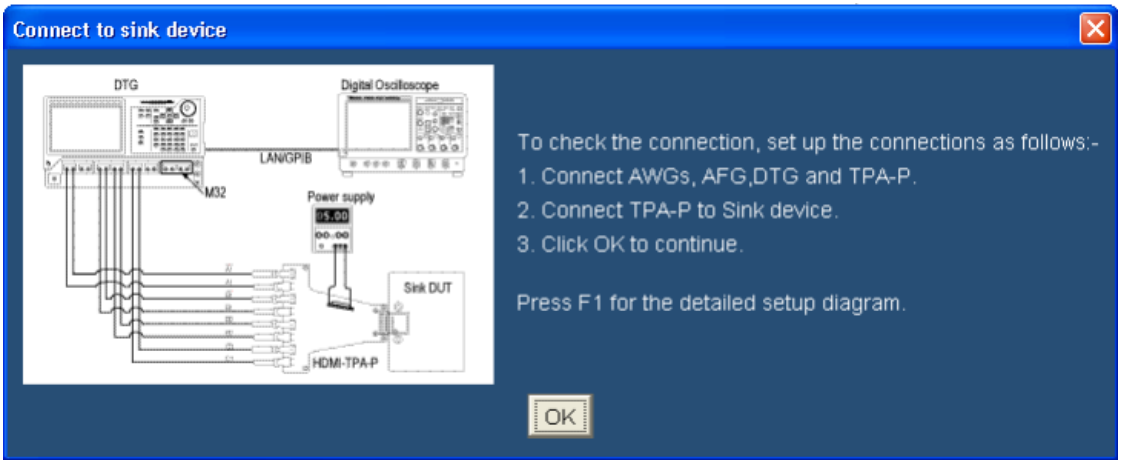
NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

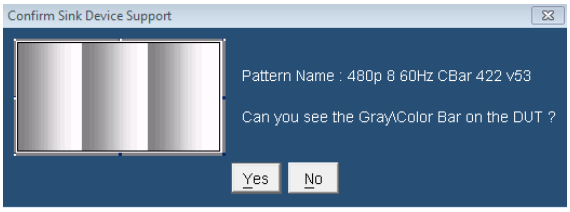
9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.
10. To test the connection and the GPIB configuration, click **Test Conn**.
11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the jitter tolerance test.

NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.
13. Follow the instructions in the Sink dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:

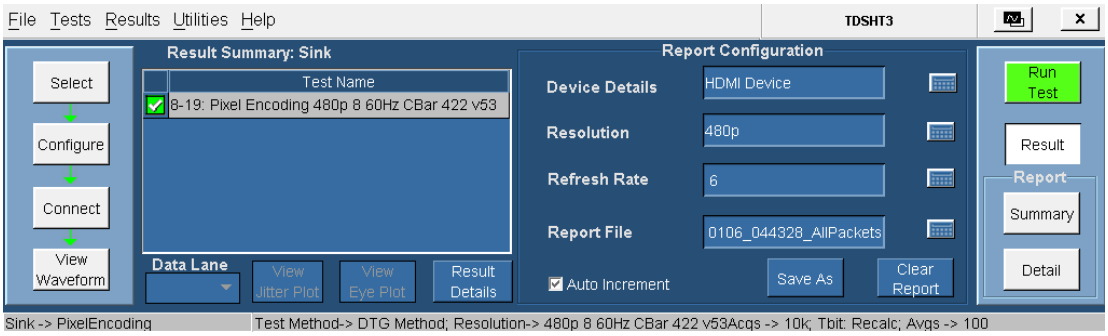


14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.



15. Follow the instructions in the dialog box.

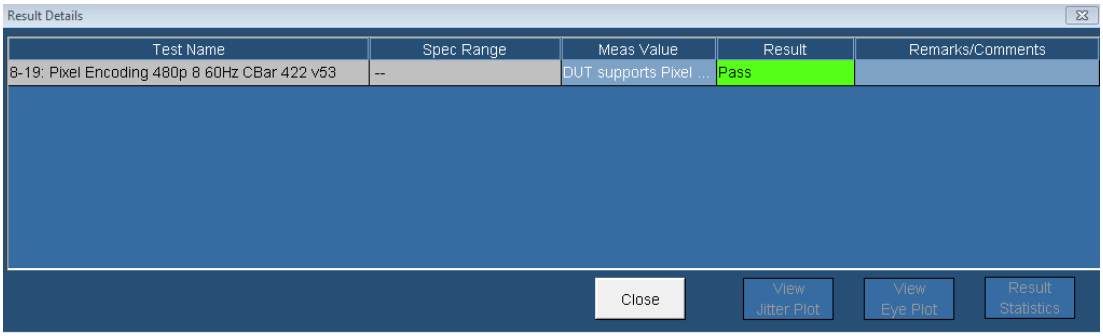
16. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected patterns)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the patterns supported by the DUT)
- Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs a 3D Video test. For the procedure on how to make this test, refer to the pixel encoding requirements test procedure (see page 342).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs.

1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer pixel encoding requirements test procedure (see page 165).
3. Refer to make connections for pixel encoding requirements (see page 165) for information on how to make connections.

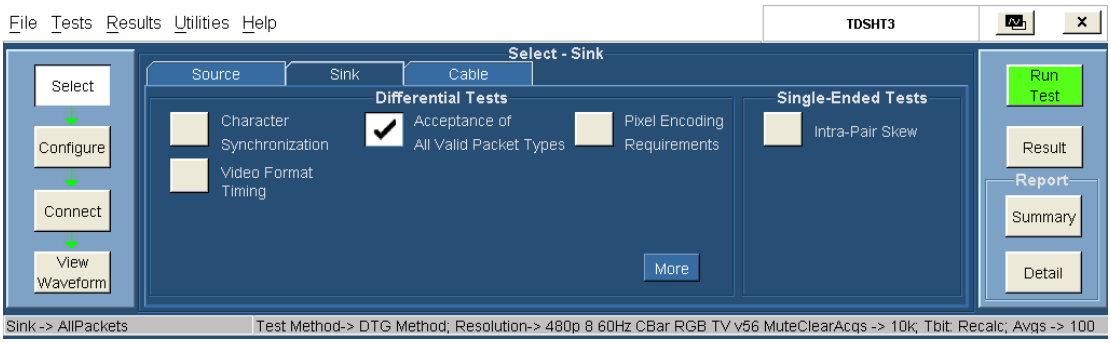
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

Test the Acceptance of All Valid Packets

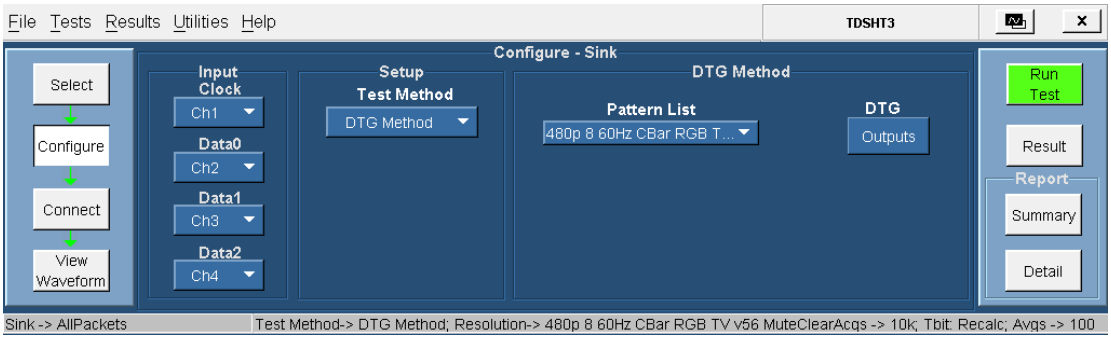
To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

To use the DDS test method, You will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

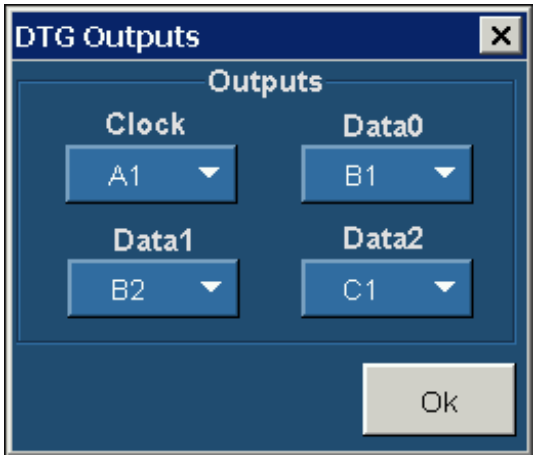
1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the All Video Packets check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.
4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).
6. In the DTG Method pane, do the following:



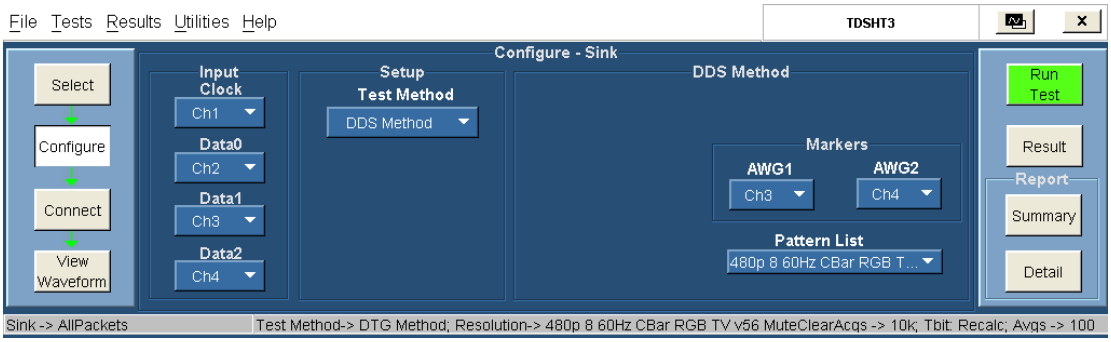
- Select the pattern(s) from the available list.
- The DTG Outputs dialog box for the DTG method has the following options:



  - Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
  - Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

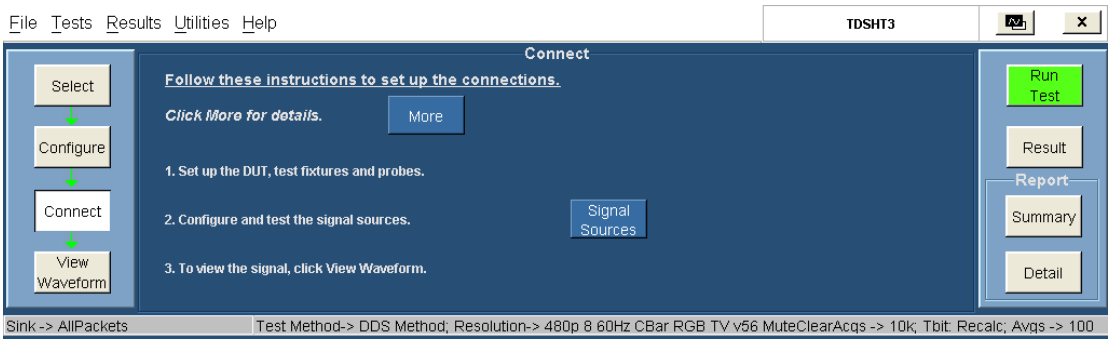
NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

In the DDS Method pane, do the following:



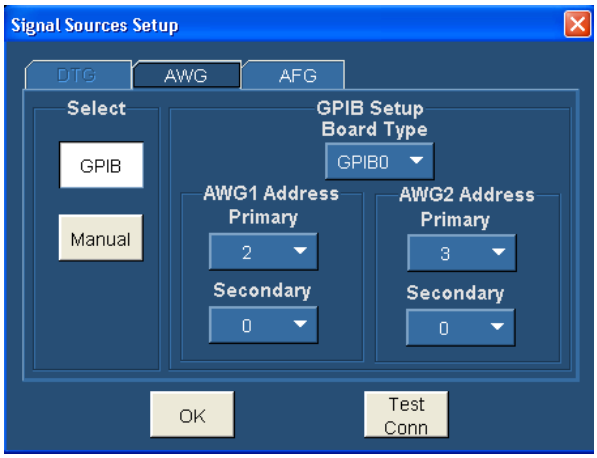
- Select one of the two: Custom 'Man with Sphere' 3D, or Standard Graybars 3D.
- In the Markers pane:
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
- Select the pattern(s) from the available list.

7. To connect the DUT, click **Tests > Connect**. Click here (see page 168) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

   The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



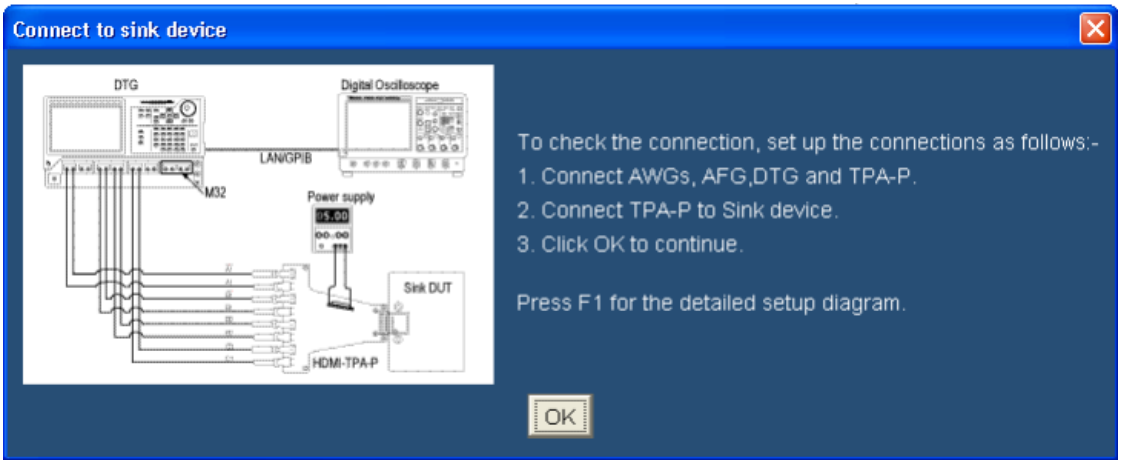
NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.
10. To test the connection and the GPIB configuration, click **Test Conn**.
11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the jitter tolerance test.

NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

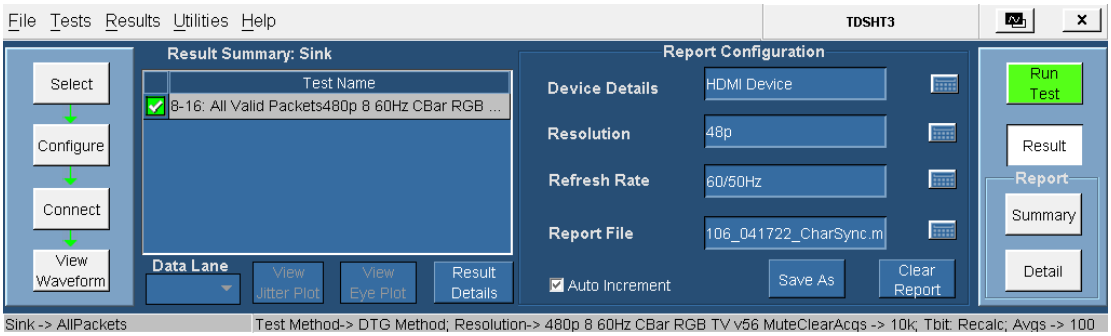
12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.
13. Follow the instructions in the Sink dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:



14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.

15. Follow the instructions in the dialog box.

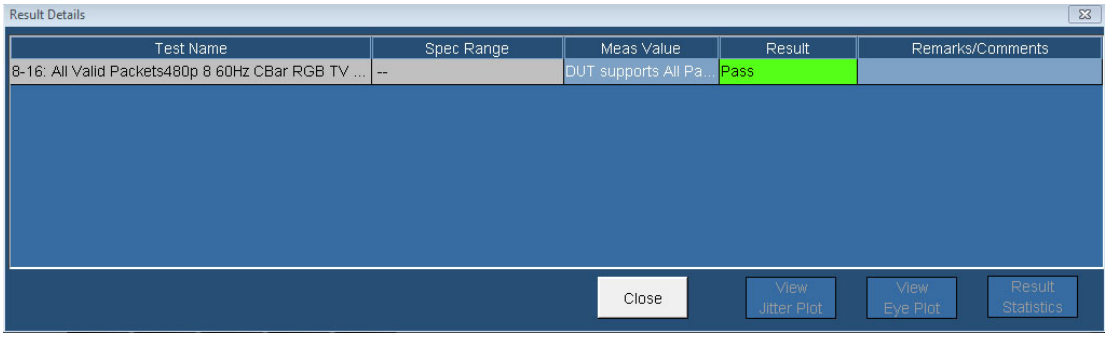
16. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected patterns)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the patterns supported by the DUT)
- Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs a 3D Video test. For the procedure on how to make this test, refer to the acceptance of all valid packets test procedure (see page 348).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs.

1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer acceptance of all valid packets test procedure (see page 348).
3. Refer to make connections for all valid packets (see page 168) for information on how to make connections.

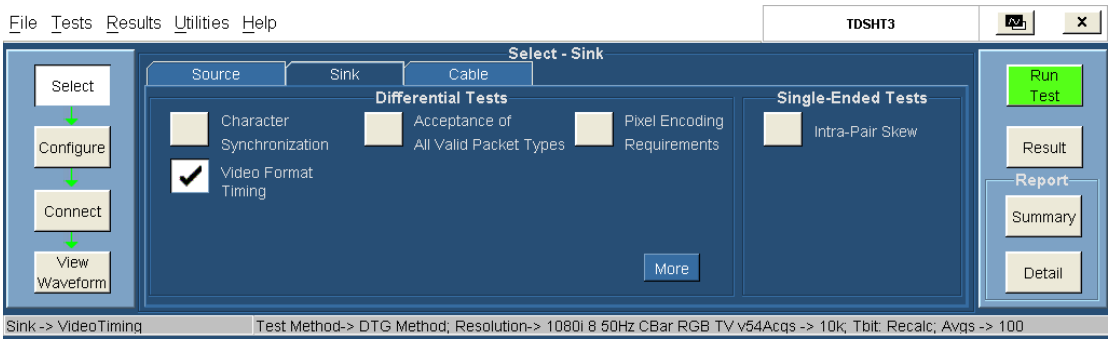
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

Test the Video Format Timing

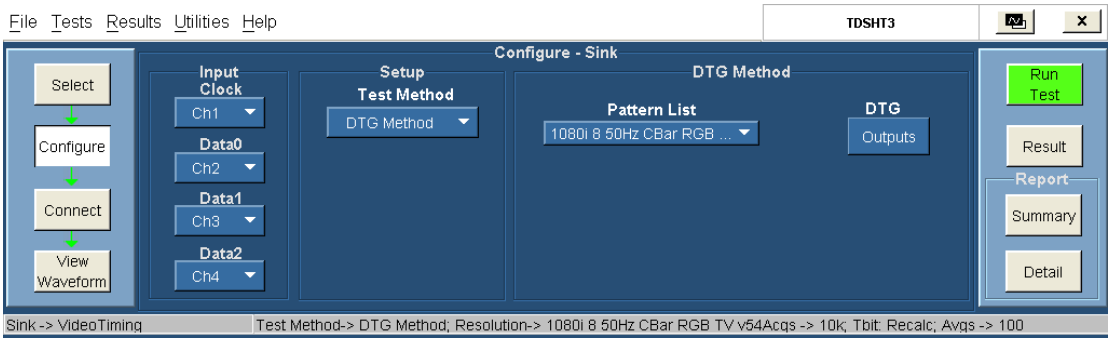
To use the DTG test method, you will need a supported oscilloscope, one digital timing generator (DTG), one differential probe, one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

To use the DDS test method, You will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

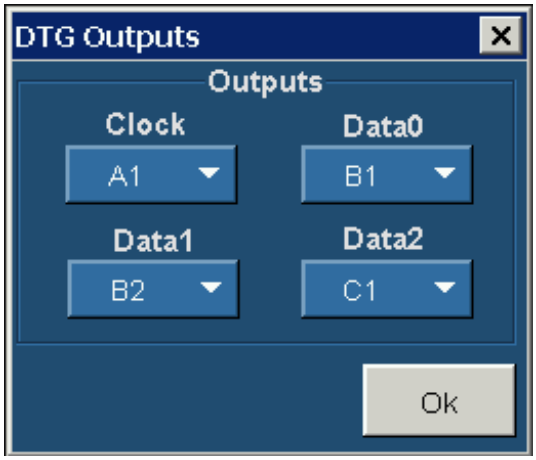
1. On the menu bar, click **Tests > Select > Sink**.
2. In the differential tests pane, select the Video Format Timing check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.
4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
5. In the Setup pane, select the appropriate test method from the available choices (DTG Method and DDS Method).
6. In the DTG Method pane, do the following:



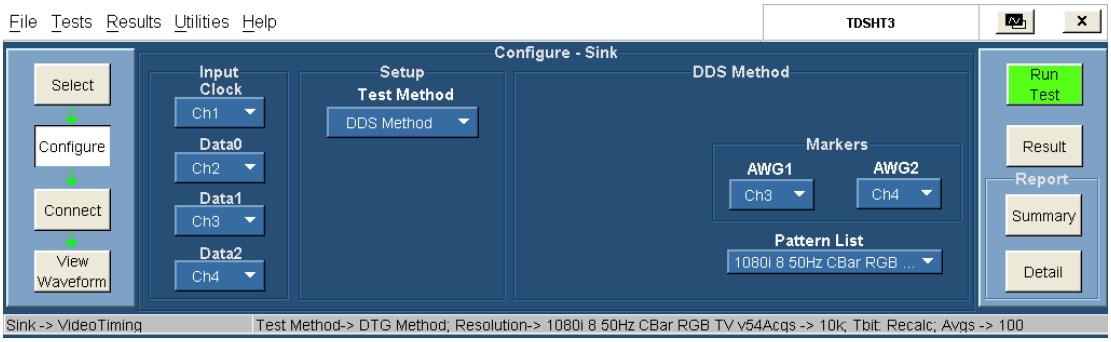
- Select the pattern(s) from the available list.
- The DTG Outputs dialog box for the DTG method has the following options:



  - Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
  - Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

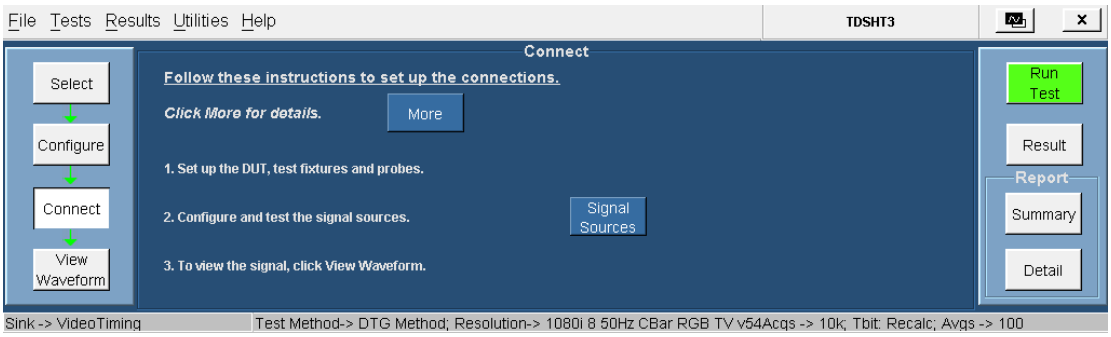
NOTE. *You cannot exit the dialog box unless each of the clock and data selections are unique.*

In the DDS Method pane, do the following:



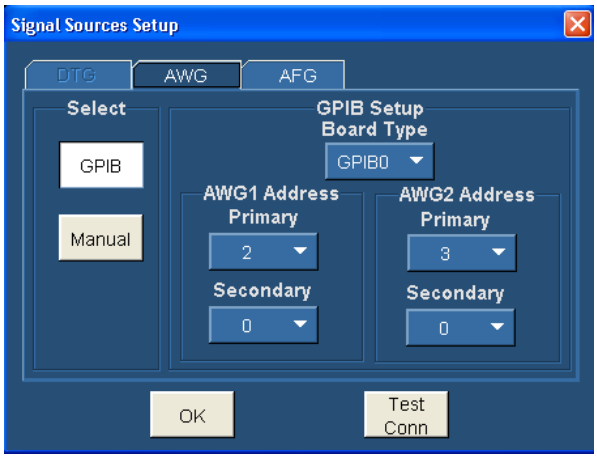
- Select one of the two: Custom 'Man with Sphere' 3D, or Standard Graybars 3D.
- In the Markers pane:
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
  - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
- Select the pattern(s) from the available list.

7. To connect the DUT, click **Tests > Connect**. Click here (see page 171) for information on how to make connections.



8. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

   The AWG tab has options to configure the Primary and Secondary Addresses of AWG1 and AWG2.



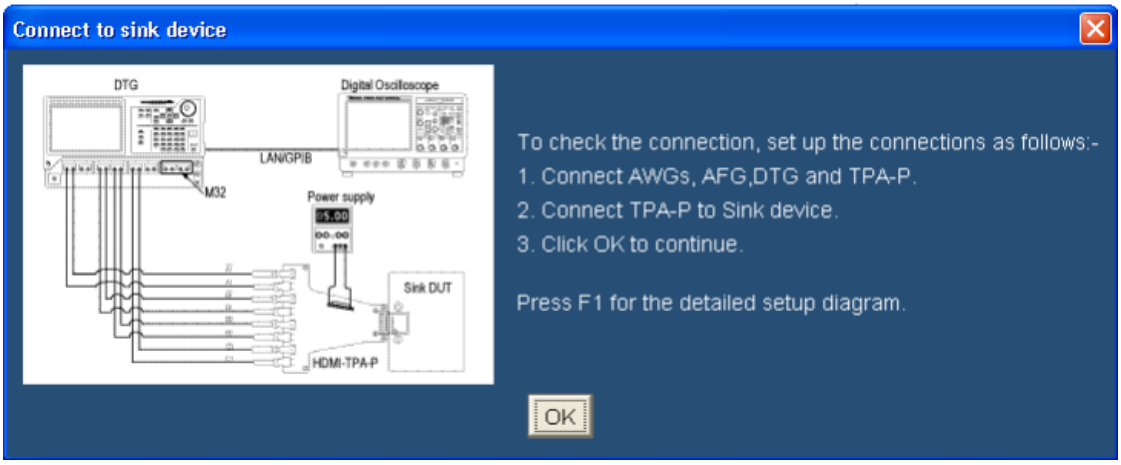
NOTE. *You cannot exit the dialog box unless each of the primary and secondary address selections are unique.*

NOTE. *The Manual test option is not available for the DDS method.*

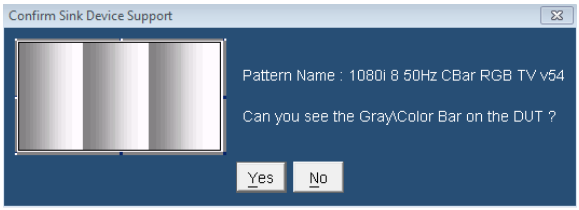
9. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.
10. To test the connection and the GPIB configuration, click **Test Conn**.
11. Because no signal is connected to the oscilloscope, you cannot view the waveform for the jitter tolerance test.

NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

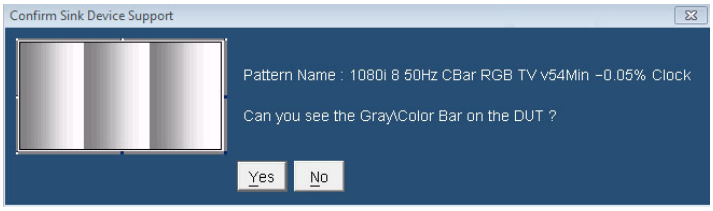
12. Click **Run Test**. The TDSHT3 Software sets up the oscilloscope and conducts the test.
13. Follow the instructions in the Sink dialog box. Click **OK**. The Connect Sink Device dialog box appears as follows:



14. Follow the instructions in the Connect Sink Device dialog box. Click **OK**. The test runs, displaying a progress indicator. The Confirm Sink Device Support dialog box appears.

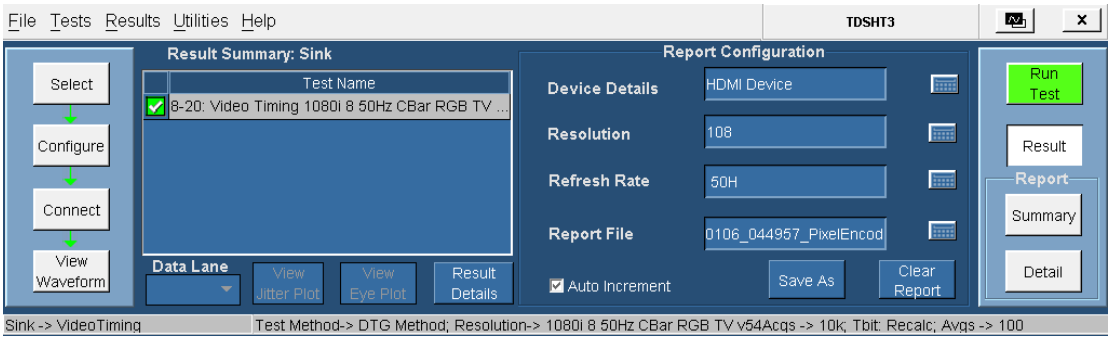


15. Follow the instructions in the dialog box. Click **Yes** in the screens that follow.



NOTE. *Clicking **No** would result in failure of the test.*

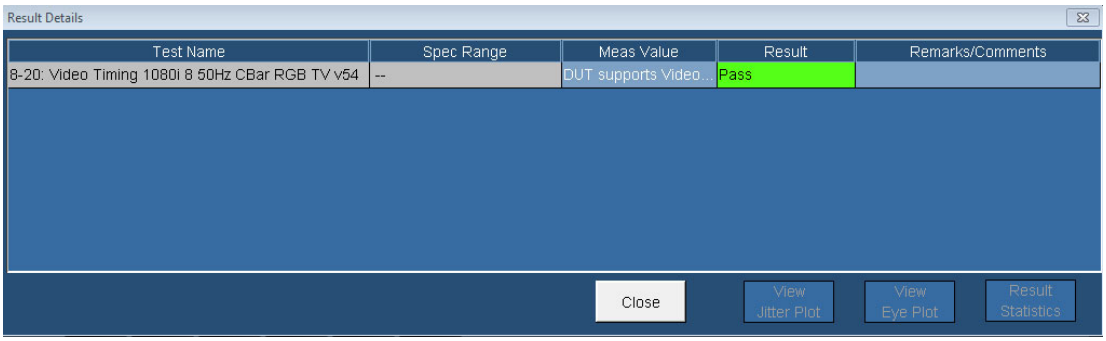
16. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name and the status (pass, fail, or error). To view the details of the results, click **Results Details**.

17. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

18. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected patterns)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the patterns supported by the DUT)
- Result (displays the status of the test as Pass, Fail, or Error)

Test Method

This sequence explains the actions that the software takes while it performs a 3D Video test. For the procedure on how to make this test, refer to the video format timing test procedure (see page 354).

For the DTG Method

1. Configure the DTG to output any sink-supported video format.
   - Load the pattern that contains repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2… during each video period.
   - Map all the logical channels to physical channels.
   - Run the DTG.
   - Enable all the output channels.
2. Verify that the DUT continues to support the signal without errors.
3. If the DUT fails to support the signal, it implies a Fail.

For the DDS Method

The DDS method does not require a DTG. The set up includes two AWGs.

1. Operate the Sink DUT to support the HDMI input signal.
2. To configure the parameters for this test, refer video format timing test procedure (see page 354).
3. Refer to make connections for video format timing (see page 171) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate pattern(s). The software prompts you to confirm the gray bars on the DUT.

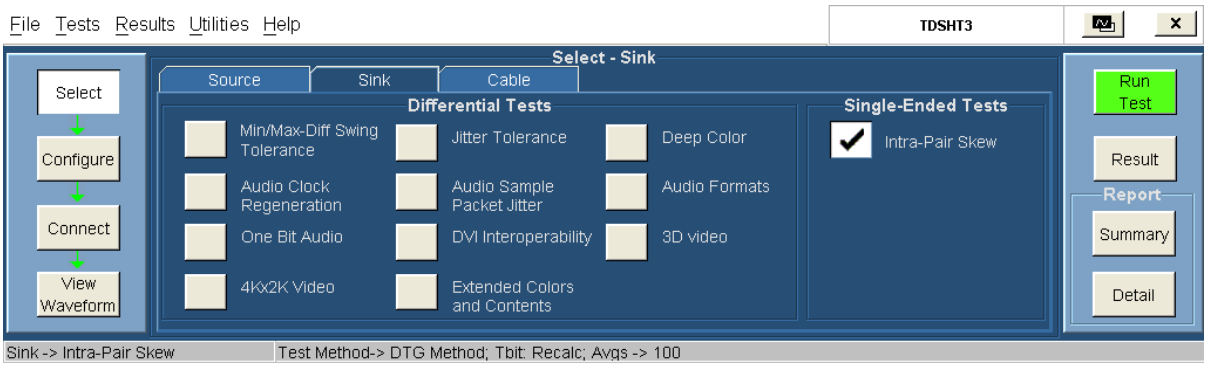
Test the Sink Intra-Pair Skew

This test allows you to confirm that the maximum allowed timing skew within each TMDS pair is supported by the Sink DUT.

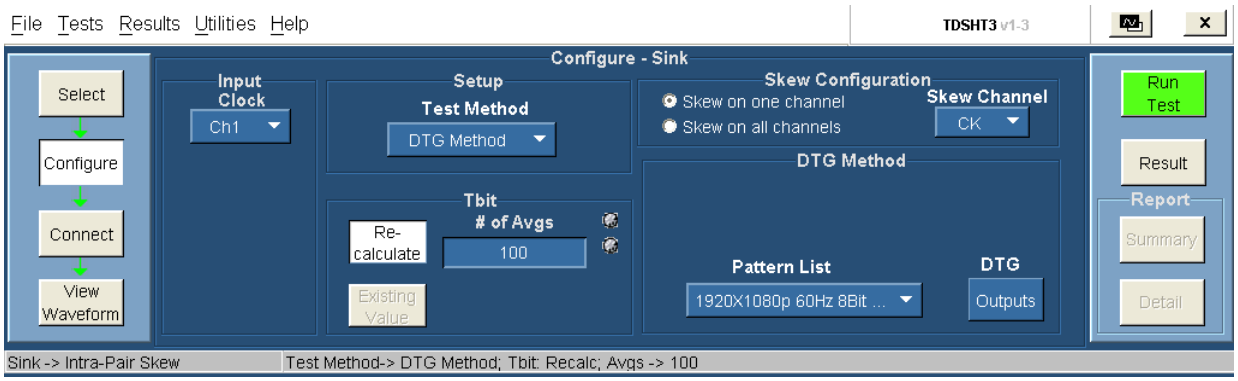
To use the DTG test method, you will need a supported oscilloscope, one differential probe, one cable emulator, one TPA-P-DI fixture, one digital timing generator (DTG), one DC power supply, eight SMA cables, one GPIB controller, and one TPA-P-TDR fixture.

To use the DDS test method, you will need a Digital Oscilloscope, two AWGs, one AFG, one differential probe, one TPA-P, one TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 0-6400 MHz low pass filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

1. On the menu bar, click **Tests > Select > Sink**.
2. In the single-ended tests pane, select the Intra-Pair Skew check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



NOTE. *The default configuration introduces skew on a single channel (Clock). If you want to calculate the intra-pair skew for all channels, connect the desired channels to A1 and A2. For example, to calculate the intra-pair skew of Data0, assign A1 to Data0 and B1 to Clock. Make appropriate changes in the test connections.*

4. In the Input pane, set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
5. Select the appropriate test method from the available choices (DTG Method and DDS Method).
6. In the Tbit pane, do the following:
   - Enter the desired number of periods that are considered to calculate Tbit. The default value is 100.
   - Click **Re-calculate** to recalculate the Tbit value.
   - Click **Existing Value** to use the previously calculated Tbit value.

7. In the Skew Configuration pane, do the following:

   - Select **Skew On All Channels** to set the skew on all the channels to introduce skew on Clock, D0, D1, and D2. All the four DTGM30 modules are required for this option.

     Select **Skew On One Channel** to set the skew on one channel.

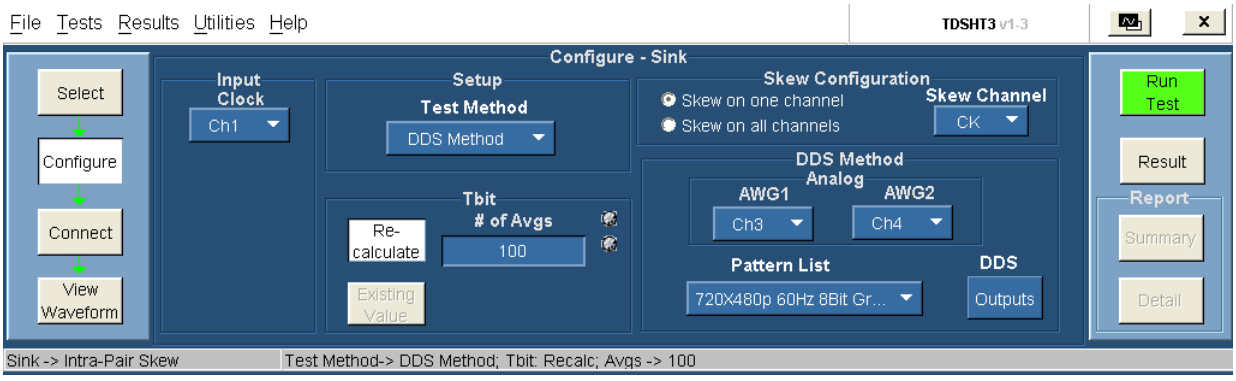
   NOTE. *The four DTGM modules can be connected as follows: Clock +ve to A1 and Clock –ve to A2, D0 +ve to B1 and D0 –ve to B2, D1 +ve to C1 and D1 –ve to C2, D2 +ve to D1 and D2 –ve to D2.*

   - Select the skew channel in which you want to introduce the skew. You can select from the available choices (Ch1, Ch2, Ch3, and Ch4).

8. If the selected test method is DTG, do the following:

   - Select the DTG pattern file from the drop-down list.
   - Click **Outputs** to display a dialog box where you can set Clock, Data0, Data1, and Data2 outputs.

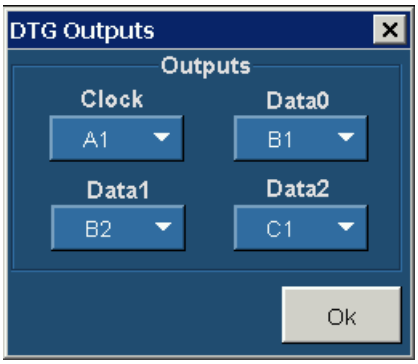
   If the selected test method is DDS, do the following:



   - In the Analog pane:
     - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
     - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
   - Select the DDS pattern file from the drop-down list.
   - Click **Outputs** to display the AWG Output dialog box.

   NOTE. *You cannot configure the AWG Outputs dialog box.*

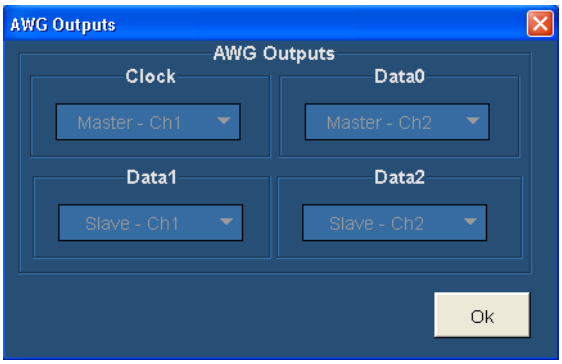
9. In the DTG Method pane, the Outputs dialog box has the following options:



- Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
- Data0, Data1, and Data2 (allows you to configure the corresponding data outputs). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

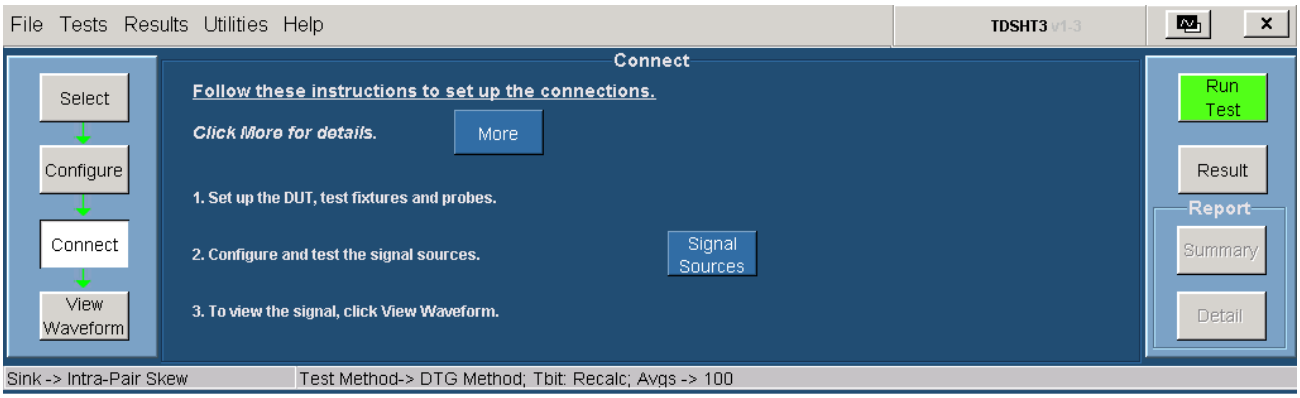
NOTE. *You cannot exit the dialog box unless each of the clock and data values are unique.*

In the DDS Method pane, the AWG Outputs dialog box has the following configurations:

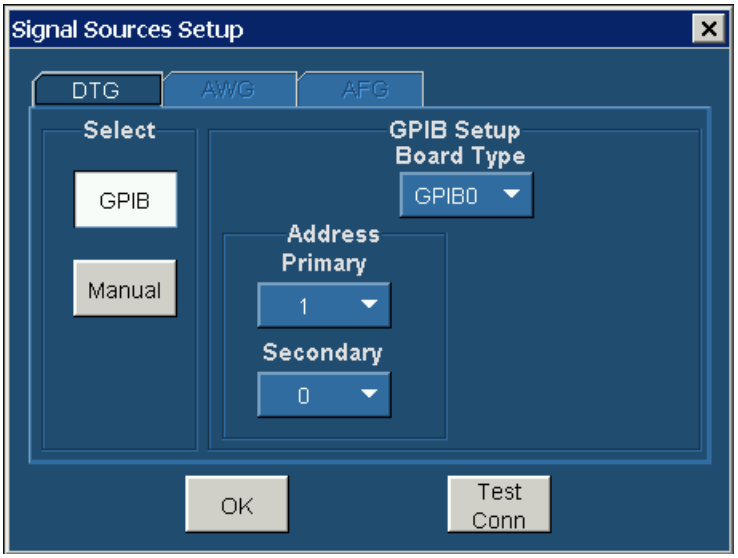


NOTE. *You cannot configure the AWG Outputs dialog box.*

10. To connect the DUT, click **Tests > Connect**. Click here (see page 174) for information on how to make connections.



11. To configure and test the GPIB connection, click **Signal Sources**. The Signal Sources Setup dialog box appears.

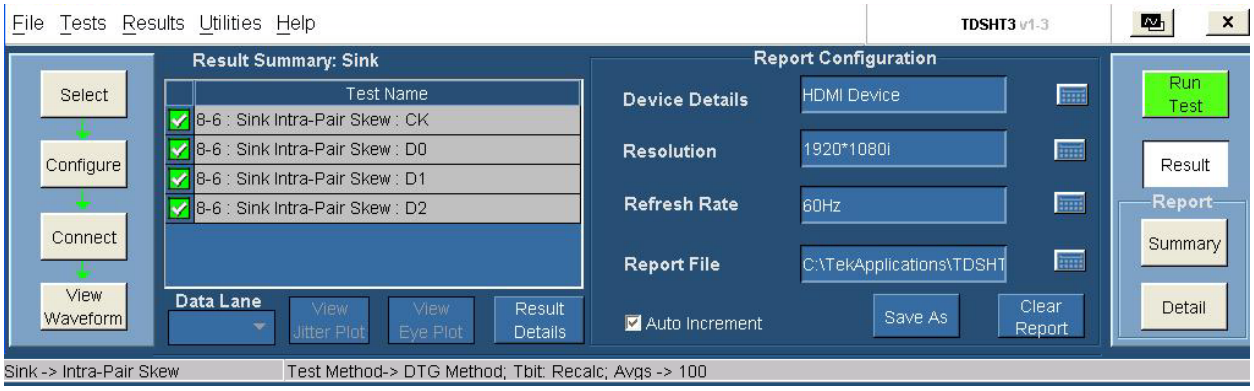


12. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.

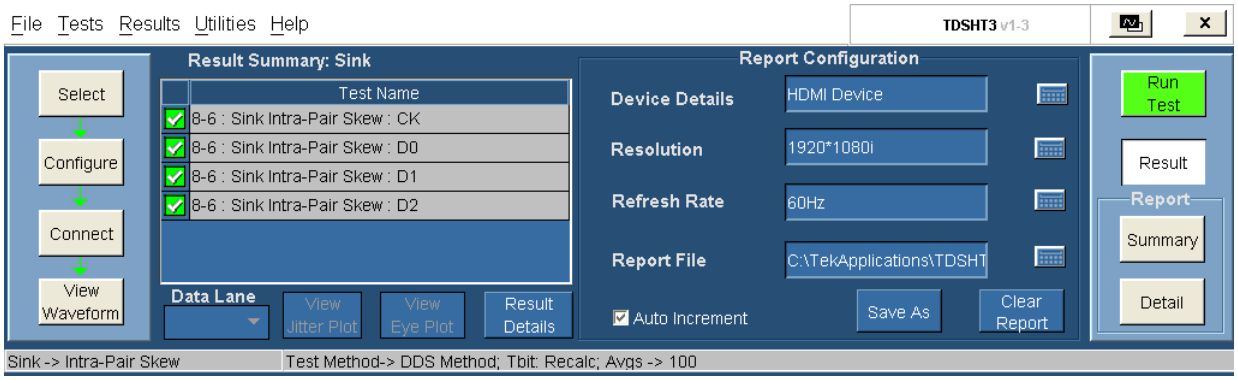
13. To test the connection and the GPIB configuration, click **Test Conn**.

14. Click **Run Test** to perform the test. The TDSHT3 Software sets up the oscilloscope and conducts the test. Follow the instructions in the dialog box. Depending on your answer, a series of dialog boxes may prompt you for your input.

15. If you successfully run the test, the software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The result summary for the DDS test method is as follows:

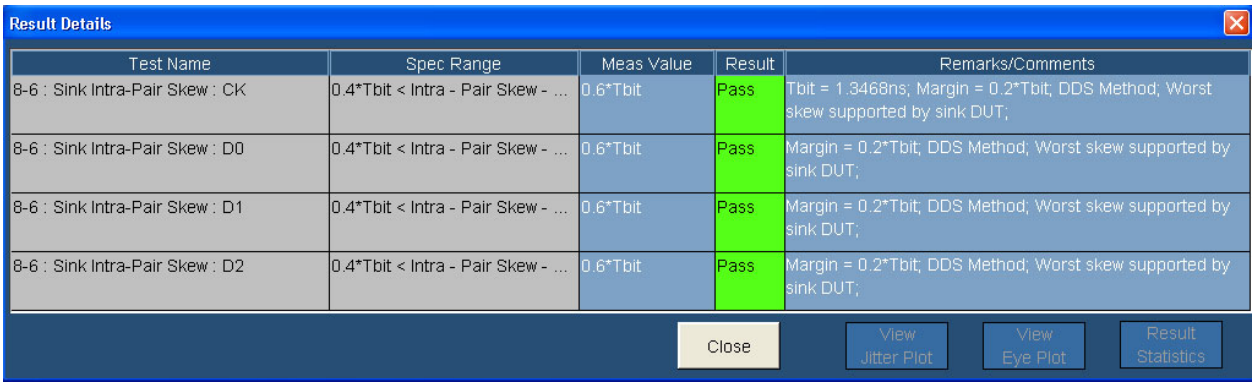


The results summary lists the test name and their status (pass, fail, or error). To view the details of the results, click **Results Details**.

16. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

17. In the result summary pane, click **Result Details**. The result details pane displays the following fields.

The result details for the DDS test method are as follows:



- Test Name (displays the test id, test name, and selected names)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the measured value)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the relevant details, such as Tbit, Vswing, and Margin. If the test could not be run, this field displays an error code (see page 397).

Test Method

For the DTG Method

This sequence explains the actions that the software takes while it performs an intra-pair skew test. For the procedure on how to make this test, refer intra-pair skew test procedure (see page 360).

1. Configure the DTG to output any sink-supported video format that uses the maximum sink-supported pixel clock frequency. If multiple formats are available, a native format is preferred.
2. Calculate Tbit by using the differential clock.
3. For each of the TMDS Clock and Data pairs that act as the tested pair:
   - Set the delay for all outputs to 0 ns. Disable “Differential Timing Offset” if it is previously enabled.
   - Move the TMDS “+” signal of the tested pair to DTG output module A, 1+.
   - Move the TMDS “–” signal of the tested pair to DTG output module A, 2+.
   - Change the DTG configuration to output the pattern for the tested TMDS channel on module A, 1.

4. When Skew on all four channels option is selected, the skew on all the four channels will be calculated based on the following conditions:
   - All four modules of the DTG must be DTGM30 modules. The test checks for the modules and throws an error if they are not from the DTGM30.
   - The configuration to run the test are A1-Clock, B1-Data 0, C1-Data 1, and D1-Data 2. If the test fails on any of the channels the skew will be inserted individually on the channels to find the channel that has failed the test.
5. In the DTG "Timing", set the tested channel (connected to 1A1) and enable "Differential Timing Offset."
6. Set the delay value in the differential timing offset to approximately ($0.1*T_{BIT}$). This corresponds to the initial intra-pair skew value.
7. Increase the skew (Differential Timing Offset) by steps of less than or equal to ($0.1*T_{BIT}$), until the Sink DUT outputs errors or until reaching either ($0.6*T_{BIT}$) or 1 nsec.
8. If errors are seen on DUT, then:
   - Reduce the skew one step, so that the Sink DUT outputs no errors.
   - If intra-pair skew is less than ($0.4*T_{BIT}$), it implies Fail.

For the DDS Method

1. Operate the Sink DUT to support the HDMI input signal.
2. For the procedure on how to make this test, refer intra-pair skew test procedure (see page 360).
3. Refer to the make connections for sink intra-pair skew (see page 180) for information on how to make connections.
4. Check the connection of the AWGs and AFG from TDSHT3.
5. Run the test. The software loads the appropriate patterns with zero skew patterns. The software prompts you to confirm the gray bars on the DUT.
6. You are prompted to connect the Clock output of the TPA-R to the configured oscilloscope channel to measure the T-bit.
7. Connect the TPA-P to the Sink DUT. The software prompts you to confirm the gray bars on the DUT.
8. Once this is confirmed, the appropriate skew signals are generated in steps of 0.1 Tbit from 0.0 Tbit as per the CTS. You are prompted to confirm for the gray bar on the DUT for each step.
9. The test fails if the sink outputs errors at any time.

NOTE. *Using a manual DDS test method is not recommended because the software performs the Sink Intra-Pair Skew test automatically and effectively.*

Test the Cable Eye Diagram (Passive and Active)

This test lets you confirm that the cable assembly outputs a compliant data eye. Check the input test signal at TP1 and verify the output of the cable for compliance at TP2.

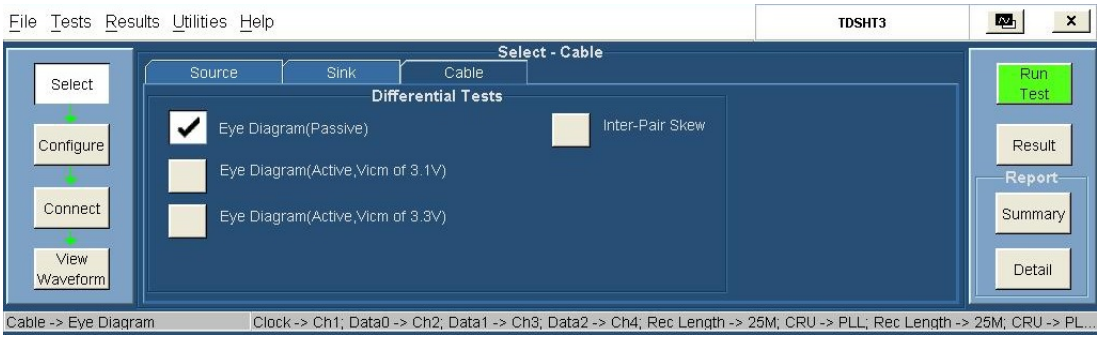
NOTE. *The passive and active Cable Eye Diagram tests use the same connection, test, and waveform view procedures.*

The signal degradation of typical passive copper cables increases with the frequency and the length of the cable. To recover data from such cables, the TDSHT3 automatically applies the reference cable equalizer (as specified in the HDMI specifications 1.4a) to the eye diagram measurement when the clock frequency is more than 165 MHz.

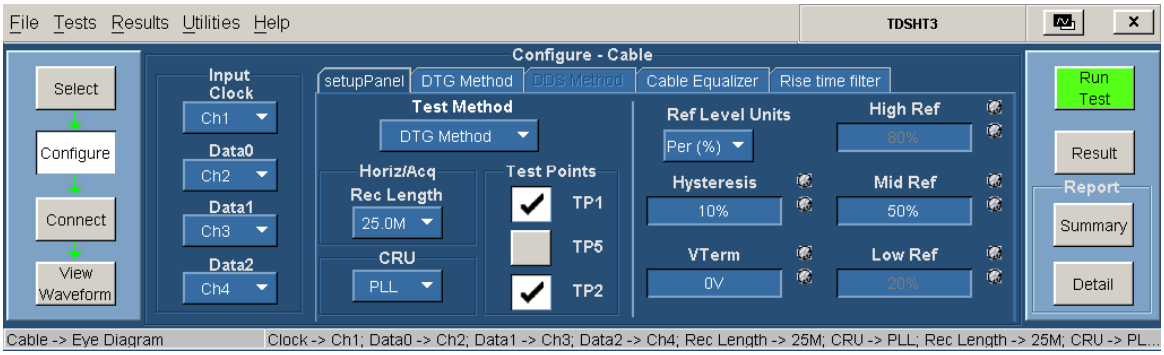
To use the DTG test method, you will need a Digital Oscilloscope, two/four differential probes, one DTG, one AFG, one GPIB controller, one DC power supply 3.3 V, eight SMA cables, one TPA-R-DI fixture, and one TPA-R-TDR fixture.

To use the DDS test method, you will need a Digital Oscilloscope, two AWGs, one AFG, two/four differential probes, one TPA-P, two TPA-R, and one accessory kit (consisting of eight matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter). For Type-E cable emulator, use the Type-E fixtures (one TF-HDMIE-TPA-P and two TF-HDMIE-TPA-R) in place of Type-A and Type-C fixtures.

1. On the menu bar, click **Tests > Select > Cable**.
2. In the differential tests pane, select the Eye Diagram check box for the type of test to perform.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard or the general purpose knob on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



4. In the Input pane, do the following:

   - Set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
   - Set the Input Data0, Data1, and Data2 to the channels that you will use for the corresponding HDMI data inputs. Select from the available choices (Ch1, Ch2, Ch3, Ch4, and Not Conn).

5. In the **Setup** tab, do the following:

   - Select the appropriate test method from the available choices (DTG Method and DDS Method).

   In the Horiz/Acq pane:

   - Enter the desired record length value for the eye tests in the Rec Length box.
   - Configure the Clock Recovery Unit in the CRU pane. Select from the available choices (PLL, Raw, and Ideal). The default value is first order PLL and is used for compliance testing. Raw and Ideal are used for analysis.

   In the Test Points pane (for the DTG and DDS methods):

   - Feed the worst possible compliant signal at TP1. By default, the TP1 check box is selected. TP1 represents the first test point.
   - The worst possible compliant signal fed at TP1 is transmitted through the cable. The same signal is tested at TP2 with the TP2 eye mask. By default, the TP2 check box is selected. TP2 represents the second test point.

For the DDS Method using the Type-E cable emulator, you can select only two test points at a time (TP1 and TP2, TP1 and TP5, or TP5 and TP2).

- If you have selected TP1 and TP2, do the following:
  - Feed the worst possible compliant signal at TP1.
  - The worst possible compliant signal fed at TP1 is transmitted through the cable. Test the same signal at TP2 with the TP2 eye mask. TP2 represents the second test point.
- If you have selected TP1 and TP5 (applicable for 74 MHz Type-E), do the following:
  - Feed the worst possible compliant signal at TP1.
  - The worst possible compliant signal fed at TP1 is transmitted through the Type-E cable. Test the same signal at TP5 with the TP5 eye mask.
- If you have selected TP5 and TP2 (applicable for 74 MHz Type-E), do the following:
  - Feed the worst possible compliant signal at TP5.
  - The worst possible compliant signal fed at TP5 is transmitted through the cable. The same signal is tested at TP2 with the TP2 eye mask.
- Set the reference level units to either Per (%) or Abs.

  Per (%) indicates that the reference levels are a percentage of the Vswing value.

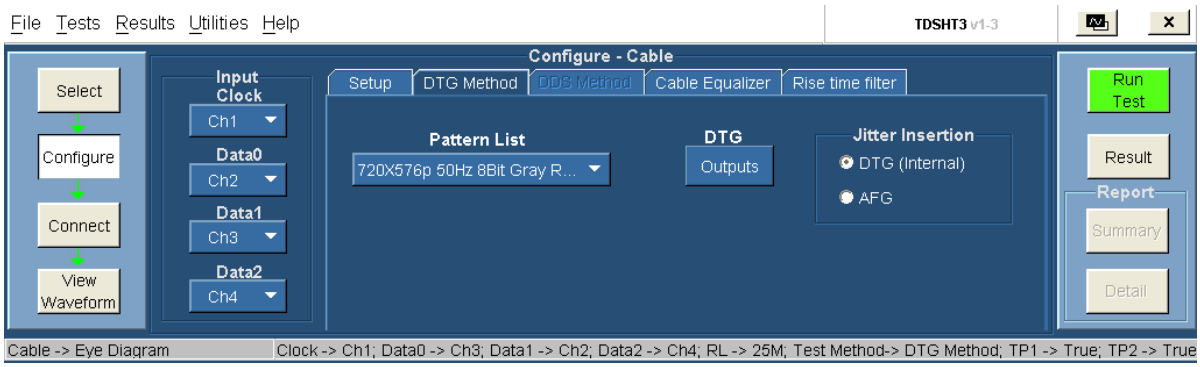
  Abs indicates that the reference levels are absolute voltage values.

  The default setting is Per (%).
- In the Hysteresis box, enter the desired hysteresis percent value. The range is from 0% to 25% and default is 10%.
- In the High box, the required high reference voltage value is set for the test. The default value is 80%.
- In the Mid Ref box, enter the desired mid reference voltage value. The range is from 25% to 75% and default is 50%.
- In the Low box, the required low reference voltage value is set for the test. The default value is 20%.
- In the Vterm box, enter the probe termination voltage. The default values are:

  Passive cable: VTerm = 0 V

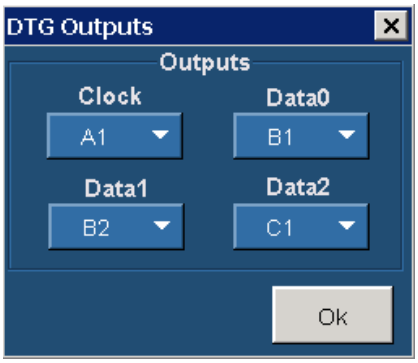
  Active cable: Vterm = 3.3 V

6. In the **DTG Method** tab, do the following:



- Select the DTG pattern file from the drop-down list.
- Click **Outputs** to display a dialog box where you can set Clock, Data0, Data1, and Data2 outputs.
- In the Jitter Insertion pane, do the following:
  - Select DTG to insert jitter using a DTG.
  - Select AFG to insert jitter using an AFG.

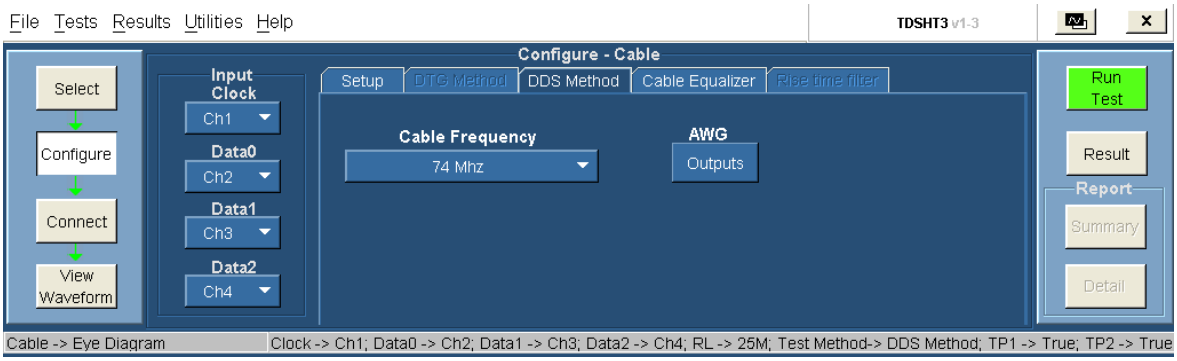
7. In the DTG Outputs dialog box, you have the following options:



- Clock (allows you to configure the clock output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).
- Data0, Data1, and Data2 (allows you to configure the corresponding data output). Select from the available choices (A1, A2, B1, B2, C1, C2, D1, and D2).

NOTE. *You cannot exit the dialog box unless each of the clock and data values are unique.*

8. In the **DDS Method** tab, do the following:



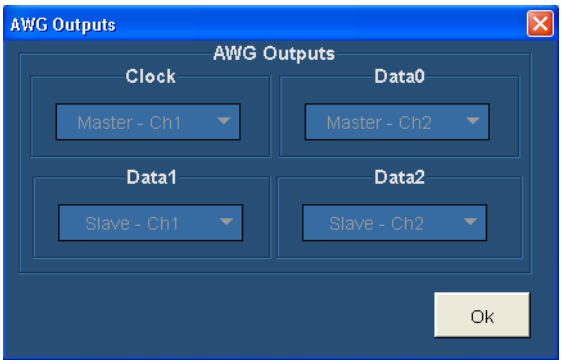
- Select the cable frequency from the drop-down list.

  Depending on the selected cable frequency, the following check box is enabled in the Cable Equalizer tab:

  - For 74 MHz and 165 MHz cable frequencies, **Do not apply equalizer for Clock and Data** check box is selected.
  - For 340 MHz cable frequency, **Use internal coefficients** check box is selected.
  - For 74 MHz Type-E cable frequency, **Use internal coefficients** check box is selected but 2.3 dB cable equalizer is used.

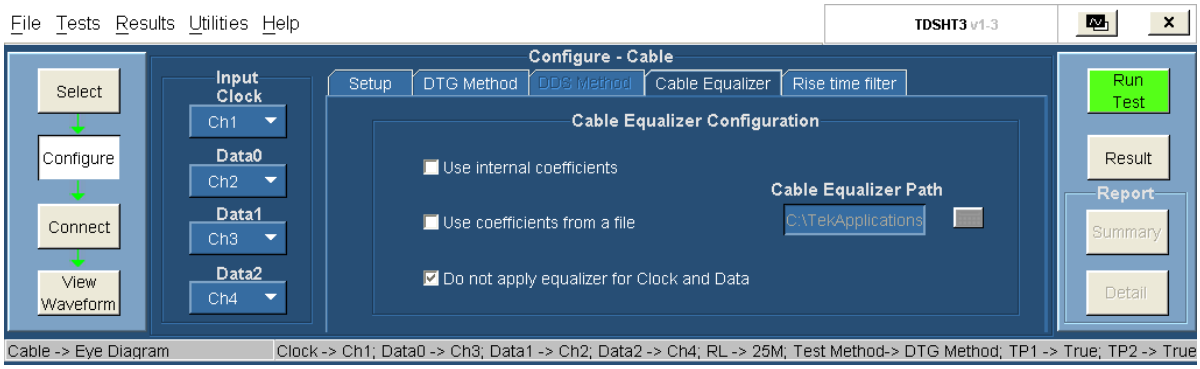
- Click **Outputs** to display the AWG dialog box.

9. In the AWG Outputs dialog box, you have the following configurations:



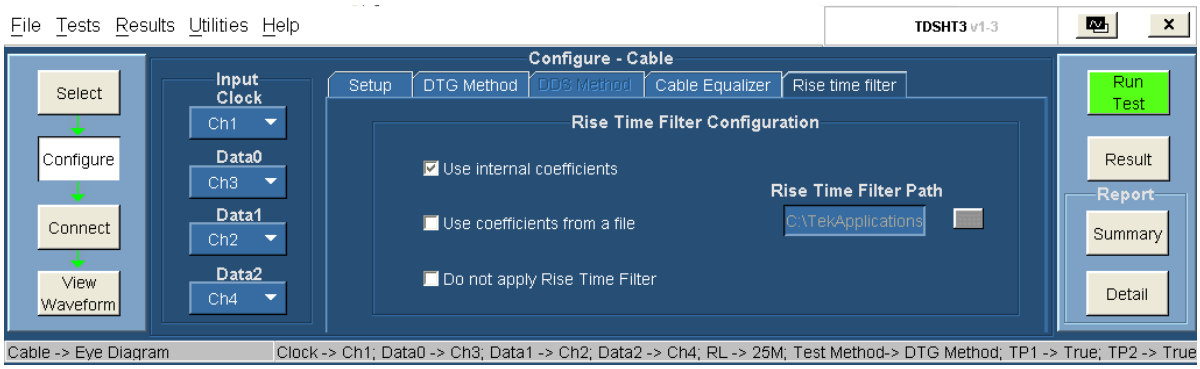
NOTE. *You cannot configure the AWG Outputs dialog box.*

10. In the **Cable Equalizer** Configuration tab, do the following:



- Select the Use Internal coefficients check box to use the internal coefficients that are already available (these coefficients are in accordance with the CTS). This is applicable for frequencies above 165 MHz.
- Select the Use coefficients from a file check box to use the coefficients from a file. Browse the cable equalizer file from the Cable Equalization Path option.
- Select Do not apply equalizer for Clock and Data check box if you do not want to apply cable equalization. This is applicable for frequencies below 165 MHz.

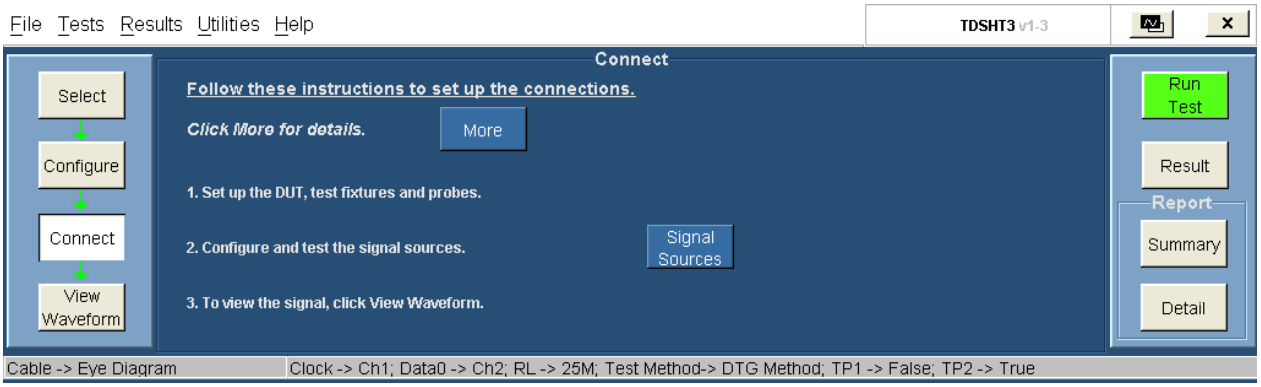
11. In the **Rise Time Filter** Configuration tab, do the following.



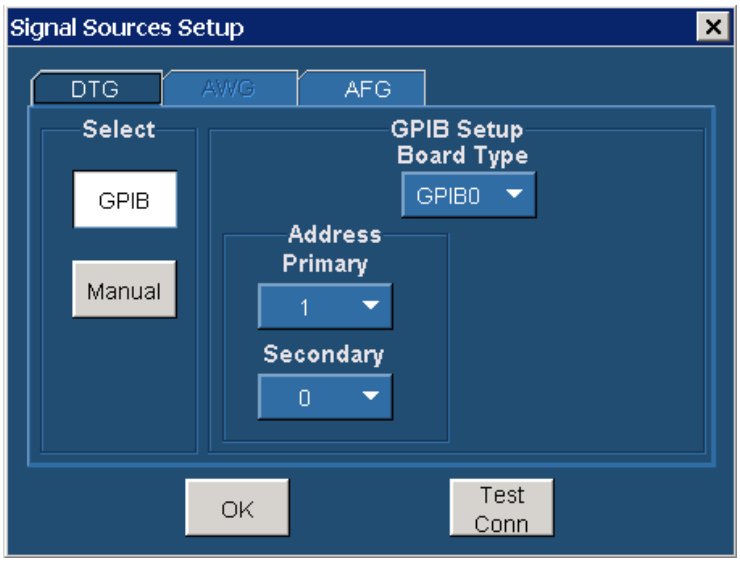
- Select the Use Internal coefficients check box to use the internal coefficients that are already available (these coefficients are in accordance with the CTS).
- Select the Use coefficients from a file check box to use the coefficients from a file. Browse the rise time filter file from the Rise Time Filter Path.
- Select Do not apply rise time filter for Clock and Data check box if you do not want to use the rise time filter.

NOTE. *You cannot configure the Rise Time Filter for the DDS method because the effect is emulated by the software.*

12. To connect the DUT, click **Tests > Connect**. Click here (see page 188) for information on how to make connections.



13. To configure and test the GPIB connection, click **Signal Sources**.



14. In the select pane, click **GPIB**. Configure the appropriate GPIB board number. Click here (see page 29) for more information.

15. To test the connection and the GPIB configuration, click **Test Conn**.

16. Because no signal is connected to the oscilloscope, you cannot view the waveform for the eye diagram test.

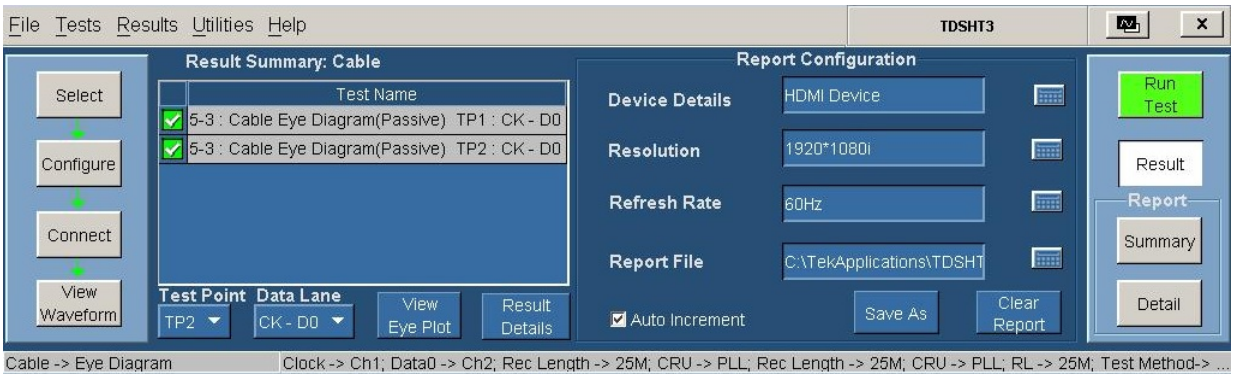
NOTE. *To run the test successfully, ensure that the Bus Timing parameter is set to 2 µsec on your GPIB board configuration.* *Click here (see page 38)* *for more information.*

17. Click **Run Test** to perform the test. The TDSHT3 Software sets up the oscilloscope and the test runs, displaying a progress indicator.

18. In the GPIB mode, the application automatically adjusts the jitter amplitude on DTG and displays the measured jitter value. Follow the on-screen instructions to enable you to re-adjust the jitter value. The software creates a worst eye and asks you to verify the worst eye. Follow the on-screen instructions. Depending on your answer, a series of dialog boxes may prompt you for your input.

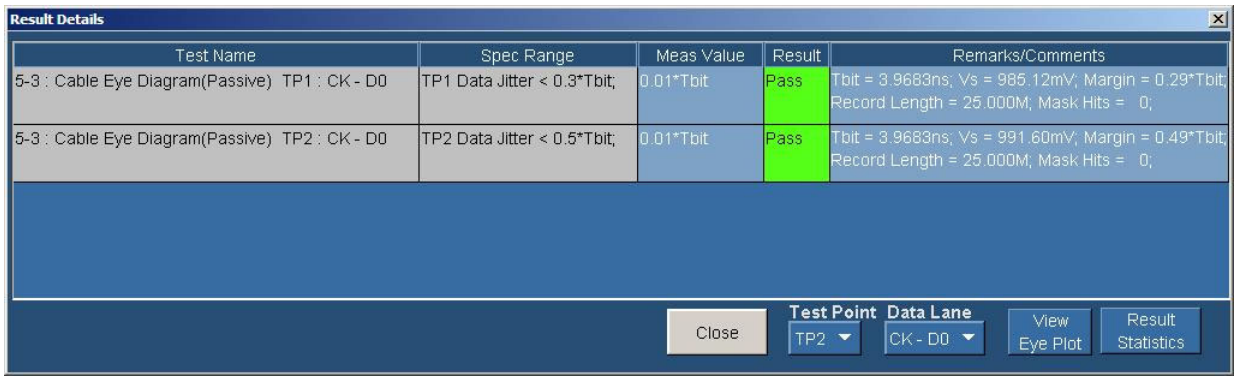
19. If you have run the test successfully, the software makes the results available automatically and displays the eye diagram plot and the clock jitter plot for both TP1 and TP2. For more information on the plots, refer the section on the source eye diagram test and the source clock jitter test. You can also view both the result summary of the test and the report configuration in the result pane as shown in the following figure:

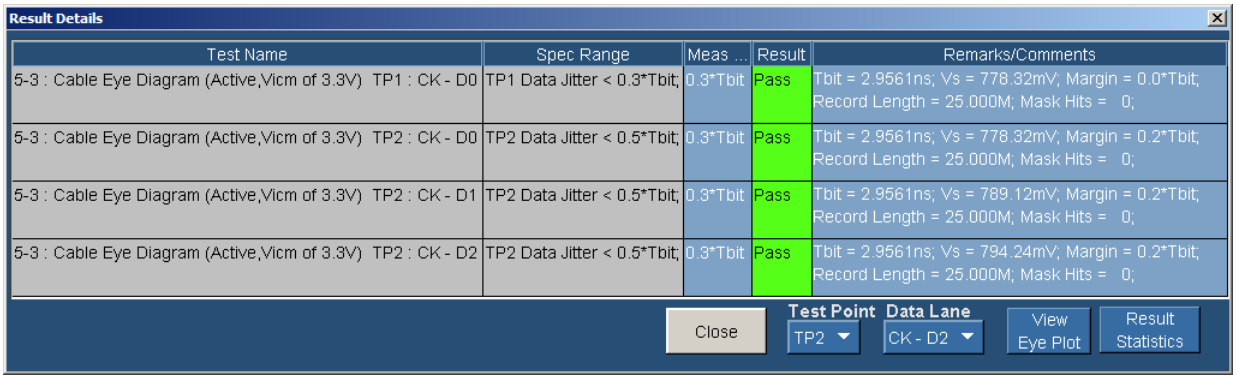
NOTE. *You can set a default report file parameters to identify and generate the report automatically.* *Click here (see page 49) for more information.*



The Result Summary pane lists the tests and each test's status (pass, fail, or error). Buttons are available to view test point, data lane, eye plot information, and test result details.

20. Click **Result Details** to view the Result Details pane to display more information on the test results. The following are examples of passive and active test result details:





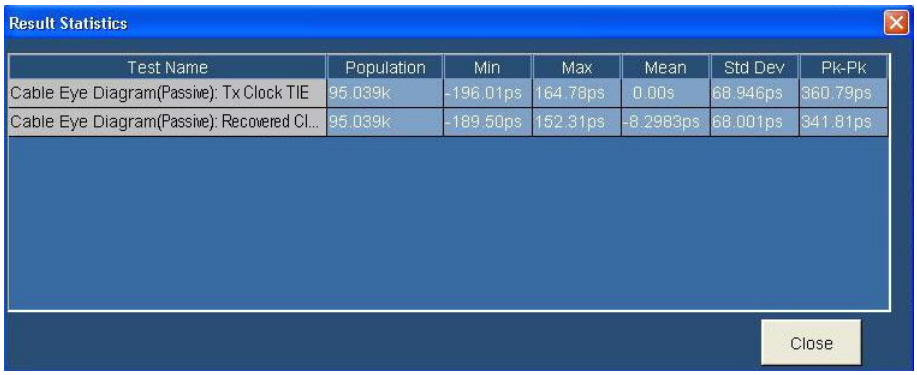
The Result Details pane displays the following fields.

- Test Name (displays the test id, test name, test point, and selected lanes)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the measured value in mV)
- Result (displays the test status: Pass, Fail, or Error)
- Remarks/Comments (displays the relevant details, such as Vswing and Margin). If the test could not be run, this field displays an error code (see page 397).
- Test Point (allows you to check the input test signal at TP1/TP5 and verify the output of the cable for compliance at TP2/TP5. From the Test Point list, select either TP1/TP5 or TP2/TP5 to view the respective details)
- Data Lane (displays the eye diagram plot of the selected data lane pair)

NOTE. *This option is applicable only for TP2/TP5.*

- View Eye Plot (allows you to view the eye plot for the selected test point and data lane for the eye diagram test)
- Result Statistics (displays statistics based on the tests)

21. In the Result Details dialog box, click **Result Statistics** to display statistics based on the tests. Click here (see page 50) for more information.



Test Method

This sequence explains the actions that the software takes while it performs an eye diagram test. For the procedure on how to make this test, refer eye diagram test procedure (see page 368).

Cable Equalizer

The signal degradation of typical passive copper cables increases with the frequency and the length of the cable. To recover data from such cables, TDSHT3 Software applies the reference cable equalizer (as specified in the HDMI specification 1.4a) automatically to the cable eye diagram measurement when the clock frequency is more than 165 MHz. For the Type-E cable, a 2.3 dB equalizer is applied at 74.25 MHz.

For the DTG Method

1. Configure the DTG to output a video format corresponding to the specified bandwidth of the cable. If no bandwidth is specified, configure the DTG to output 1920 x 1080i @ 60 Hz (74.25 MHz pixel clock).
   - Load the appropriate pattern file.
   - Set the logical channel to physical channel mapping.
   - Run the pattern.
   - Enable all the DTG outputs.
2. Configure the DTG to output worst-case eye as follows:
   - Adjust jitter on TMDS_CLOCK pair to output 0.4 ns at 500 KHz (worst jitter permitted at (TP1 = $0.3*T_{BIT}$) at 75 MHz).
   - Adjust the output swing voltage to 500 mV for every TMDS single-ended signal.
   - Using jitter/eye analyzer, measure the TMDS_CLOCK jitter and eye diagram of all the three TMDS_DATA pairs.
   - Repeat and readjust as necessary to create the worst-case eye diagram.

3. Set up the oscilloscope as follows:
   - Set the memory length to at least 25 M points.
   - Set the single-shot trigger at the rising edge of TMDS Clock (50 percent).
   - Set the sample rate to ≥ 10 GS/s based on the oscilloscope.
   - Adjust the vertical scale to accommodate the waveform in six vertical divisions.
4. Perform software clock recovery as follows:
   - Set the reference level to 50 percent of the clock and hysteresis to 10 percent of V_{SWING}.
   - Calculate the Software CRU filter as follows.

     $H(s) = 1/(1+s\tau)$, where $\tau = 40$ nsec.
5. Connect the cable DUT between the TPA-R-TDR and TPA-R-DI adapters.
6. Measure jitter at TPA-R-DI (the procedure is the same as that for the source eye measurement).
   - If the data jitter is greater than 0.67 ns (= $0.5*T_{BIT}$ at 75 MHz), it implies a Fail.
   - Calculate the measurement BOX vertical setting as follows:
     - $V_C = (V_H+VL)/2 = \pm 5$ mV
   - Test the eye diagram with sink minimum eye mask. If any of the points violate the mask, it implies Fail.
7. Adjust the DTG swing voltage to (V_H, V_L) = (3.3 V, 2.9 V) without jitter (clock jitter should remain at the worst case input condition).
8. Measure the eye mask on all the TMDS_DATA channels at CTP2.
9. If any of the measured eyes do not meet the sink minimum eye mask, it implies a Fail.

For the DDS Method

In the Cable Equalizer tab, select one of the cable frequencies (74 MHz, 165 MHz, 340 MHz, and 74 MHz Type-E). When you select the cable frequency:

- Appropriate test patterns are loaded.
- Relevant cable equalizer is enabled as required.
- Worst case TP1/TP5 patterns are loaded.
- With the DUT connection, the test is performed depending on the selected data lane (TP2 or TP5).

1. To configure the parameters for this test, see cable eye diagram (passive) test procedure (see page 368).
2. See the make connections for cable eye diagram (passive) (see page 197) for information on how to make connections.
3. Check the connection of the AWGs and AFG from TDSHT3.

4. Run the test. The software loads the appropriate patterns with TP1/TP5 waveforms and plots the eye diagram.
5. Connect the cable DUT between AWG and oscilloscope.
6. The software will plot the eye diagram with TP5/TP2 eye mask.

NOTE. *Using a manual DDS test method is not recommended because the software sets up and performs the Cable Eye Diagram test automatically and effectively.*

NOTE. *The Cable Eye Diagram (Active) tests use the same connection, test, and waveform view procedures as those for the Cable Eye Diagram (Passive) tests*

NOTE. *The Cable Eye Diagram (Active) tests do not support DDS method testing.*

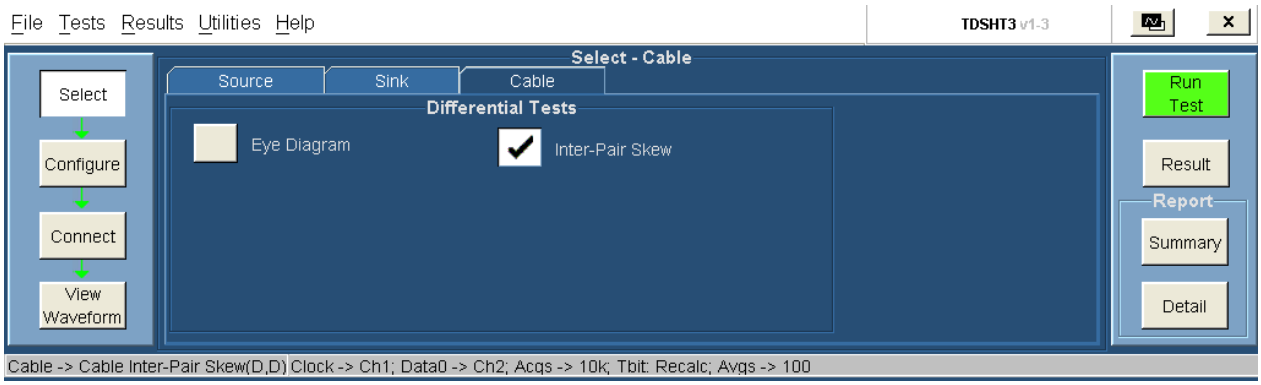
Test the Cable Inter-Pair Skew

This test allows you to confirm that any skew between the differential pairs in the TMDS portion of the HDMI link does not exceed the limits in the specification.

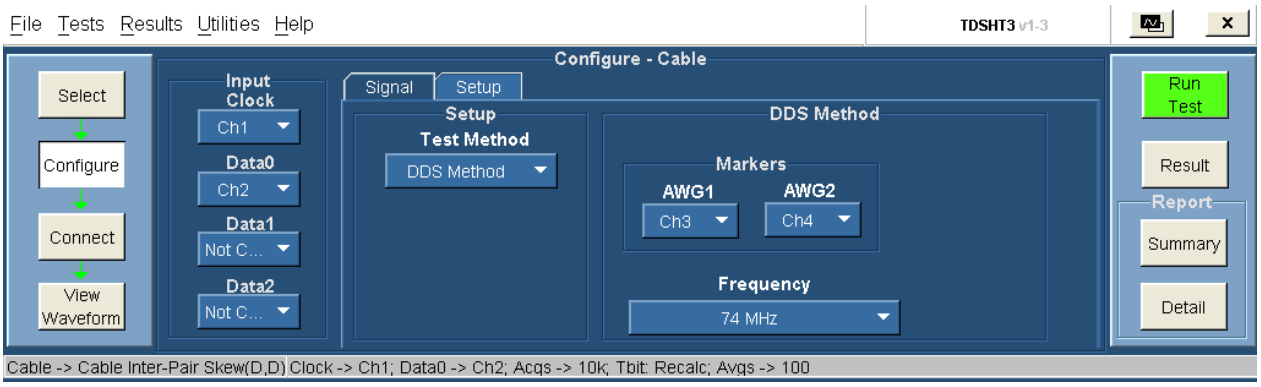
NOTE. *This test is performed only for **repeater cable testing**.*

You will need a Digital Oscilloscope, two AWGs, one AFG, two differential probes, one TPA-P, two TPA-R, two TCA SMA cables, and one accessory kit (consisting of seven matched SMA cable pairs, eight bias-tees, eight 120 ps TTC filters, three GPIB-HS cables, four BNC cables, and one BNC-T adapter).

1. On the menu bar, click **Tests > Cable > Inter-Pair Skew**.
2. In the differential tests pane, select the Inter-Pair Skew check box.



3. To change the configuration settings, click **Tests > Configure**. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard (see page 26) or the general purpose knob (see page 28) on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings. It is recommended that you save the configuration settings before you choose to select Recall Default or close the application.



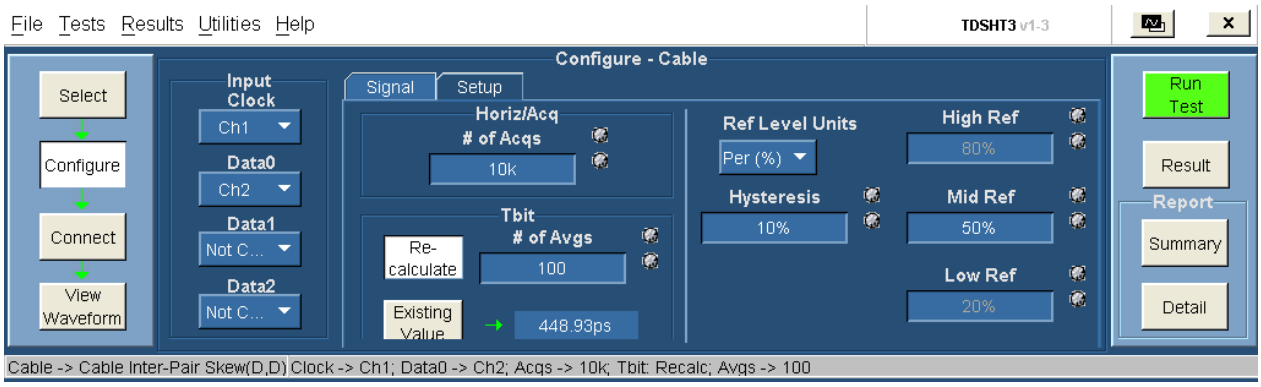
4. In the Signal tab, do the following:

   - Select the appropriate test method from the available choices (DTG Method and DDS Method).

   NOTE. *The DTG method is not supported for the Cable Inter-Pair Skew test.*

   - In the DDS Method pane, do the following:
     - In the Markers pane, select the oscilloscope channel to use for routing the synchronization pulse from the AWG1. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch3.
     - Select the oscilloscope channel to use for routing the synchronization pulse from the AWG2. The available choices are: Ch1, Ch2, Ch3, and Ch4. The default value is Ch4.
   - Select the cable frequency from the drop-down list.

5. In the Setup tab, do the following:



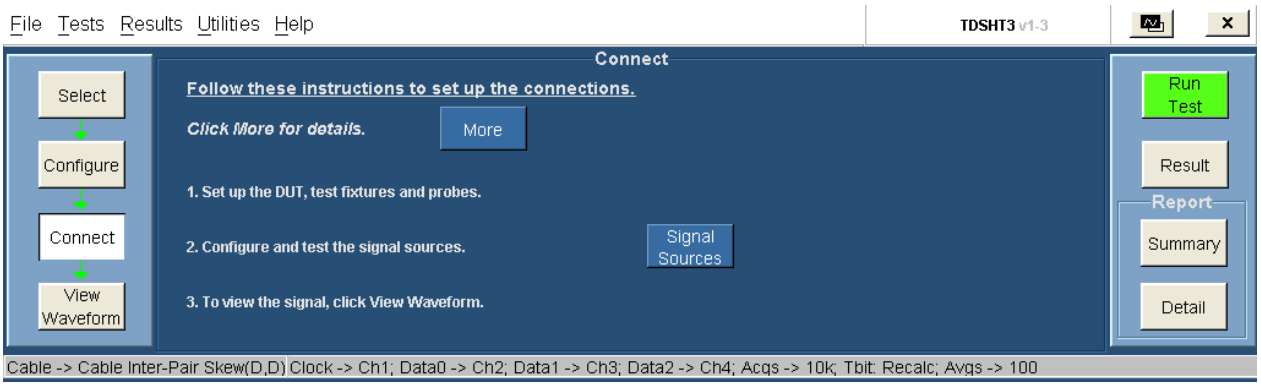
- In the input pane, do the following:
  - Set the Input Clock to the channel that you will use for the HDMI clock input. Select from the available choices (Ch1, Ch2, Ch3, and Ch4).
  - Set the Input Data0, Data1, and Data2 to the channel that you will use for the corresponding HDMI data inputs. Select from the available choices (Ch1, Ch2, Ch3, Ch4, and Not Conn).
- In the horiz/acq pane, enter the desired number of acquisitions that are required for the test. The range is from 10 K to 1 M and default is 10 K.
- In the tbit pane, do the following:
  - Click **Re-calculate** to recalculate the Tbit value.
  - Click **Existing Value** to use the previously calculated Tbit value.
  - Enter the number of averages (periods) that are required for the test. The range is from 2 to 1000 (1 K) and default is 100.
- In the Ref Level Units box, set the reference level units to either Per (%) or Abs.

  Per (%) indicates that the reference levels are a percentage of the Vswing value.

  Abs indicates that the reference levels are absolute voltage values.

  The default setting is Per (%).
- In the Hysteresis box, enter the desired hysteresis percent value. The range is from 0% to 25% and default is 10%.
- In the High box, the required high reference voltage value is set for the test. The default value is 80%.
- In the Mid box, enter the desired mid reference voltage value. The range is from 25% to 75% and default is 50%.
- In the Low box, the required low reference voltage value is set for the test. The default value is 20%.

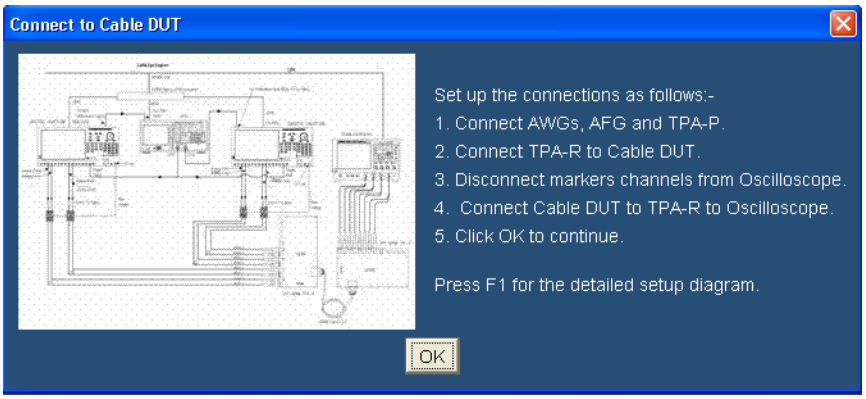
6. To connect the DUT, click **Tests > Connect**. Click here (see page 201) for information on how to make connections.



7. Click **Run Test** to run the test.

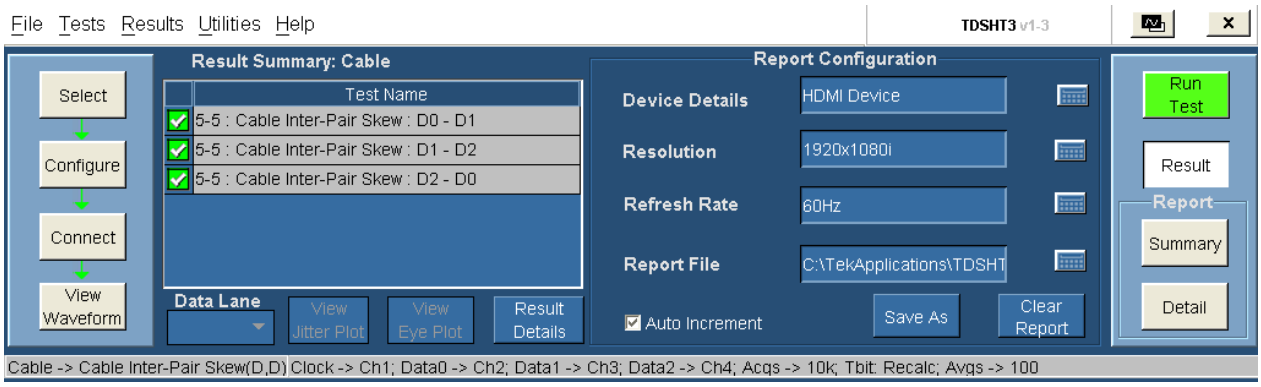
NOTE. *To synchronize the two AWGs, connect the marker channels to the oscilloscope.* *Click here (see page 201)* *for information on how to make connections.*

8. Once the synchronization of the two AWGs completes, the Connect to Cable DUT dialog box appears as follows:



Follow the instructions in this dialog box to make connections to measure inter-pair skew. Click here (see page 204) for information on how to make connections. The TDSHT3 Software sets up the oscilloscope and the test runs, displaying a progress indicator.

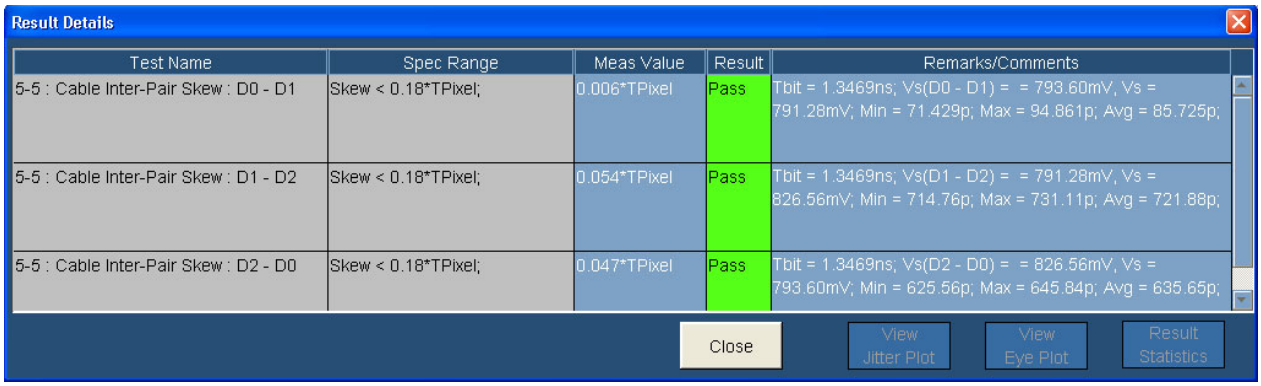
9. The software makes the results available automatically and displays the result summary. You can also view the report configuration details in the result pane.



The results summary lists the test name, status of the test (pass, fail or error), and jitter plot. To view the details of the results, click **Results Details**.

10. Set the report details to identify and generate the report automatically. You can set a default report file. Click here (see page 49) for more information.

11. In the result summary pane, click **Result Details**. The result details pane displays the following fields.



- Test Name (displays the test id, test name, and selected lanes)
- Spec Range (displays the HDMI standards and test specifications limit for the test)
- Meas Value (displays the measured value)
- Result (displays the status of the test as Pass, Fail, or Error)
- Remarks/Comments (displays the relevant details, such as Tbit, Vswing, and Margin. If the test could not be run, this field displays an error code (see page 397).

Test Method

NOTE. *This test is performed only for* ***repeater cable testing****.*

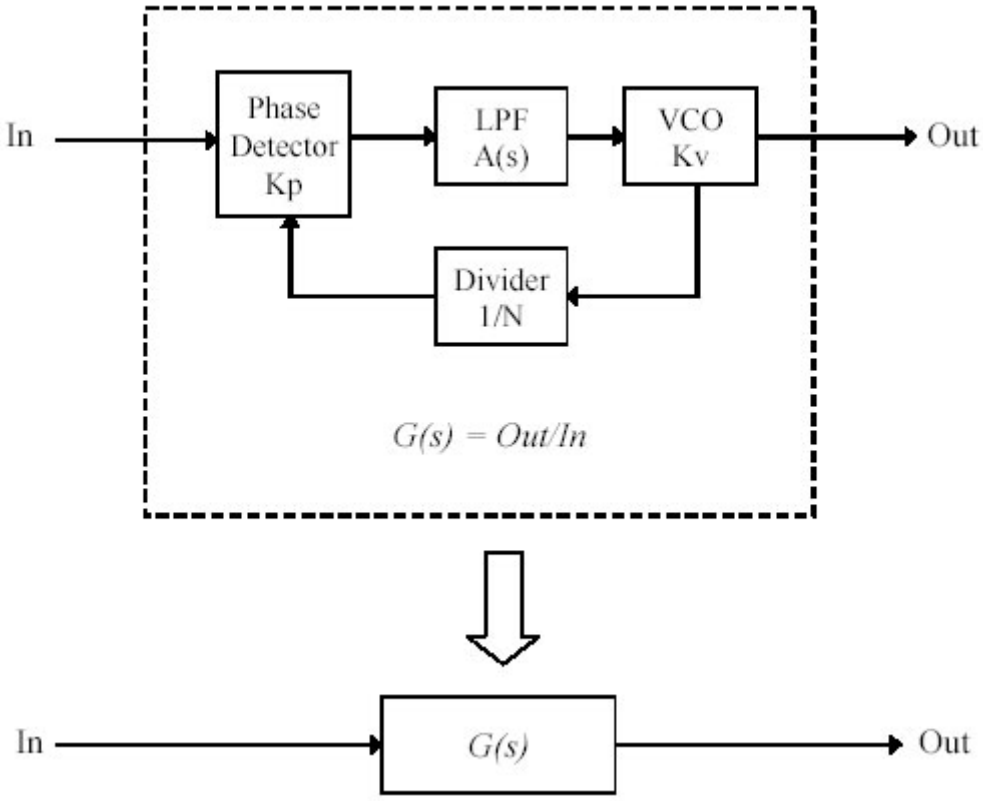
- To configure the parameters for this test, refer cable inter-pair skew procedure (see page 379).
- Refer to the connection diagram for synchronizing (see page 201) for information on how to make connections.
- Check the connection of the AWGs and AFG from TDSHT3.
- Run the test. The software loads the patterns on both the AWGs.
- Once the synchronization of both the AWGs is done, remove the marker channels from the oscilloscope.
- Connect the Input Data0 and Data2 to the oscilloscope to calculate inter-pair skew. Click here (see page 204) for information on how to make connections.
- Run the test to calculate inter-pair skew.

NOTE. *Using a manual DDS test method is not recommended because the software performs the Cable Inter-Pair Skew test automatically and effectively.*

Software CRU Technology

The HDMI specification mandates the Clock Recovery Unit (CRU) by using a Phase Locked Loop (PLL) with first order transfer function characteristics, to test both the jitter and the eye diagram. A PLL-based CRU implemented in hardware makes correlation of test results difficult due to differences in vendor-specific implementations. Software PLL techniques can extract clock and timing data from a serial data stream. The following method shows a practical and affordable way to satisfy the requirement:

PLL Characteristics



The diagram shows a simplified block diagram of generic phase-locked loop (PLL). A PLL consists of the Phase Detector (PD), Low Pass Filter (LPF), Voltage Controlled Oscillator (VCO), and Frequency Divider (FD).

The phase of the input signal is compared to the phase of FD output. The input of the FD is the output of VCO, whose frequency is controlled by the LPF output. The LPF output is a filtered form of the PD output. When the phase of FD output is leading compared to the input phase, the PD output changes to decrease the VCO frequency. Thus, the FD output will lag. Due to the effect of this feedback mechanism, the frequency of VCO is locked to N-times of the input frequency.

The LPF restricts the quick variation of the incoming signal, so that high frequency changes in the input phase are attenuated before they are transferred to consecutive functional blocks. Therefore, the VCO output represents the average phase of input signal even if the input signal does not have the constant phase rotation (frequency). Using this approach, the PLL circuitry recovers the clock information from the modulated input signal.

The transfer function from the input phase to the output phase is represented by following equation:

$$G(s) = \frac{\frac{Kp \cdot Kv \cdot H(s)}{s}}{1 + \frac{Kp \cdot Kv \cdot H(s)}{s \cdot N}} = \frac{N \cdot Kp \cdot Kv \cdot H(s)}{s \cdot N + Kp \cdot Kv \cdot H(s)}$$

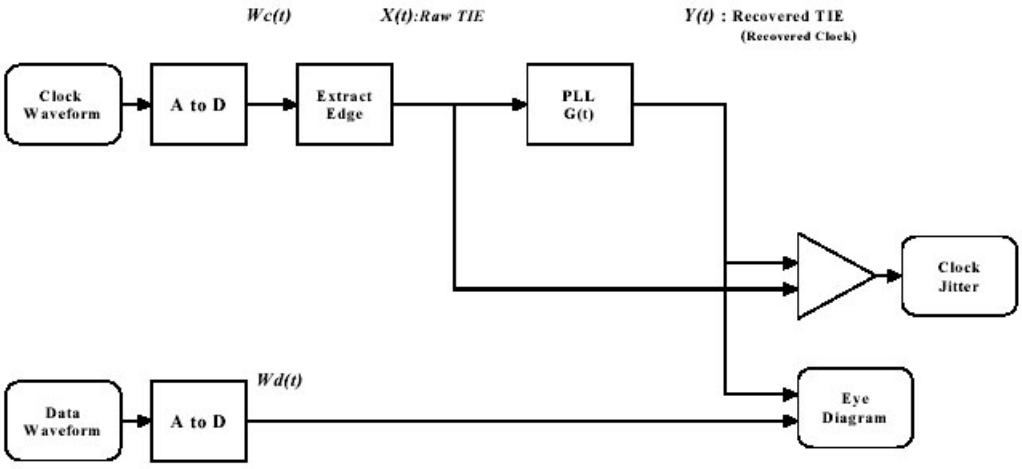
where Kp and Kv are the sensitivity coefficients of PD and VCO respectively, and N is the division factor of FD. H(s) is the transfer function of LPF in the frequency domain.

Assuming that N, Kp, and Kv are constant, the function G(s) can be simplified as follows:

$$G(s) = \frac{K_2 \cdot H(s)}{s + K_1 \cdot H(s)}$$

Note that G(s) becomes the first order low-pass filter only when H(s) is constant, namely, when H(s) is non-dependent on the frequency. This means that H(s) is not a low-pass filter in this case. On the contrary, it is well known that the PLL is not stable without a low-pass filter in place of H(s). Therefore, the first order transfer function that is required by CRU for HDMI may not be realized by the PLL circuitry as shown in the earlier PLL Functional Block diagram.

Conventional Method



The diagram shows a simple PLL design for CRU, measuring both the clock jitter and eye diagram within a digital oscilloscope. The input signal is first converted to digital information with an A/D converter. The phase of the input signal is extracted by finding the rising (or falling) edges of the digitized signal. A digital simulation of an actual hardware PLL circuit may be realized because the input and output signals exist as just digital information. In this case, the voltage values at several points in the PLL circuit are expressed in the time domain, and are repetitively calculated to derive their time variation. The time interval of the calculation must be sufficiently small to retain the high precision of the simulation. Hence, it requires significant digital processing capability to simulate actual PLL within a reasonable amount of time.

In this method, the phase transfer function of the PLL is determined by the characteristics of the simulated components. As long as the simulation observes the laws of physics, the resultant transfer function does not differ from that of the actual hardware PLL circuit. Given the time to process the data in the simulation, using this method is not advisable. The first order transfer function to be realized by this method may not be useful either.

Another method to simulate a PLL in software is to use its time domain transfer function from the input phase error to output timing information. The impulse response is used as the time domain transfer function. In this case, given the input signal X(t), the integral operation shown next gives the output signal Y(t).

$$Y(t) = \int_{\tau=-\infty}^{\infty} X(t) \cdot G(\tau - t) d\tau$$

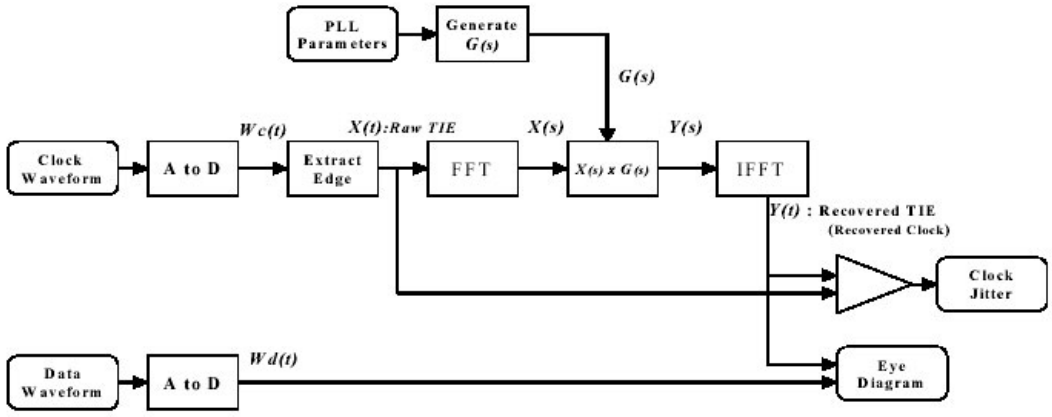
where G(t) is the time domain representation of G(s) mentioned in the previous section. This is called a convolution integral. In this case, the input signal is represented as discrete-time samples. The integration shown earlier should also be performed in discrete fashion as follows:

$$y(n) = \sum_{m=-\infty}^{\infty} g(m) \cdot x(n-m) = \sum_{m=-\infty}^{\infty} g(n-m) \cdot x(m)$$

There are two disadvantages in the time domain convolution method. One is that it still requires a huge number of multiplications and additions to calculate the values of all time points, as easily seen from the form of the equation above. Another is that it is not always practical to express the time domain transfer function as an explicit mathematical representation. In many cases, the human interpretation of the transfer function is made in frequency domain. Some means of conversion is required to derive the time domain response from the frequency domain characteristics. This requirement will complicate the design of the user interface.

It is important to mention that the first order transfer function characteristics can be realized by this convolution method, even though it has the difficulties described earlier. This method is inherently stable as far as an appropriate impulse response is adopted, because it does not include a feedback loop.

Proposed Method



The PLL circuitry acts as a low-pass filter for incoming time information. In the frequency domain, the filter function is simply realized by multiplying of the frequency response coefficients to the input spectrum. The convolution integral in the time domain is equivalent to simple multiplication between frequency-domain functions derived by the Fourier Transform. If the time information and the PLL characteristics are transformed to frequency domain, the PLL processing becomes much easier than in the time domain.

$$Y(s) = G(s) \cdot X(s)$$

As seen in this equation, the calculation becomes one multiplication (though between complex numbers) per sample point. Hence, the demand for digital processing performance is very low.

After the filter function is performed, the time information of the output signal may be derived with inverse transformation. Using an FFT algorithm, the forward and inverse transformation can be executed in relatively short time compared to simulation in time domain. Thus, the total time to calculate the recovered clock can be significantly reduced.

Jitter Test

The jitter of the incoming clock signal is measured by statistically analyzing the time difference between the incoming and recovered clocks. The timing information of both signals is already retained in digital form, so the jitter calculation is simple and straightforward. Usually, the peak-to-peak jitter value and the standard deviation (RMS) jitter value are used for evaluating the signal quality.

$$Jpp = \Delta T \max - \Delta T \min$$

$$J\sigma = \sqrt{\frac{\sum \left(\Delta T_n - \overline{\Delta T}\right)^2}{N}}$$

Appropriate sample points should be chosen to measure the jitter for specific cases such as the clock-to-data jitter at the first bit. Such a requirement is addressed by specifying a rectangular area with time range of [–T..+T] and voltage range of [–V..+V].

To obtain an accurate test, a large number of samples are required. As the earlier area restriction reduces the number of measured samples, the capability to process more and more samples is desired. Using the proposed method, it becomes realistic to gather a huge amount of statistical information for a more precise test.

Eye Diagram

An eye diagram is the incoming data waveform repeatedly drawn with the recovered clock used as the time reference. The recovered clock is represented as time information. It may be used to derive the position where the input data waveform should be drawn. The resulting diagram will precisely indicate the true marginal area with which the reliability of data transmission is determined.

The vertical coordinate to draw the incoming waveform is determined by using the data value itself. Determine the horizontal coordinate (x) by the following equation:

$$Xcoord = Tn - Tref$$

where Tn is the time of incoming waveform, and Tref is the time of the reference signal (the recovered clock signal).

About HTML/MHT Reports

HTML/MHT Reports enhance the TDSHT3 Software capabilities by simplifying the process of creating and maintaining results. It automates the process of compiling the test results and generating the reports. The application generates an MHT file that can be opened in Internet Explorer.

Reports Formats

The generated reports (see page 392) are in .mht format and include the following configured set of information:

- **Configuration:** This section includes the following:
  - **Setup Configuration** such as the oscilloscope information and application version.
  - **Device Configuration** such as Device Details, Resolution, and Refresh Rate.
  - **Compliance Summary** such as the total tests performed and Pass/Fail status.
- **Test Summary:** This section displays the Test Name, Lanes, Specification Range, Measurement Value, and Results.
- **Detailed Results:** This section includes the following:
  - **Results** such as Specification Range, Measurement Value, Tbit, Vswing, Margin, Record length, Mask Hits, and Results.
  - **Waveform/Plot** such as selected plots and/or oscilloscope waveforms.

Sample Report

A sample report is as follows:

HDMI Compliance Test Software: Measurement Report

Tektronix Enabling Innovation

Wed Apr 01 13:11:26 IST 2009

Cable Tests Report

Configuration

Setup Configuration

Oscilloscope Info	DPO70804 - 4.3.0 Build 95
TDSHT3v1-3 Version	5.0.0 Build 15

Device Configuration

Device Details	HDMI Device
Clock Frequency(Mhz)	74.2531
Resolution	
Refresh Rate	

Compliance Summary

Total Tests (for all data lanes)	4
Tests Completed	4
Pass	4
Fail	0

Test Summary

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	5-3 : Cable Eye Diagram TP1	CK - D0	TP1 Data Jitter < 0.3*Tbit;	0.29*Tbit	Pass
2	5-3 : Cable Eye Diagram TP5	CK - D0	TP5 Data Jitter < 0.38*Tbit;	0.35*Tbit	Pass
3	5-3 : Cable Eye Diagram TP5	CK - D1	TP5 Data Jitter < 0.38*Tbit;	0.34*Tbit	Pass
4	5-3 : Cable Eye Diagram TP5	CK - D2	TP5 Data Jitter < 0.38*Tbit;	0.34*Tbit	Pass

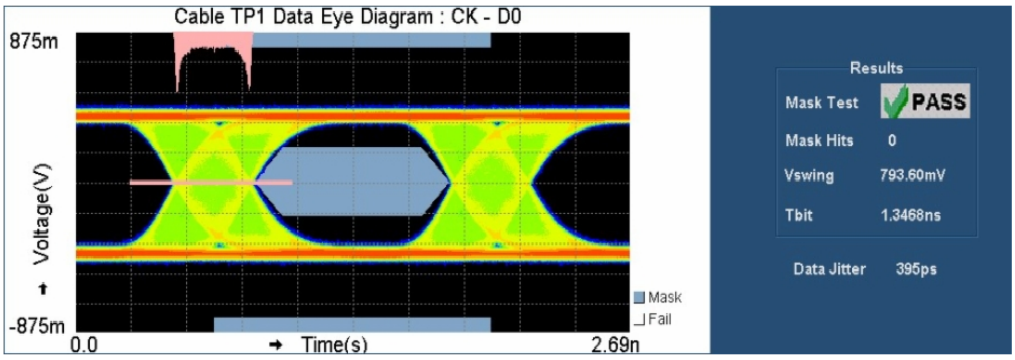
Detailed Results

5-3 : Cable Eye Diagram TP1 : CK - D0

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
TP1 Data Jitter < 0.3*Tbit;	0.29*Tbit	1.3468ns	789.12mV	0.01*Tbit	25.000M	0	Pass

Waveform/Plot



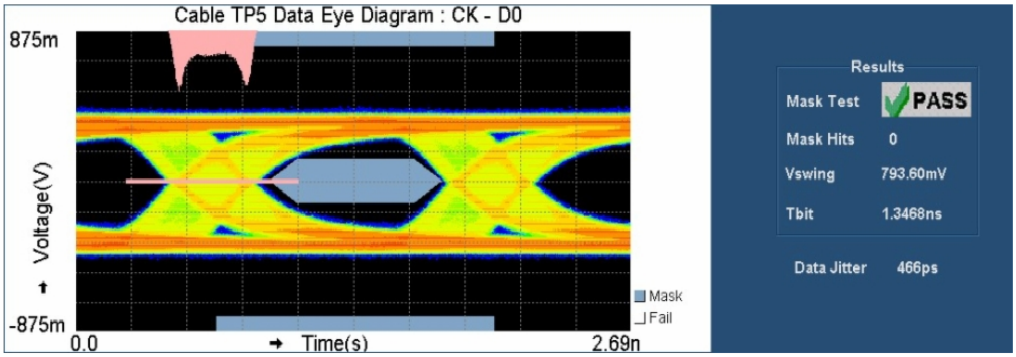
Return to Test Summary

5-3 : Cable Eye Diagram TP5 : CK - D0

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
TP5 Data Jitter < 0.38*Tbit;	0.35*Tbit	1.3468ns	793.60mV	0.03*Tbit	25.000M	0	Pass

Waveform/Plot



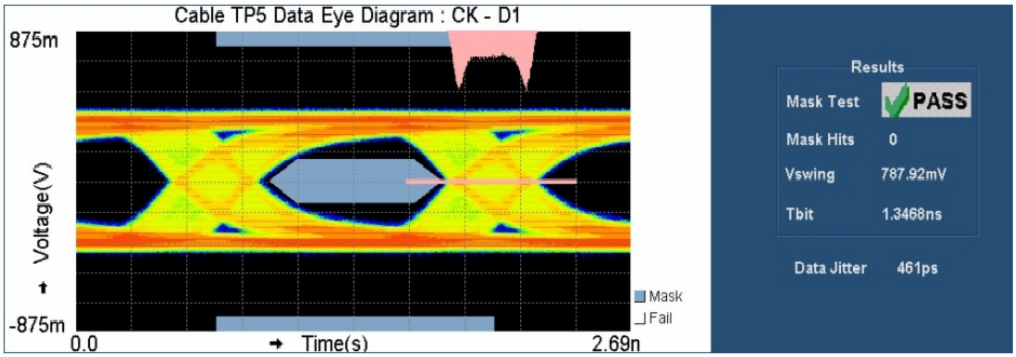
Return to Test Summary

5-3 : Cable Eye Diagram TP5 : CK - D1

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
TP5 Data Jitter < 0.38*Tbit;	0.34*Tbit	1.3468ns	787.92mV	0.04*Tbit	25.000M	0	Pass

Waveform/Plot



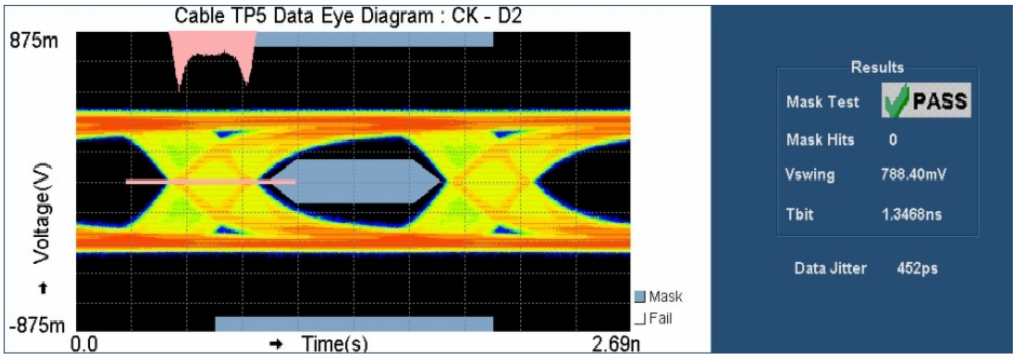
Return to Test Summary

5-3 : Cable Eye Diagram TP5 : CK - D2

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
TP5 Data Jitter < 0.38*Tbit;	0.34*Tbit	1.3468ns	788.40mV	0.04*Tbit	25.000M	0	Pass

Waveform/Plot



Return to Test Summary

Return to top

Default Settings

Parameter	Selection	Default setting
Select	Flow Controls	Select
	Device Type Tab	Source (Differential Tests)
	Source Test	Eye Diagram
	Sink Test	Min/Max-Diff Swing Tolerance (Differential)
	Cable Test	Eye Diagram
Source Configuration	Clock Input	Ch1
	Data0 Input	Ch2
	Data1 Input	Ch3
	Data2 Input	Ch4
CRU	Clock	PLL
Others	Ref Level Units	Percentage
Sink Configuration	DTG file path	C:\TekApplications\TD-SHT3v1-3\ComplianceTest-Patterns\ PC\1920X1080i 50Hz 8 Bit Gray RGB PC V3-3.dtg
	Clock output from DTG	A1
	Data0 output from DTG	B1
	Data1 output from DTG	B2
	Data2 output from DTG	C1
Signal Sources	Signal Sources Tab	DTG AWG Unavailable AFG Unavailable
	Control Type	GPIB
	Board Type	GPIB0
	GPIB Address (Primary)	1
	GPIB Address (Secondary)	0
View Waveform	Clock/Data Waveforms	
Result Summary	View Jitter Plot	Unavailable
	View Eye Plot	Unavailable
	Data Lane	Unavailable
	Test Point	Unavailable
Result Details	View Jitter Plot	Unavailable
	View Eye Plot	Unavailable
	Result Statistics	Unavailable

Parameter	Selection	Default setting
Deskew	External	From Input Setup - Input - Ch1
		From Input Setup - Hysteresis - 10%
		From Input Setup - Ref Level - 50%
		To Input Setup - Input - Ch2
		To Input Setup - Hysteresis - 10%
		To Input Setup - Ref Level - 50%
		Slope - Rise
		Slope - # of Slopes - 1
	Internal	From Input Setup - Input - Ch1
		To Input Setup - Input - Ch2
		Slope - Rise
Report Configuration pane	Device Details	HDMI Device
	Resolution	1920*1080i
	Refresh Rate	60 Hz
	Report File	Disabled
	Auto Increment	Selected
	Save As	Disabled
	Clear Report	Enabled

Error Codes

The following table lists the error codes, their descriptions, and the possible solutions:

Error code	Error message	Description	Possible solution
101	Input is “Not Conn.”	Both the selected sources are not connected.	Select valid channels (Ch1-Ch2, Ref1-Ref2) for at least clock/data source/data source (differential tests) or for input1/input2 (single-ended tests).
102	Conflict in the selection of inputs.	The sources that are selected for the two inputs are the same. The inputs clock source and data source for differential tests, input 1 and input 2 for single-ended tests.	Select different channel sources for input 1 and input 2 for single-ended tests and different channel sources for clock source and data source for differential tests.
103	The combination of Ref and Live input signals is not valid.	The software supports both Ref or both Live combinations of channels.	Select both ref channels or both live channels for clock and data source.
104	Ref Wfm is not valid.	The software cannot switch on ref waveforms. Ref waveforms could be empty.	Recall the required ref waveform from the appropriate file on the oscilloscope.
105	Conflict in GPIB Selection.	There is a conflict in the selection of GPIB address. One or more addresses are repeated.	Ensure that no two GPIB addresses are identical.
106	Conflict in the selection of input types.	There is a conflict in the selection of the inputs. One or more inputs are repeated.	Ensure that the combination of the selected inputs are unique.
107	Four channel feature is supported only on DPO70000, DSA70000, and MSO70000 series oscilloscopes with bandwidths greater than or equal to 4 GHz.	The four channel feature is not supported in the oscilloscope.	Reduce the number of channels to two and proceed.
110	Unable to acquire waveform.	The oscilloscope is not able to acquire the signal and trigger.	Ensure that the software configurations are proper. Check the probes and test fixture connections. If the test uses serial trigger, ensure that the CTL pattern is present on the waveform.
111	Not enough acquisitions to perform the test.	The software expects to acquire a minimum number of acquisitions that are configured.	Ensure that the software configurations are proper. Check the probes and test fixture connections.

Error code	Error message	Description	Possible solution
113	Error in importing the Wfm.	The software could not import the waveform from acquisition. This happens when there is no valid waveform in the acquisition memory.	Check the probes and test fixture connections. Run the test again.
114	Improper Wfm.	Signal is not probed at the proper test points.	Refer to the connections diagram and probe the proper signal.
115	Ref Wfms have different Record Lengths/Sample Rates.	The ref waveforms have different sample rates and/or record lengths.	Use waveforms that are acquired simultaneously for ref waveforms.
121	Ref Levels entered are outside the range of the Wfm.	Unable to locate the edges on the waveform at the transition because the levels configured do not fall within the transition of the waveform.	Enter the Ref Level voltage value where the transition occurs on the waveform. Enter 50 percent of the level of the peak-to-peak transition level for mid-ref levels, 80 percent of the peak-to-peak for high-ref levels, and 20 percent of the peak-to-peak for low ref levels.
122	((Hysteresis Level/2) + Ref Level) cannot be greater than 100 percent.	((Hysteresis Level/2) + Ref Level) has to be within 100 percent for edge finding.	Set both the ref and (Hysteresis Level/2) to be less than 100 percent.
123	High Level is less than or equal to Low Level.	The configured high level value is less than the low level value.	Configure the high level to be greater than the low level.
131	Error in calculating Tbit.	Not a valid clock waveform.	Supply a valid clock waveform and run the test again.
132	Clock input is required to calculate Tbit.	The Tbit value has to be calculated before you run a test that uses only data source(s).	1. Select and run a test that uses clock source for Tbit value. 2. Click **Connect**, select clock source, and then click **Re-calculate Tbit** before you run the test.
152	Select any test to continue.	Configure, Connect, View Waveform, and Run Test need at least one test to be selected.	Select at least one test before you click either **Configure**, **Connect**, **View Waveform**, or **Run Test**.
161	Unable to recover clock.	Improper waveform or the software components are missing.	Supply the proper waveform. Reinstall the software.
171	Unable to find edges.	The waveform may be noisy or the hysteresis level may be low.	Check the probes and test fixture connections. Increase the hysteresis band level.
172	Not enough edges.	Number of edges found on the waveform is less than the minimum number of edges that is required for the test.	Decrease the horizontal scale to have more complete cycles of the waveform. Adjust the hysteresis level of the signal to find the edge at the required level.

Error code	Error message	Description	Possible solution
173	Unable to calculate skew.	Could not find the mid of the waveform.	Check the probes and test fixture connections.
174	CTL pattern not found.	The CTL pattern (see page 250) was not found on the waveform.	Ensure that the appropriate pattern is present on the source waveform. Change the polarity of the waveform.
175	Option ST is not installed on the oscilloscope.	Option ST is not available on the oscilloscope.	Install Option ST.
178	Unable to calculate Vswing.	Signal is not probed at the proper test points.	Follow the instructions in the setup diagram and probe the proper signal.
181	Check the DTG connection.	DTG connection has failed. This could happen if: ■ The DTG is not switched on. ■ There is a mismatch in the GPIB-ENET configuration, software GPIB configuration, or DTG remote control configuration. ■ The GPIB cable is not connected properly.	■ Switch on the DTG and wait for the DTG software to load. ■ Check GPIB connections. ■ Ensure that the primary and secondary addresses of DTG in the remote control match the GPIB-ENET configuration of the oscilloscope. ■ Ensure that the GPIB-ENET configuration on your oscilloscope matches the signal sources configuration in the software.
182	File not found in the DTG.	The configured file is not found in the DTG.	Ensure that the specified file in the software is present in the DTG. Specify a file name that is present in the DTG.
183	Invalid logical channel.	The logical channel is invalid.	Provide a proper logical channel.
184	Conflict in selection of outputs from the DTG.	The same physical channel (A1, A2, B1, B2, C1, C2, D1, D2) is selected for any two logical channels (Clock, Data0, Data1, Data2).	Select different physical channels (A1, A2, B1, B2, C1, C2, D1, D2) for a given logical channel (Clock, Data0, Data1, Data2).
191	Check the AWG connection.	AWG connection has failed. This could happen if: ■ The AWG is not switched on. ■ There is a mismatch in the GPIB-ENET configuration, application GPIB configuration, and AWG remote control configuration. ■ The GPIB cable is not connected properly.	Switch on the AWG and wait for the AWG software to load. Check GPIB connections. Ensure that the primary address of AWG in the **Utility > Network > Address** matches with the GPIB-ENET configuration of the oscilloscope. Ensure that the GPIB-ENET configuration on your oscilloscope matches the signal sources configuration in the software.

Error code	Error message	Description	Possible solution
192	File not found in the AWG.	File is not present in the AWG.	Ensure that the required file is present in the AWG.
193	Check the Signal Sources connection.	Signal sources connection has failed. It may be due to DTG or AWG connection failure. DTG connection has failed. This could happen if: ■ The DTG is not switched on. ■ There is a mismatch in the GPIB-ENET configuration, software GPIB configuration, and DTG remote control configuration. ■ If the GPIB cable is not connected properly. AWG connection has failed. This could happen if: ■ The AWG is not switched on. ■ There is a mismatch in the GPIB-ENET configuration, software GPIB configuration, and AWG remote control configuration. ■ If the GPIB cable is not connected properly. ■ Primary addresses of DTG and AWG are same.	For the DTG connection failure: ■ Switch on the DTG and wait for the DTG software to load. ■ Check the GPIB connections. ■ Ensure that the primary address of DTG in the remote control matches the GPIB-ENET configuration of the oscilloscope. ■ Ensure that the GPIB-ENET configuration on your oscilloscope matches the signal sources configuration in the software. For AWG connection failure: ■ Switch on the AWG and wait for the AWG software to load. ■ Check the GPIB connections. ■ Ensure that the primary address of AWG in the Utility > Network > Address matches with the GPIB-ENET configuration of the oscilloscope. ■ Ensure that the GPIB-ENET configuration on your oscilloscope and signal sources configuration in the software match. Select distinct primary addresses for the DTG and AWG.
194	Jitter value is unavailable.	Signal is not probed at the proper test points.	Follow the instructions in the setup diagram and probe the proper signal.
196	Invalid DUT frequency.	The frequency of the DUT configured in Configure > Setup > DUT Freq (MHz) does not match with the frequency of the signal generated from the DTG.	Load the required pattern on the DTG and check the frequency of the signal. Ensure that the same frequency has been configured in the DUT Freq (MHz).

Error code	Error message	Description	Possible solution
201	Edges on the Wfm are lesser than the configured number of edges.	Deskew number of edges set by the user to perform the deskew is not available on the waveform.	Ensure that the edges in the waveform and the display in the numeric input are the same. Adjust the horizontal scale to increase the number of transitions that is required to adjust the deskew.
202	Calculated skew is greater than the oscilloscope skew range.	The calculated skew value is greater than the oscilloscope deskew range.	The deskew will be done to the maximum deskew value that is applicable to the oscilloscope.
203	Cycle has less than 20 sample points.	Insufficient number of samples in a complete cycle. The number of data points in the identified cycle is less than 20.	Increase the sampling rate.
211	Select the test point(s) to continue.	No test points are selected.	Select any one or both of the test points in cable configuration.
221	Mask cannot be moved beyond this position.	Upper and lower masks have exceeded their boundary values. The mask co-ordinates are beyond the plottable area.	Change the Mask Movement mode from Coarse to Fine. After changing to Fine, you will be able to move a bit further. If you are already in Fine mode, and this message appears, you are in the maximum/minimum possible position.
222	Unable to calculate mask margins.	An error occurred while calculating the mask margins.	The signal may be wrong (noise, invalid pattern). Connection to the probe tip may be loose. Recheck the connection and run the test again.

Error code	Error message	Description	Possible solution
251	Check the AFG connection.	Connection to AFG has failed. This could happen if: ■ The AFG is not switched on. ■ There is a mismatch in the GPIB-ENET configuration, software GPIB configuration, and AFG remote control configuration. ■ If the GPIB cable is not connected properly. ■ Primary addresses of the signal sources are same.	Perform the following: ■ Switch on the AFG and wait for the AFG software to load. ■ Check the GPIB connections. ■ Ensure that the primary address of AFG in the remote control matches the GPIB-ENET configuration of the oscilloscope. ■ Ensure that the GPIB-ENET configuration on your oscilloscope matches the signal sources configuration in the software. ■ Select distinct primary addresses for the signal sources.
252	Four DTGM30 modules are required to run this measurement.	An error occurs when any of the four connected modules is not DTGM30.	Connect four DTGM30 modules to the DTG and run the test.
401	AWG pattern directory not found.	The required directory is not present in the AWG.	Reinstall the AWG pattern files.
402	Unable to turn on the AWG output due to invalid external input clock. Connect the external clock and turn ON the outputs to proceed.	Invalid/missing external clock.	Ensure that the correct external clock is connected before turning ON the outputs.
412	Unable to calibrate. The measured jitter value is high.	Calibration has failed. This could happen if: ■ The cable and test fixture connections are not correct. ■ Base pattern on which the calibration is performed is not correct.	Perform the following: ■ Check the cable and test fixture connections. ■ Reinstall the base pattern.
413	Unable to calibrate. The measured jitter value is zero.	Calibration has failed. This could happen if: ■ The cable and test fixture connections are not correct. ■ Base pattern on which the calibration is performed is not correct.	Perform the following: ■ Check the cable and test fixture connections. ■ Reinstall the base pattern.

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