Tektronix
Demo 3 Board
Instruction Manual

www.tek.com
071-2862-02

Contacting Tektronix

Tektronix, Inc.
14150 SW Karl Braun Drive
P.O. Box 500
Beaverton, OR 97077
USA

For product information, sales, service, and technical support:

- In North America, call 1-800-833-9200.
- Worldwide, visit www.tek.com to find contacts in your area.

Tektronix Demo 3 Board instructions

The Tektronix Demo 3 Board provides signals that you can use to demonstrate key waveform triggering and capture features of Tektronix oscilloscopes.

Environmental considerations

This section provides information about the environmental impact of the product.

Product end-of-life handling

Observe the following guidelines when recycling an instrument or component:

Equipment recycling. Production of this equipment required the extraction and use of natural resources. The equipment may contain substances that could be harmful to the environment or human health if improperly handled at the product's end of life. In order to avoid release of such substances into the environment and to reduce the use of natural resources, we encourage you to recycle this product in an appropriate system that will ensure that most of the materials are reused or recycled appropriately.

This symbol indicates that this product complies with the applicable European Union requirements according to Directives 2012/19/EU and 2006/66/EC on waste electrical and electronic equipment (WEEE) and batteries. For information about recycling options, check the Tektronix Web site (www.tektronix.com/productrecycling).

Preventing electrostatic damage

Electrostatic discharge (ESD) can damage components on the demo board. To prevent, ESD:

- Do not touch exposed components or connector pins unless you are using ESD protective measures, such as wearing an antistatic wrist strap.
- Handle the demo board as little as possible.
- Do not slide the demo board over any surface.
- Transport and store the demo board in a static-protected bag or container.

Connect power

1. Connect the dual USB **A** Host connectors into two USB Host ports on your PC or other USB device. You need to connect both USB A connectors to provide adequate power to the demo board.

NOTE. *The Tektronix Demo 3 board requires approximately 0.8 A to operate.*

---

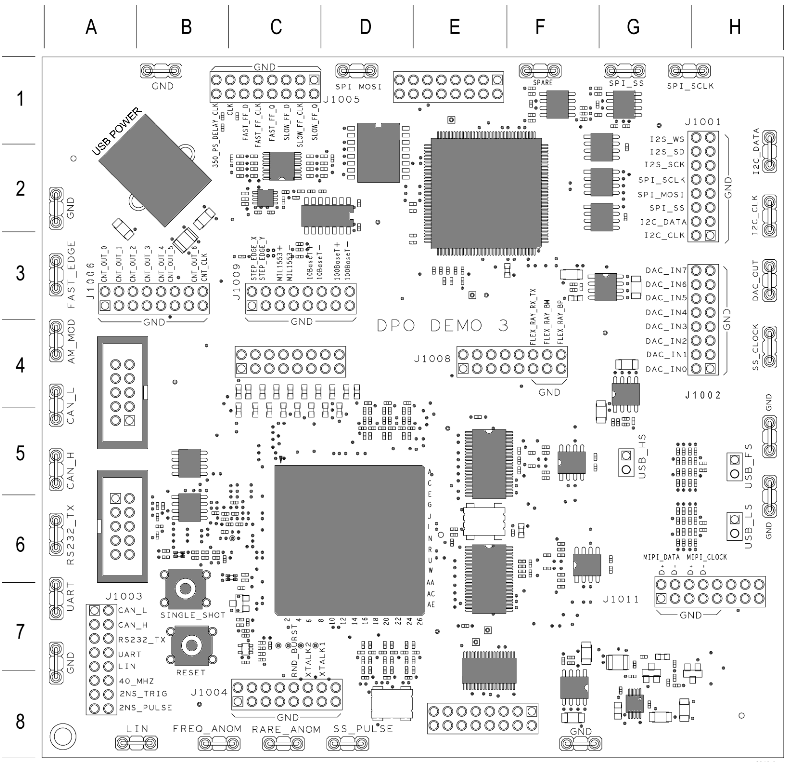
2. Connect the single USB **B** Device connector to the demo board. A green LED on the board turns on and remains steady when you apply adequate power to the board.

NOTE. *The purpose of the USB cable is to provide power to the demo board. No communication occurs over the USB cable.*

All available signals (except for single-shot) are present on their connectors when you apply power to the demo board. Push the RESET button immediately after connecting power. You should also push the RESET button after connecting a probe or test leads to the demo board and before taking measurements.

Signal locations

The following diagram includes a grid to help you locate signal outputs. To find a particular signal output on the board, look up the connector grid location in the following *Signal Descriptions* section and use the grid location information to find the signal on the demo board.



Signal descriptions

2 ns pulse

Board label: 2NS_PULSE
Grid location: A8

Description: This signal is a 2 ns to 3 ns, 2.5 V pulse at a 3.3 ms repetition rate. Use this signal to demonstrate the minimum pulse width capture specification of an instrument digital acquisition system.

2 ns pulse trigger

Board label: 2NS_TRIG
Grid location: A8

Description: This is the trigger edge signal for the 2 ns pulse. A falling edge on this signal occurs approximately 5 ns before the 2 ns pulse.

350 ps delayed clock

Board label: CLK, 350_PS_DELAY_CLK
Grid location: B1

Description: This is a 156 kHz square wave signal and a delayed copy. Use the nominal 350 ps delay to demonstrate the timing resolution of digital channels.

40 MHz square wave

Board label: 40_MHZ
Grid location: A8

Description: This is a 40 MHz square wave signal. This signal is not a perfect square wave shape and is intended to provide a fast repetitive signal to demonstrate high speed measurement capability.

AM modulation

Board label: AM_MOD
Grid location: A4

Description: This is a 1.25 MHz carrier amplitude signal modulated by a 1.25 kHz sine wave signal.

The AM Mod signal is centered around ground.

Set the oscilloscope trigger level to either the top or bottom of the waveform to stabilize it on the display.

CAN bus

Board label: CAN_H, CAN_L
Grid location: A4, A5, A7

Description: These are the CAN (Controller Area Network) bus signals between two CAN transceivers.

The bit rate of the data packet is 500 kbps.

Counter clock

Board label: CNT_CLK
Grid location: B3

Description: This is the 1.25 MHz clock signal for the 7-bit Counter Output described next.

Counter output bits

Board label: CNT_OUT0: CNT_OUT6
Grid location: A3, B3

Description: These are the 7-bits of the binary counter. The LSB is CNT_OUT0 at 625 KHz, that is, half of the counter input clock.

The Counter Output Bits and the Counter Clock signals are on eight adjacent sets of header pins for easy connection to a digital probe.

Crosstalk

Board label: XTALK1, XTALK2
Grid location: C8

Description: These two signals have significant crosstalk between them. Use them to demonstrate high-speed digital acquisition.

DAC input, parallel

Board label: DAC_IN0: DAC_IN7
Grid location: H3, H4

Description: These are the 8-bit parallel output signals of the port expander in the middle of the mixed signal chain. The sine wave data from the SPI bus is converted to 8 parallel bits to drive the DAC. DAC_IN0 is the LSB. (See Figure 1.)

See the previous SPI Bus description for packet details.

DAC output

Board label: DAC_OUT
Grid location: H3

Description: This is the output of the DAC at the end of the mixed signal chain. The DAC is driven from the port expander. The DAC output is a sine wave. Since the output is not filtered, the digitizing levels are present in the output waveform. (See Figure 1.)

The resulting DAC voltage is a sine wave with an amplitude 0 to 3 volts, and a period of 31 ms.

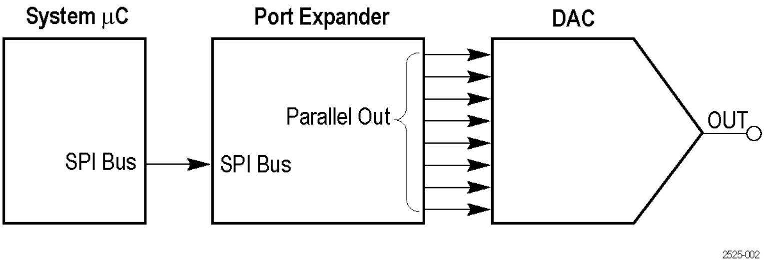


Figure 1: Mixed signal chain block diagram

Ethernet bus

Board label: 10BaseT+, 10BaseT-, 100BaseT+, 100BaseT-
Grid location: C3, D3

Description: Ethernet Serial Bus signals, driven as differential pairs:

- The 10Base-T signal pair communicates at 10 Mbit/s.
- The 100Base-TX signal pair communicates at 100 Mbit/s.

Fast edge

Board label: FAST_EDGE
Grid location: A3

Description: This is a 156 kHz capacitively coupled pulse signal with a 1.5 ns rise and fall time.

Fast FF clock

Board label: FAST_FF_CLK
Grid location: C1

Description: This is the 1.25 MHz clock input signal to a fairly fast flip-flop. The pulse width of this clock signal varies slowly.

Fast FF data

Board label: FAST_FF_D
Grid location: C1

Description: This is the 1.25 MHz data input signal to a fairly fast flip-flop that is asynchronous to the clock input.

Fast FF Q output

Board label: FAST_FF_Q
Grid location: C1

Description: This is the Q output signal of the fairly fast flip-flop. This signal shows metastable behavior infrequently.

FlexRay

Board label: FLEXRAY_BP, FLEXRAY_BM, FLEXRAY_TX/RX
Grid location: F4

Description: These FlexRay signals consist of the following test points:

- FlexRay_BP, the positive half of a differential FlexRay bus
- FlexRay_BM, the negative half of a differential FlexRay bus
- FlexRay_Tx/Rx, the single-ended logic signal between the controller and the transceiver

The data rate is at 10 Mb/s. The swing is 0 to 3.3 V. Tri-state is at 1.65 V (BP and BM only). There are 15 individual 198-bit long frames.

Frequent anomaly

Board label: FREQ_ANOM
Grid location: B8, C8

Description: There are two frequently occurring anomalies in this pulse train.

A half height runt signal occurs approximately every 3.28 ms. Use a Runt trigger to isolate the signal.

A 25 ns (narrow) pulse appears approximately every 3.28 ms. Use a Pulse Width or Glitch trigger to isolate the signal.

The pulse train is a repeating group of three pulses. The three pulses are 100 ns, 200 ns, and 100 ns wide, with a 100 ns low between. The group repeats at a 1.6 μs rate.

The anomaly is a group of four pulses. The four pulses are 100 ns, 50 ns (narrow), 100 ns (runt), and 100 ns wide, with a 100 ns low between, except for a 50 ns low before the runt.

I^{2}C bus

Board label: I2C_CLK, I2C_DATA
Grid location: H1, H2

Description: These are the I^{2}C (Inter-IC Communication) bus signals between the μC and a serial EEPROM.

There are several different types of data packets.

The clock rate is a 200 kHz, 0 to 5 volt signal.

I^{2}S (Inter-IC Sound) bus

Board label: I2S_SCK, I2S_WS, I2S_SD
Grid location: H1, H2

Description: This is an I^{2}S (Inter-IC sound) serial bus.

The clock rate is 2.5 MHz.

LIN bus

Board label: LIN
Grid location: A7, A8, B8

Description: This is the LIN (Local Interconnect Network) bus signal between two LIN transceivers.

The bus speed is 19.2 kbaud. It contains a mix of version 1.x and 2.x frames.

MIL-STD-1553

Board label: MIL1553+, MIL1553-
Grid location: C3

Description: A dual, redundant, differential-pair, protocol-bus controller controlling multiple Remote Terminals. Messages consist of one or more 16-bit words, where each word is preceded by a 3 µs sync pulse and followed by an odd parity bit.

Random burst

Board label: RNDM_BURST
Grid location: C8

Description: This is the signal that produces Bursts of 100 ns wide logic pulses every 6.6 ms. The pattern is a pseudorandom bit sequence that repeats every 128 bursts and has a 6.32 µs duration.

Rare anomaly

Board label: RARE_ANOM
Grid location: C8

Description: There are two less-frequent anomalies in this pulse train that can show up on high waveform capture rate oscilloscopes.

A half-height runt signal occurs approximately every 838.8 ms. Use a Runt trigger to isolate the signal.

A 25 ns (narrow) pulse appears in approximately 838.8 ms. Use a Pulse Width trigger to isolate the signal.

The pulse train is a repeating group of three pulses. The three pulses are 100 ns, 200 ns, and 100 ns wide, with a 100 ns low between each pulse. The group repeats at a 1.6 µs rate.

The anomaly is a group of four pulses. The four pulses are 50 ns, 25 ns (narrow), 100 ns (runt), and 100 ns wide, with a 100 ns low between each pulse, except for a 25 ns low before the narrow pulse.

Reset button

Board label: RESET
Grid location: B7

Description: Push the **RESET** button to start RS-232 signals from a common start point and to reset other functionality should the board become corrupted due to static electricity or some other cause.

RS232 UART, transmit

Board label: UART, RS232_TX
Grid location: A6, A7

Description: The UART signal is the noninverted logic level input to the RS-232 UART from the µC. The inverted transmit signal (TX) is the RS-232 voltage level serial bus signal.

The decoded data packets display the ASCII string Tektronix, Enabling Innovation.

There are no matching receive or data flow control signals.

The baud rate is 9600. The data format is 1 start bit, and 8 data bits with no parity.

Single shot button

Board label: SINGLE SHOT
Grid location: B7

Description: Push the **SINGLE SHOT** button to initiate a 200 ns pulse on the SS_PULSE signal connector (at grid location D8).

Single shot pulse

Board label: SS_PULSE
Grid location: D8

Description: This is a 200 ns wide positive pulse that is initiated by the SINGLE SHOT push button (grid location B7). The Demo 3 board provides one pulse per button push.

Slow FF clock

Board label: SLOW_FF_CLK
Grid location: C1

Description: This is the 1.25 MHz clock input signal to a slow flip-flop.

Slow FF data

Board label: SLOW_FF_D
Grid location: C1

Description: This is the 1.25 MHz data input signal to a slow flip-flop that is asynchronous to the clock input.

Slow FF Q output

Board label: SLOW_FF_Q
Grid location: C1

Description: This is the Q output signal of the slow flip-flop. This signal shows metastable behavior frequently.

SPI bus

Board label: SPI_SCLK, SPI_SS, SPI_MOSI
Grid location: G1, H1, H2, D1

Description: These are the SPI (Serial Peripheral Interface) serial bus signals. (See Figure 1.)

The SPI bus works as follows:

- SCLK rising edge clock
- Active Low SS
- Active High MOSI data

This is the beginning of the mixed signal chain. See the descriptions of these signals: DAC Input, Parallel and DAC Output.

Packets occur approximately every 500 µs. The SPI packet contents are transferred to the Parallel DAC Input bus at the end of the packet. The Parallel DAC Input bus then changes the voltage output of the DAC.

The resulting DAC output is a sine wave with an amplitude 0 to 3 volts, and a period of 31 ms.

The clock rate is a 200 kHz, 0 to 5 volt signal.

Spread spectrum clock

Board label: SS_CLOCK
Grid location: H4

Description: Nominally 98.5 MHz spread spectrum clock with triangular modulation for demonstrating timing measurement trends over time.

Step Edge X, Step Edge Y

Board label: STEP_EDGE_X, STEP_EDGE_Y
Grid location: C3

Description: These two identical step edge (rising edge) signals, when used together, let you demonstrate different probe loading effects. Connect two different probes simultaneously, with one on Step Edge X and the other on Step Edge Y, and compare the rise times from each probe for these identical signals.

For example, if you put a low input capacitance probe, like the Tektronix TPP1000, on one of these signals and an alternative, higher input capacitance probe, like the Tektronix P6139A, on the other signal, capture the waveforms on an oscilloscope and then overlay the two captured signals, the waveform from the lower input capacitance TPP1000 will show a faster rise time.

USB bus

Board label: USB_LS, USB_FS, USB_HS
Grid location: G5, H5, H6

Description: Universal Serial Bus signals, defined by USB 2.0, and driven as differential pairs:

- USB_LS signal, the Low Speed USB standard, transmitting data at 1.5 Mbit/s.
- USB_FS signal, the Full Speed USB standard, transmitting data at 12 Mbit/s.
- USB_HS signal, the High Speed USB standard, transmitting data at 480 Mbits/s.