Tektronix Logic Analyzers

▶ Family Selection Guide

▶ Applications

	TLA520x	TLA7012	TLA7016
Timing and State Analysis	Yes	Yes	Yes
Single-processor/Bus Analysis	Yes	Yes	Yes
Real-time Instruction Trace Analysis	Yes	Yes	Yes
Protocol Analysis	Yes	Yes	Yes
Source Code Debug	Yes	Yes	Yes
Performance Analysis	Yes	Yes	Yes
Multi-processor/Bus Analysis	No	Yes	Yes
Digital Stimulus and Control	No	Yes	Yes
Digital Signal Quality Analysis	Yes	Yes	Yes
System Validation	No	No	Yes

▶ Mainframe Selection

	TLA520x	TLA7012	TLA7016
Modular Mainframe	No	Yes	Yes
Number of module slots	Not applicable	2	6
Operating System	Microsoft Windows XP Professional with Multi-Lingual User Interface Pack		
Internal Display Size and Resolution	10.4 in. (26.4 cm), 1024x768	15 in. (38.1 cm), 1024x768	Requires either TLA7PC1 Benchtop PC Controller or user-supplied PC
External Display Resolution	1024x768 (Primary) 1600x1200 (Secondary)	1600x1200	1600x1200 (TLA7PC1) or dependent upon user-supplied PC
Number of External Displays	2	2	Up to 4 with TLA7PC1 and additional video display cards; Up to 8 with user-supplied PC and additional video display cards
Standard Data Window Types	Waveform, Listing, Graph, Histogram (Performance Analysis), Source Code, Protocol		
Remote Control with Microsoft .NET	Yes		

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	TLA520x	TLA7N4	TLA7NAx	TLA7Axx
Channels	34, 68, 102, 136	136 per module	34, 68, 102, 136 per module	34, 68, 102, 136 per module
Max Channels per Timebase (merged)	136	272 in TLA7012; 408 in TLA7016	272 in TLA7012; 680 in TLA7016	272 in TLA7012; 680 in TLA7016
Max Channels per Mainframe	136	272 in TLA7012; 816 in TLA7016		
Max Channels per System	136	2,176 (with eight TLA7012s and one TL708EX); 6,528 (with eight TLA7016s and one TL708EX		
Max Independent Buses per System	1	16 (with eight TLA7012s and one TL708EX); 48 (with eight TLA7016s and one TL708EX)		
State Clock Rate	235 MHz	100 MHz std.; 200 MHz opt.	235 MHz std.; 450 MHz opt.	120 MHz std.; 235, 450 MHz opt.
Max State Clock Rate	235 MHz	200 MHz	450 MHz	800 MHz (half channel mode)
Max State Data Rate	470/235 Mb/s (half/full channels)	400/200 Mb/s (half/full channels)	470/235 Mb/s (half/full channels)	1,250/900/450 Mb/s (quarter/half/full channels)
MagniVu™ Timing (all channels, all the time)	125 ps (8 GHz) with 16 Kb depth	500 ps (2 GHz) with 2 Kb depth	125 ps (8 GHz) with 16 Kb depth	125 ps (8 GHz) with 16 Kb depth
Simultaneous State and Timing Through Same Probe	Yes	Yes	Yes	Yes
Analog Measurements Through Same Probe	No	No	No	Yes
Timing	500 ps (2 GHz)/ 1 ns (1 GHz)/ 2 ns (500 MHz) (quarter/ half/full channels)	2 ns (500 MHz)/ 4 ns (250 MHz) (half/ full channels)	500 ps (2 GHz)/ 1 ns (1 GHz)/ 2 ns (500 MHz) (quarter/ half/full channels)	500 ps (2 GHz)/ 1 ns (1 GHz)/ 2 ns (500 MHz) (quarter/ half/full channels)
Analog Outputs (four per module - analog MUX)	No	No	No	Yes
Record Length	2 Mb/1 Mb/512 Kb to 32/16/8 Mb (quarter/half/full channels with timestamp)	128/64 Kb to 8/4 Mb (half/full channels with timestamp)	2 Mb/1 Mb/512 Kb to 128/64/32 Mb (quarter/half/full channels with timestamp)	512/256/128 Kb to 256/128/64 Mb (quarter/half/ full channels with timestamp)
Source Synchronous Clocking	Yes	No	No	Yes

▸ Digital Storage Oscilloscope Capability

	TDS Oscilloscopes[*1] (External)
Channels per Oscilloscope	2 and 4
Max Channels per Mainframe	4
Max Channels per System	4
Bandwidth	60 MHz to 15 GHz
Sample Rate	1.0 GS/s to 40 GS/s
Vertical Resolution	8-Bits and 9-Bits
Record Length	2.5 Kb to 64 Mb

[*1] For a complete list of currently supported TDS oscilloscopes, please visit our website http://www.tektronix.com/iview

▸ Pattern Generator Module

	TLA7PG2
Channels	64
Max Channels per Bus (merged)	128 (with TLA7012); 384 (with TLA7016)
Max Channels per Mainframe	128 (with TLA7012); 384 (with TLA7016)
Max Channels per System	1,024 (with eight TLA7012s and one TL708EX); 3,072 (with eight TLA7016s and one TL708EX)
Pattern Speed (half/full channels)	268/134 MHz
Record Length (half/full channels)	512/256 Kb to 2/1 Mb
Logic Families Supported	CMOS/TTL, ECL, LVCMOS, PECL/LVPECL, LVDS, Variable

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Our most up-to-date product information is available at:
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