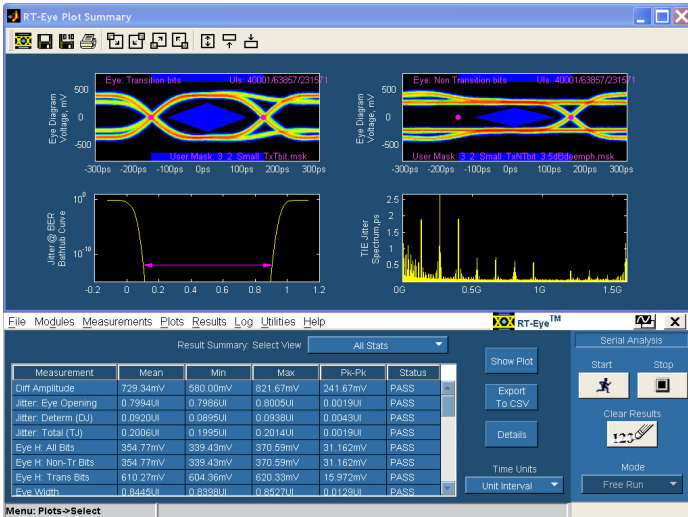


TDSRT-Eye™ v2.0

Serial Data Compliance and Analysis Software Data Sheet



- Amplitude, Timing, and Jitter Measurements (including RJ, DJ, and Total Jitter at 10^{-12} BER on Repetitive and Arbitrary Patterns)
- Bit Error Locator Highlights Mask Failures on the Real-time Waveform
- Automated Pass/Fail Waveform Mask and Measurement Limit Testing
- Multiple Graticule Plotting Windows for Simultaneous Eye-diagram, Histogram, Spectrum, and Bathtub-curve Analysis
- Compliance Analysis Modules (Optional) Provide Plug-fest Level Tests
 - Available: PCI Express (Opt. PCE), InfiniBand (Opt. IBA); SATA and SAS Analysis module (Opt. SST), FB-DIMM (Opt. FBD)
 - Other Standards: Under Development
- Custom and Standard Specific Report Generation

Applications

Analog Validation and Compliance Testing of Emerging Serial Data Standards Including:

- PCI Express
- FB-DIMM
- InfiniBand
- Serial ATA
- Serial Attached SCSI (SAS)
- Fibre Channel
- 10 GbE XAUI
- 10 GbFC XAUI
- IEEE 1394b
- RapidIO

Features & Benefits

- MyTest Provides Measurement Results with a Touch of a Button
- Serial Data Wizard for Easy Setup
- Real-time Acquisition and Analysis on Electrical Standards Beyond 10.25 Gb/s (DPO72004)
- Patented Real-time Eye (RT-Eye) Clock Recovery and Eye Rendering Provides:
 - High-precision Eye Diagrams and Accurate Jitter Measurements
 - Standard Specific Clock Recovery
 - Transition/Nontransition Bit Eye Diagram and De-emphasis Measurements
 - Accumulated Waveform Database Eye Diagrams
- Patented Software PLL-based Clock and Data Recovery Accurately Models System Performance
- SmartGating Feature for Flexible Clock Recovery and Measurement Windowing

Accurate, Simple, and Customizable Physical Layer Testing on Emerging Serial Data Standards Beyond 10 Gb/s

When designing to industry standards, analog validation and compliance testing is critical to ensure device interoperability. TDSRT-Eye v2.0 Serial Data Compliance and Analysis software (Opt. RTE), used with the DPO70000, TDS/CSA7000/B, and TDS6000/B/C Series of high-performance oscilloscopes and proper probing solutions, provides the complete solution for analog validation and compliance testing of serial data buses.

RT-Eye v2.0 Clock Recovery and Eye Rendering

The first step in creating an eye diagram and performing accurate jitter measurements on data is recovering the clock from the serial bit stream. The RT-Eye eye rendering technique provides user-selectable algorithms (PLL or Constant Clock) to recover the clock. This technique provides the following benefits:

High-precision Eye Diagrams – Since the waveform is captured from a single trigger event, and the clock is recovered through software, this method provides a much lower jitter noise floor (JNF) than most equivalent-time (ET) hardware-based clock recovery techniques.

Standard Specific Clock Recovery – Patented PLL-based clock recovery is most common in many data communications standards. However, some standards such as PCI Express require supporting many receiver clock recovery topologies such as phase interpolation and oversampling. Software-based clock recovery allows you to select the clock recovery method that best suits your device. Further, use of the SmartGating feature allows the user to define a clock recovery window within the acquisition as well as an additional analysis window that defines where in the recovery window the measurements will be made.

Transition/Nontransition Bit Separation and De-emphasis Measurements – The real-time capture provides the ability to differentiate between transition bits and trailing bits for mask testing and measurements useful in systems employing de-emphasis (form of active equalization also known as pre-emphasis or equalization). Amplitude measurements can be made separately on the emphasized bits and the non-emphasized bits, allowing a de-emphasis measurement ratio to be displayed.

Accumulated Waveform Database Eye Diagrams – The accumulated waveform database provides a three-dimensional eye-diagram plot. If the software is put in Free Run mode, the eye diagram is accumulated over time much like traditionally equivalent time displays.

Waveform Eye Diagrams and Jitter Measurements are Inseparable

In the past, waveform mask testing and jitter measurements have been performed with at least two, and sometimes three pieces of instrumentation. Waveform eye diagrams were viewed with sequential equivalent time-sampling oscilloscopes or real-time oscilloscopes operating in an equivalent-time mode. BERT and/or time interval analyzers were required to make total jitter measurements. The TDSRT-Eye v2.0 software uses patented techniques to separate jitter components (RJ, DJ, and TJ at 10^{-12} BER) in serial data bit streams captured with a real-time oscilloscope, whether the signal has a repeating pattern or if it is arbitrary. This technique is recognized by the T11.2 MJSQ as an alternative to using other specialized equipment. More recently, some standards in the computer industry, such as PCI Express and Serial ATA, require that jitter measurements be performed on a specified number of consecutive (contiguous) bits, a requirement only satisfied by real-time oscilloscope technology. Whichever jitter measurement method is required, TDSRT-Eye v2.0 software performs eye diagrams and various industry-specified jitter measurements from a single real-time waveform acquisition. Additional confidence can be gained by accumulating statistics over multiple acquisitions. This allows you to use a single high-performance real-time oscilloscope for design, debug, validation, and compliance of your serial data components.

Simple Parametric Limits Modules

Mask testing and jitter measurements performed with TDSRT-Eye v2.0 software can be turned into a custom compliance test by defining a Limits File and a User Mask file. A Limits File allows you to select which measurements you want to perform Pass/Fail compliance testing on. Test limits on masks and measurements can be edited and saved into User Mask and Limits Files.

Standard-specific Compliance and Analysis Modules

TDSRT-Eye v2.0 software can also be configured with optional compliance and analysis modules. The modules provide specific Pass/Fail waveform mask and measurement limit testing in conformance with industry-hosted plug fests and workshops. Compliance and analysis modules currently available include:

PCI Express Compliance Module – The PCI Express compliance module (Opt. PCE), when ordered with TDSRT-Eye v2.0 software, provides the complete solution for electrical compliance tests. Module includes physical layer measurements defined at the Driver, Add-in Card, System, Receiver, and Reference Clock test points as defined in Revision 1.0a and 1.1 of the PCI Express specifications (Base Specification and Card Electrical Mechanical (CEM) Specifications). The Use SigTest feature allows for the import and automated setup for using the SigTest software provided by the PCI-SIG. Preliminary testing for Gen2 (5.0 Gb/s) is also provided.

FB-DIMM Compliance Module – The FB-DIMM (Fully Buffered - Dual Inline Memory Module) compliance module (Opt. FBD), when ordered with TDSRT-Eye v2.0 software, provides the complete solutions for electrical compliance tests. Module includes physical layer measurements defined in the JEDEC High-speed PTP (Point-to-Point) Link specification.

SATA and SAS Analysis Module – The SATA and SAS analysis module (Opt. SST), when ordered with TDSRT-Eye, provides the test solution to conduct electrical tests. Module includes physical measurements specified in SATA Working Group and T10 (SAS) committee.

InfiniBand Compliance Module – The InfiniBand compliance module (Opt. IBA), when ordered with TDSRT-Eye v2.0 software, provides the complete solution for electrical compliance tests. The module includes physical layer measurements called out in Chapter 6 of version 1.1 of the InfiniBand architecture specification.

Custom and Standard Specific Report Generation

Whether you're documenting results in the validation stage of your design or archiving compliance reports for future reference, the TDSRT-Eye v2.0 software provides both standard compliance report templates and a Report Generator that allows you to customize your test reports.

Characteristics

Bit Rates Supported – Minimum system (including probe) is defined by oscilloscope bandwidth (GHz)/1.5 Gbps for 3rd harmonic of fundamental signal frequency. Some standards require 5th harmonic. Consult industry working group for minimum oscilloscope bandwidth required for compliance.

MyTest – Combines saved setup, autoset, and run functions to provide results with a single button press.

Serial Data Wizard – Step-by-step for easy setup of Serial Analysis Module.

Measurements

Timing – Eye Width, Rise Time, Fall Time, Unit Interval, Bit Rate, Differential Skew.

Amplitude – Eye Height, Differential Voltage, High Amplitude, Low Amplitude, Common-mode DC Voltage, Common-mode AC Voltage, De-emphasis.

Jitter – Patented RJ/DF decomposition resolves jitter at BER (RJ, DJ, TJ, and Jitter Eye Opening for a specified Bit Error Ratio) for repeating or arbitrary patterns, Jitter TIE (Data Time Interval Error).

Reference Clock (Opt. PCE and FBD only) – Voltage (High, Low, Differential), Timing (Rising Edge, Falling Edge, Period, Duty Cycle), Jitter (Cycle-Cycle, Total).

Mask and Measurement Compliance Testing (Pass/Fail) – User-definable mask geometries (User Mask) and measurement limit definition (Limits File). Masks and Limits hardcoded in Compliance Modules.

Clock Recovery – Patented software PLL (fc/1667 or custom) – User-definable 1st order or 2nd order with damping factor, Mean, Median, Gated.

SmartGating with Scan – Provides up to two gated regions for clock recovery and measurement results. Gating Options - Cursors, Unit Intervals, Edges. Gated regions can be set up to scan a portion or all of the waveform.

Population Control – Halts measurement accumulation on a specified measurement population or number of acquisitions.

Plots – Define up to four plots on multiple graticules. Plots can be viewed on instrument display or second monitor. Supported Plot Types: Patented Real-time Eye Diagrams with and without mask (Transition Bit, Nontransition Bit, All Bits), Waveform (with Bit Error Locator), Histogram, Spectrum, Bathtub Curve.

Worst-case Waveform Logging – Provides capture of worst-case waveform for specified test condition.

Remote Control for Automation – The software can be controlled over GPIB or 100BaseT LAN connection. Windows and Unix remote operation is supported.

Online Help – Provides easy reference to standard test definitions.

Tektronix Oscilloscopes Supported

DPO/DSA70000, DPO7000, TDS6000/B/C, and TDS/CSA7000/B Series oscilloscopes (1.5 GHz models and above)

Minimum System Requirements (Legacy Products)

- Windows 2K OS (order upgrade TDS7UP, CSA7UP, or TDS6UP Opt. W2K)
- SDRAM (order upgrade 040-1682-xx, 256 MB DIMM module)
- 850 MHz Processor (order upgrade TDS7UP, CSA7UP, or TDS6UP Opt. CPU)
- 512 MB minimum RAM: 1 GB strongly recommended
- Version 2.5.3 Firmware and above

Ordering Information

TDSRTE

Includes: Software on a compact disk, online documentation, and quick reference guide. Five-time free trial available to all supported instrument models.

When Ordering a New Oscilloscope:

Order from the options listed below:

Opt. RTE – RT-Eye™ v2.0 Serial Data Analysis Software (Requires ≥ 1.5 GHz instrument).

Opt. PCE – Adds PCI Express Compliance Module (Requires RTE and ≥ 4 GHz instrument).

Opt. IBA – Adds InfiniBand Compliance Module (Requires RTE and ≥ 4 GHz instrument).

Opt. FBD – Adds Fully Buffered DIMM Compliance Module (Requires RTE and ≥ 6 GHz instrument).

Opt. SST – Adds SATA and SAS Analysis Module (Requires RTE and ≥ 6 GHz instrument).

When Upgrading an Existing Oscilloscope:

Order from the options listed below:

Opt. RTE – RT-Eye™ v2.0 Serial Data Analysis Software.

Opt. PCE – Adds PCI Express Compliance Module (Requires RTE and ≥ 4 GHz instrument).

Opt. IBA – Adds InfiniBand Compliance Module (Requires RTE and ≥ 4 GHz instrument).

Opt. FBD – Adds Fully Buffered DIMM Compliance Module (Requires RTE and ≥ 6 GHz instrument).

Opt. SST – Adds SATA and SAS Analysis Module (Requires RTE and ≥ 6 GHz instrument).

Recommended Accessories

P7500 – Trimode differential probe.

P7313SMA – 12.5 GHz differential acquisition system with SMA inputs.

AWG7102 – Arbitrary waveform generator.

DTG5274 – Data timing generator.

Test Fixtures

SATA Test Fixtures

TF-SATA-NE Serial ATA Near-end Test Fixture

TF-SATA-FE Serial ATA Far-end Test Fixture

TF-SATA-IS Serial ATA In-system Test Fixture

SATA Test Fixtures are available from –

Crescent Heart Software / Crescent Heart Systems

2143 SE 55th Avenue, Portland, OR 97215-3925 USA

503-232-2232 voice / 503-232-2255 fax

<http://www.c-h-s.com/>

E-mail - sales@c-h-s.com

PCI Express Test Fixtures –

Refer to www.pcisig.com for CBB (Compliance Base Board) and CLB (Compliance Load Board).

InfiniBand Test Fixtures –

Consult IBTA Electrical Compliance WG.

FB-DIMM Test Fixtures –

NEX-TDSFBDP: FBD Oscilloscope Probing Kit available through Tektronix partner, Nexus Technology at <http://www.busboards.com>.

TDS4238B: JEDEC Slot Parametric Test Fixture for Slot Test Point testing. For more details, contact your Tektronix representative.

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For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit www.tektronix.com



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