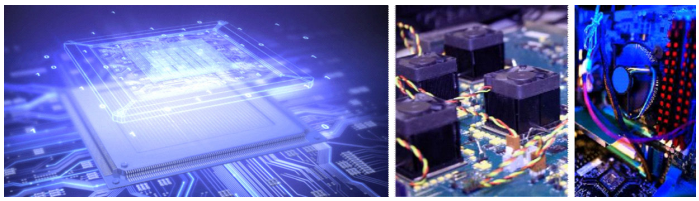
Certus ASIC Prototyping Debug Solution

Providing Full RTL-Level Visibility for Multi-FPGA Prototypes



Features & Benefits

- Full RTL-level Visibility
- Single Time-correlated System View of ASIC Design
- Compressed, Loss-less System-scale Time Captures
- Cycle-accurate Conditional Capture
- RTL-level Naming including Complex and Enumerated Types
- Complex, Multi-state Triggering
- Seamless Integration with FPGA Vendor CAD Flows

Tektronix®

Overview

Certus ASIC prototyping solution provides full RTL-level visibility into multi-FPGA prototyping platforms to change the way engineers approach ASIC prototyping, break critical bottlenecks, and substantially reduce cost and time to comprehensively verify complex ASIC design.

Certus is a flexible and proven solution for your most complex debug challenges. Certus can be used on all high-end Xilinx or Altera FPGAs and across a wide range of existing FPGA prototyping boards regardless of the I/O or FPGA topology of your particular ASIC design. Certus requires no special I/O, connectors, or FPGA topology. Simple JTAG connectivity allows full time-correlated debug across FPGAs.

Certus Implementor

The easy-to-use Certus Implementor tool applies advanced proprietary algorithms to help you quickly select thousands of signals of interest to create full visibility. All modifications are done at the RTL-level and work seamlessly through the Xilinx, Altera, Mentor, or Synopsys tool flows.

The Implementor can be used before or after partitioning of the design in a multi-FPGA system.

Certus Analyzer

During verification, the capture probes are managed by the Certus Analyzer tool through the JTAG port. Complex triggers are easy to set up. The Certus Analyzer also takes the resulting highly compressed captures and uses proprietary algorithms to recreate the internal chip data and to time-correlate the captures from different clock domains and FPGAs into one view.

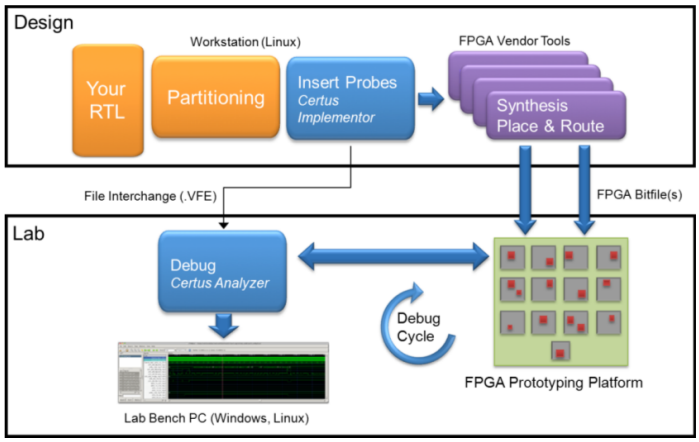
Characteristics

General

Characteristic	Description
Operating System Support	Ubuntu 9 (32 and 64 bit) Ubuntu 10 (32 and 64 bit) Red Hat Enterprise Linux 4 (32 and 64 bit) Red Hat Enterprise Linux 5 (32 and 64 bit) SUSE Linux Enterprise 11 (32 and 64 bit) Windows XP (32 and 64 bit) – Analyzer only Windows 7 (32 and 64 bit) – Analyzer only
Language Support	IEEE 1076-1993/1987 (VHDL) IEEE 1800-2009 (SystemVerilog) IEEE 1364-2001 (Verilog) “Mixed-language” combinations of the above

Target FPGA

Characteristic	Description
JTAG Probes	Altera USB-Blaster All Xilinx JTAG Probes (Xilinx Impact 12.4 or later must be installed) Amontec JTAGKey, JTAGKey2
JTAG TAP Interfaces	Altera TAP Xilinx Virtex-4, Virtex-5, Virtex-6, Virtex-7, Spartan-3, Spartan-6, Kintex-7 TAPs Tektronix-supplied JTAG TAP
FPGA Synthesis Tools/Flows	Mentor Precision (2010a or later) Synopsys Synplify (2010.09 or later) Xilinx ISE (12.4 or later) Altera Quartus (11.0 or later)



Certus design flow.

Instruments

Characteristic	Description
General	- Bit- and word-level compression of trace data before storage (independent per capture station) with potential compression ratios >1000X - Inter-station cross-triggering between all capture stations including across FPGAs - External trigger-in/trigger-out – requires two dedicated FPGA I/O pins
Number of Independent Capture Stations per FPGA	1 to 255
Number of Instrumented FPGAs per JTAG Chain	1 to 63
Station Widths (Configurable per capture station)	16, 32, 64, 128, 256, 512, 1024
Station Storage RAM Sizes (Configurable per station)	1 Kbits to 8 Mbits
Maximum Capture Station Operating Frequency (Measured on Virtex-5 FPGA)	Up to 150 MHz
Any-Signal-Any-Time Bit-level Signal Selection	Up to 128 K signals per station
Flexible Instrumentation Options to Allow Lightweight Capture Scenarios	LUT utilization formula: LUT Cost (measured on Virtex-6) ~= 1500 + 3000(m/128) + 1n m = maximum simultaneous observations n = total number of observable signals

Implementor

Characteristic	Description
General	- RTL-level naming for VHDL, Verilog, and SystemVerilog during instrumentation - Automatic clock discovery during instrumentation - Automatic assignment of observed signals to clock capture stations during instrumentation - Equivalent signal identification (prevents re-instrumenting of redundant RTL structures) - Hierarchical signal browsing during signal selection in Implementor - GUI or TCL-based Batch mode for Implementor - Implementor project file to enable efficient re-instrumentation of existing RTL - Minimum impact "in-place" modification of original design RTL - Automatic black-boxing of unknown modules - User-controlled black-boxing of modules pre-elaboration (increases runtime performance)
Instrumentable RTL Constructs	Input Ports Output Ports Sequential Elements Combinational Signals Base elements of multi-dimensional arrays (all languages) Base elements of complex data types and interfaces (VHDL and SystemVerilog) Enumerated types (VHDL and SystemVerilog)
OptiRank (Design or block level)	State Machine Identification Output Ports Critical Node Identification Critical Node Ranking
Automatic Signal Selection during Instrumentation (at any design level)	All inputs All outputs All flip-flops All state bits
Import of Signal Selection in Implementor from Existing Formats	Verdi session file DVE session file Plain Text XML

Analyzer

Characteristic	Description
General	- Time correlation of capture station data across clock domains and FPGAs (single coherent waveform view from all instruments) - GUI or command-line based Batch mode for Analyzer - Analyzer project with unlimited named configurations to store signal selections and triggers - VCD file generation to enable waveform viewing with industry-standard waveform viewers - User-configurable automatic launch of waveform viewer from Analyzer window - RTL-level naming for analysis and data presentation - Hierarchical browsing of signals during signal selection in Analyzer - Automatic real-time frequency detection on a per capture station basis
Time-aware Conditional Capture	Continuous mode Windowing mode
Bus-based Triggering	Up to width of capture station
Multi-state triggering	Up to 2 states per station

Ordering Information

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For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit **www.tektronix.com**

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