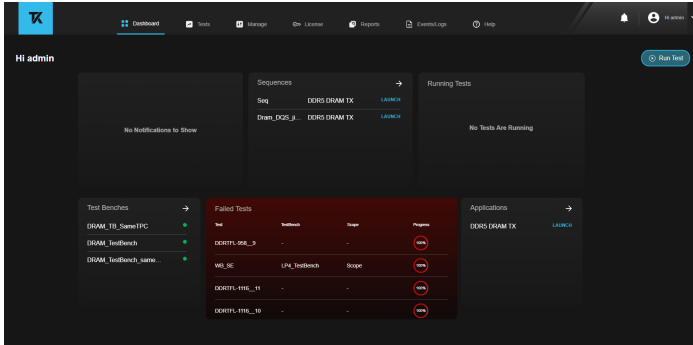


Clarius DDR5 DRAM Tx Compliance and Debug Solution Datasheet



The DDR (Dual Data Rate) is a dominant and fast-growing memory technology. It offers high data transfer rates required for virtual computing applications, from consumer products to the most powerful servers. The high speed of these signals requires high-performance measurement tools. The Tektronix Clarius Compliance DDR5 DRAM Transmitter solution is an automated test application used to validate and debug the DDR5 designs of the DUT as per the JEDEC specifications. The solution enables you to achieve new levels of productivity, efficiency, and measurement reliability.

The Clarius compliance is a new-generation compliance test automation software platform that offers a range of features and benefits as follows:

- High asset utilization and faster test times - Disaggregated architecture to offload analysis from the oscilloscope.
- Easy workflow integration – Leverage REST API's and SDK for faster automation.
- Unified user interface for all technology standards across Transmitter and Receiver.
- Integrated data management for results, reports, and waveforms in UI along with dashboard view.

Key features

- Supports 37 measurements of DDR5 DRAM Tx Tests as per DDR5 JEDEC specification:
 - Supports 12 Tx DQS Jitter Tests
 - Supports 13 Tx DQ Jitter Tests
 - Supports 12 Tx DQ Stressed Eye Tests
- The user-defined acquisition mode enables users to conduct application measurements by adjusting the oscilloscope settings, such as sample rate, record length, bandwidth, and other parameters according to their preferences and requirements mode for all scenarios.
- Retain Vertical Scale setting supported during acquisition for all scenarios.
- Customize Number of UIs for Tx DQ Stressed Eye test.
- Custom BER support for Tx DQ Stressed Eye tests.
- Custom Limit support for all tests.
- Supports multi-run feature for all measurements.

- Supports all the data rate as per JEDEC.
- Custom Data Rate support up to 15000 MT/s.
- Signal Validation support for all measurements.
- De-embedding support for all measurements.
- DUT automation support using batch file
- Automatic and manual support of Scope Noise Compensation for Tx DQS and Tx DQ Jitter tests.
- Automatic and manual support of DCA Training.
- Variable DUT Termination voltage support.
- Vref-DQ Mode support for Tx DQ Jitter and Stressed Eye tests using different methods.
 - Widest Eye Opening
 - Peak to Peak
 - Amplitude
 - User Defined
- DUT Power Cycle Utility: Manage power states (ON/OFF) and adjust voltage/current across all channels of a Keithley Power Supply via direct address connectivity.
- Import sequence feature allows for recalling test setups, so users don't have to manually configure each time.
- Single and Dual Rank DUT support.
- For the Stressed Eye test, two distinct analysis methods are available.
 - Use one edge of the UI
 - Use both edges of the UI
- Pause before acquisition feature is supported.

Applications

The Tektronix provides industry leading DDR5 solution that empowers engineers designing cutting-edge servers, computers, and embedded applications to confidently navigate both DDR5 memory design and validation. It provides a comprehensive suite of tools to tackle design challenges and ensure compliance with the latest DDR5 DRAM JEDEC specifications.

The Tektronix Clarius DDR5 DRAM TX compliance solution is compatible with the following Tektronix oscilloscope models:

- DPO72304SX, DPO72504SX, and DPO73304SX.
- Non-ATI channels of DPO75002SX, DPO75902SX, DPO77002SX, DPS75004SX, DPS75904SX, and DPS77004SX.

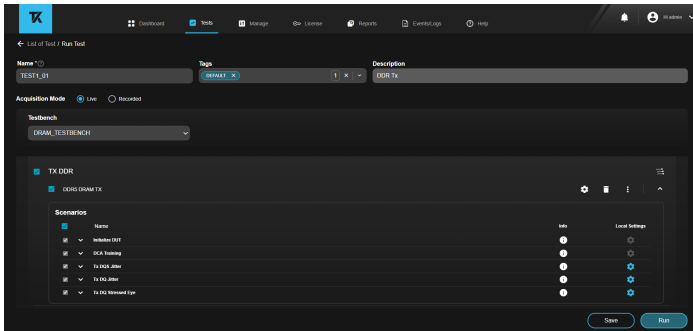
The above-mentioned Tektronix oscilloscopes are designed to meet the challenges of the next generation memory standards and provide the industry's leading vertical noise performance with the highest number of effective bits (ENOB) and flattest frequency response for oscilloscopes in their class.

Specifications

DDR5 DRAM Tx tests

The Clarius DDR5 DRAM Tx solution streamlines the compliance testing process for DDR5 systems and devices, empowering you to achieve faster time-to-market with several innovative features.

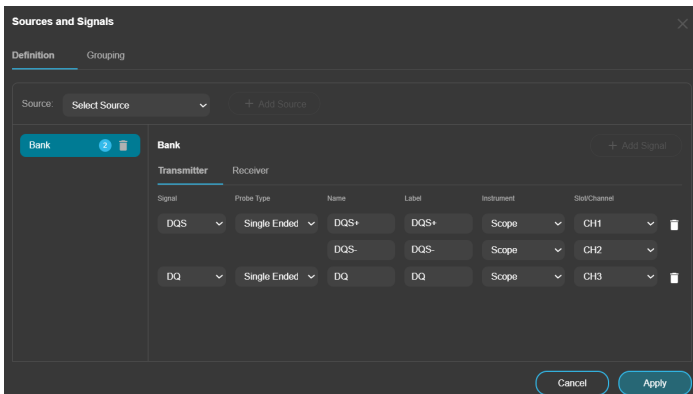
Experience a user-friendly, step-by-step interface that accelerates test setup. Effortlessly configure key settings like data rate, acquisition parameters, and test limits within a single, intuitive global configuration window. The interface groups tests logically by category (e.g., Tx DQS Jitter, Tx DQ Jitter, Tx DQ Stressed Eye) and allows for individual measurement selection within each group.



Clarius DDR5 DRAM Tx – application launch screen

Sources and signals

The Clarius DDR5 DRAM Tx application comes with a unique feature to select or deselect the signal. Once the signal is selected in the sources and signals panel, the user can select the signal source connected to the oscilloscope.



Sources and Signals panel – signal source selection

User defined acquisition mode

The Clarius DDR5 DRAM Tx application empowers users with granular control over oscilloscope settings through User Defined Acquisition (UDA) mode. This allows customization of scope acquisition parameters like sample rate, bandwidth, record length etc directly within the automation framework. UDA facilitates tailored test setups for specific JEDEC DDR5 compliance needs, streamlining workflows and reducing errors.

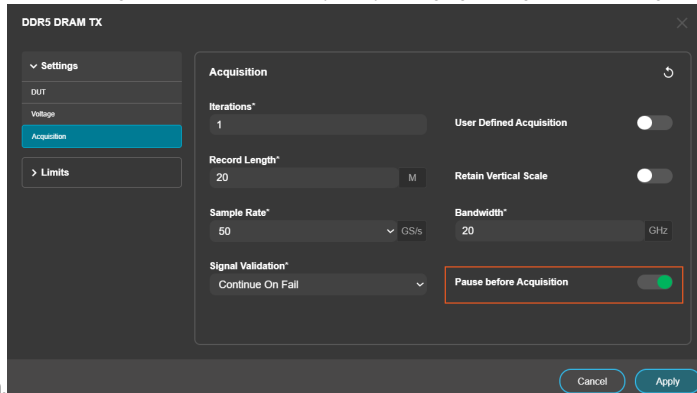
UDA's control extends beyond compliance testing. By adjusting acquisition settings on-the-fly during test execution, engineers can gain deeper insights into signal behavior, enabling faster debug and issue resolution.

DCA Training

The Duty Cycle Adjuster (DCA) Training algorithm uses period and duty cycle measurements on the ODD and EVEN cycle of the DRAM clock to determine the DCA optimal mode register settings. This presents a significant advancement in addressing the industry's critical need to improve signal reliability and performance by reducing duty cycle error and phase mismatch translated jitter.

Pause before acquisition

Gain more control on signal validation and analysis by changing settings/scripts during the test run using Pause before



acquisition.

De-embed filters

Easily de-embed the fixture and cable effects by applying suitable de-embed filters within the DDR5 standard. Apply filter is applicable for all measurements and setting is present in test level setting.



De-embed filters

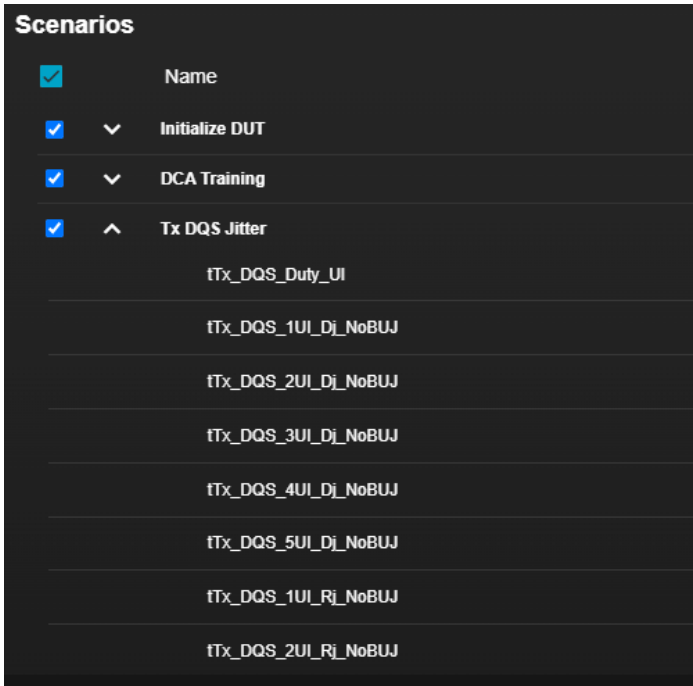
Comprehensive measurements

The Clarius DDR5 DRAM Tx compliance solution adds a long list of JEDEC specific measurements for DDR5 memory standards. It covers Jitter and Stressed Eye measurements as per the JEDEC standards.

Test selection

The Clarius DDR5 DRAM Tx compliance solution test selection panel allows the user to select the various measurements supported by the application.

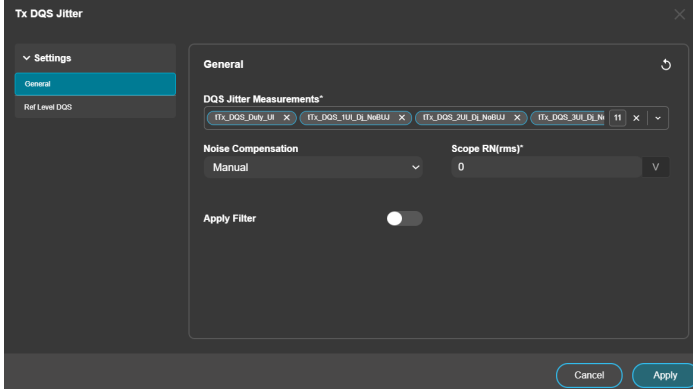
- Supports 37 measurements of DDR5 DRAM Tx Tests as per DDR5 JEDEC specification:
 - Supports 12 Tx DQS Jitter Tests
 - Supports 13 Tx DQ Jitter Tests
 - Supports 12 Tx DQ Stressed Eye Tests



Test selection – tree view of measurement

Configurations

Ease of use measurement configuration to configure measurements by group instead of running through all the 34 measurements.

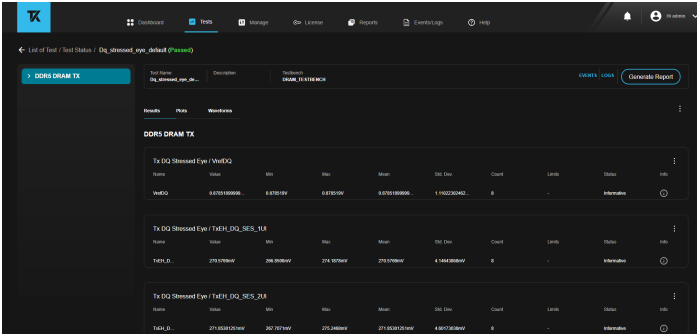


Configurations

Results and reporting

The measurement configurations and JEDEC pass/fail limits are automatically applied for the selected measurements based on the memory specification and the selected speed grade. The results report includes DDR measurements statistical data, measurement plots, and the screenshot of the waveforms with the cursors.

When test execution is complete, the application automatically opens the Results panel and displays the summary of test results.



Measurement results

| Clarius DDR5 DRAM TX Test Report | | | |
|----------------------------------|-------------------------|--------------------------------------|-------------------------------|
| Setup Information | | | |
| Test Name | DQ_stressed_Eye_Default | Scope Model Number | DPO733045X |
| DUT ID | DUT001 | Scope Serial Number | KR200033C |
| Date and Time | 2024-12-02 11:39:52.452 | SPC ₁ Factory Calibration | PASS. |
| Overall Test Result | PASSED | Scope F/W version | CF-91.1CT PV:10.14.1 Build 15 |
| Overall Execution Time | 00:10:58 | Clarius Version | 2.0.0-master.864 |
| Execution Mode | LIVE | App Version | 2.0.0-master.484 |
| Data Rate | 3200 MT/s | Jedec Specification | JESD79-SC.01_v1.31 |
| Iterations | 1 | Record Length | 20 M |
| User Define Acquisition | Disabled | Sample Rate | 50 GS/s |
| Retain Vertical Scale | Disabled | Bandwidth | 20 GHz |
| DIMM Type | RDIMM | DUT Type | DRAM |
| DDR5 Module Rank | Dual Rank | DUT Automation | Enabled |
| Signal Validation | Continue On Fail | | |
| Additional Comments | None | | |
| Probe and De-Skew Information | | | |
| Source | Probe Type | Probe Serial Number | De-Skew Value |
| CH1 | N/A | N/A | 0.000000 s |
| CH2 | TCA292D | None | 0.000000 s |
| CH3 | TCA292D | N/A | 0.000000 s |
| CH4 | TCA292D | N/A | 0.000000 s |
| Test Summary | | | |
| Test Name | Test Group Name | Status | |
| VreDQ | Tx DQ Stressed Eye | PASSED | |
| TxEH_DQ_SE5_1U1 | Tx DQ Stressed Eye | PASSED | |
| TxEH_DQ_SE5_2U1 | Tx DQ Stressed Eye | PASSED | |
| TxEH_DQ_SE5_3U1 | Tx DQ Stressed Eye | PASSED | |
| TxEH_DQ_SE5_4U1 | Tx DQ Stressed Eye | PASSED | |
| TxEH_DQ_SE5_5U1 | Tx DQ Stressed Eye | PASSED | |
| TxEW_DQ_SE5_1U1 | Tx DQ Stressed Eye | PASSED | |
| TxEW_DQ_SE5_2U1 | Tx DQ Stressed Eye | PASSED | |

Measurement report

Verification versus debug

The Clarius DDR5 DRAM Tx compliance solution offers a one-stop shop for both ensuring your designs meet DDR5 specifications and efficiently debugging any issues that may arise.

Automated Compliance Testing: Run comprehensive compliance tests with complete confidence. The solution automates the entire process, eliminating manual steps and ensuring consistent, reliable results.

Advanced Debug Capabilities: Should an issue surface during testing, the Clarius DDR5 DRAM Tx compliance solution goes beyond simply identifying the failure. It captures and stores worst-case signal waveforms for later in-depth analysis using DPOJET, our powerful advanced Jitter and Timing analysis software. DPOJET offers both generic jitter and timing analysis measurements to address a wide range of debug needs, as well as DDR5-specific measurements to ensure your design adheres to the latest memory standard. With complete control over measurement settings, you can customize each analysis to gain deeper insights into the root cause of failures, accelerating debug cycles.

Ordering information

Hardware requirements

| Item | Description | Quantity | Type | Vendor | Requirement |
|--|--|----------|-----------|-----------------------|-------------|
| DPO72304DX or MSO72304DX or DPO72304SX | ≥ 23 GHz Oscilloscope, Windows 10 OS | 1 | Equipment | Tektronix | Required |
| MP1900A or AWG5200 or AWG70000 | Bit error rate tester or waveform generator | 1 | Equipment | Anritsu/ Tektronix | Required |
| 2230-30-3 | 3 Channel programmable power supply | 1 | Equipment | Keithley | Required |
| Host PC/Laptop | Refer to System requirements | - | Laptop/PC | - | Required |
| MS46122B | USB Vector network analyzer, 1 MHz - 8 GHz | 1 | Equipment | Anritsu | Recommended |

Test fixtures and accessories

| Item | Description | Quantity | Type | Vendor | Requirement |
|-------------|---------------------------------------|----------|-----------|-----------|-------------|
| A9-CTC2-01 | CTC2 Test fixture | 1 | Fixture | Astek | Required |
| A9-AUTO-01 | Astek reset automation kit | 1 | Fixture | Astek | Required |
| PMCABLE1M | SMA-SMA, 1M, phase matched cable pair | 4 | Accessory | Tektronix | Required |
| 174-6657-01 | SMA-SMP adaptor, right angle (pair) | 4 | Accessory | Tektronix | Required |

Software requirements

Compliance

| Item | Description | Quantity | Type | Vendor | Requirement |
|--------------|---|----------|--------|-----------|-------------|
| DDR5 DRAM Tx | Clarius DDR5 Tx Compliance Oscilloscope Software. Refer to License details | 1 | Option | Tektronix | Required |

Debug

| Item | Description | Quantity | Type | Vendor | Requirement |
|--------|--|----------|--------|-----------|-------------|
| SDLA64 | Serial Data Link Analysis for Win 64-bit Scopes. | 1 | Option | Tektronix | Required |
| DJA | DPOJET Jitter Analysis. | 1 | Option | Tektronix | Required |

System requirements

| Prerequisites | Recommended requirements |
|------------------|---|
| Operating system | Windows 10 Enterprise and Pro (version 21H1 and above) or Windows 11 Enterprise and Pro (version 21H2 and above) Language: English (United States) only |
| CPU cores | 16 |
| RAM | 64 GB |
| Disk space | 300 GB HDD/SSD of free disk space |
| Internet speed | 1 Gbps |
| Browser | Microsoft Edge (default) or Google Chrome |

Table continued...

| Prerequisites | Recommended requirements |
|---------------------|----------------------------|
| Additional software | Python 3.12.x ¹ |

License options

Clarius DDR5 DRAM Tx Software Options

| License terms | License option | Description |
|---------------|-----------------|--|
| Subscription | AT-DDR5-Tx-NS1 | Clarius DDR5 Tx Automation Test Software; Node-locked, Subscription, 1 Year |
| | AT- DDR5-Tx-NS3 | Clarius DDR5 Tx Automation Test Software; Node-locked, Subscription, 3 Years |
| | AT- DDR5-Tx-FS1 | Clarius DDR5 Tx Automation Test Software; Floating, Subscription, 1 Year |
| | AT- DDR5-Tx-FS3 | Clarius DDR5 Tx Automation Test Software; Floating, Subscription, 3 Years |



Tektronix is ISO 14001:2015 and ISO 9001:2015 certified by DEKRA.



Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

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¹ Python installation is required for SDK and DUT control automator.

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For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit www.tek.com.

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