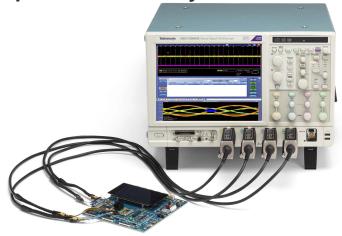
# Tektronix<sup>®</sup>

# LPDDR5-5X Memory Interface Electrical Verification and Debug

# Opt. LPDDR5SYS - System Level Transmitter Tests Datasheet



The DDR (Dual Data Rate) is a dominant and fast-growing memory technology. It offers high data transfer rates required for virtually computing applications, from consumer products to the most powerful servers. The high speed of these signals requires high-performance measurement tools. The Tektronix TekExpress DDR Tx is an automated test application used to validate and debug the LPDDR5-5X designs of the DUT as per the JEDEC specifications. The solution enables you to achieve new levels of productivity, efficiency, and measurement reliability.

#### **Key features**

- Supports 158 measurements of LPDDR5-5X System Transmitter Tests as per LPDDR5 JEDEC specification:
  - · 33 Clock measurements
  - 11 Write Clock measurements
  - 58 Write Data measurements
  - 1 Write Data tDQ2DQ measurement
  - 30 Read Data measurements
  - 13 CA Rx Specification measurements
  - 12 CS Rx Specification measurements
- User-Defined Acquisition (UDA) mode for Clock, Write Clock, CA, CS, Data Strobe, and data for both Write and Read traffic (or bursts).

**UDA**: The TekExpress DDR Tx for LPDDR5-5X Transmitter Solution puts control back where it should be, with the user. User defined acquisition mode allows you to run LPDDR5-5X JEDEC compliance measurements by customizing scope settings like sample rate, record length, bandwidth, and more

- De-embedding support for Clock, Write Clock, CA, CS, Data Strobe, and data for both Write and Read traffic (or bursts)
- Number of UIs support for Clock, Write Clock and Read/Write data measurements

- Multi-Run feature is applicable for all tests
- Save worst case waveform in known/TekExpress sessions
- Retain Vertical Scale settings supported during acquisition
- · User-friendly measurement configurations
- Test report to reflect all the statistics of the measurement
- User can select the source and the channel in the acquisition panel
- Multiple Burst Detection Method supported Read and Write, Write Only, Read Only, and Visual Search
- Hexagon shape mask and margin analysis for Write Data, CA, CS Eye measurement
- Custom Data Rate support upto 15000MT/s
- Single Ended mode support

#### **Applications**

Tektronix provides the most comprehensive solution to serve the needs of the engineers designing DDR silicon for server, computer, graphics systems, mobile, embedded systems, and for those who are validating the physical-layer compliance of DDR Memory Compliance Test Specification.

The Tektronix option LPDDR5SYS (TekExpress DDR Tx) includes compliance and debug solution for the following:

- DRAM components
- System boards
- · Embedded systems
- Mobile
- Automotive
- Internet of things (IoT)

The Tektronix option LPDDR5SYS is compatible with the following Tektronix oscilloscope models:

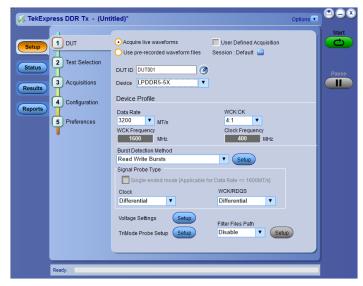
- MSO71604DX, MSO72004DX, MSO72304DX, MSO72504DX, and MSO73304DX.
- DPO71604DX, DPO72004DX, DPO72304DX, DPO72504DX, and DPO73304DX.
- DPO71604SX, DPO72004SX, DPO72304SX, DPO72504SX, and DPO73304SX.
- Non-ATI channels of DPO75002SX, DPO75902SX, DPO7702SX, DPS75004SX, DPS75904SX, and DPS77004SX.

The above-mentioned Tektronix oscilloscopes are designed to meet the challenges of the next generation memory standards and provide the industry's leading vertical noise performance with the highest number of effective bits (ENOB) and flattest frequency response for oscilloscopes in their class.

#### LPDDR5-5X system level tests

The Tektronix TekExpress DDR Tx solution reduces the effort and accelerates the compliance testing for DDR systems and devices with several unique and innovative capabilities.

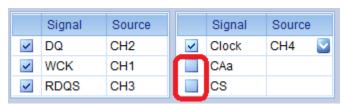
The TekExpress DDR Tx application provides a simple, step-by-step, and easy-to-use interface to speed up the testing process. User can select the memory technology of interest in Device, Data Rate, Burst Detection Method, select the probing configuration used for Clock, and strobe in the Setup DUT panel. Perform the test selection in the next step as per the measurement group (Clock, Command Address, Data Strobe, and Data for both Read and Write traffic (or bursts)) and individual measurements within the group provide different methods of Burst detection.



TekExpress DDR Tx – application launch screen for LPDDR5-5X

#### **Acquisitions**

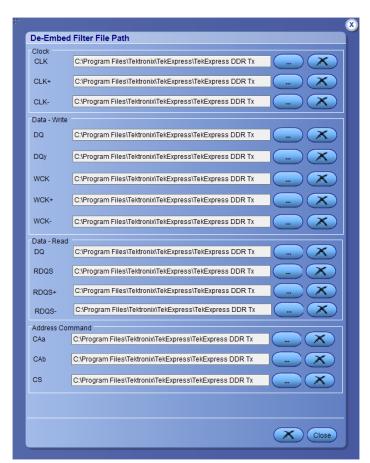
The TekExpress DDR Tx application comes with a unique feature to select or deselect the signal. Once the signal is selected in the acquisition panel, the user can select the signal source connected to the oscilloscope.



Acquisition panel - signal source selection for LPDDR5-5X

#### **De-embed filters**

Easily de-embed the interposer and the probe effects by applying suitable de-embed filters within the LPDDR5-5X standard.



De-embed filters for LPDDR5-5X

## **Comprehensive measurements**

The option LPDDR5SYS adds a long list of JEDEC specific measurements for LPDDR5-5X memory standards. The TekExpress DDR Tx application covers Electrical measurements, Timing measurements, and Eye Diagram measurements as per the JEDEC standards.

#### **Automated Read and Write Burst detection**

The TekExpress DDR Tx provides different ways to detect the burst cycles that are used to perform measurements:

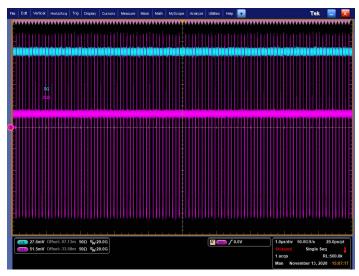
- Read Write Bursts when the DUT traffic is configured to send both Read and Write bursts then this method is used for burst detection.
- Write Only when the DUT traffic is configured to send all Write Bursts then this method is used for burst detection.
- Read Only when the DUT traffic is configured to send all Read Bursts then this method is used for burst detection.
- Visual Search defining Visual Trigger areas to identify and gate area of interest for measurements

Burst Detection Method
Read Write Bursts
Read Write Bursts
Write Only Bursts
Read Only Bursts
Visual Search

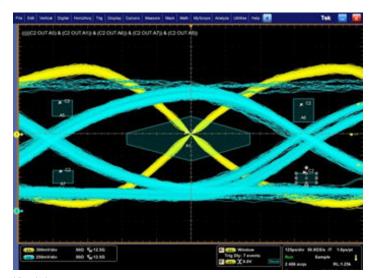
#### Burst detection



Automated Write Burst detection - for Write Bursts



Automated Read Burst detection - for Read Bursts

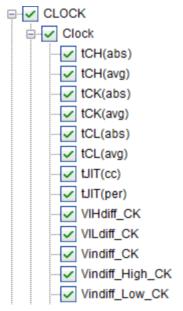


Visual trigger

#### **Test selection**

The TekExpress DDR Tx test selection panel allows the user to select the various measurements supported by the application.

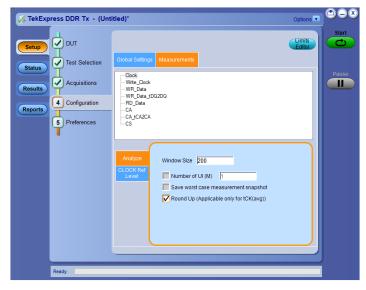
- Supports 158 measurements of LPDDR5-5X System Transmitter Tests as per LPDDR5 JEDEC specification:
  - 33 Clock measurements.
  - 11 Write Clock measurements.
  - 58 Write Data measurements.
  - 1 Write Data tDQ2DQ measurement.
  - 30 Read Data measurements.
  - 13 CA Rx Specification measurements.
  - 12 CS Rx Specification measurements.



Test selection panel - tree view of measurements

#### **Configurations**

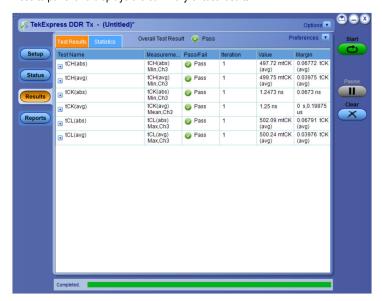
Ease of use measurement configuration to configure measurements by group instead of running through all the 50+ measurements.



## Results and reporting with waveform

The measurement configurations and JEDEC pass/fail limits are automatically applied for the selected measurements based on the memory specification and the selected speed grade. The results report includes DDR measurements of statistical data, measurement plots, and the screenshot of the waveforms with the cursors. Hyperlinks within the report allow you to navigate between the sections.

When test execution is complete, the application automatically opens the Results panel and displays the summary of test results.



Measurement results

		aive				TekEx	press I	DDR Tx						
IE/	tro	ШХ				Transn	nitter Tes	t Report						
Setup Informa	tion													
DUT ID				UT001			Scor	e Model			DPO77002	-SX		
Date/Time				6/2023 3:05:23	PM			e Serial Number			KR200027			
Device Type					SPC, Factory Calibration				PASS: PASS					
TekExpress W					e F/W Version				GF:91.1CT FV:10.14.0 Build 13					
App Version								10.5.0.8						
JEDEC Spec Re	C Spec Revision JES D209-58			Cloc	Clock Signal Probing			Differentia	Differential					
DUT Signal	ignal Live			WCF	WCK/RDQS Signal Probing			Differentia	Differential					
User Defined				isabled				Rate			3200 MT/s			
Overall Execution Time				0:00:44			Clos	k Frequency			800 MHz			
Overall Test R	esult		Pa	133				Frequency			1600 MHz			
								Clock			2:1			
							Bano	lwidth			20 GHz			
DUT COMMEN	T:	General Co	mment - DDR	Tx										
Probe Informa	tion													
Source				gnal			Prob	e Type			Probe Seria	al Number		
CH1			-					292D"			"None"			
CH2			-				*nor				"N /A"			
CH3			С	lock				2920"			"N /A"			
CH4			-				*nor	e.			TN /AT			
(O(abs) (O(ass) (C(abs)					Pass Pass									
							Pass							
tCL(avg)							Pass							
tCH(abs)	Maximal						Pass Pass							
tCl.(avg) tCl(abs) Measurement	Meas use d Value	Test Result	Ite ration	Margin	Low Limit	High Limit	Pass Pass Std Dev	Mean	Max	Min	P-P	Population	Max-CC	Min-CC
eCH(abs) Measurement Details tCH(abs) Min, Ch3		Test Result	Ite ration	Margin 0.06772 tCK(a vg)	Low Limit 0.43 tCX(avg)	-	Pass Pass		Max 502.17 mtCK (avg)	Min 497.72 mtCK (avg)	P-P 4.4557 mtCK (avg)	Population 8000	Max-CC 3.0544 msCK (avg)	
tCl.(avq) tCH(abs) Measurement Details tCH(abs) Min.	Value 497.72 mtCK			0.06772 tCK(a		-	Pass Pass Std Dev \$67.84 utCK	(a 499.85 mtCK	502.17 mtCK	497.72 mtCK	4.4557 mtCK		3.0544 mtCK (avg)	-2.9339 (avg)
tCH(abs) Measurement Details tCH(abs) Min, Ch3	Value 497.72 mtCK			0.06772 tCK(a		-	Pass Pass Std Dev \$67.84 utCK	(a 499.85 mtCK	502.17 mtCK	497.72 mtCK	4.4557 mtCK		3.0544 mtCK (avg)	-2.9339 (avg)
tOL(avg)  tOH(abs)  Measurement Details tOH(abs) Min, Ch3 COMMENTS  tOH(avg)	Value 497.72 mtCK (avg)	Pass	1	0.06772 tCK(a vg)	0.43 tCK(avg)	N.A	Pass Pass Std Dev 567.84 utCK vg)	(a 499.85 mtCK (avg)	502:17 mtCK (avg)	497.72 mtCK (avg)	4.4557 m1CK (avg)	8000	3.0544 mtCK (avg) Back t	-2.9339 (avg)
tCL(sug)  tCH(sbs)  Measurement Details tCH(sbs) Min, Ch3 COMMENTS	Value 497.72 mtCK (avg) Measured Value			0.06772 tCK(a vg)	0.43 tCK(avg)	-	Pass Pass Std Dev \$67.84 utCK	(a 499.85 mtCK	502.17 mtCK	497.72 mtCK	4.4557 mtCK (avg)		3.0544 mtCK (avg)	-2.9339
tCL(avg) tCH(abs) Measurement Details tCH(abs) Min, Ch3 COMMENTS tCH(avg) Measurement Details tCH(avg) Min,	Value 497.72 mtCK (avg) Measured Value 499.75 mtCK	Pass Test Result	1 Iteration	0.06772 tCK(a vg)  Margin  0.03975 tCK(a	0.43 tCK(avg)	N.A High Limit	Std Dev 567.84 utCk vg) Std Dev 34.296 utCk	(a 499.85 mtCK (avg) Mean (a 499.85 mtCK	S02:17 mtCK (avg)  Max  499:96 mtCK	497.72 mtCK (avg)  Min 499.75 mtCK	4.4557 m tCK (avg)	8000 Population	3.0544 mtCK (avg)  Back t  Max-CC  13.133 utCK(a	-2.9339 (avg) Summary Min-CC -12.186
tCL(avg) tCH(abs) Measurement Details tCH(abs) Min, Ch3 COMMENTS tCH(avg) Measurement Details tCH(avg) Min, Ch3	Value 497.72 mtCK (avg) Measured Value	Pass	1	0.06772 tCK(a vg)	0.43 tCK(avg)	N.A	Pass Pass Std Dev S67.84 utCK vg) Std Dev	(a 499.85 mtCK (avg)	502.17 mtCK (avg)	497.72 mtCK (avg)	4.4557 mtCK (avg)	8000	3.0544 mtCK (avg) Back t	-2.9339 (avg) o Summary Min-CC
tCH(abs) Measurement Details tCH(abs) Min, Ch3 COMMENTS tCH(avg) Measurement Details tCH(avg) Min, Ch3	Value 497.72 mtCK (avg) Measured Value 499.75 mtCK	Pass Test Result	1 Iteration	0.06772 tCK(a vg)  Margin  0.03975 tCK(a	0.43 tCK(avg)	N.A High Limit	Std Dev 567.84 utCk vg) Std Dev 34.296 utCk	(a 499.85 mtCK (avg) Mean (a 499.85 mtCK	S02:17 mtCK (avg)  Max  499:96 mtCK	497.72 mtCK (avg)  Min 499.75 mtCK	4.4557 m tCK (avg)	8000 Population	Back t  Max-CC  13.133 usCK(avg)	-2.9339 (avg) o Summary Min-CC -12.186 (avg)
tCH(abs) Measurement Details IOH(abs) Min, Ch3 COMMENTS  TOH(avg) Measurement Details IOH(avg) Min, Ch3 COMMENTS	Value 497.72 mtCK (avg) Measured Value 499.75 mtCK	Pass Test Result	1 Iteration	0.06772 tCK(a vg)  Margin  0.03975 tCK(a	0.43 tCK(avg)	N.A High Limit	Std Dev S67.84 utCk vg) Std Dev 34.296 utCk	(a 499.85 mtCK (avg) Mean (a 499.85 mtCK	S02:17 mtCK (avg)  Max  499:96 mtCK	497.72 mtCK (avg)  Min 499.75 mtCK	4.4557 m tCK (avg)	8000 Population	Back t  Max-CC  13.133 usCK(avg)	-2.9339 (avg) o Summary Min+CC -12.186 (avg)
tCl(avg)  Measurement Details (CH(abs) Min, Ch(abs) Min, Ch(abs) Min, Ch(avg) Measurement Details tCH(avg) Min, Ch(avg) Mi	Value 497.72 mrCK (avg) Measured Value 499.75 mrCK (avg)	Pass Test Result	1 Iteration	0.06772 tCK(a vg)  Margin  0.03975 tCK(a	0.43 tCK(avg)	N.A High Limit	Std Dev S67.84 utCk vg) Std Dev 34.296 utCk	(a 499.85 mtCK (avg) Mean (a 499.85 mtCK	S02:17 mtCK (avg)  Max  499:96 mtCK	497.72 mtCK (avg)  Min 499.75 mtCK	4.4557 m tCK (avg)	8000 Population	Back t  Max-CC  13.133 usCK(avg)	-2.9339 (avg) o Summary Min-CC -12.186 (avg)
tCl.(avg)  rCH(abs)  Measurement Details (CHubs) Min. Chil COMMENTS  rCH(avg)  Measurement Details (CHubs)  COMMENTS  rCH(avg)  Measurement  rChil COMMENTS  rCH(avg)  Measurement  rChil COMMENTS	Value 497.72 mtCK (avg)  Measured Value 499.75 mtCK (avg)  Measured	Pass Test Result Pass	Ite sation	0.06772 tCK(a vg)  Margin 0.03975 tCK(a vg)	0.43 tCK(avg)  Low Limit  0.46 tCK(avg)	N.A High Limit	Pass Pass Pass Std Dev S67.84 urck vg) Std Dev 34.296 urck vg)	(a) 499.85 mtCK (avg) Mean (a) 499.85 mtCK (avg)	S02:17 mtCK (avg)  Max  499:96 mtCK	497.72 mtCK (avg)  Min 499.75 mtCK	4.4557 m tCK (avg)	8000 Population 7801	3.0544 mtCK (avg)  Back t  Max-CC  13.133 wtCK(avg)  Back t	-2.9339 (avg) o Summary Min-CC -12.186 (avg)
tCL(ave)  tCH(abs) Measurement Details (CH4abs) Min. Ch3 COMMENTS  tCH(ave) Measurement Details COMMENTS  tCH(ave) Min. Ch3 Measurement Details Measurement Details	Value 497.72 msCK (avg)  Measured Value 499.75 msCK (avg)  Measured Value	Pass Test Result	Ite ration I	0.06772 tCK(a vg)  Margin 0.03975 tCK(a vg)	0.43 tCK(avg)  Low Limit 0.46 tCK(avg)	N.A High Limit N.A	Pass Pass Pass Std Dev	(a 499.85 mtCK (avg) Mean (a 499.85 mtCK	S02:17 mtCK (avg)  Max  499.96 mtCK (avg)	497.72 mtCK (avg)  Min  499.75 mtCK (avg)	4.4557 m tCK (avg) P-P 200.47 utCK(avg) P-P	8000 Population	Back t  Max-CC  13.133 usCK(avg)	-2.9339 (avg) o Summary Min-CC -12.186 (avg) o Summary
tCL(avg) tCH(abs) Measurement Details (CH(abs) Min, Ch3 COMMENTS  CH4(avg) Measurement Details (CH4(avg) Min, Ch3 COMMENTS  CH4(avg) Min, Ch3 COMMENTS  COMMENTS  COMMENTS  COMMENTS  COMMENTS  COMMENTS  COMMENTS  COMMENTS	Value 497.72 mtCK (avg)  Measured Value 499.75 mtCK (avg)  Measured	Pass Test Result Pass	Ite sation	0.06772 tCK(a vg)  Margin 0.03975 tCK(a vg)	0.43 tCK(avg)  Low Limit  0.46 tCK(avg)	N.A High Limit	Pass Pass Pass Std Dev S67.84 urck vg) Std Dev 34.296 urck vg)	(a) 499.85 mtCK (avg) Mean (a) 499.85 mtCK (avg)	S02:17 mtCK (avg)  Max  499.96 mtCK (avg)	497.72 mtCK (avg) Min 499.75 mtCK (avg)	4.4557 m tCK (avg) P-P 200.47 utCK(avg)	8000 Population 7801	3.0544 mtCK (avg)  Back t  Max-CC  13.133 wtCK(avg)  Back t	-2.9339 (avg)  Summary  Min-CC -12.186 (avg)  Summary
tCH(abs)  tCH(abs)  Measurement Details  CCH(abs) Min. Chi CCH(abs) Min. Chi CCMMENTS  CH(avg)  Measurement Details  CCMMENTS  COMMENTS	Value 497.72 msCK (avg)  Measured Value 499.75 msCK (avg)  Measured Value	Pass Test Result Pass Test Result	Ite ration I	0.06772 tCK(a vg)  Margin 0.03975 tCK(a vg)	0.43 tCK(avg)  Low Limit 0.46 tCK(avg)	N.A High Limit N.A	Pass Pass Pass Std Dev	(a) 499.85 mtCK (avg)  Mean (a) 499.85 mtCK (avg)	S02.17 mtCK (avg)  Max  499.96 mtCK (avg)	497.72 mtCK (avg)  Min  499.75 mtCK (avg)	4.4557 m tCK (avg) P-P 200.47 utCK(avg) P-P	Population 7801	3.0544 mtCK (avg)  Back t  Mace-CC  4.3841 ps	-2.9339 (avg) Summary Min-CC -12.186 (avg) Summary Min-CC -4.4922
ICL (ang)  ICH (abs)  Measurement Details (CH (abs) Min. Ch3 COMMENTS	Value 497.72 msCK (avg)  Measured Value 499.75 msCK (avg)  Measured Value	Pass Test Result Pass Test Result	Ite ration I	0.06772 tCK(a vg)  Margin 0.03975 tCK(a vg)	0.43 tCK(avg)  Low Limit 0.46 tCK(avg)	N.A High Limit N.A	Pass Pass Pass Std Dev	(a) 499.85 mtCK (avg)  Mean (a) 499.85 mtCK (avg)	S02.17 mtCK (avg)  Max  499.96 mtCK (avg)	497.72 mtCK (avg)  Min  499.75 mtCK (avg)	4.4557 m tCK (avg) P-P 200.47 utCK(avg) P-P	Population 7801	3.0544 mtCK (avg)  Back t  Mace-CC  4.3841 ps	-2.9339 (avg)  Summary  Min-CC -12.186 (avg)  Summary  Min-CC -4.4922
TCL (ave) TCH (abs) Measurement Details (CH (abs) Min, Service Measurement (CH (abs) Min, Child TCH (ave) TCH (ave) Measurement TCH (ave) Measurement TCH (abs) Measurement TCH (abs) TCH (abs) Measurement TCH (abs) TC	Value 499.72 mtCK (ang)  Measured Value 499.75 mtCK (ang)  Measured Value 1.2473 ns	Pass Test Result Pass Test Result	Ite ration I	0.06772 tCK(a vg)  Margin 0.03975 tCK(a vg)	0.43 tCK(avg)  Low Limit 0.46 tCK(avg)	N.A High Limit N.A	Pass Pass Pass Std Dev	(a) 499.85 mtCK (avg)  Mean (a) 499.85 mtCK (avg)	S02.17 mtCK (avg)  Max  499.96 mtCK (avg)	497.72 mtCK (avg)  Min  499.75 mtCK (avg)	4.4557 m tCK (avg) P-P 200.47 utCK(avg) P-P	Population 7801	3.0544 mtCK (avg)  Back t  Mace-CC  4.3841 ps	-2.9339 (avg) Summary Min-CC -12.186 (avg) Summary Min-CC -4.4922
ICL (not)  ICH (abs)  Measurement Details  ICH (abs) Min. Cold  Cold  Cold  Cold  Cold  Cold  Cold  Cold  Cold  Measurement Details  COMMENTS  COMMENTS  COMMENTS  Measurement Details  Measurement Details  COMMENTS  COMMENTS  COMMENTS  COMMENTS  COMMENTS  COMMENTS  COMMENTS  COMMENTS	Value 497.72 mrCK (ang)  Measured Value 499.75 mrCK (ang)  Measured Value 1.2473 ns	Pass Test Result Pass Test Result	Ite ration I	0.06772 tCK(a vg)  Margin 0.03975 tCK(a vg)	0.43 tCK(avg)  Low Limit 0.46 tCK(avg)	N.A High Limit N.A	Pass Pass Pass Std Dev	(a) 499.85 mtCK (avg)  Mean (a) 499.85 mtCK (avg)	S02.17 mtCK (avg)  Max  499.96 mtCK (avg)	497.72 mtCK (avg)  Min  499.75 mtCK (avg)	4.4557 m tCK (avg) P-P 200.47 utCK(avg) P-P	Population 7801	3.0544 mtCK (avg)  Back t  Mace-CC  4.3841 ps	-2.9339 (avg) o Summary Min-CC -12.186 (avg) o Summary
tOL(abs)  tOH(abs)  Measurement Details  tOH(abs) Min, Sourcement Solidas) Min, Solidas Min, Sol	Value 499.72 mtCK (ang)  Measured Value 499.75 mtCK (ang)  Measured Value 1.2473 ns	Pass Test Result Pass Yest Result Pass	Iteration  Iteration  Iteration	0.06772 tCK(a vg)  Margin 0.03975 tCK(a vg)  Margin 0.0673 ns	0.48 tCK(avg)  Low-Limit 0.46 tCK(avg)  Low-Limit 1.18 ns	N.A. High Limit N.A. High Limit	Pass Pass Pass Std Dev Std Dev Std Dev 34.296 utck wg) Std Dev 777.66 fs	(a 499.85 mtCK (avg)  Mean  (a 499.85 mtCK (avg)  Mean  1.25 ns	502.17 mtCK (avg)  Max 499.96 mtCK (avg)  Masc 1.2526 ns	492.72 mtCK (avg) Min 499.75 mtCK (avg) Min 1.2473 ns	4.4557 m3CK   (avg)   P-P   200.47 u1CK(avg)   P-P   5.2582 ps	Population 7801	3.0544 mtCK (avg)  Back t  Macc-CC  13.133 utCK/a  vg)  Back t  Macc-CC  4.3841 ps  Back t	-2.9339 (avg) Summary Min-CC -12.186 (avg) Summary Min-CC -4.4922

Measurement report

#### Verification versus debug

The TekExpress DDR Tx application provides a comprehensive set of JEDEC timing and electrical measurements for the LPDDR5-5X standard. Also, it provides access to the DPOJET Advanced Jitter and Timing analysis engine that allows flexibility to reconfigure the existing measurements or to perform new measurements that are not defined by the JEDEC specification using new user-specified test limits.

### Oscilloscope triggering and waveform identification

The Tektronix Pinpoint® trigger system provides the most comprehensive high-performance trigger system in the industry. The Pinpoint trigger system encompasses threshold and timing related triggers, Dual A and B Event Triggering, Logic Qualification, Window Triggering, and Reset Triggering.

The Advanced Search and Mark feature in the Tektronix MSO/ DPO5000. DPO7000, and MSO/DPO70000 Series oscilloscopes find unique events in the waveforms. It scans acquired waveform data for multiple occurrences of an event and marks each occurrence.

The Search and Mark feature has a close relationship with the Pinpoint trigger system since they both can be used to discriminate signal characteristics. Search and Mark includes signal-shape discrimination features of the Pinpoint trigger system and extends them across live channels, stored data, and math waveforms.

The Visual Trigger makes the identification of the desired waveform events quick and easy by scanning all the acquired analog waveforms and comparing them with the geometric shapes on the display. By discarding the acquired waveforms which do not meet the graphical definition, Visual Triggering extends the oscilloscope's trigger capabilities beyond the traditional hardware trigger system.

# **Specifications**

# **Supported oscilloscopes**

- MSO71604DX, MSO72004DX, MSO72304DX, MSO72504DX, and MSO73304DX.
- DPO71604DX, DPO72004DX, DPO72304DX, DPO72504DX, and DPO73304DX.
- DPO71604SX, DPO72004SX, DPO72304SX, DPO72504SX, and DPO73304SX.
- Non-ATI channels of DPO75002SX, DPO75902SX, DPO7702SX, DPS75004SX, DPS75904SX, and DPS77004SX.

Data rate	Minimum bandwidth	Channels	Description
Up to 9600 MT/s	16 GHz	4	<ul> <li>MSO71604DX</li> <li>DPO71604SX</li> <li>DPO71604DX</li> </ul>

#### **Recommended probes**

Active probes	Description
P7720	20 GHz TriMode probe with TekFlex connector technology
P7716	16 GHz TriMode probe with TekFlex connector technology

Probe tips	Description
P77STFLXA/P77STCABL	Active, Solder-in Tip with TekFlex connector technology, probe tips to probe directly on the motherboard/vias or interposers with 0 $\Omega$ resistor.
P77STFLXB/P77STLRCB	Active, Solder-in Tip with TekFlex connector technology, probe tips to probe on the SI Interposer with 100 $\Omega$ resistor (Nexus XH Series Interposer).
P77STFLRA	Active, long reach solder-in tip with TekFlex connector technology
P77HTFLRA	Active, long reach high temperature solder-in tip with TekFlex connector technology
P77STFLRB	Active, long reach 55 $\Omega$ Solder-in tip with TekFlex Connector technology for DDR/LPDDR electrical Validation with interposers
P77HTFLRB	Active, long reach 55 $\Omega$ Solder in tip with TekFlex Connector technology for high-temperature DDR/LPDDR electrical Validation with interposers (up to 125 °C)
SI Interposer	EdgeProbeTM, Direct Attach, and Socketed Interposer are available from Nexus. Order directly from Nexus. Request the s-par files for all individual signals on the interposer instead of getting a generic nominal s-par model.
	Refer the Nexus's page for more information: www.nexustechnology.com/products/memory-interposers/lpddr5-mobile-memory-interposers/

# **Ordering information**

# To order a new DPO/MS070000 Series

Nomenclature	Description
SX, DX >= 16G	
DPO-UP LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO71604DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO71604SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO72004DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO72004SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO72304DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO72304SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO72504DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO73304SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO72504SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO73304DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO75002SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO75902SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO7702SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
MSO72304DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
MSO71604DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
MSO72004DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
MSO72504DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
MSO73304DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPS75004SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPS75904SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
Table continued	

Nomenclature	Description
DPS77004SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and
	Analysis Software (require options SDLA64, DJA, and VET)

## To order floating licenses on existing DPO/MS070000 Series

Product Nomenclature	Description	Mapped Options	Required Options
DPOFL-LPDDR5SYS	License; LPDDR5 System-level Tx TekExpress Compliance/ Debug Automation Software; Floating	LPDDR5SYS	SDLA64, DJA, and VET
DPOFT-LPDDR5SYS	License; LPDDR5 System-level Tx TekExpress Compliance/ Debug Automation Software; Floating Trial	LPDDR5SYS	SDLA64, DJA, and VET



Tektronix is ISO 14001:2015 and ISO 9001:2015 certified by DEKRA.



Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.



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For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit <a href="https://www.tek.com">www.tek.com</a>. Copyright © Tektronix, Inc. All rights reserved. Tektronix products are covered by U.S. and foreign patents, issued and pending. Information in this publication supersedes that in all previously published material. Specification and price change privileges reserved. TEKTRONIX and TEK are registered trademarks of Tektronix, Inc. All other trade names referenced are the service marks, trademarks, or registered trademarks of their respective companies.

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