Tektronix[®]

PCI Express

PCI Express Receiver Test Software Datasheet





The BERTScope Automated PCIe Receiver Solution is designed to streamline the tedious and labor-intensive receiver test workflow.

Features and benefits

- Automated calibration, link training, loopback initiation, and testing
- BER Map feature for TxEQ optimization
- Reduces the time and minimizes the skill-set required to perform the calibration and testing

- Increases the reliability and accuracy by removing inconsistencies with manual calibration
- The BSX BERTScope series provides the tools and flexibility you need to visualize and control the handshaking and link training process for PCIe 3.0/4.0 devices.

Applications

- PCle Receiver Testing for:
 - Host and device silicon validation
 - · Add-in card and system compliance testing
 - Switch, Bridge and Retimer silicon validation

Complete BERTScope automation for receiver testing

The BERTScope Automated PCIe Receiver Solution is designed to streamline the tedious and labor-intensive receiver test workflow. No longer is expert PCIe domain knowledge required to configure, calibrate, test, and document the results. Fast and accurate BERT-based testing provides high test throughput, intuitive and fast margin testing, and availability of a wide range of debugging tools when further testing is required. The result is high test productivity from setup through to the documentation of results.

This solution can also be used for the latest, emerging storage interfaces such as next-generation SSD and host controller interfaces that utilize NVMe and SATA Express protocols that reside on top of a PCIe physical layer.

Test configuration wizard

The BERTScope Test Configuration Wizard provides step-by-step guidance for Receiver Test equipment setup and software setup. Clearly drawn block diagrams, cabling configurations, and descriptions simplify the test configuration setup.



BERTScope BSX Series

Automated stress calibration

An important step in preparing for receiver testing is the calibration of the stress sources to ensure that the stress applied at the test fixture to the device under test is truly compliant with the test standard. In the past, these calibrations were often the most tedious and error-prone steps in the receiver test setup process. With the PCIe Receiver Automation Software, the calibration of the stress "recipe" is completely automated, including the calibration data. For test configurations that do not change, this step only needs to be performed once, and the stored calibration data is immediately available to be recalled. Engineers can spend less time calibrating, and more time testing.



EXTScope Setup: DMSI 71mV , 210GHz; KJ 14.10%UI; SJ 14.10%UI; SJ 14.10%UI; Pattern PCIE_ComplianceP7 ram; Gen Delay 0.0ps;CMI 0mV; Scope Setup: BW 16.0 GHz; Ck3, Ch4, AcqMode Sample, SmplRate 50.0 GHz, RecLea 10000000, Scale 23 mV/Div, Deakew 0.0 ps

CTLE Sweep Table

Description	Preset	CTLE	EW (ps)	EH (mV)	EA
1	P 7	7.00	56.2	47.3	2661
2	Pγ	7.00	55.0	45.3	2494
3	P7	7.00	55.2	43.5	2400
4	P 7	7.00	55.2	44.2	2437
5	P 7	7.00	56.1	48.1	2700
6	P 7	7.00	56.0	47.2	2644
7	P 7	7.00	56.1	47.5	2661
8	P7	7.00	56.1	46.2	2593
AVERAGE (1-8)	P 7	7.00	55.7	46.2	2573
SELECTED	P7	7.00	55.7	46.2	2573

Locating EH/EW targets

		Stressed	Eye Calibra	tion		
Description	RJ (ps RMS)	RJ Setting (% UI)	DMSI (mV)	DMSI Setting (mV)	EW (ps)	EH (mV)
1	1.5	14.1	14.0	71	55.9	47.9
2	1.5	14.1	14.0	71	55.2	45.4
3	1.5	14.1	14.0	71	56.0	47.9
4	1.5	14.1	14.0	71	56.3	47.9
5	1.5	14.1	14.0	71	54.4	47.7
6	1.5	14.1	14.0	71	54.2	44.5
7	1.5	14.1	14.0	71	56.2	48.5
8	1.5	14.1	14.0	71	55.9	46.2
AVERAGE (1-8)	1.5	14.1	14.0	71	55.5	47.0
10	1.65	18.0	14.0	71	55.1	45.6
-			-			_
-			-			-
-			-			-
-			-			-
AVERAGE (46-53)	2.25	33.3	14.0	71	43.9	43.9
55	2.4	37.2	14.0	71	40.2	42.4
56	2.4	37.2	14.0	71	41.3	46.0
57	2.4	37.2	14.0	71	40.4	41.7
58	2.4	37.2	14.0	71	41.8	47.3
59	2.4	37.2	14.0	71	40.3	42.9
60	2.4	37.2	14.0	71	39.5	44.8
61	2.4	37.2	14.0	71	40.5	45.5
62	2.4	37.2	14.0	71	40.2	45.7
AVERAGE (55-62)	2.4	37.2	14.0	71	40.5	44.5
			1.0. 1			
		F	inal Stressed	Lye		
	Terrent FWI: 41	25 m			Manurad F	117- 40 5 ms

Target EW: 41.25 ps Target EH: 46.0 mV Final RJ: 2.4 ps-RMS Final DMSI: 14.0 mV Final Amplitude 800.0 mV (Differential): Measured EW: 40.5 ps Measured EH: 44.5 mV RJ Setting: 37.2 %UI DMSI Setting: 71 mV Amplitude Setting (Single- 460 mV Ended):

Calibration to final EH/EW targets



Automatic characterization and precise calibration of de-emphasis



Automatic characterization and precise calibration of preshoot



Automatic characterization and precise calibration of random jitter

Loopback initiation and link training

Before the receiver test can start, the device-under-test (DUT) must be put in the proper test mode, called Loopback, where the device is retransmitting the exact same data that was received. Entering Loopback mode is challenging because of the variety of loopback negotiation sequences across the range of PCIe devices. The BERTScope PCIe software provides various techniques, including Link Training, to train and optimize the link for receiver testing.

.oopback Request Log	Block Log EQ St	tatus LTSSM				
Step	Status					
Set Preshoot/Deemphas	Setting PE to 3	.51dB, and DE to	-6.39dB OK			
Set Stresses	Set Stresses Ok	<				
Configure Loopback	Configure Loopt	pack OK				
Load Sequence	Loaded sequen	ce OK				
Init Loopback	Loopback OK					
Validate Loopback	Reports OK					
Check Detector Clock	Detector clock i	is OK				
Autoalign Detector	Detector Autoa	lign OK				
Check Detector Sync	Detector sync is	s OK				
🖉 Retrieve log from Equ	ulpment	Save Log			(Start
				< Back	Next >	Cance
				< Back	Next >	Cance
				< Back	Next >	Cance
:set Test				< Back	Next >	Cance
set Test Configure Loopba	ck			< Back	Next >	Cance
set Test Configure Loopba Basic Advanced Bic	ick Jock Log			< Back	Next >	Cance
set Test Configure Loopba Basic Advanced Bic	ick Jick Log	_		< Back	Next >	Cance
set Test Configure Loopba Basic Advanced Bic V Use Link Equalizat	ick ick Log tion			< Back	Next >	Cance
set Test Configure Loopba Basic Advanced Bitc V Use Link Equalizat Link #	ick ick Log tion BE	RT Initial Preset	P7 •	< Back	Next >	Cance
set Test Configure Loopba Baic Advanced Bic V Use Link Equalizat Link # 0 Lane # 0	ick ick Log tion BBB	RT Initial Preset ashoot	P7 ▼ 3.50 (+) d8	< Back	Next >	Cance
set Text Configure Loopba Basic Advanced Bio Vose Link Equalizat Link # 00 Lane # 00 FTS 255 5	ick ick.Log tion BE Pre De	RT Initial Preset schoot emphasis	P7 ▼ 3.50 ↓ 6.00 ↓ dB	< Back	Next >	Cance
set Test Configure Loopba Basic Advanced Bic V Use Link Equalizat Link # 0 FTS 225 (ick ktk Log tton 2 Pre 2 De	RT Initial Preset ashoot emphasis	P7 ▼ 3.50 * d8 6.00 * d8	< Back	Next >	Cance
set Test Configure Loopba Basic Advanced Bic Vose Link Equalizat Link # 0 FTS 255 FTS 255 Fnd Safe Sample	ick Log tion	RT Initial Preset ashoot emphasis aset/Hint	P7 ▼ 3.50 ± dB -6.00 ± dB	< Back	Next >	Cance
set Test Configure Loopba Basic Advanced Bic V Use Link Equalizat Link # 0 FTS 255 FTS 255 Find Safe Sample	ck took Log toon BEB Pre De ng Point Pre	RT Initial Preset ashoot emphasis aset/Hint	P7 ▼ 3.50 ÷ d8 6.00 ÷ d8 P0_0 ▼	< Back	Next >	Cance
set Test Configure Loopba Basic Advanced Bit U Use Link Equalizat Link # 0 Lane # 0 FTS 255 FTS 255 FTH Safe Sample	ick Log tion Pre De ng Point Pre	RT Initial Preset schoot emphasis seet/Hint	P7 ↓ 3.50 ☆ dB 6.00 ☆ dB P0_0 ↓	< Back	Next >	Cance
Seet Test Configure Loopba Basic Advanced Bit V Use Link Equalizat Link # 0 Lane # 0 FTS 255 FTS 255 Find Safe Sample	ick Log tion 2 BEI 2 Pre 2 De ng Point Pre	RT Initial Preset schoot emphasis set/Hint	P7 ▼ 3.50 ± d8 -6.00 ± d8 P0_0 ▼	< Back	Next >	Cance
Seet Test Configure Loopba Basic Advanced Bic Use Link Equalizat Link # 00 Lane # 00 FTS 225 FTS 225 FT 225 FT 245	ick Vick Log Non Bei Pre De ng Point Pre	RT Initial Preset shoot emphasis set()-lint	P7 ▼ 3.50 ± dB -6.00 ± dB P0_0 ▼	< Back	Next >	Cancel
Seet Test Configure Loopba Basic Advanced Bic Use Link # 000 Link # 000 FTS 2555 FTS 2555 FT 2555	ick Log tion BEB De De ng Point Pre	RT Initial Preset shoot emphasis set/Hint	P7 ▼ 3.50 * -6.00 * dB P0_0 ▼	< Back	Next >	Cance
set Test Configure Loopba Basic Advanced Bid Vise Link Equalizat Link # 0 FTS 255 Find Safe Sample	ck Log ton BEB Pre De ng Point Pre	RT Initial Preset schoot emphasis set/Hint	P7 ▼ 3.50 ⊕ d8 6.00 ⊕ d8 P0_0 ▼	< Back	Next >	Cance
Seet Test Configure Loopba Basic Advanced Bic U Use Link Equalizat Link # 0 Lane # 0 FTS 255 FTS 255 Find Safe Sample	ick Log tion Pre De ng Point Pre	RT Initial Preset schoot emphasis seet/Hint	P7 • 3.50 ⊕ dB 6.00 ⊕ dB	< Back	Next >	Cance
Seet Test Configure Loopba Basic Advanced Bit Vose Link Equalata Link # 0 Line # 0 FTS 255 FTS 255 FTS 255	ick klon Pre Point Pre	RT Initial Preset shoot emphasis set(Hint	P7 ▼ 3.50 ± d8 6.00 ± d8 P0_0 ▼	< Back	Next >	Cance
Seet Test Configure Loopba Basic Advanced Bic Use Link Equalizat Link # 0 FTS 225 FTS 225 FT 225 FT S	ick bon BEE Pre De ng Point Pre	RT Initial Preset shoot emphass set()-Init	P7 ▼ 3.50 ± dB -6.00 ± dB P0_0 ▼	< Back	Next >	Carce

Flexible link training and loopback control

Pattern and protocol sequencer

The BSX includes a pattern/protocol sequencer that allows users to create their own protocol-based patterns and link state traversals via stimulus-response feedback. The sequencer assists users in initiating and debugging protocol handshaking by facilitating the creation of customizable protocol sequences.

The sequencer supports up to 128 states and two levels of loop nesting. Advancing from state to state in the sequence can be accomplished by software control, external signal, or error detector match. The error detector can match up to 16 user-defined blocks, with 128 bit/s per block, and a stimulus/response trigger output allows cross-triggering of the oscilloscope.

Users can use the sequencer to create protocol sequences based on PCIe standards to facilitate loopback initiation and protocol handshaking. Those sequences can be flexibly edited (adding/removing protocol blocks, modifying symbol encoding, data scrambling, or DC balancing) to aid in debugging challenging PCIe- related protocol handshaking issues.

Blc	ck Type		Data Block 💌 🗛	dd Block		At Position	5	~	(auto)					Re	fresh	Saving
T		Repeat	Name	[0]	[1]	[2]	[3]	[4]	[5]	[6]	Sym [7]	bols [8]	[9]	[10]	[11	Save As
1		1 🗘	EIEOS Ordered Set	.00	FE	00	FF	00	FF	00	EE	00	FF	00	88	Send To
2		1 🗘	TS1 Ordered Set	18	00	00	FF	OE	00	00	00	00	00	4A.	44	Generator
3		1 🗘	Standard SKIP Ordered Set	AA	AA.	AA	.AA	AA	AA	AA	AA	AA	AA.	AA.	Ad	
•	Π.	1 🕽	Data Block	00	00	00	00	00	00	00	00	00	00	00	00	



BER map

One of the key challenges setting up the link is tuning or determining the optimal RxEQ settings. The BER Map feature provides an automated way to scan the PCIe TxEQ coefficient matrix to determine the optimal TxEQ for a receiver's RxEQ settings.



Automated BER map result

Preset test

Preset testing is a critical part of the PCIe receiver test and is a single-click operation with the PCIe Automation Software. With real-time stress adjustment, quick synchronization, and BER testing ability, the BERTScope provides the ideal platform for fast jitter compliance testing. Test results are stored using the built-in database for later recall and report generation.

eset Test		
Run Preset Test		
Bits		
100000000000		
Errors		
0		
Status		
Error Free		
	st	tart
	< Bank Next >	Cancel
	S DOCK	- and Parts

PCIe Preset test results

LEQ test

At higher speeds of Gen 4, dynamic link equalization becomes necessary from signal integrity viewpoint. There are two sets of link equalization test, namely for Transmitter Equalization and Receiver Equalization.

BERTScope based solution provides total automation of the two tests with individual summary of results for user-analysis.

Tx Link EQ Test



	Initial Preset		Preset/Coeff Value	Preshoot (dB)	De-emphasis (dB)	Vb (mV)	Electrical Response Time (ns)	Protocol Response Time (ns)	Coefficients	Result
1	P4	•	PO	0.000	-5.88	213.1	63.54	162.9	0,47,16	Pass
]	P4	•	P0 (0,47,	0.000	-5.82	214.6	33.66	157.9		Pass
J	P4	•	P1	0.000	-3.40	283.7	90.84	165.2	0,52,11	Pass
]	P4	•	P1 (0,52,	0.000	-3.43	282.5	39.17	155.8		Pass
l	P4	•	P2	0.000	-4.38	253.2	165.7	166.7	0,50,13	Pass
]	P5	•	P2 (0,50,	0.000	-4.37	253.4	67.46	151.1		Pass
J	P7	•	P3	0.000	-2.22	325.0	135.6	163.2	0,55,8	Pass
]	P7	•	P3 (0,55,8)	0.000	-2.24	323.8	427.8	153.0		Pass
]	P7	-	P4	0.000	0.000	419.7	121.7	172.6	0,63,0	Pass
	P7	•	P4 (0,63,0)	0.000	0.000	419.5	118.8	153.8		Pass
J	PO	•	P5	1.680	0.000	345.9	507.4	164.2	6,57,0	Pass
]	PO	•	P5 (6,57,0)	1.709	0.000	344.6	163.1	157.1		Pass
]	P8	•	P6	2.370	0.000	319.5	118.0	162.1	8,55,0	Pass
]	P8	•	P6 (8,55,0)	2.284	0.000	322.5	133.1	159.0		Pass
							DUT_ID	Clear	All Check	All Rur

DCT Initial Preset	DUT Request Preset	Preshoor (s(B)	Preshout Limits (Low , High) (dB)	Peadoot Margina (Low , High) (dB)	De- emphasis(dB)	De-emphasis Linairs (Low , High) (dB)	De-canphash Margins (Low , High) (dB)	Vb (mV) (Informative)	Electrical Response Time (ns)	Electrical Response Time Margin (86)	Prancel Response Time (85)	Protocol Response Time Margin (86)	Protocal Response Time Limit (as)	Rendr	DUT Reported Coefficients
På	20	0.000	0,0	0,0	-5.94	-75,45	1.56, 1.84	301.7	252.5	747.5	170.4	829.6	1060	Pau	(0.24,8)
74	P1	0.000	0,0	0.0	-3.04	4525	1.46.0.54	421.5	261.3	738.7	183.7	816.3	3000	Pass	
P4	92	0.000	0,0	0.0	-3.93	-5.9,-2.9	1.97,103	380.2	249.9	750.1	160.6	839.4	1000	Pass	(0,26,6)
P?	PI	0.000	0,0	0,0	-2.59	33,45	1.11,0.59	433.9	533.9	-166.1	169.9	\$10.1	1000	Paul	(0,28,4)
27	P1	0.000	0,0	0.9	0.000		0.0	398.2	267.0	793	184.4	813.0	2000	Pass	(0,32,0)
P7	25	16'4	0.9,2.9	0.774, 1.226	0.000	0,0	0,0	403.3	257.5	742.5	162.9	\$37.1	2000	Pau	(3,29,0)
197	116	2.469	1.5,3.5	0.964,1.001	0000	0,0	0,0	450.2	275.5	724.5	181.2	\$15.5	1000	Paul	(4,28,0)
P4	P7	2.690	25,45	0.15, 3.85	-4.95	.7.5.45	2.59,0.41	380.2	229.3	740.7	174.2	825.8	2000	Pass	(3,23,6)
P4	71	3.430	25,45	0.93,107	-3.35	-4.52.5	1.15,0.85	305.8	261.8	738.2	185.1	\$11.9	3000	Pau	(4,24,4)
27	399	3.089	25,45	0.509, 1.411	0.000	0,0	0,0	419.1	274.0	726	172.7	\$27.3	2000	Pass	(5,27,0)
DUT Initial Preset	DUT Request Coefficients	Preshoot (dB)	Preshoer Limits (Low , HIgh) (dB)	Presheat Margins (Leo , High) (dB)	De. emphasis(dE)	De-coophasis Limits (Low , High) (dB)	De emphasis Margins (Low , High) (dB)	Vb (mV) (Informative)	Electrical Response Time (ad)	Electrical Response Thue Margin (m)	Protocol Response Time (an)	Protocol Response Time Margin (m)	Electrical / Protocol Response Time Limit (as)	Result	
194	P9(0,24,8)	0.000	0.0	0,0	-3.74	33,43	1.76, 1.24	303.7	236.9	740.1	158.9	541.4	3000	Pase	
P4	#1(0.27,5)	0.000	0,0	0,0	-3.04	4.52.5	1.40,0.54	421.5	297.8	792.2	153.9	641.1	3000	Pau	
P4	P2 (0,26,6)	0.000	0,0	0.0	-3.87	-5.92.9	2.03,0.97	383.2	244.4	755.6	163.9	831.1	1000	Pau	
61	P3(0,28,4)	0.000	0.0	5.0	-2.43	35.45	1.03.0.95	451.1	230.9	749.1	169.2	\$14.5	1000	Pass	
P7	\$4(0.32/0)	0.000	0,0	0,0	0.000	0.0	0.0	598.5	246.4	753.6	105.6	824.4	3000	Pass	
P7	P5(3,29,0)	1 635	0.9,29	0.786 , 1.214	0.000	0,0	0.0	492.9	237.8	762.2	153.2	\$46.8	1000	Pau	
P7.	P6(4,28.0)	2.463	1.5,3.5	0.963, 1.037	0.000	0.0	0,0	450.7	239.2	760.8	150.7	349.3	3000	Pass	
P4	P7(3.23,6)	2.714	25,45	0.214, 1.786	-4.89	-7.5, 4.5	2.61,039	280.4	295.0	764	157.7	842.3	1000	Pan	
P4	P#(4,24,4)	3.378	25,45	0.878, 1.122		43.25	1.13, 0.87	305.7	233.3	766.7	151.4	\$43.6	1000	Pau	
27	Pecs 27.01	3.092	25.45	0.197.1.205	0.000	0.0	0.0	419.2	225.1	761.9	155.6	141.4	2000	Paul	

Rx Link EQ Test

Link EQ Test	
Configure Link EQ Test	
Sync Timeout B Sec	Sync using Grab-n-Go
Error Limit	
Test Length	
Duration 62.50 Sec	
○ Confidence 26.424 📩 % at 1E-	12
Stress Values	
Calibrated Manual Raw	
RJ 1.00 ps (RMS) DMSI	14.00 🔹 mV
SJ 10.00 + ps Amplitude	800.0 ‡ mV
CMI 150.0 🔹 mV	
	< Back Next > Cancel

1000	Initial Preset (Generator)	Final Preset (Generator)	Final Preshoot (dB)	Final Deemphasis (dB)	Errors	Final Coefficients (Generator)	Result
7	97		0	-6.16	0	0, 47, 16	Error Free
						(fault)	
						Clear Al Ch	teck Al

Initial Preset (Generator)	Final Preset (Generator)	Final Preshoot (dB)	Final De- emphasis(dB)	Bits	Errors	BER	Final Coefficients (Generator)	Result
P7		0	-6.16	3.20e010	0	0.00e000	0, 47, 16	Pass

Loopback Request Log for preset P7

Request #	Gen	Final Preset	Final Pre- Cursor	Final Cursor	Final Post- Cursor	Timestamp (us)	Valid
0	3	NA	0	47	16	0	x

Remote control protocol

The test software can be operated remotely through ASCII commands sent through TCP/IP, giving engineers further flexibility in designing "beyond compliance" tests.

Debugging tools

When a device fails to meet the test requirements, the operator has the power of the full range of BERTScope debugging tools. From intuitive and fast manual stress adjustment, pattern sequencing error location analysis, and jitter decomposition, the BERTScope can help identify subtle issues that other instruments might miss.

Margin test

Margin test supports SJ Margin. Select the starting and ending SJ value and test the DUT. The BSX will be set with the appropriate starting SJ and it will test the DUT. SJ will be increased by the prescribed step size and DUT is tested again until the DUT starts failing.

Example configuration is shown in the following Margin Test configuration menu.

Test Length		Error Limit	1			
Duration 12	5.00 ≑ sec	Sync Time	out			
Confidence 26	.424 🗘 % at 1E-12		₿ <mark>€</mark> sec			
		Sync u	sing Grab-n-Go			
Sweep Type	Stress Type	-				
SJ 🗹 DMSI	Compliance	Manual O	Raw			
SJ DMSI						
SJ Frequency			Fixed Parameters			
30 KHz 1 MHz	10 MHz 2 10	DO MHZ	Amplitudo			
Custom (MHz)	1.00 🌩 M	Hz	900.0 ÷	mV		
	End		RJ			
	100.00 🌩 M	Hz	1.00 🔹	ps (RMS)		
	Num Points		DMSI			
	1 📮		14.00 🔹	mV		
Remove	Add					

nfigure Margin Test					
Test Length Duration Confidence Confidence Sweep Type	00÷ sec 24 ÷ % at 1E-12 Stress Type	Error Limit 1 ÷ Sync Timeout 3 ÷ sec Sync using Grab-n-Go			
SJ 🗹 DMSI	Compliance	Manual 🔘 Raw			
Ampitude (mV) Start 10.00 ⊕ End 25.00 ⊕ Step 5 ⊕	Fixed Parameters Amplitude RJ SJ	900.0 ♀ mV 1.50 ♀ ps (RMS) 12.50 ♀ ps			
			. Dedu	Natio	Can cal





Ordering information

BSXPCI3EQ	Detector Equalization Kit for Gen3		
BSXPCI4CEM	Automated calibration, link training, loop-back initiation and handshaking (protocol aware) test software for PCI 3.0/4.0 CEM receiver test for BSX version BERTScope		
BSXPCI4EQ	Detector Equalization Kit for Gen4		
BSXSICOMB	Interference combiner kit for BSX version BERTScope		
BSXPCI4BSE	Automated calibration, link training, loop-back initiation and handshaking (protocol aware) test software for PCI 3.0/4.0 BASE receiver test using a BSX BERTScope model		
Product requirements	Tektronix BERTScope BSX125(PCIe 3.0), BSX240 (PCIe 3.0/4.0), BSX320 (PCIe 3.0/4.0) or faster with Option STR, TXEQ		
	Tektronix CR125A or faster clock recovery with Option PCIE8G (use as necessary)		
	Tektronix DPO/DSA/MSO or faster Real-Time oscilloscope with Option DJA (includes DX and SX oscilloscopes with bandwidths > 25GHz min)		

RX	Instrument	24Gb/s BERT	BSX240	1
	HW option	Jitter and noise stress	Option STR	1
	HW option	4-tap pre-emphasis	Option TXEQ	1
	SW option	PCIe4 RX test / Link EQ software	BSXPCI4CEM	1
	Kit	Interference combiner kit	BSXSICOMB	1
	Kit	Detector equalization kit	BSXPCI4EQ	1
	Cable	SMA-SMA cable pair, 18 inches	174-6663-01	1
	Cable	1-meter SMA-SMA cable pair, 1.5psec skew	PMCABLE1M	2
	[Optional] Cable	SMA - SMP cable pair, 102mm, <1psec skew>	174-6657-01	2
	Cable	SMA - SMP cable pair, 1-meter	174-6659-01	1
	Cable	Right angle SMA-SMA cable, 0.2m	174-6664-01	1
	Cable	Huber Suhner SMP-SMP cable pair 12 inches	80345501 (Huber-Suhner)	2
Link EQ	SW option	Link EQ option for Gen3 & Gen4. Requires BSXPCI4CEM	BSXPCI4LEQ	1
	SW option	PCIe1/2/3/4 decoder	Option SR-PCIE	1
	Kit	Power Divider, >25GHz with 2.92mm connector	PSPL5333 or similar	4
	Kit	DC block (Bandwidth >25GHz with 2.92 connector and capacitance 265nF (or greater)	PSPL5509 or similar	4
	Cable	SMA-SMA cable pair, 18 inches	174-6663-01	2
	Adapter	2.92mm Male to 2.92mm Male Adapter	SM3242 (Fairview Microwave)	4
	Cable	Right angle SMA-SMA cable, 0.5m	174-6666-01	1
	Cable	1-meter SMA-SMA cable pair, 1.5psec skew	PMCABLE1M	4

Host system software requirements

Microsoft Windows 7 or later

Microsoft Explorer 6.0 SP1 or later

Microsoft Access

Accessories

Recommended test fixtures, cables, and tools

Item	Image
Description : [PCI-SIG] PCIe 4.0 Preliminary CEM Fixture Kit PN : PCIe-CLB-X1X16, PCIe-CLB-X4X8, PCIe-CBB-MAIN, and PCIe-VAR-ISI The PCIe 4.0 CEM Beta fixtures require a VNA based characterization to determine the 16 GT/s Rx Link Equalization Test. This characterization will not be performed by Quantity : 1	the appropriate Insertion Loss for performing the 16 GT/s Tx Signal Quality Test and y the PCI-SIG, but must be performed by the end user after the fixtures are delivered.
Description: PCI Express Compliance Base Board (CBB) test fixture, revision 3.0. For testing PCI Express Add-in Cards, x1/x4/x8/x16. Vendor: PCI-SIG www.pcisig.com/specifications/order_form Vendor PN: CBB3 Tektronix PN: Only available from PCI-SIG Quantity: 1	
Description: PCI Express Compliance Load Board (CLB3) test fixture, revision 3.0. For testing PCI Express Platforms, x1 & x16 PCIe connectors. Vendor: PCI-SIG www.pcisig.com/specifications/order_form Vendor PN: x1/x16 CLB3 Tektronix PN: Only available from PCI-SIG Quantity: 1	
Description: PCI Express Compliance Load Board (CLB3), Revision 3.0. For testing PCI Express Platforms, x4 & x8 PCIe connectors. Vendor: PCI-SIG www.pcisig.com/specifications/order_form Vendor PN: x4/x8 CLB3 Tektronix PN: Only available from PCI-SIG Quantity: 1	



Item	Image
Description: SMA-to-SMA, Right-Angle, 300 mm Vendor: HUBER+SUHNER www.hubersuhner.com/en Vendor PN: 84210131, T+M MF141/16SMA/16SMA/300mm Tektronix PN: 174-6665-00 Quantity: 1	
Description: SMA-to-SMP right-angle cable pair, 102 mm, 1 ps phase-matched. Vendor: Rosenberger. www.rosenberger.com/us_en Vendor PN: 71L-19K2-32K1-00102B Tektronix PN: 174-6657-xx Quantity: 3 cable pairs	
Description: SMA-to-SMP right-angle cable pair, 1 m, 1 ps phase-matched Vendor: Rosenberger www.rosenberger.com/us_en Vendor PN: 71M-19K2-32S1-01000D Tektronix PN: 174-6659-xx Quantity: 1 cable pair	
Description: SMA torque wrench, 8.0 in-lbs. Vendor: Fairview Microwave www.fairviewmicrowave.com/sma-fixed-torque-wrench-click-st-sma3-p.aspx Vendor PN: ST-SMA3 Tektronix PN: 003-1940-xx Quantity: 1	2 M Le company

Datasheet



CE Marking Not Applicable.



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* European toll-free number. If not accessible, call: +41 52 675 3777

For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit www.tek.com.

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