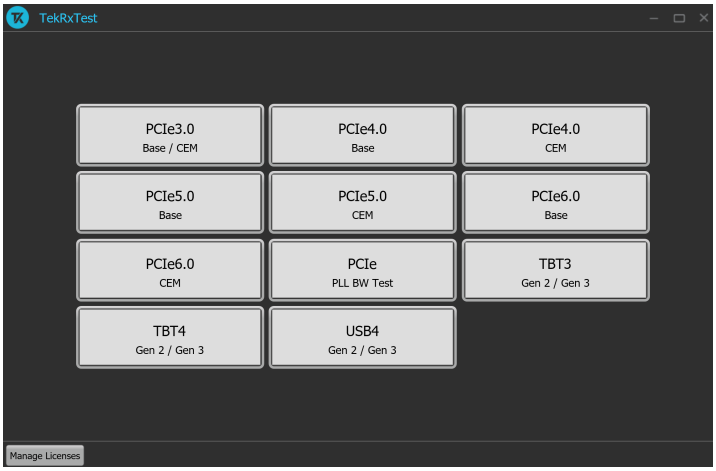
Tektronix PCI Express
TekRxTest Suite Datasheet



Improve the accuracy and precision of cutting-edge PCI Express 6.0 Receiver (Rx) validation with Tektronix automation software. Remove the complexity of Rx testing with a step-by-step user guided interface designed by industry leaders actively engaged in the standards bodies. Industry engagement ensures this solution will evolves in step with the technology. Achieving the correct balance of simplicity, user control has been the focus of the design team to ensure your device can complete link training testing with calibrated stress and be efficiently tested with optimized PHY settings.

Applications

- PCI Express 64 GT/s, 32 GT/s, 16 GT/s, and 8 GT/s
- Gen6/Gen5/Gen4/Gen3 Base specification (silicon validation) and Gen6/Gen5/Gen4/Gen3 CEM specification (system verification and compliance)
- Root Complex and Non-Root Complex silicon
- Systems (motherboards and servers), Add-in Cards, Switches, Bridges, and Extension Devices (retimers and redrivers)

Features and benefits

General

- Receiver automation software for Tektronix DPO70000SX Series Real Time Oscilloscopes and Anritsu MP1900A BERT
- Wizard based user interface for each step of calibration and test
- Pop-up user tips to simplify decision making
- Latest industry tool support (SigTest and Seasim)
- Calibration and test reports

PCI Express Gen6 (64 GT/s)

- Stressed Eye Calibration (64 GT/s)
- Base and CEM
- TP3 – AC/DC Balance, Amplitude, Tx Equalization, Sinusoidal Jitter tones, and Random Jitter
- TP2 – DMI, CMI, Preset and CTLE Selection, Stressed Eye
- Automated Oscilloscope Noise Compensation for SJ and RJ calibration
- Insertion Loss computation powered by Seasim Statistical Simulation Tool
- RxLink Equalization Test (64 GT/s)
- TxLink Equalization Test (64 GT/s)
- Jitter Tolerance Test (64 GT/s)

PCI Express Gen5 (32 GT/s)

- Stressed Eye Calibration (32 GT/s)
- Base and CEM
- TP3 – AC/DC Balance, Amplitude, Tx Equalization, Sinusoidal Jitter tones, and Random Jitter
- TP2 – DMI, CMI, Preset and CTLE Selection, Stressed Eye
- Automated loopback through Configuration and Recovery
- Insertion Loss computation powered by Seasim Statistical Simulation Tool
- Rx Link Equalization Test (32 GT/s)
- Tx Link Equalization Test (32 GT/s)
- Jitter Tolerance Test (32 GT/s)
- Advanced debug mode for troubleshooting

PCI Express Gen4 (16 GT/s)

- Stressed Eye Calibration (16 GT/s)
- Base and CEM
- TP1 – AC/DC Balance, Amplitude, Tx Equalization, Sinusoidal Jitter tones, and Random Jitter
- TP2 – DMI, CMI, Preset and CTLE Selection, Stressed Eye
- Automated loopback through Configuration and Recovery
- Insertion Loss computation powered by Seasim Statistical Simulation Tool
- Rx Link Equalization Test (16 GT/s)
- Tx Link Equalization Test (16 GT/s)
- Jitter Tolerance Test (16 GT/s)
- Advanced debug mode for troubleshooting

PCI Express Gen3 (8 GT/s)

- Stressed Eye Calibration (8 GT/s)
- CEM
- TP3 - AC/DC Balance, Amplitude, Tx Equalization, Sinusoidal Jitter tones, and Random Jitter

- TP2 - DMI, and Stressed Eye
- Rx Link Equalization Test (8 GT/s)
- Tx Link Equalization Test (8 GT/s)
- Jitter Tolerance Test (8 GT/s)
- Advanced debug mode for troubleshooting

PCI Express PLL Bandwidth and Peaking

- PCI Express PLL Bandwidth and Peaking automation softwares for Tektronix DPO70000SX Series Real-Time Oscilloscopes and Anritsu MP1900A BERT
- Support for Gen 3/4/5 Tx PLL testing
- Support for Anritsu SI PPG (NRZ) and PAM4 PPG
- Similar software look and feel as the Receiver test suite
- Supports testing with compliance (P0 to P10) and jitter measurement (toggle) patterns
- Software CTLE improves accuracy for high loss channel cases

Stressed eye calibration

Calibration of the stressed eye signal, generated by the BERT's PPG is important to ensure the receiver is tested in alignment with the PCI-SIG specifications with the proper amount of impairments. New challenges at 64 GT/s demand the fully automated approach taken by the Tektronix PCI Express Receiver Test Suite to avoid alternative tedious and error-prone approaches. Let the domain expertise and experience of the Tektronix engineers guide you through the steps of calibration starting with accurate TP3 measurements and ending with a TP2 eye diagram easily obtained within the tolerances required. Engineers will spend less time calibrating and more time collecting meaningful data on receiver performance and margin.

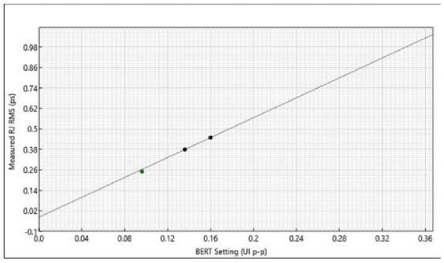
TP3 calibration

PCI Express Gen6 (64 GT/s) and Gen5 (32 GT/s)

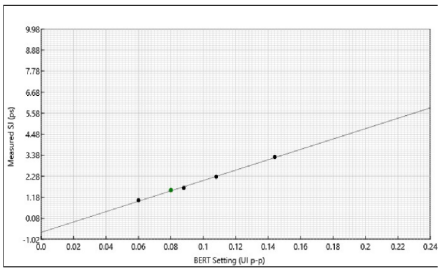
The TP3 (point after cable from BERT PPG to oscilloscope) calibration is mandatory for all devices to ensure tolerances are met at the defined reference plane. The Tektronix PCI Express Receiver Test Suite wizard will guide the user through all the necessary steps to ensure the pre-channel signal matches the specification requirements to ensure future calibration steps are completed with ease.

1. AC-DC balance – Small amounts of Tx EQ de-emphasis are enabled to balance low and high-frequency sections of the pattern at a common reference plane.
2. Amplitude – The differential voltage swing is required to be within 720 – 800 mV.
3. Tx Equalization Presets – Calibration of pre-shoot 1, pre-shoot 2 (Gen6 only), and de-emphasis is required to ensure true preset levels are used for testing receivers.
4. IL measurement – Channel insertion loss is calculated using Seasim between TP1 and TP3 (loss before the TP3 reference is computed here for later removal).
5. Random Jitter (RJ) – RJ is calibrated to be 0.25 ps [Gen6], 0.5 ps [Gen5] (RMS value) nominally.
6. Sinusoidal Jitter (SJ) – SJ is calibrated over the required range of 1-3 ps [Gen6]/1-5 ps [Gen5] (p-p) at 100 MHz frequency.

RJ Calibration	Setting: 0.096 UI p-p (Nominal - 0.25 ps RMS)
	Pattern: Toggle_1bit_PAM4
	Important RT Scope Settings: BW: 50.0 GHz, Sample Rate: 200.0 GS/s, Record Length: 12.5M
	RJ Regression Line Parameters: Slope = 2.917, Intercept = -0.017



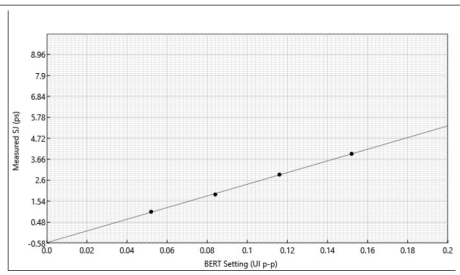
SJ Calibration	Setting: 0.08 UI p-p (Nominal - 1.563 ps)
	Pattern: 1b1b_CP_L0_Gen6
	Important RT Scope Settings: BW: 50.0 GHz, Sample Rate: 200.0 GS/s, Record Length: 12.5M
	SJ Regression Line Parameters: Slope = 27.143, Intercept = -0.649



RJ and SJ calibration for Gen6.

7. SJ@210 MHz – This calibration is required for JTOL measurements with some calibrations.

SJ@210 MHz Cal	Regression Line Parameters: Slope = 29.509, Intercept = -0.557
	Pattern: 1b1b_CP_L0_Gen6
	Important RT Scope Settings: BW: 50.0 GHz, Sample Rate: 200.0 GS/s, Record Length: 12.5M



SJ@210 MHz calibration for Gen6.

8. Multi-tone SJ – For JTOL measurements where up to maximum 14 frequencies are used, calibration for frequencies other than 100 MHz is required to be performed.

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PCIe6.0 CEM Receiver Calibration Report

TP3 Calibration Results

Details	
Unique ID	[Example_TP3_Calibration]
Date/Time	08 May 2024, 13:14
Generated By	TEK

Additional Comments
No Comments

Test Equipment	
BERT	ANRITSU, MP1900A, 6261788378
BERT FW Version	10.01.02
Rx Test SW Version	6.4.2.29
RT Scope	TEKTRONIX, DPO77002SX, B321456
RT Scope FW Version	10.12.0 Build 26
TekRxService Version	3.0.0.15
DPOJET Version	10.4.0.7

Result Summary	
TP3 Calibration	Unique ID: [Example_TP3_Calibration]
	Balanced De-emphasis: -0.6 dB
	Differential Amplitude: 800.0 mV / Single - Ended Amplitude setting: 608 mV
	SJ Setting: 0.052 UI p-p @ 100 MHz (Nominal SJ 1.563 ps / 0.05 UI p-p)
	RJ Setting: 0.08 UI p-p (Nominal RJ 0.25 ps RMS / 0.113 UI p-p)
	SJ@210 MHz Regression Line Parameters: Slope = 33.84, Intercept = -0.151
	Multi-tone SJ Calibration performed for 5 frequencies

Sample calibration report.

Automatic characterization and precise calibration of presets, RJ, and SJ along with the important parameters used for calibration like pattern type, oscilloscope, BERT settings, regression line slopes, and intercept for reference.

TP2 calibration

PCI Express Gen6 (64 GT/s), Gen5 (32 GT/s), Gen4 (16 GT/s), and Gen3 (8 GT/s)

The TP2 (end of channel) calibration is a complex process requiring a deep understanding of the BERT, Real Time Oscilloscope, post-processing tools, and the PCIe specifications. The Tektronix PCI Express Receiver Test Suite will remove the complexity and ensure the desired results are achieved through user-friendly automation. Time to complete TP2 is critical, so efficient techniques have been implemented to ensure an accurate stressed eye is achieved within a reasonable time scale. From calibration of DMI (Differential Mode Interference modeling cross-talk) to the fine granularity adjustments to SJ and DMI necessary to find the stressed eye solutions space, our automation software will guide you through this otherwise daunting task.

1. DMI – The differential mode interference is required to be calibrated within 5-25 mV (p-p) [Gen6] / 5-30 mV (p-p) [Gen5] / 10-25 mV (p-p) [Gen4] / 10-100 mV(p-p) [Gen3] by capturing the 2.1 GHz sinusoidal output for a duration of 40 ns.
2. CMI – The common-mode interference is required to be calibrated for a nominal voltage of 75 mV (p-p) [Gen6] / 150 mV (p-p) [Gen5 and Gen4] by capturing the 120 MHz sinusoidal output for a duration of 62.5 us.
3. Channel insertion loss for DMI/CMI and eye diagram measurements computed with Seasim (TP1 to TP2/TP2P for 16 GT/s and TP3 to TP2/TP2P for 32 GT/s and 64 GT/s).
4. Channel selection based on optimal Tx EQ Preset and Rx CTLE – Base Specification compliant for Eye Area criteria.
5. Stressed-Eye calibration – Fine-tuning of the eye using amplitude, SJ (RJ in case of Gen3), and DMI is utilized to place the stressed eye within allowed tolerances. Automated TP2 calibration plots and stressed eye calibration details along with other important parameters like pattern type, oscilloscope and BERT settings, and regression line slopes and intercept for reference.

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PCIe6.0 CEM Receiver Calibration Report

System TP2 Calibration Results

Details	
Unique ID	[Example_TP2_SYSTEM_Calibration]
Date/Time	09 February 2023, 02:41
Generated By	TEK

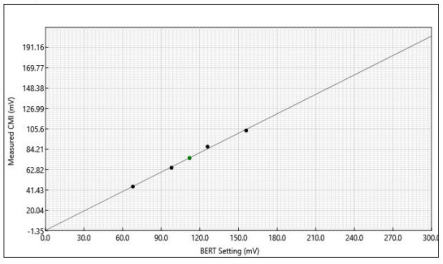
Additional Comments
No Comments

Test Equipment	
BERT	ANRITSU, MP1900A, 6261788378
BERT FW Version	9.00.00.54
Rx Test SW Version	6.4.1.31
Analysis SW Version	Sigtest Version 5.1.04, Seasim Version 2.0.101a
RT Scope	TEKTRONIX, DPO77002SX, B321456
RT Scope FW Version	10.12.0 Build 26
TekRxService Version	3.0.0.15
DPOJET Version	10.4.0.7

Calibration Summary	
TP2 Calibration	Unique ID: [Example_TP2_SYSTEM_Calibration]
	Full Channel Loss: Not Run
	DMI/CMI Loss: 23.977 dB
	Selected Preset: Q5
	Selected CTLE: 15.0 dB
	ISI Pair: Not Available
	Status: Converged
	Final Calibrated EW: 3.2 ps (2.825 ps ≤ Target EW ≤ 3.425 ps)

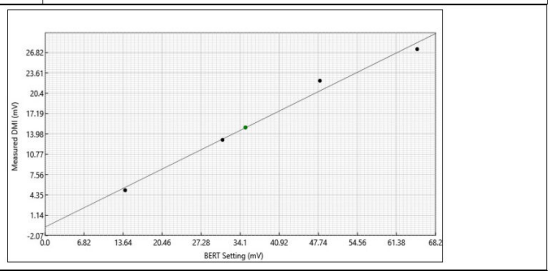
Root complex TP2 calibration sample report.

CMI	Setting: 112 mV (Nominal - 75.0 mV)
	Pattern: Electrical_Idle
	Important RT Scope Settings: BW: 33.0 GHz, Sample Rate: 200.0 GS/s, Record Length: 12.5M
	Regression Line Parameters: Slope = 0.68, Intercept = -1.007



AIC CMI calibration result.

DMI	Setting: 35 mV @ 2.1 GHz (Nominal - 15.0 mV)
	Pattern: Electrical_Idle
	Important RT Scope Settings: BW: 33.0 GHz, Sample Rate: 200.0 GS/s, Record Length: 8K
	Regression Line Parameters: Slope = 0.448, Intercept = -0.734



AIC DMI calibration result.

Stressed Eye Calibration	Final SJ Stress Level: 1.563 ps
	Final DMI Stress Level: 11.0 mV
	Final Amplitude Level: 800.0 mV
	Pattern: Toggle_512bits_PAM4

Index	SJ (ps)	DMI (mV)	Amp (mV)	Eye Width (ps)	Eye Height (mV)
1	1.563	15	800	2.656	4.48
2	1.563	15	800	2.5	4.312
3	1.563	15	800	2.656	4.746
4	1.563	15	800	2.5	3.73
5	1.563	15	800	2.656	4.473
6	1.563	15	800	2.812	4.472
7	1.563	15	800	2.344	4.073
8	1.563	15	800	2.656	4.743
AVERAGE	1.563	15	800	2.598	4.379
9	1.563	13	800	2.969	5.084
10	1.563	13	800	2.812	4.914
11	1.563	13	800	2.969	5.35
12	1.563	13	800	2.656	4.293
13	1.563	13	800	2.969	5.075
14	1.563	13	800	3.281	5.083
15	1.563	13	800	2.656	4.671
16	1.563	13	800	2.969	5.347
AVERAGE	1.563	13	800	2.91	4.977
17	1.563	11	800	3.281	5.677
18	1.563	11	800	3.125	5.505
19	1.563	11	800	3.281	5.944
20	1.563	11	800	2.969	4.898
21	1.563	11	800	3.281	5.708
22	1.563	11	800	3.438	5.685
23	1.563	11	800	2.969	5.259
24	1.563	11	800	3.281	5.939
AVERAGE	1.563	11	800	3.203	5.577
SELECTED	1.563	11	800	3.203	5.577

Stressed eye calibration result.

6. Stressed eye calibration supported using Sigtest (Gen3/Gen4/Gen5) and Seasim (Gen5/Gen6).
7. Eye height
   - 6 ± 0.5 mV @ BER E-6 [Gen6]
   - 15 ± 1.5 mV @ BER E-12 [Gen5 and Gen4]
   - 47.5 ± 2.5 mV @ BER E-12 [Gen3 System]
   - 43.5 ± 2.5 mV @ BER E-12 [Gen3 AIC]
8. Eye Width
   - 3.125 ± 0.3 ps @ BER E-6 [Gen6]
   - 9.375 ± 0.5 ps @ BER E-12 [Gen5]
   - 18.75 ± 0.5 ps @ BER E-12 [Gen4]
   - 44 ± 1 ps @ BER E-12 [Gen3 System]
   - 40.25 ± 1 ps @ BER E-12 [Gen3 AIC]

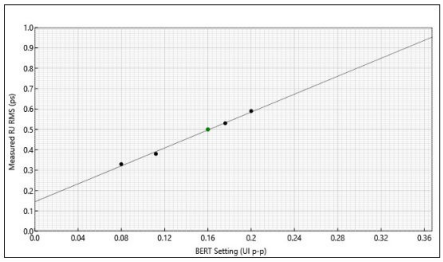
TP1 calibration

PCI Express Gen4 (16 GT/s) and Gen3 (8 GT/s)

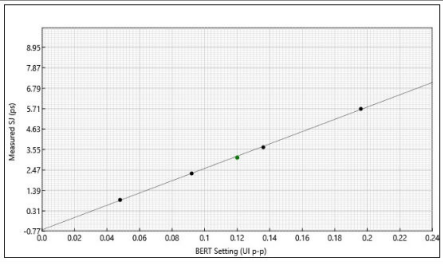
The TP1 (point after cable from BERT PPG to oscilloscope) calibration is mandatory for all devices to ensure tolerances are met at the defined reference plane. The Tektronix PCI Express Receiver Test Suite wizard will guide the user through all the necessary steps to pre-channel signal is true to the specification requirements to ensure future calibration steps complete with ease.

1. AC-DC balance – Small amounts of Tx EQ de-emphasis are enabled to balance low and high-frequency sections of the pattern at a common reference plane.
2. Amplitude – The differential voltage swing is required to be within 720 – 800 mV.
3. Tx Equalization Presets – Calibration of pre-shoot and de-emphasis is required to ensure true preset levels are used for testing receivers.
4. Random Jitter (RJ) – RJ is calibrated to be 1 ps (RMS) for Gen4 and 1.5 ps (RMS) for Gen3 nominally.

RJ Calibration	Setting: 0.16 UI p-p (Nominal - 0.5 ps RMS)
	Pattern: Toggle_1bit
	Important RT Scope Settings: BW: 50.0 GHz, Sample Rate: 200.0 GS/s, Record Length: 12.5M
	RJ Regression Line Parameters: Slope = 2.2, Intercept = 0.145



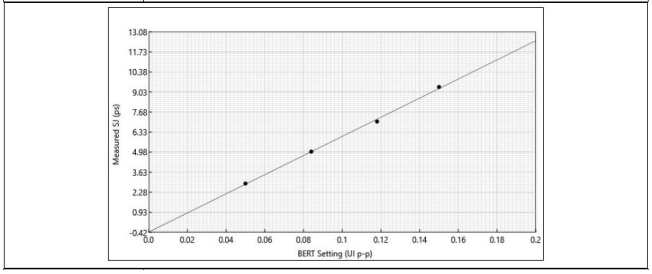
SJ Calibration	Setting: 0.12 UI p-p (Nominal - 3.125 ps)
	Pattern: 128b130b_CP_L0_Gen5_P7
	Important RT Scope Settings: BW: 50.0 GHz, Sample Rate: 200.0 GS/s, Record Length: 12.5M
	SJ Regression Line Parameters: Slope = 32.433, Intercept = -0.687



RJ and SJ calibration for Gen 4.

5. Sinusoidal Jitter (SJ) – SJ is calibrated over the required range of 5-10 ps (p-p) including the nominal SJ specification of 0.1 UI (or 6.25 ps for Gen4 and 12.5 ps for Gen3) at 100 MHz frequency.
6. SJ@210 MHz – This calibration is required for JTOL measurements with some calibrations (only for Gen4).

SJ@210 MHz Cal	Regression Line Parameters: Slope = 64.404, Intercept = -0.4
	Pattern: 128b130b_CP_L0_Gen4_P7
	Important RT Scope Settings: BW: 25.0 GHz, Sample Rate: 100.0 GS/s, Record Length: 12500000

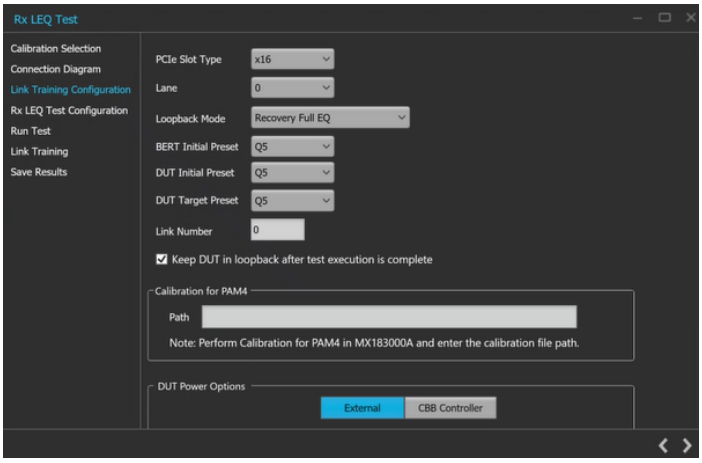


SJ@210 MHz calibration for Gen4.

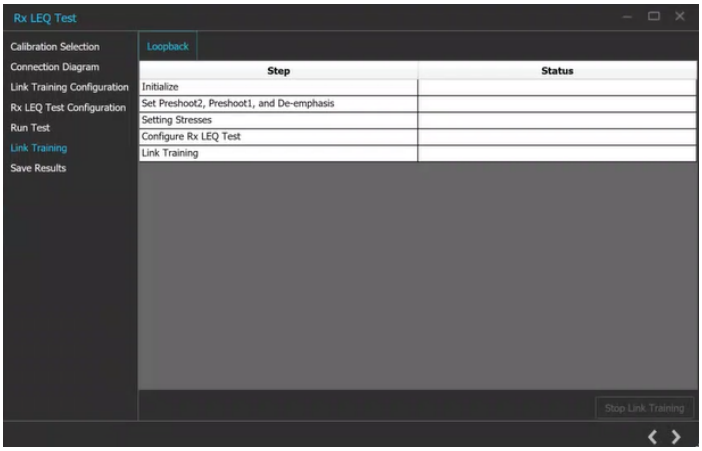
7. Multi-tone SJ – For JTOL measurements where up to maximum of 14 frequencies are used, calibration for frequencies other than 100 MHz is required to be performed.

Link training

Prior to receiver testing, the Device-Under-Test (DUT) must be placed into loopback, where the signal digitized at the Rx latch is re-transmitted by the corresponding Tx giving visibility into a possible bit or burst errors. Entering the loopback test mode requires a complex dance through the Link Training Status State Machine (LTSSM) between the BERT and DUT. The Tektronix PCI Express Receiver Test Suite automates this sequence allowing loopback through configuration (short path) and loopback through recovery (full training of the link Tx and Rx) for different levels of receiver testing. Relevant parameters are exposed to allow user control over this process without unnecessary complexity.



Link training configuration.



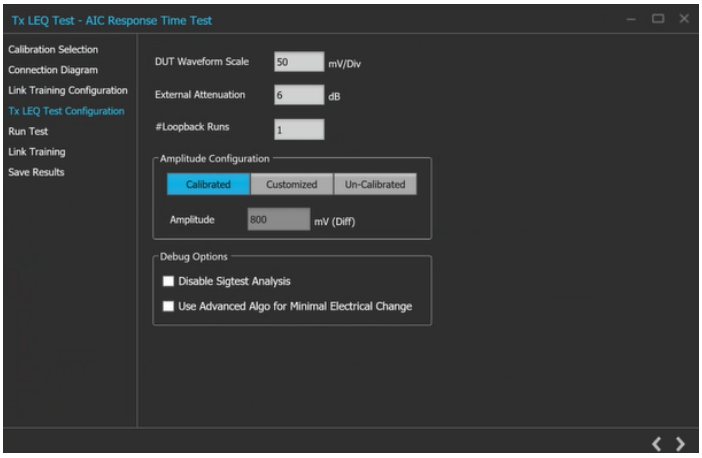
Flexible link training and loopback control.

Receiver and transmitter link equalization testing

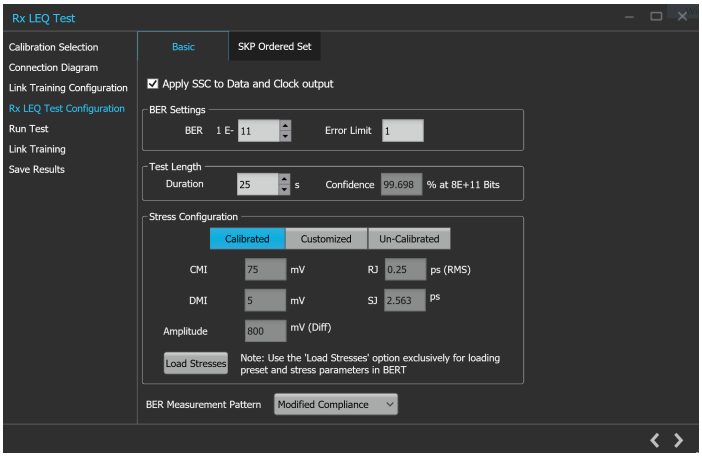
PCI Express compliance at 64 GT/s, 32 GT/s, 16 GT/s, and 8 GT/s requires performing a Receiver Link Equalization test (checking analog Rx performance with a stressed signal after full link training) and a Transmitter Link Equalization test (ensuring key digital timing limits are achieved when an Rx makes Tx change requests to its link partner).

The Tektronix PCI Express Receiver Test Suite controls the BERT and RT Oscilloscope during these required tests to provide efficient test results with minimal overhead and control only where needed.

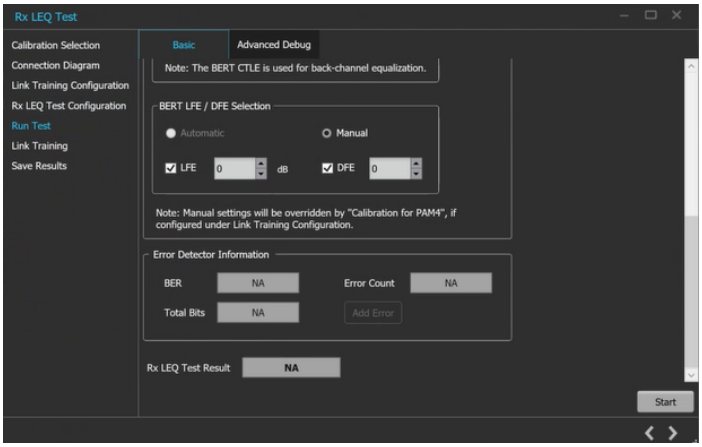
The advanced debug mode provides additional troubleshooting capability for LEQ tests, allowing customised stressors, Tx presets, custom patterns, auto-search CTLE, and CDR tuning.



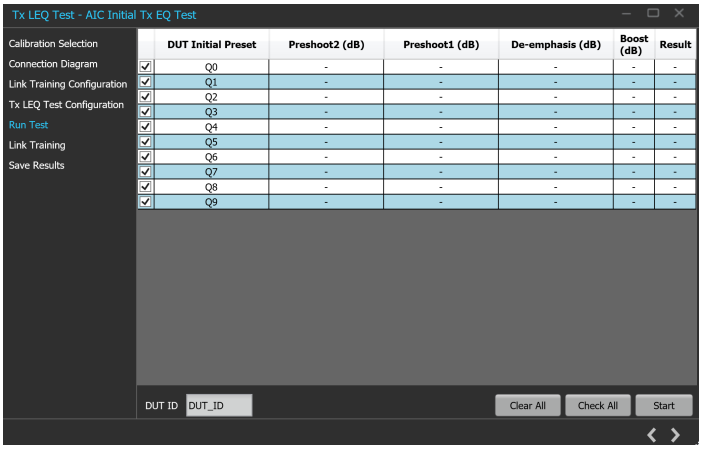
Tx LEQ test configuration.



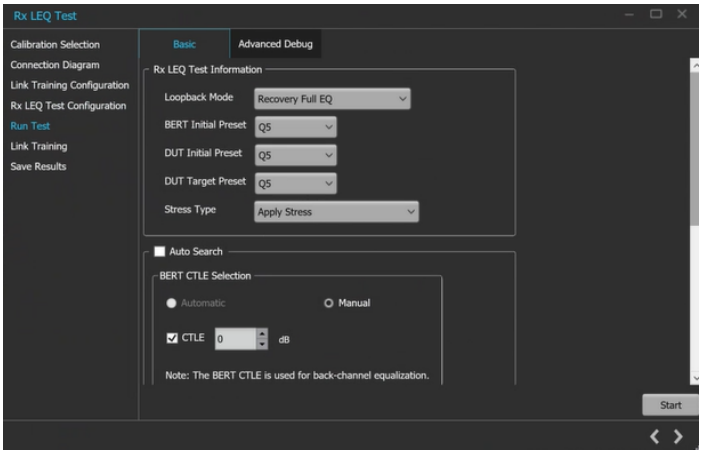
Rx LEQ test configuration.



Rx LEQ test Run Test



Tx LEQ execution tab.



Rx LEQ execution tab.

Tektronix

PCIe6.0 CEM Receiver Test Report

AIC LEQ Response Time Test Results

Details	
Unique ID	Demo
Date/Time	14 October 2024, 4:24 PM
Generated By	TEK

Additional Comments
Q0,Q1,Q2,Q3,Q5

Test Equipment	
BERT	ANRITSU, MP1900A, 6272608792
BERT FW Version	10.03.04
Rx Test SW Version	6.4.3.19
Analysis SW Version	Sigtest Version 6.1.06
RT Scope	TEKTRONIX, DPO77002SX, B321740
RT Scope FW Version	10.14.0 Build 15

TP3 Calibration Summary	
Unique ID	TP3Cal_13102024
Balanced De-emphasis	-0.6 dB
Differential Amplitude	800.0 mV / Single - Ended Amplitude setting: 624 mV

Test Results

DUT Initial Preset	Target Preset/Coeff		Preshoot2 (dB)	Preshoot1 (dB)	De-Emph (dB)	Boost (dB) (Informative)	Electrical Response Time (ns)	DUT Reported Coefficients	Result
Q2	Q0	Preset	0	0	0	0	136.4	(0,0,32,0)	PASS
Q2		Coeff	0	0	0	0	62.53	-	PASS
Q2	Q1	Preset	0.029	1.346	0.090	1.269	138.4	(0,2,30,0)	PASS
Q2		Coeff	0.095	1.442	0.420	1.088	112.7	-	PASS
Q0	Q2	Preset	-0.20	3.625	0.356	3.392	98.60	(0,5,27,0)	PASS
Q0		Coeff	-0.01	3.052	-0.00	3.054	74.84	-	PASS
Q2	Q3	Preset	-0.12	0.369	-1.13	1.459	146.6	(0,0,30,2)	PASS
Q2		Coeff	-0.20	-0.46	-1.49	1.105	100.3	-	PASS

Tx LEQ AIC response time test results.

Tektronix

PCIe6.0 CEM Receiver Test Report

AIC Rx LEQ Test Results

Details	
Unique ID	Demo
Date/Time	07 June 2024, 9:12 AM
Generated By	Tek

Additional Comments
Rx LEQ Pass 1.9 E11

Test Equipment	
BERT	ANRITSU, MP1900A, 6272594808
BERT FW Version	10.02.50.01
Rx Test SW Version	6.4.3.7

Calibration Summary	
TP2 Calibration	Unique ID: 06_03_24_DB
	Full Channel Loss: Not Run
	ISI Pair: 0 & 27
	Status: Converged
	Final Calibrated EW: 3.1 ps (2.825 ps ≤ Target EW ≤ 3.425 ps)
	Final Calibrated EH: 6.0 mV (5.5 mV ≤ Target EH ≤ 6.5 mV)
	Final SJ Stress Level: 1.563 ps / 0.08 UI p-p BERT Setting (1 ps ≤ SJ Sweep ≤ 3 ps)
	Final Amplitude Level: 800.0 mV (Differential) / 542 mV (Single-Ended) BERT Setting
	Final DMI Stress Level: 9.0 mV / 21 mV BERT Setting (5 mV ≤ DMI Sweep ≤ 25 mV)
	Final CMI Stress Level: 75.0 mV / 112 mV BERT Setting
TP3 Calibration	Unique ID: TP3_FYI_Gen6_Final
	Differential Amplitude: 800.0 mV / Single - Ended Amplitude setting: 542 mV
	SJ Setting: 0.08 UI p-p @ 100 MHz (Nominal SJ 1.563 ps / 0.05 UI p-p)
	RJ Setting: 0.096 UI p-p (Nominal RJ 0.25 ps RMS / 0.113 UI p-p)
Rx LEQ Test	Loopback Configuration: Link Training
	Loopback Mode: Recovery Full EQ
	Clock Architecture: Common
	Apply SSC to Data and Clock Output: OFF
	BERT Initial Preset: Q2
	DUT Initial Preset: Q1
	DUT Target Preset: Q1
	Link #: 0 , Lane #: 0
	CTLE: Disabled
	BER Measurement Pattern: Modified Compliance
	BER: 1E-06
	Test Duration: 3.00 s
	Test Confidence: 100.00% at 1E+11 Bits
	Stress Configuration: Calibrated
	Stress Type: Apply Stress
	RJ: 0.25 ps (RMS)
	SJ: 1.563 ps
	DMI: 9.00 mV
	CMI: 75.00 mV
	Amplitude: 800.00 mV

Rx LEQ Test Results	
Status	PASS
BER	7.1293E-07
Error Count	135564
Initial BERT Preset	Q2
Final BERT Preset	-------
Final BERT Coefficients	(-------, -------, -------, -------)

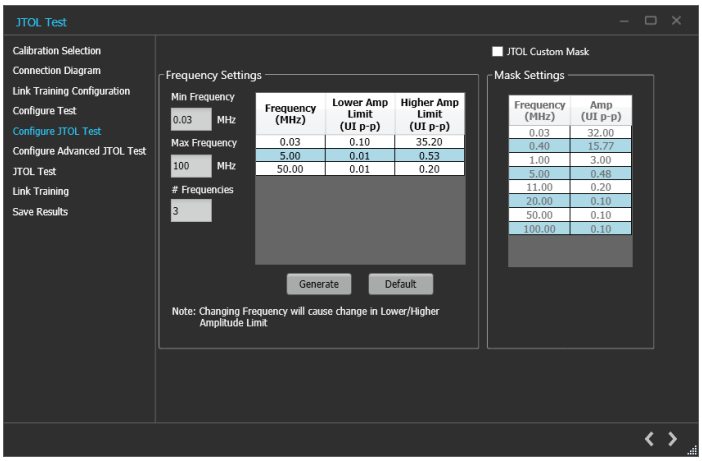
AIC Rx LEQ test results.

Remote control protocol

The test software can be operated remotely through SCPI commands; allows seamless integration of custom test flow.

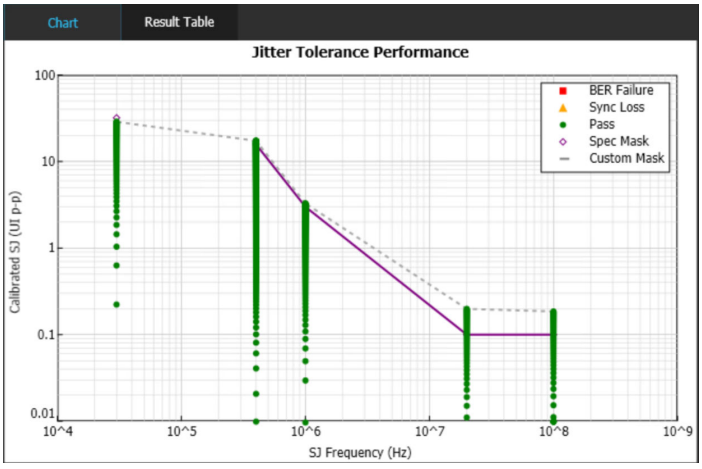
Jitter Tolerance (JTOL) test

Jitter Tolerance (JTOL) testing requires sweeping numerous calibrated SJ tones from low to high amplitude to see how the receiver-under-test CDR tracks the stress (typically in the presence of other noise & jitter sources). Custom JTOL pass/fail masks can be configured while testing with different search algorithms (upward linear, logarithmic, etc.). The Tektronix PCI Express Receiver Test Suite allows engineers minimal setup with quick and descriptive test reports.

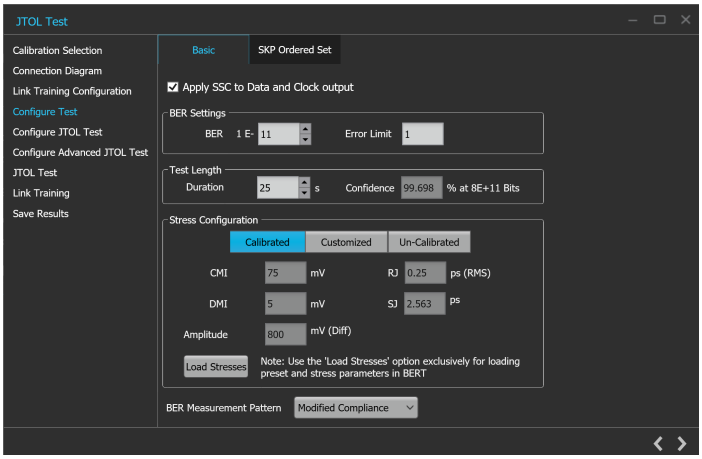


JTOL test configuration settings.

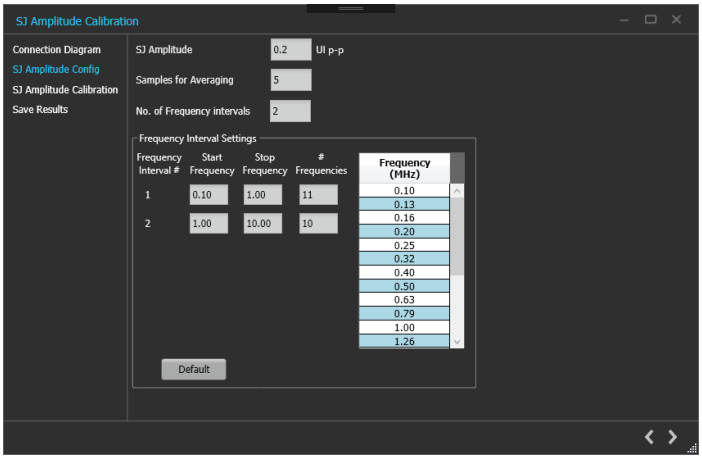
Both the custom mask and the specification mask are provided in the JTOL test to have a better understanding of the DUT performance, especially at the design stage. The Receiver solution performs an automatic back channel equalization and sampling point optimization to ensuring the best conditions for the DUT transmitted data traffic to be accurately comprehended at the BERT receiver ensuring the correct determination of BER performance.



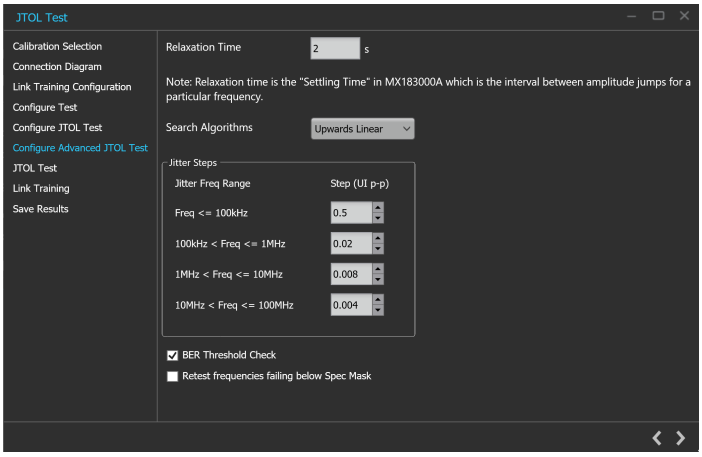
JTOL test result with specification.



Error detector and stress settings for JTOL.



SJ amplitude calibration.



Different margin search algorithm settings for JTOL test.

Result Summary	
SJ Amplitude Cal	SJ Amplitude: 0.2 UI p-p
	Samples for averaging: 5

Frequency (MHz)	Run1 (ps)	Run2 (ps)	Run3 (ps)	Run4 (ps)	Run5 (ps)	Average (ps)
0.10	6.446	6.445	6.376	6.006	6.209	6.296
0.13	6.348	6.159	6.198	6.171	6.32	6.239
0.16	6	6.45	6.546	6.296	6.367	6.332
0.20	6.228	5.983	6.576	5.831	6.538	6.231
0.25	6.177	6.398	6.27	6.362	6.273	6.296
0.32	6.553	6.447	6.254	6.268	6.287	6.362
0.40	6.325	6.386	6.438	6.342	6.248	6.348
0.50	6.184	6.343	6.192	6.288	6.395	6.28
0.63	6.239	6.345	6.296	6.337	6.426	6.329
0.79	6.28	6.299	6.263	6.267	6.263	6.274
1.00	6.261	6.276	6.177	6.455	6.338	6.301
1.26	6.374	6.255	6.293	6.38	6.374	6.335
1.58	6.35	6.248	6.245	6.367	6.317	6.305
2.00	6.198	6.404	6.186	6.398	6.262	6.29
2.51	6.327	6.268	6.242	6.217	6.281	6.267
3.16	6.264	6.295	6.262	6.295	6.242	6.272
3.98	6.354	6.255	6.264	6.31	6.326	6.302
5.01	6.328	6.217	6.245	6.228	6.258	6.255
6.31	6.23	6.254	6.346	6.31	6.221	6.272
7.94	6.207	6.199	6.234	6.281	6.282	6.241
10.00	6.21	6.222	6.25	6.192	6.271	6.229

Result summary for SJ Amplitude calibration.

PCIe PLL bandwidth and peaking

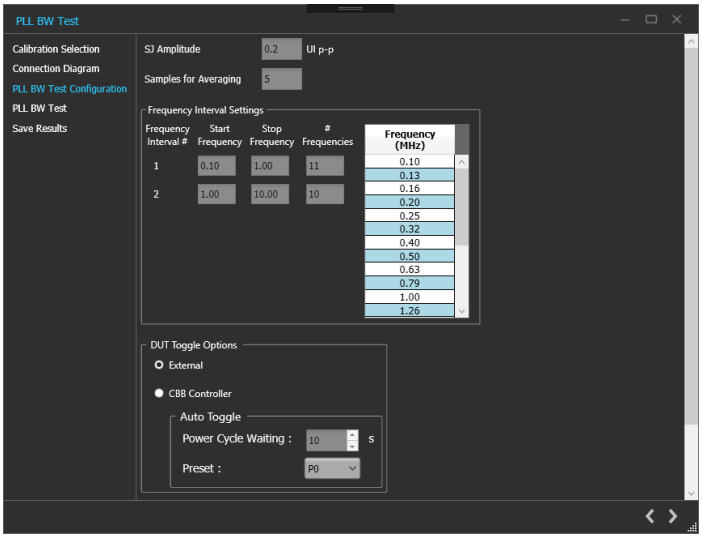
This test verifies that the Add-In Card Tx PLL has the correct bandwidth and peaking. Providing a 100 MHz reference clock to the DUT with a calibrated amount of SJ allows us to measure how much SJ passes through the DUT's Tx PLL for a certain SJ tone. Performing this process across multiple tones allows the construction of the PLL frequency response to measure both bandwidth and peaking.

SJ Amplitude Calibration for Gen 5/4/3

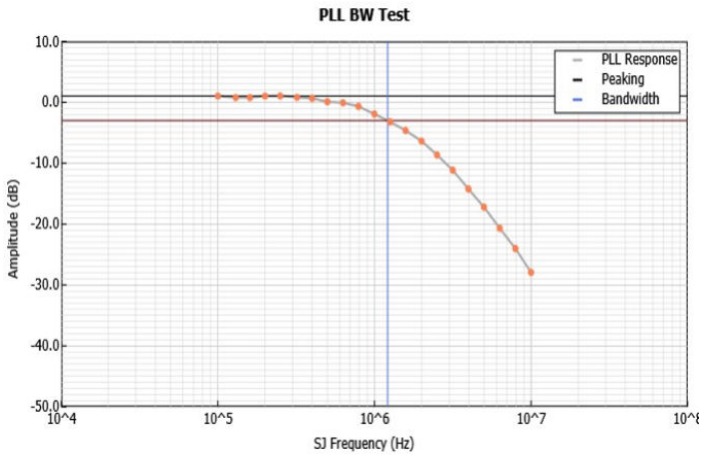
- Calibration of SJ amplitude to modulate the 100 MHz Refclk used by DUT's Tx PLL
- Adjustable SJ amplitude
- User-controlled SJ frequency selection to ensure adequate resolution at peaking & 3dB point
- Increased averaging can be used to minimize variation (5 recommended)
- Software CTLE ensures support for higher loss channels and various DUT Tx patterns

PLL bandwidth and peaking measurements

- Bandwidth and peaking reported for selected data rates
- DUT Tx can transmit compliance patterns or jitter measurement (toggle) patterns
- Consistent DSP algorithm used for SJ calibration and DUT testing
- Test report with PLL bandwidth, peaking, frequency response plot, and individual measurements



PLL bandwidth test.



Test results.

Ordering information

PCIe Gen6 BASE and CEM software options

Item	Description	Type
RXSW-FL1-PCIE6	License; PCI Gen 6 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Floating 1-Year Subscription	Software
RXSW-FLP-PCIE6	License; PCI Gen 6 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Floating Perpetual	Software
RXSW-NL1-PCIE6	License; PCI Gen 6 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Node-Locked 1-Year Subscription	Software
RXSW-NLP-PCIE6	License; PCI Gen 6 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Node-Locked Perpetual	Software

PCIe Gen5 BASE and CEM software options

Item	Description	Type
RXSW-NL1-PCIE5	License; PCI Gen 5 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Node-Locked 1-Year Subscription	Software
RXSW-NLP-PCIE5	License; PCI Gen 5 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Node-Locked Perpetual	Software
RXSW-FL1-PCIE5	License; PCI Gen 5 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Floating 1-Year Subscription	Software
RXSW-FLP-PCIE5	License; PCI Gen 5 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Floating Perpetual	Software

PCIe Gen4 BASE and CEM software options

Item	Description	Type
RXSW-NL1-PCIE4C	License; PCI Gen 4 BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Node-Locked 1-Year Subscription	Software
RXSW-NLP-PCIE4C	License; PCI Gen 4 BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Node-Locked Perpetual	Software
RXSW-FL1-PCIE4C	License; PCI Gen 4 BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Floating 1-Year Subscription	Software
RXSW-FLP-PCIE4C	License; PCI Gen 4 BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Floating Perpetual	Software

Overall Setup list:

PCIe Gen 6 CEM Rx

Item	Vendor	Type	Requirement	Quantity	Description	Notes
MP1900A	*Anritsu*	Equipment	Required	1	≥32Gb/s BERT with PAM4 PPG (MU196020A), PAM4 ED (MU196040B), and CDR (MU196060A)	Cables required for connection between BERT modules shall be included by the 3rd party vendor. Configuration for BERT provided by Anritsu. NRZ or PAM4 Config can be used for Gen3/4/5. Customer to work with Anritsu to get the exact BERT configuration and quote.
DPS75004SX	Tektronix	Equipment	Required	1	Dual Stack 50GHz Sx Scope	50G or better. Backward compatible to PCIe Gen1/2/3/4/5. Depending on the bench locations for the DUT, scope and BERT the user can either go with 2pr - PMCABLE1M and 1pr 174-6663-01, OR, 3pr - PMCABLE1M.
DPO7AFP	Tektronix	Equipment	Optional	1	Auxiliary Front Panel	-
DPO7RFK2	Tektronix	Tek Accessory	Required	2	Attenuator Kit	Attenuator kit + DC Blocks + V-K adapters
C7239	*CentricRF*	3rd Party	Optional	2	2.92mm Female to 2.4mm Female Adapter Right Angle VSWR 1.15 40Ghz	Optional adapters to reduce the protrusion distance of the ATI SX scope front end. FMAD1227 from Fairview Microwave can be another option.
DJA	Tektronix	Option	Required	1	DPOJET Advanced option	DPOJET advanced Jitter, Eye & Timing Analysis SW option (Used for Multi-tone SJ calibration for PCIe4/5/6, PLL BW measurements)
SDLA64	Tektronix	Option	Recommended	1	Serial Data Link Analysis Software	Embedding/De-embedding/s-parameter filter generation/Receiver Virtualization & Analysis Software
PMCABLE1M	Tektronix	Tek Accessory	Required	2 or 3	Cable pair; 2.92-to-2.92mm, Straight, 1.5ps matched, 1000mm, 40GHz	Equipment connection to fixtures and DUT
174-6663-01	Tektronix	Tek Accessory	Optional	0 or 1	Cable pair; 2.92-to-2.92mm, Straight, 1.5ps matched, 500mm, 40GHz	Signal Connection between scope and BERT for Tx LEQ
174-6666-01	Tektronix	Tek Accessory	Required	1	Cable; SMA-to-SMA, Right Angle-Right Angle, 500mm	Signal Connection between scope and BERT for Tx LEQ AUX Trigger
174-6659-01	Tektronix	Tek Accessory	Required	1	Cable pair; SMA-to-SMP, Right Angle, 1ps phase-matched, 1000mm, 20GHz	Refclk connection between DUT & BERT

Table continued…

Item	Vendor	Type	Requirement	Quantity	Description	Notes
MPR40M	*Fairview Microwave*	3rd Party	Required	2	2-Way Power Divider 2.92mm Connectors, 40 GHz	Split signal from DUT Tx to the scope and Error Detector
C7035	*CentricRF*	3rd Party	Optional	4	Right Angle Male-Female 2.92mm adapter	Cable management
C7049	*CentricRF*	3rd Party	Required	2	2.92mm Male to 2.92mm Male Adaptor	Power divider output to scope input
ZTM2	*Mini-circuits*	Equipment	Optional	1 to 2	40GHz RF switch for automated multi-lane testing	Contact Tektronix for model and configuration assistance
PowerUSB - Basic	*PowerUSB*	3rd Party	Optional	1	Power USB Power Strip	Automate DUT power cycle
PCIe 6.0 CEM Test Fixture (TBD)	*PCI-SIG*	Test Fixtures	Required	1	Gen 6 CEM Test Fixtures	PCI-SIG annouced to initiate a poll to request for interest of Beta fixture as of 3/11/2024
RXSW-NLP-PCIE6	Tektronix	Software	Required	1	Gen6 BASE & CEM RX test software - Node-Locked, Perpetual	BERT stress calibration, JTOL, RX margin, test reports. Choose one license type.
RXSW-NL1-PCIE6	Tektronix	Software	Required		Gen6 BASE & CEM RX test software - Node Locked, Time Based, 1 year	
RXSW-FLP-PCIE6	Tektronix	Software	Required		Gen6 BASE & CEM RX test software - Floating, Perpetual	
RXSW-FL1-PCIE6	Tektronix	Software	Required		Gen6 BASE & CEM RX test software - Floating, Time Based, 1 year	

Note: Another matched pair of cables (e.g. 174-6663-01) will be required if the Active redriver is used for Rx or Tx LEQ.

Gen5 CEM Test Fixtures are not backwards compatible for Gen3 & Gen4 CEM Rx.

It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit.

PCIe Gen6 Base Rx

Item	Vendor	Type	R/O	Quantity	Description	Notes
DPS75004SX	Tektronix	Equipment	Required	1	Dual-Stack 50 GHz Sx oscilloscope	50 GHz or better
DPO7RFK2	Tektronix	Tektronix accessory	Required	2	Attenuator kit	Attenuator kit + DC blocks
103047400	Tektronix	Tektronix accessory	Required	2	Connector savers (1.85 mm)	1.85 mm oscilloscope channel input connection
Anritsu MP1900A [1]	Anritsu	3rd party equipment	Required	1	Bit Error Rate Tester (BERT)	Configuration provided by 3rd party
DJA	Tektronix	Equipment SW option	Required	1	DPOJET advanced option	DPOJET advanced Jitter, Eye and Timing Analysis SW option

Table continued…

[1] Configuration for BERT provided by 3rd party vendor.

Item	Vendor	Type	R/O	Quantity	Description	Notes
PAMJET-E	Tektronix	Equipment SW option	Required	1	PAM4 tool	PCIe Gen6 PAM4 measurement
PAMJET PCIe Option	Tektronix	Equipment SW option	Required	1	PAMJET PCIe Option	
Gen5 Base Test Fixture Set	PCI-SIG	Test fixtures	Required	1	Gen 5 Base Rev3 Test Fixtures[2]	Rev3 is Meg6 material with MMPX connectors[3]
PMCABLE1M	Tektronix	Tektronix accessory	Required	2	Cable pair; 2.92-to-2.92 mm, Straight, 1.5 ps phase-matched, 40 GHz	Equipment connections to fixtures and DUT
174-6659-01	Tektronix	Tektronix accessory	Required	1	Cable pair; SMA - SMP cable pair	Refclk connection between DUT and BERT
C7035	CentricRF	3rd party	Optional	4	Right Angle Male-Female 2.92 mm adapter	Cable management
RXSW-FL1-PCIE6	Tektronix	SW option	Required	1	PCI Gen 6 Rx BASE automation software for Tektronix oscilloscopes and Anritsu BERT License	Floating 1-Year Subscription OR
RXSW-FLP-PCIE6						Floating Perpetual OR
RXSW-NL1-PCIE6						Node-Locked 1-Year Subscription OR
RXSW-NLP-PCIE6						Node-Locked Perpetual

PCIe Gen5 Base Rx

Item	Vendor	Type	R/O	Quantity	Description	Notes
DPS75004SX	Tektronix	Equipment	Required	1	Dual-Stack 50 GHz Sx Oscilloscope	50 G or better[4]
DPO7RFK2	Tektronix	Tektronix accessory	Required	2	Attenuator kit	Attenuator kit + DC blocks
103047400	Tektronix	Tektronix accessory	Required	2	Connector savers (1.85 mm)	1.85 mm oscilloscope channel input connection
Anritsu MP1900A[1]	Anritsu	3rd party equipment	Required	1	Bit Error Rate Tester (BERT)[5]	Configuration provided by 3rd party
DJA	Tektronix	Equipment SW option	Required	1	DPOJET advanced option	DPOJET advanced option
SDLA64	Tektronix	Equipment SW option	Required	1	Serial Data Link Analysis (SDLA) Software	Serial Data Link Analysis (SDLA) Software
174-6659-01	Tektronix	Tektronix accessory	Required	1 pr	Cable; SMA - SMP cable pair	Refclk connection between DUT & BERT
PMCABLE1M	Tektronix	Tektronix accessory	Required	2 pr	Cable; 2.92-to-2.92 mm, Straight, 1.5 ps phase-matched, 40 GHz	Equipment connections to relica channel & DUT
Gen5 Base Test Fixture Set	PCI-SIG	Test fixtures	Required	1	Gen 5 Base Rev3 Test Fixtures[2]	Rev3 is Meg6 material with MMPX connectors[3]

Table continued…

2 Gen5 BaseTest Fixtures are not backwards compatible for Gen3 & Gen4 Base Rx

3 It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit

4 If ATI channels will be used for refclk measurements they will need Option Key 4 (50 XL)

5 Cables required for connection between BERT modules shall be included for the 3rd party vendor

Item	Vendor	Type	R/O	Quantity	Description	Notes
RXSW-FL1-PCIE5 or RXSW-FLP-PCIE5 or RXSW-NL1-PCIE5 or RXSW-NLP-PCIE5	Tektronix	SW option	Required	1	PCIe Gen5 Receiver Software	License;PCI Gen 5 Rx CEM and BASE automation software for Tektronix oscilloscopes and Anritsu BERT; Floating 1-Year Subscription OR Floating Perpetual OR Node-Locked 1-Year Subscription OR Node-Locked Perpetual

PCIe Gen5 CEM LEQ

Item	Vendor	Type	R/O	Quantity	Description	Notes
DPS75004SX	Tektronix	Equipment	Required	1	Dual-Stack 50 GHz Sx oscilloscope	50 G or better[4]
DPO7RFK2	Tektronix	Tektronix accessory	Required	2	Attenuator kit	Attenuator kit + DC blocks
103047400	Tektronix	Tektronix accessory	Required	2	Connector savers (1.85 mm)	1.85 mm oscilloscope channel input connection
Anritsu MP1900A[1]	Anritsu	3rd party equipment	Required	1	Bit Error Rate Tester (BERT) [5]	Configuration provided by 3rd party
DJA	Tektronix	Equipment SW option	Required	1	DPOJET advanced option	DPOJET advanced option
SDLA64	Tektronix	Equipment SW option	Required	1	Serial Data Link Analysis (SDLA) software	Serial Data Link Analysis (SDLA) software
PMCABLE1M	Tektronix	Tektronix accessory	Required	2 pr	Cable; 2.92-to-2.92 mm, straight, 1.5 ps phase-matched, 40 GHz	Equipment connection to fixtures and DUT
174-6663-01	Tektronix	Tektronix accessory	Required	1 pr	Cable; 2.92-to-2.92 mm, straight, 1.5 ps phase-matched, 500 mm, 40 GHz	Signal connection between oscilloscope and BERT for Tx LEQ
174-6666-01	Tektronix	Tektronix accessory	Required	2 pr	Cable; SMA-to-SMA, Right Angle-Right Angle, 500 mm	Signal connection between oscilloscope and BERT for Tx LEQ & Trigger
174-6659-01	Tektronix	Tektronix accessory	Required	1 pr	Cable; SMA - SMP cable pair	Refclk connection between DUT & BERT
MPR40M	Fairview Microwave	3rd party	Required	2	Power divider	Split signal from DUT Tx to the oscilloscope and Error Detector
C7035	CentricRF	3rd party	Optional	4	Right Angle Male-Female 2.92 mm adapter	Cable management
C7049	CentricRF	3rd party	Required	3	2.92 mm Male to 2.92 mm Male adaptor	Power divider output to oscilloscope input
Redriver	3rd party	3rd party equipment	Optional	1	Active Gen5 Redriver (back channel equalization)[6]	High loss back channels (DUT Tx to Error Detector) may need EQ
PowerUSB - Basic	PowerUSB	3rd party	Optional	1	Power USB Power Strip	Automate DUT power cycle
TF-PCIE5-CEM-X16	PCI-SIG	Test fixtures	Required	1	Gen 5 CEM Test fixtures[7]	Tektronix fixtures are not officially approved by PCI-SIG[3]

Table continued…

6 Another matched pair of cables (e.g. 174-6663-xx) will be required if the Active redriver is used for Rx or Tx LEQ

7 Gen5 CEM Test Fixtures are not backwards compatible for Gen3 & Gen4 CEM Rx

Item	Vendor	Type	R/O	Quantity	Description	Notes
RXSW-FL1-PCIE5 or RXSW-FLP-PCIE5 or RXSW-NL1-PCIE5 or RXSW-NLP-PCIE5	Tektronix	SW option	Required	1	PCIe Gen5 Receiver software	License;PCI Gen 5 Rx CEM and BASE automation software for Tektronix oscilloscopes and Anritsu BERT; Floating 1-Year Subscription OR Floating Perpetual OR Node-Locked 1-Year Subscription OR Node-Locked Perpetual

PCIe Gen4 Base

Item	Vendor	Type	R/O	Quantity	Description	Notes
DPO70KSX/DX	Tektronix	Equipment	Required	1	Bandwidth >= 25 GHz Oscilloscope	25 G or better^{1}
Anritsu MP1900A	Anritsu	3^{rd} party equipment	Required	1	Bit Error Rate Tester (BERT)^{2}	Configuration provided by 3^{rd} party
DJA	Tektronix	Equipment SW option	Required	1	DPOJET advanced option	DPOJET advanced option
174-6659-01	Tektronix	Tektronix accessory	Required	1 pr	Cable; SMA - SMP cable pair	Refclk connection between DUT & BERT
PMCABLE1M	Tektronix	Tektronix accessory	Required	2 pr	Cable; 2.92-to-2.92 mm, Straight, 1.5 ps phase-matched, 40 GHz	Equipment connections to replica channel & DUT
Gen4 Base Test Fixture Set	PCI-SIG	Test fixtures	Required	1	Gen 4 Base Rev3 Test Fixtures^{3}	Provided by PCI-SIG
RXSW-FL1-PCIE4C	Tektronix	SW option	Required	1	PCIe Gen4 Receiver Software	Gen4 BASE and CEM Rx test software - Floating, Time Based, 1 year
RXSW-FLP-PCIE4C						Gen4 BASE and CEM Rx test software - Floating, Perpetual
RXSW-NL1-PCIE4C						Gen4 BASE and CEM Rx test software - Node Locked, Time Based, 1 year
RXSW-NLP-PCIE4C						Gen4 BASE and CEM Rx test software - Node-Locked, Perpetual

PCIe Gen4 CEM

Item	Vendor	Type	R/O	Quantity	Description	Notes
DPO72504DX, DPO73304SX	Tektronix	Equipment	Required	1	≥25 GHz minimum bandwidth oscilloscope	
DJA	Tektronix	Option	Required	1	DPOJET Advanced option	DPOJET advanced Jitter, Eye & Timing Analysis SW option

Table continued…

Item	Vendor	Type	R/O	Quantity	Description	Notes
MP1900A	Anritsu	Equipment	Required	Pick 1	Anritsu ≥16 Gb/s BERT, add RXSW-XXX-PCIE4C RX software	NRZ or PAM4 Config can be used for Gen3/4/5
BSX240	Tektronix				Tektronix 24 Gb/s BERT, options TXEQ, STR, add BSXSICOMB and BSXPCI4CEM software	
174-6659-00	Tektronix	Tek Accessories	Required	1	Cable pair; 2.92 mm-to-SMP, Right Angle, 1ps matched, 1000 mm, 20 GHz	PCIe refclk from BSX to CBB (AIC) or Pcie refclk out of CLB to BSX refclk input (rear).
174-6663-01	Tektronix	Tek Accessories	Required	0 or 1	Cable pair; 2.92 mm to 2.92 mm, Straight, 1.5 ps matched, 500 mm, 40 GHz	Power divider out to Error Detector in
174-6665-00	Tektronix	Tek Accessories	Required	1	Cable; 2.92 mm to 2.92 mm, Right Angle-Right Angle, 300 mm, 20 GHz	BSX Subrate clock out to BSX Error Detector clock in.
174-6666-01	Tektronix	Tek Accessories	Required	1	Cable; SMA-to-SMA, Right Angle-Right Angle, 500 mm, 20 GHz	BSX Pattern Trigger out to TekScope Aux input
PMCABLE1M	Tektronix	Tek Accessories	Required	2 or 3	Cable pair; 2.92 mm to 2.92 mm, Straight, 1.5 ps matched, 1000 mm, 40 GHz	BSX TX out to DUT RX in and DUT TX out to Power Divider input.
SMP Terminator	Fairview Microwave	3rd Party	Required	Depends	50 Ohm (Female)	Quantity depends on the number of unused lane. x1 = Qty 0, x4 = Qty 6, x8 = Qty 14, x16 = Qty 30.
MPR40-2	Fairview Microwave	3rd Party	Required	2	2-Way Power Divider 2.92 mm Connectors, 40 GHz	Or equivalent
SM3242	Fairview Microwave	3rd Party	Required	2	Adapter, 2.92 mm Male to 2.92 mm Male	Power divider output to TekScope input
SD3473	Fairview Microwave	3rd Party	Required	2	DC Block, 26.5 GHz	Or equivalent
ATX Power supply	Corsair	3rd Party	Required	1	ATX power supply for System board power	As required for DUT power. Any vendor ATX power supply will work.
PCIe Gen 4 Test Fixtures	PCI-SIG	3rd Party	Required	1	Gen4 CBB, CLB and Variable ISI board	Available only from PCI-SIG directly
SMP-SMP Cables	PCI-SIG	3rd Party	Required	4	SMP-SMP cables	
SMA-SMP (2.6")	PCI-SIG	3rd Party	Required	4	SMP-SMP cables	
Power USB – Basic	Power USB	3rd Party	Optional	1	Power USB power strip	For DUT reset automation. Not compatable with 240 VAC systems
AH54192A	Anritsu	3rd Party	Optional	1	PCIe Gen4 Active Redriver (back channel equalization)	High loss back channels (DUT Tx to Error Detector) may need Active Equalization
C7035	Centric RF	3rd Party	Recommended	6	Adapter; 2.92 mm Right Angle Male-Female	BERT I/O and Power Divider output to BSX Eror Detector

Table continued…

Item	Vendor	Type	R/O	Quantity	Description	Notes
RXSW-NLP-PCIE4C	Tektronix	Software	Required	Pick 1	Gen4 RX CEM and BASE test software - Node-Locked, Perpetual	
RXSW-NL1-PCIE4C					Gen4 RX CEM and BASE test software - Node Locked, Time Based, 1 year	
RXSW-FLP-PCIE4C					Gen4 RX CEM and BASE test software - Floating, Perpetual	
RXSW-FL1-PCIE4C					Gen4 RX CEM and BASE test software - Floating, Time Based, 1 year	

PCI PLL Bandwidth (Gen 5/4/3)

Item	Vendor	Type	R/O	Quantity	Description
MP1900A	Anritsu	Equipment	Required	1	≥32 Gb/s BERT
DPS73304SX	Tektronix	Equipment	Required	1	Single Stack 33 GHz or better (e.g. Dual-Stack 50 GHz SX oscilloscope)
DPO7AFP	Tektronix	Equipment	Optional	1	Auxiliary Front Panel
DPO7RFK2	Tektronix	Tektronix Accessory	Required	2	Attenuator Kit
PMCABLE1M	Tektronix	Tektronix Accessory	Required	2	Cable pair; 2.92-to-2.92 mm, Straight, 1.5 ps matched, 1000 mm, 40 GHz
DJA	Tektronix	Option	Required	1	DPOJET Advanced option
TF-PCIE5-CEM-X1[8]	PCI-SIG	Test Fixtures	Required	1	Gen 5 CEM Test Fixtures
TF-PCIE5-CEM-X16[8]	PCI-SIG	Test Fixtures	Required		
RXSW-NLP-PLLBW-PCEG5 or RXSW-NL1-PLLBW-PCEG5 or RXSW-FLP-PLLBW-PCEG5 or RXSW-FL1-PLLBW-PCEG5	Tektronix	Software	Required	1	License; PCIe Gen 5/4/3 PLL BW Software; Perpetual; Node-Locked OR 1 year subscription; Node-Locked OR Perpetual; Floating OR 1 year subscription; Floating

Host system software requirements Microsoft Windows 10

Tektronix is registered to ISO 9001:2015 and ISO 14001:2015.

[8] It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit

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For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit *www.tek.com*.

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