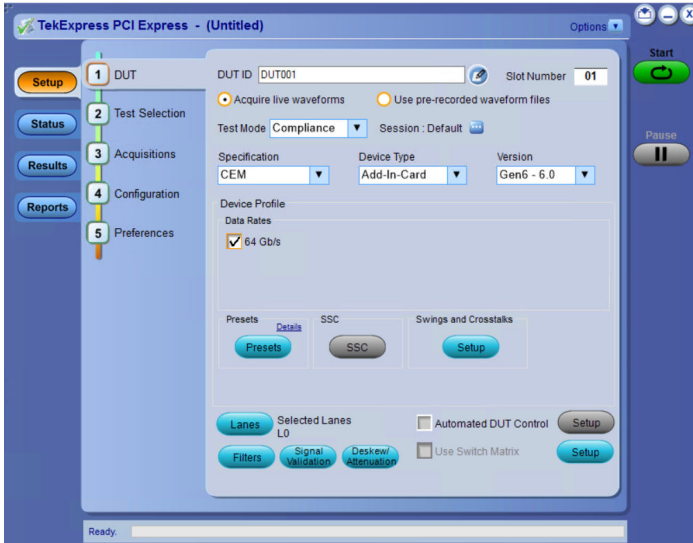


PCI Express® Transmitter Compliance/Debug Test Solution

DPO-MSO70000 Option PCE6, PCE5, PCE4, and PCE3 Datasheet

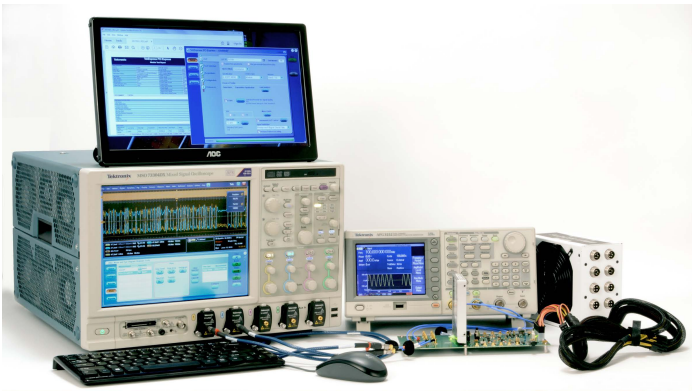
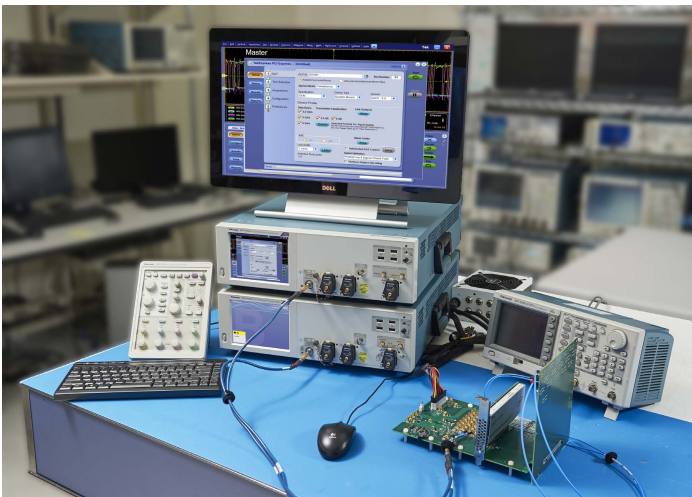


compatibility of Non-return-to-zero (NRZ). The multilevel (PAM4) signaling brings new signal integrity challenges to both design and validation efforts. Tektronix PCI Express 6.0 compliance testing software minimizes the challenges by automated testing that ensures measurement accuracy and repeatability.

The software Option PCE6 (Gen 6), PCE5 (Gen 5), PCE4 (Gen 4), and PCE3 (Gen 1/2/3) applications provide the most comprehensive solution for PCI Express Transmitter and System Reference Clock compliance testing as well as debug and validation of PCI Express devices per the PCI-SIG® Base & CEM specifications.

Features and benefits

- Support for PCI Express Gen 1 to Gen 6 Base and CEM transmitter testing for the Tektronix DPO/MSO70000 Series oscilloscopes
- Reference Clock jitter and signal integrity measurements for Gen 1 to Gen 5 using Intel Clock Jitter Tool, Skyworks PCIe Clock Jitter Tool, and Tektronix DPOJET
- 64 GT/s (PAM4) signal integrity measurements using PAMJET/DPOJET
- PCIe Gen 6 Tx Equalization Preset test using Linear Fit Pulse Response method
- Autoset oscilloscope for both vertical and horizontal scales for accurate and specification compliant measurements
- Automated acquisition and waveform management to simplify testing across supported data rates, Tx compliance patterns, and lane widths
- Automated DUT control to step through data rates and compliance patterns
- RF switch automation of PCIe Gen 3 to Gen 5 test solution, supporting up to x16 lanes
- Support for NVMe and CXL physical layer testing
- De-embed the impact of a break-out channel, test fixtures, and cables to achieve measurements at the test point of interest (requires Option SDLA Serial Data Link Analysis)
- Flexible test selection: configurable list of test items per the Base specification and CEM specification. Enabling retest of measurement of interest
- SigTest integration: Uses SigTest EXE (using command line interface) to perform the analysis of acquired waveforms, providing the ability to test a system using the PCI-SIG®-recommended analysis tool
- Enable parallel waveform analysis for faster test throughput
- Adopted new AC Fit method for measuring PCI Express 5.0 Tx Preset.
- Generating single test report with summary with Pass/Fail results, and detailed informative test items and eye diagrams
- Summary table at the top of the report for quick glance of results for normative measurement
- Pattern matching: Verifies that the correct set of compliance patterns are sent by the transmitter before acquiring signals for compliance analysis. The features only support up to Gen3 to the last of the list

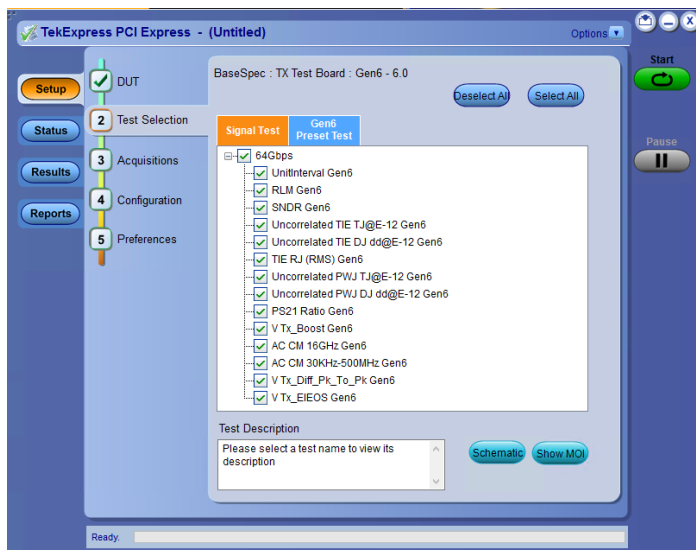


The PCI Express 6.0 introduced Four-Level Pulse Amplitude Modulation (PAM4) signaling to achieve 64 GT/s data rate while maintaining backward

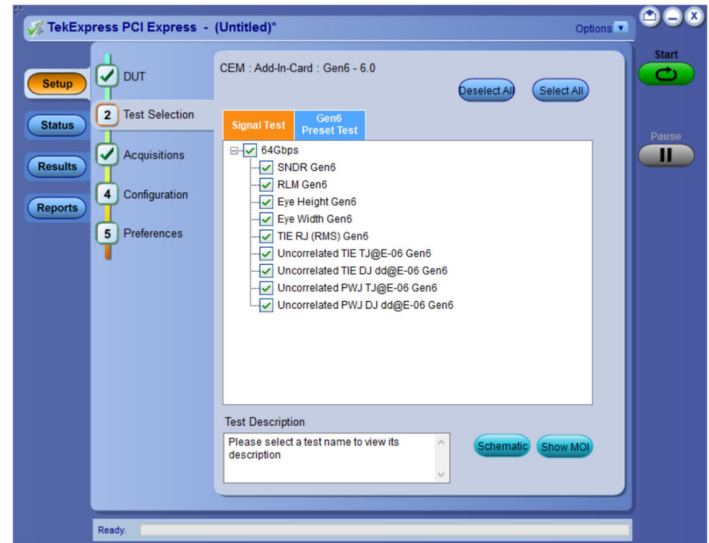
- PHY level protocol decode: Decodes and displays the PCIe data in a protocol-aware view. A time-correlated event table view with waveforms allows for quickly searching through events of interest, and this only supports to Gen3
- Multi-lane testing: Perform analysis on multiple lanes of PCI express data to speed up the Tx analysis in a multi-lane system
- Compliance and debug: Provides a toolkit of DPOJET-based setups to quickly switch into debug and validation mode when a DUT fails compliance
- Comprehensive programmatic interface: Enables automation of programs and scripts to call PCIe related TekExpress functions

Applications

Tektronix provides the most comprehensive solutions for validation and compliance of PCI Express transmitters at the Base (silicon) and system level including support for CEM, U.2, and M.2 interfaces. Numerous protocols utilizing the PCI Express physical layer including NVMe and CXL can take advantage of the transmitter and reference clock automation under TekExpress software solution.



TekExpress PCIe test selection for compliance test analysis



Gen 6 CEM measurements of signal test



Gen 6 CEM measurements of preset test

The Tektronix Option PCE3 (Gen 1/2/3), PCE4 (Gen 4), PCE5 (Gen 5) and PCE6 (Gen 6) includes compliance and debug testing and electrical validation for the following:

- Root complex base Tx jitter and voltage
- Endpoint base Tx jitter and voltage
- Switches
- Bridges
- Add-In cards
- System boards
- Embedded systems
- Express module

The Tektronix Option PCE3, PCE4 and PCE5 applications include a TekExpress™ compliance automation solution that integrates SigTest from the

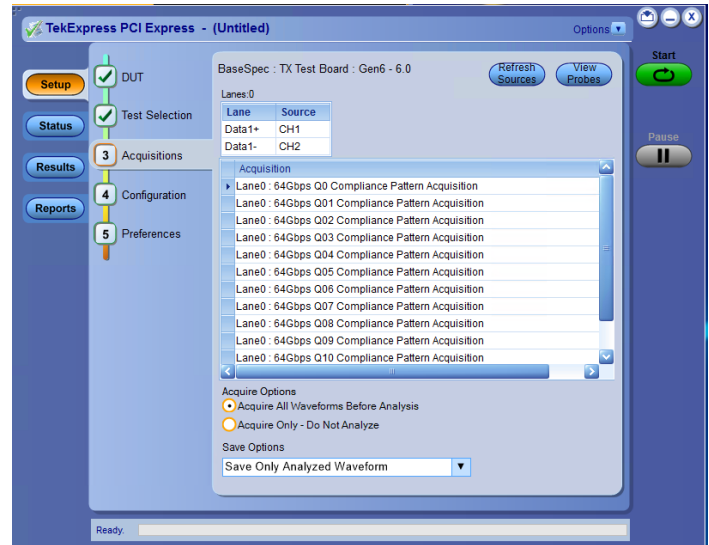
PCI-SIG as well as Tektronix DPOJET-based PCI Express Jitter and Eye Diagram analysis tools for debug purposes in a single software package.

The Tektronix Option PCE6 (Gen 6) includes the following signal quality measurements:

Measurements	BASE Tx Test Board Gen 6	Add-In Card Gen 6	System Board Gen 6
UnitInterval	✓		
AC_CM 16 GHz	✓		
AC_CM 30 KHz-500 MHz	✓		
PS21 Ratio	✓		
VTx_EIEOS	✓		
VTx_Diff_pk_To_Diff_pk	✓		
VTx_Boost	✓		
Uncorrelated TIE TJ@E-06	✓	✓	
Uncorrelated TIE DJ DD@E-06	✓	✓	
Uncorrelated PWJ TJ@E-06	✓	✓	
Uncorrelated PWJ DJ DD@E-06	✓	✓	
TIE RJ (RMS)	✓	✓	
SNDR	✓	✓	
RLM	✓	✓	✓
EyeHeight		✓	✓
EyeWidth		✓	✓

TekExpress compliance automation is available now for PCIe Gen 1-3 CEM and Gen 3 Base via Option PCE3, Gen 4 Base and CEM via Option PCE4, Gen 5 Base and CEM via Option PCE5, and Gen 6 Base and CEM via Option PCE6.

The Tektronix Option PCE3, Option PCE4, Option PCE5, and Option PCE6 applications are compatible with Tektronix DPO/MSO70000 series oscilloscopes that are designed to meet the challenges of the next generation of serial data standards such as PCI Express. The Tektronix DPO/MSO70000 series of oscilloscopes have been approved by PCI-SIG for compliance testing.



TekExpress oscilloscope acquisition setup

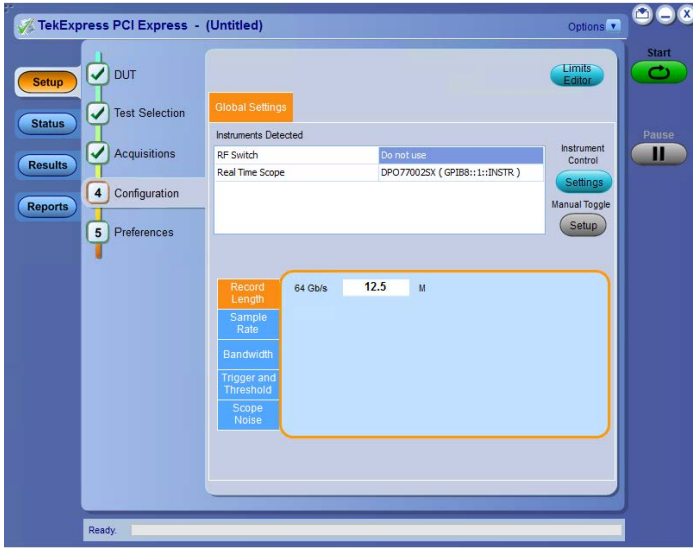
Compliance testing

The PCI-SIG provides PCI Express compliance tests for testing PCI Express CEM form factor, including System and Add-in-card (AIC). For a PCI Express system or a device to be placed on the Integrators List, the system or device must pass interoperability and compliance testing. For electrical validation, the PCI-SIG uses SigTest Post Capture Analysis Software that uses acquisitions from an oscilloscope connected to the PCI-SIG's CBB (main board + riser) test fixture for add-in cards or CLB test fixture for systems to perform the analysis. Manually capturing the required waveforms and analyzing them is tedious, time consuming, and error prone.

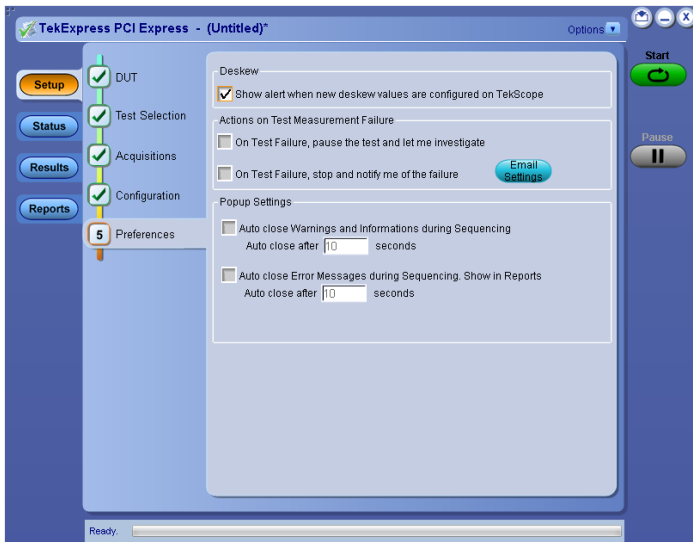
The Tektronix Option PCE3, Option PCE4, Option PCE5, and Option PCE6 TekExpress Automation for PCI Express Transmitter Compliance reduces the effort and accelerates the compliance testing for PCI Express systems and devices with several unique and innovative capabilities. These options ultimately allow the testing of devices that support various technologies, such as NVMe, which is supported as an add-in card device, or through a U.2 or M.2 connector.

The Tektronix Option PCE3, PCE4, PCE5, and PCE6 TekExpress Automation software can control the DUT using selected models of a Tektronix AFG (Arbitrary Function Generator) or AWG, GRL PCIe 3/4 Controller Anritsu Z2025A CBB Controller, or NI USB6501 CBB controller to toggle DUT and automatically cycle it through various speeds, de-emphasis, and presets that are necessary for the compliance test. This eliminates the error-prone manual push button approach normally used for DUT control on the CBB and CLB test fixtures. This feature only supports to CEM testing.

A complete test run requires multiple waveforms to be acquired at different DUT settings per lane. This waveform set will increase by the number of lanes that need to be analyzed. The ability to manage and store the required data for analysis and future reference is an important criterion for any compliance solution. The Option PCE3, Option PCE4, Option PCE5, and Option PCE6 TekExpress automation software, apart from adjusting the horizontal and vertical settings as well as the acquisition depth for optimal signal quality for accurate analysis, provides easy analysis to manage multiple acquired waveforms.



TekExpress setup configuration



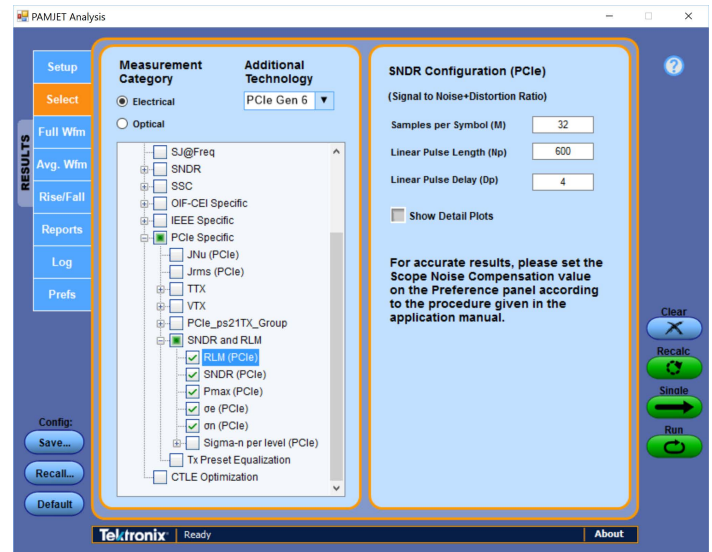
TekExpress setup preferences

Options PCE3, PCE4, PCE5 makes use of the PCI-SIG's SigTest EXE to analyze the acquired waveforms. Thus makes the results of the analysis consistent with the SigTest post-capture analysis software used at PCI-SIG workshops for compliance testing.

The Option PCE3, PCE4, and PCE5 TekExpress automation software provides flexibility in selecting data rates, voltage swing, presets, and the tests to run. It also provides the option to de-embed the effects of the channel and the test fixtures and provide an accurate representation of the signal at the pins as required by the specification.

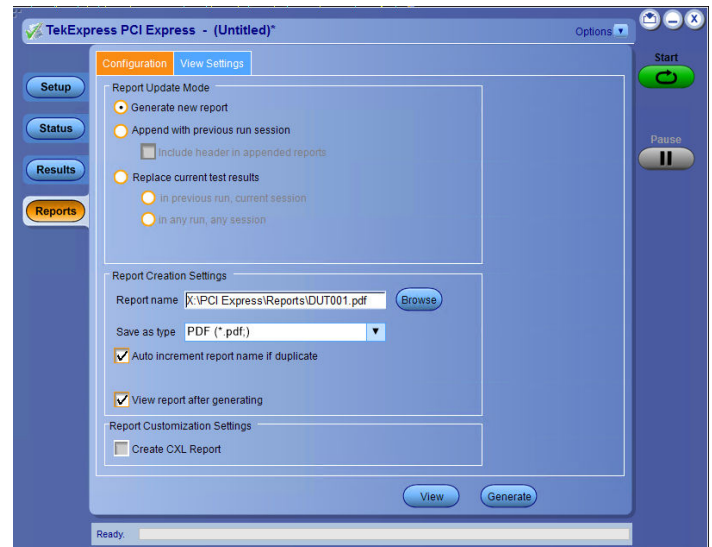
PCE6 TekExpress uses Tektronix PAM analysis tool PAMJET for the measurement. During analysis, TekExpress will automatically set up the tool as per the specification, capture results, and report them to the user. PAMJET also allows expert users to configure the PAMJET tool to test the DUT in non-specification settings for debugging purposes.

PAMJET introduces the Signal to Noise Distortion Ratio (SNDR) measurements with measurement methodology updated to support the latest PCI Express 6.0 Base and CEM Specification. Support for instrument noise compensation is integrated to improve measurement accuracy.



Selection of Measurement Category in PAM4 Transmitter Analysis

All the analysis results are compiled in a PDF/HTML/CSV formatted report that can include pass/fail summary, eye diagrams, setup configuration, and user comments. The contents of the report can be customized to include information of interest such as append results and custom report generation based on test name pass/fail equalization.



TekExpress report generation preferences

TekExpress PCI Express - (Untitled)*

Overall Test Result: Pass

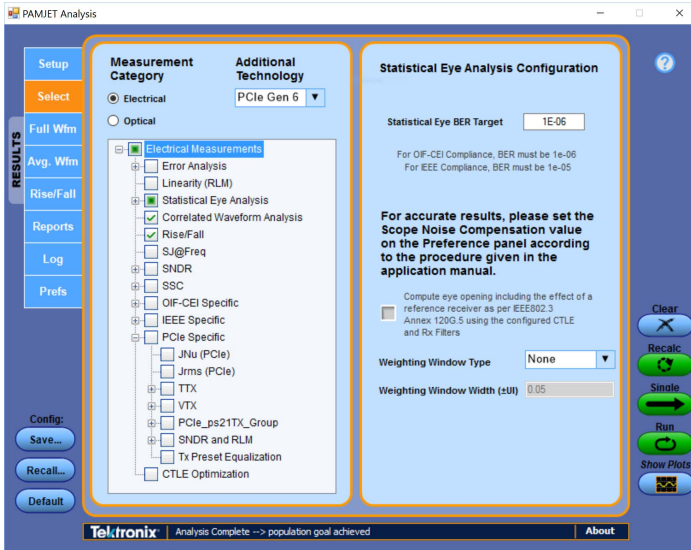
Description	Details	Generation	Pass/Fail	Value	Margin
Lane0			Pass		
Unit Interval	Mean Unit Interval	2.5Gbps	Pass	400.028 ps	L:0.148ps H:0.092ps
High Limit			Pass	400.12	
Low Limit			Pass	399.88	
Unit Interval	Min Unit Interval	2.5Gbps	Pass	400.028 ps	L:0.148ps
Unit Interval	Max Unit Interval	2.5Gbps	Pass	400.028 ps	H:0.092ps
Mask Hits (All Bits)	Mask Hits	2.5Gbps	Pass	0 hits	N.A
Composit Eye Height	Composit Eye Height	2.5Gbps	Informative	583.147 mV	N.A
Number Passing Eyes	Number Passing Eyes	2.5Gbps	Pass	2495	L:2495
Number Failing Eyes	Number Failing Eyes	2.5Gbps	Pass	0	H:0
Transition Eye Diagram	Min Transition Eye Height	2.5Gbps	Informative	714.774 mV	N.A
Transition Eye Diagram	Min Transition Voltage	2.5Gbps	Pass	-454.658 mV	L:145.342 mV
Transition Eye Diagram	Max Transition Voltage	2.5Gbps	Pass	453.819 mV	H:146.181 mV
Transition Eye Diagram	Min Transition Top Margin	2.5Gbps	Pass	97.638 mV	L:97.638m V
Transition Eye Diagram	Min Transition Bottom Margin	2.5Gbps	Pass	-103.136 mV	H:103.136 mV

Completed:

TekExpress results summary

PAMJET for GEN 6 measurements

Tektronix PAMJET is an industry-leading PAM4 analysis tool with best in class clock recovery and integrated configurable reference receiver, which is used for Gen 6 measurements. This PAMJET tool can configure the measurement, perform Bessel Thompson filtering, clock recovery, CTLE, Pattern Guidance, and report the results. These built-in functions are specifically designed to aid the Gen 6 Base and CEM testing.



PAMJET Gen 6 measurement



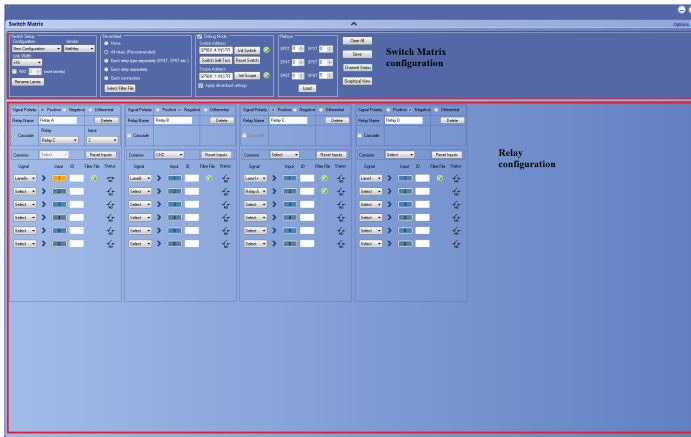
PAMJET PCIe Gen 6 analysis

Reference Clock Testing with TekExpress

Reference Clock testing has moved from optional to required for many designs due to the jitter limit decrease driven by the highest data rates supported by the PCI-SIG standards. Additionally, with the removal of dual-port (data and clock Tx testing) for Gen 5 systems, compliance is required on the reference clock. The TekExpress PCIe solution has now integrated the SkyWorks Clock Jitter Tool to allow an automated hassle-free Reference Clock testing. Once the user connects the Reference Clock output to the oscilloscope, the TekExpress PCIe software will acquire the signal, invoke the SkyWorks Clock Jitter Tool, and provide Reference Clock test results from Gen 1 to Gen 5. Instrument noise compensations is supported with the Skyworks Clock Jitter Tool.

Switch Matrix automation

Switch Matrix application allows to configure and setup automated multi-lane testing using RF switch. The solution allows you to map each of the several transmitter signals and forward the selected input either to another relay or to the oscilloscope channel. Option SWX-PCE supports x12 and x16 lanes using Keithley. While Keithley, Gigatronics supports up to Gen4, and Minicircuits supports up to Gen5 switches respectively, and enhances throughput and automated test speed.



Switch Matrix application settings



Switch configuration example

Debug and validation

If a DUT or Add-In card fails any portion of the compliance test, the application includes a DPOJET-based debug and analysis tool kit customized for debug and validation of PCI Express interfaces.

The new jitter measurements introduced with PCIe Gen 3 and Gen 4 provide separate limits for data dependent (DDJ) and uncorrelated deterministic jitter (UDJDD). It is important to separate DDJ (which can be compensated with transmitter and receiver equalization) and UDJDD (which can be caused by effects such as crosstalk and power supply noise).

Apart from the above Jitter measurements, Pulse Width Jitter (PWJ) is a new measurement that addresses the increased channel loss at 8 to 16 Gb/s. The purpose of the PWJ measurement is to ensure that lone bits meet minimum pulse width requirements. All new jitter measurements implement Q-scale extrapolation as defined in the base specification. The Tektronix Option PCE3, PCE4, PCE5, and PCE6 provide the complete set of PCI Express 3.0, 4.0, 5.0, and 6.0 Base Spec jitter measurements enabling silicon designers to verify that their silicon meets the base specification requirements.

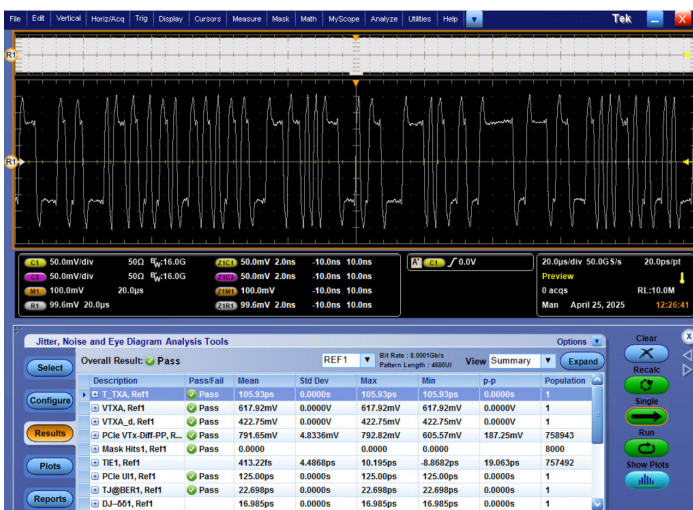
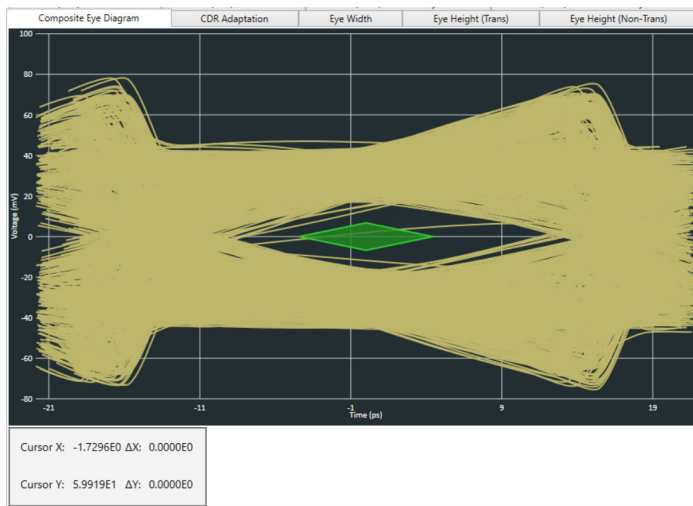
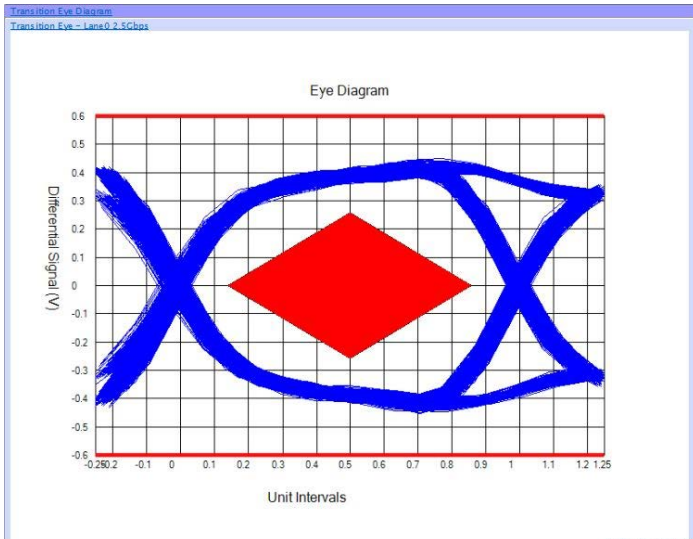
Furthermore, the base specification requirements are defined at the pins of the transmitter. Before the measurements are computed the test channel must be de-embedded. De-embed filters can be easily created using the Tektronix Option SDLA64 Serial Data Link Analysis software and then quickly entered into the Option PCE3 and Option PCE4 base specification measurement setup and saved for future use. In addition to jitter, Option PCE3 and Option PCE4 also provide voltage, package loss, and transmitter equalization measurements.

Option PCE3 and Option PCE4 leverage the channel modeling and receiver equalization functionality of the Tektronix Option SDLA64 software to support CEM measurements. Unlike other solutions, Option PCE3 and Option PCE4 provide full visibility to the signal as it has been modified to embed the compliance channel and provide receiver equalization. Eye diagrams and measurements can be set up to visually see the results of channel embedding, CTLE application, and DFE. For example, when determining the optimal Rx Equalization settings (CTLE setting and DFE tap value) the resulting eye diagrams and measurements show the effects of post processing on the acquired signal. Compliance measurements can then be taken on the waveform.

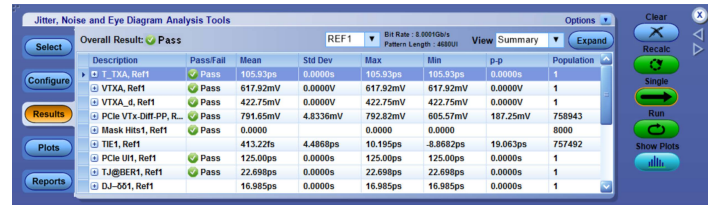
Tektronix® TekExpress PCIe Tx Add-In-Card Test Report			
Setup Information			
DUT ID	DUT001	Scope Model	DPO77002SX
Date/Time	4/16/2025 5:13:31 AM	Scope Serial Number	B321505
Device Type	CEM	SPC Factory Calibration	PASS/PASS
TekExpress PCIe Tx Version	v10.8.0.75	Scope FW Version	v10.15.0 Build 3
TekExpress Framework Version	v5.11.0.11	DPOJET Version	v10.5.0.2
TekExpress Execution Mode	Live	Channel Info	ATI
Compliance Mode	Yes	Probe CH1 Model	none
Spec Version	Gen6 - 6.0	Probe CH1 Serial Number	N/A
Voltage Swing	Full	Probe CH2 Model	none
SSC Status	Off	Probe CH2 Serial Number	N/A
ScnNumber	01	PAWJET Version	v10.10.1.746
Deskew Automation	Disabled		
Deskew Value	CH1 : 0 ps, CH2 : 29 ps		
Toggle Mode	Automatic		
Toggle Device	AFQ3252		
Eye - CTLE Optimization Mode	Auto		
Jitter - CTLE Optimization Mode	Auto		
PW - CTLE Optimization Mode	Auto		
Overall Test Result	Pass		
Overall Execution Time	01:45:02		
DUT COMMENT:		DUT001	

SNDR Gen6							
Measurement Details	Lane Name	Data Rate	Equalization	Measured Value	Test Result	Margin	
PCIe SNDR Mean	Lane0	64Gbps	OOCompliancePstern	34.211 dB	Pass	LL: 0.211dB, HL: 34dB	NA
PCIe Pstern Mean	Lane0	64Gbps	OOCompliancePstern	235.56 mV	Informative	LL: 201.56mV, HL: 34mV	NA
PCIe SignalE Mean	Lane0	64Gbps	OOCompliancePstern	2.9609 mV	Informative	LL: -31.0391mV, HL: 34mV	NA
PCIe SignalN Mean	Lane0	64Gbps	OOCompliancePstern	3.5035 mV	Informative	LL: -30.4965mV, HL: 34mV	NA

TekExpress PCI Express test report



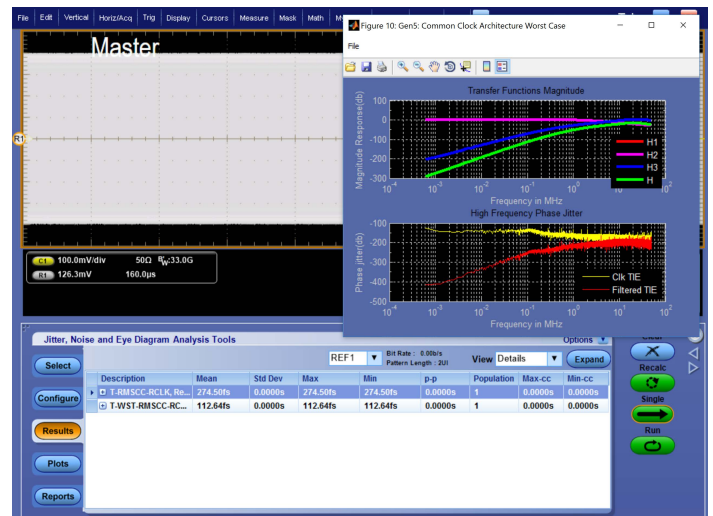
DPOJET PCE3 base specification measurement suite



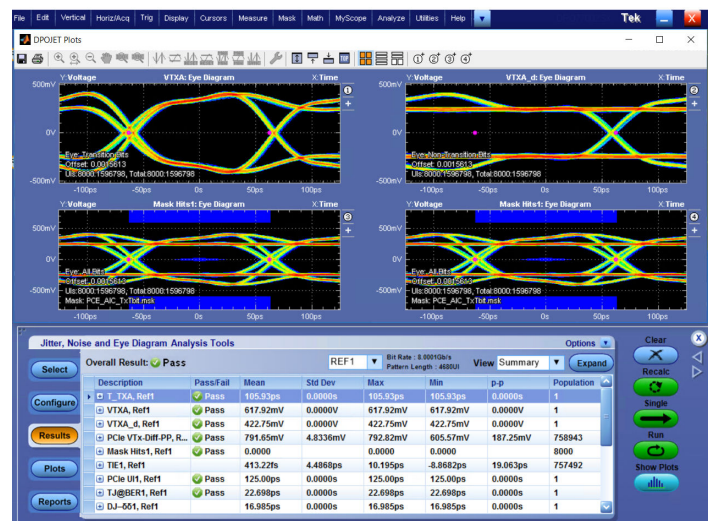
DPOJET PCE3 base specification measurement suite

DPOJET based Reference Clock measurements

The Tektronix DPOJET based RefClock measurements provide a reliable way to implement the Reference clock specifications described in the PCI Express Base Specification Rev 1.0 for Gen 1, Gen 2, Gen 3, Gen 4 and Gen 5.



Example of RefClk measurements, together with generated plots



DPOJET measurements and their plots

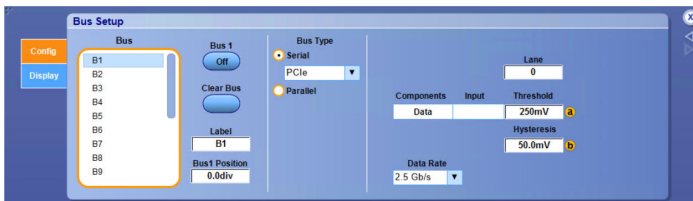
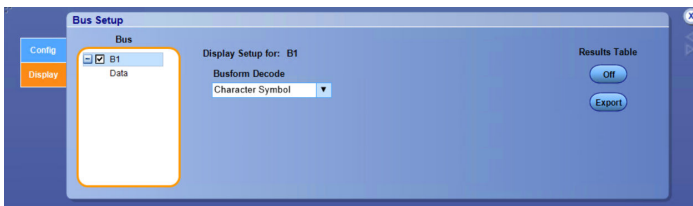
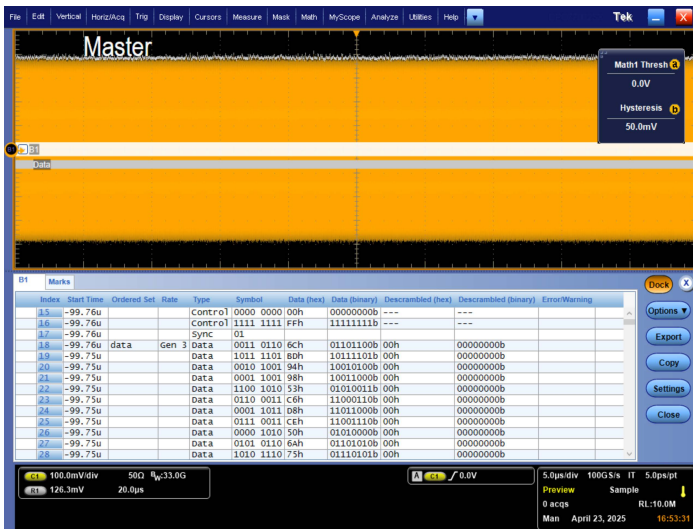
Comprehensive programmatic interface

You can use Standard Commands for Programmable Instruments (SCPI) to communicate with the TekExpress application. The Online Help document of

TekExpress application describes the steps for TCPIP socket configuration and TekVISA configuration to execute the SCPI commands.

PCI Express Decoder for Gen 1 - 4 (Option SR-PCle)

Decode and Display of PCIe data in a protocol-aware view with the characters and names that are familiar from the standard such as the ordered sets: SKP, Electrical Idle, and EIEOS. A time correlated event table view with waveform allows for quickly searching through events of interest simultaneously. All decoding features support PCIe generations 1 - 4. The PCIe trigger is easily configured through Bus Setup under the oscilloscope's Vertical menu with a variety of user-adjustable settings. The PCIe data stream is integrated with serial bus trigger and search for PCIe Gen 1 and Gen 2 allows for triggering on information of interest.



Comprehensive measurements for PCIe validation, debug, and precompliance

Tektronix Option PCE3, Option PCE4 and Option PCE5 provide measurements that span multiple test points and versions of the PCIe specification. All PCIe specifications, test points, and measurements supported are listed in the following sections.

Test method	Spec revision	PCI Express specification title	Test points defined
Rev 1.1	Rev 1.1	Base Specification	Transmitter and Receiver
	Rev 1.1	CEM Specification	System and Add-in Card Reference Clock
	Rev 1.0	Express Module Specification	Transmitter Path and System Board
	Rev 1.0	PCMCIA Express Card Standard	Host System Transmitter Express Card Transmitter
	Ver. 3.0 Rev 1.1	Mobile PCI Express Module (MXM) Electromechanical Specification	PCI Express
Rev 2.0	Rev 1.0	External Cabling Specification	Transmitter and Receiver Path
	Rev 2.0	Base Specification	Transmitter and Receiver Mobile Low-power Transmitter
	Rev 2.0	CEM Specification	System and Add-in Card (3.5 and 6 dB de-emphasis)
	Ver. 3.0 Rev 1.1	Mobile PCI Express Module (MXM) Electromechanical Specification	PCI Express
	Rev 1.0	Base Specification	Transmitter
Rev 3.0	Rev 1.0	CEM Specification	System and Add-in Card
	Rev 3.0	Test Specification	System and Add-in Card
	Rev 1.0	CEM Specification	System and Add-in Card
Rev 4.0	Rev 1.0	Base Specification	Transmitter
	Rev 1.0	CEM Specification	Transmitter
Rev 6.2	Rev 1.0	Base Specification	Transmitter
	Rev 0.7 - CEM	CEM Specification	Transmitter

Specifications

All specifications apply to all models unless noted otherwise.

Supported Reference clock measurements

Supported Reference clock measurements

Generation	Architecture	Measurements	Limits
PCIe 1.1	Common clock	T-CC- RCLK	Specified
		T-WST-CC- RCLK	Specified
	Independent RefClock	IR2.5GBPS	Specified
PCIe 2.1	Common clock	T-RMSSC-RCLK-5GBPS	Specified
		T-WST-RMSSC-RCLK-5GBPS	Specified
	Independent RefClock	IR5GBPS	Specified
PCIe 3.1	Common clock	T-RMSSC-RCLK	Specified
		T-WST-RMSSC-RCLK	Specified
	Independent RefClock	IR8GBPS	Specified
PCIe 4.0	Common clock	PCIE4_T-RMSSC-REFCLK	Specified
		PCIE4_T-WST-RMSSC-REFCLK	Specified
	Independent RefClock	IR16GBPS	Specified
PCIe 5.0	Common clock	PCIE5_T-RMSSC-REFCLK	Specified
		PCIE5_T-WST-RMSSC-REFclk	Specified
	Independent RefClock	IR32GBPS	Specified

Supported AC reference clock measurements

AC reference clock specifications ¹

Generation	Specifications	Measurements	Symbol
Common across all generations	AC reference clock specifications	Cycle to Cycle jitter	CC_JITTER
		Differential Input High Voltage	V_IH
		Differential Input Low Voltage	V_IL
		Duty Cycle	Duty Cycle
		Absolute Max input voltage	V _{max}
		Absolute Min input voltage	V _{min}
		Absolute Period (including Jitter and Spread Spectrum modulation)	Period Abs
		Falling Edge Rate	Falling-Edge-Rate
		Rising Edge Rate	Rising-Edge-Rate
		Average Clock Period Accuracy	Avg Prd Accur
		Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching	Rise fall Match
		Absolute crossing point voltage	VCROSS
		SSC SlewRate	SSC SlewRate

PCI Express 6.0 Base and CEM transmitter measurements

TX test	Pattern	Notes
SNDR	Compliance	Signal Noise Distortion Ratio
Voltage Differential Peak to Peak	Compliance	Measured with 64 levels 3s & 64 level 0ss
Transmit Equalization	Compliance	Q0-Q10 (PAM4) with AC step method
Tx Equalization Boost	Compliance	Q10 (full swing) & Q4 (reduced swing)
EIEOS min Voltage Swing	Compliance	Include package loss impact
Ratio Level Mismatch	Compliance	PAM4 measurement only
Uncorealted Tj	52UI Jitter Measurement	Jitter computed on each unique transission
Uncorealted Dj	52UI Jitter Measurement	Jitter computed on each unique transission
Uncorealted Dj	52UI Jitter Measurement	Informative
Pulser Width Jitter Tj	High Swing Toggle	0303 level pattern; noise comp included
Pulser Width Jitter Dj_dd	High Swing Toggle	0303 level pattern; noise comp included
Pulser Width Jitter Rj	High Swing Toggle	Informative
PS21	Compliance	Pseudo package dose

¹ PCIe TekExpress runs AC Reference Clock measurement using SkyWorks Clock Jitter tool and additionally report

- Ring Back Voltage
- Overshoot Voltage relative to V(IH)
- Undershoot Voltage relative to V(IL)

Parameter	PAMJET measurement	64 GT/s Limit Rev 0.7
SNDR	SNDR (PCle)	34 dB (min)
RLM	R _{LM} (PCle)	95% (min)
Uncorrelated Jitter T _j	T _{TX-uTJ} (PCle)	4.00 ps @ E-6 (max)
Uncorrelated Jitter Dj-dd	T _{TX-uDJDD} (PCle)	1.563 ps @ E-6 (max)
Uncorrelated Jitter R _j	T _{TX-uRJ} (PCle)	Informative
Pulse Width Jitter T _j	T _{TX-UPW-TJ} (PCle)	4.00 ps @ E-6 (max)
Pulse Width Jitter Dj-dd	T _{TX-UPW-DJDD} (PCle)	1.25 ps @ E-6 (max)
Pulse Width Jitter R _j	T _{TX-UPW-RJ} (PCle)	Informative
Tx Preset Test (Q0 to Q10)	Tx Preset Equalization	See Table below

Tx preset ratios and corresponding coefficient values for 64.0 GT/s

Preset #	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c ₋₂	c ₋₁	c ₊₁	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q0	0.0 ± 0.5	0.0 ± 0.5	0.0 ± 0.5	0.000	0.000	0.000	1.000	1.000	1.000	1.000
Q1	0.0 ± 0.5	-1.6 ± 0.5	0.0 ± 0.5	0.000	0.083	0.000	0.834	0.834	1.000	0.834
Q2	0.0 ± 0.5	3.5 ± 0.5	0.0 ± 0.5	0.000	0.167	0.000	1.000	0.834	0.834	0.834
Q3	0.0 ± 0.5	0.0 ± 0.5	-1.6 ± 0.5	0.000	0.000	-0.083	1.000	0.834	0.834	0.834
Q4	0.0 ± 0.5	0.0 ± 0.5	-3.5 ± 0.5	0.000	0.000	-0.167	1.000	1.666	1.666	1.666
Q5	-1.3 ± 0.5	4.7 ± 1.0	0.0 ± 0.5	0.042	-0.208	0.000	0.0584	0.0584	1.000	1.500
Q6	-1.6 ± 0.5	3.5 ± 0.5	-3.5 ± 0.5	0.042	-0.125	-0.125	0.750	1.500	0.750	0.416
Q7	2.9 ± 0.5	4.7 ± 1.0	0.0 ± 0.5	0.083	-0.208	0.000	0.0584	0.0584	1.000	0.418
Q8	3.5 ± 0.5	6.0 ± 1.0	0.0 ± 0.5	0.083	-0.250	0.000	0.500	0.500	1.000	0.334
Q9	-4.4 ± 1.0	6.9 ± 1.0	-1.6 ± 0.5	0.083	-0.250	0.042	0.500	0.416	0.916	0.250
Q10	0.0 ± 0.5	0.0 ± 0.5	Note 2	0.000	0.000	Note 2	1.000	Note 2	Note 2	Note 2

Supported base specification measurements

Supported PCI Express 4.0 Base Transmitter measurements

Parameter	DPOJET measurement	8.0 GT/s, Rev 3.0	16.0 GT/s, Rev 1.0
Full Swing Tx voltage with noTxEq	V-TX-FS-NO-EQ	Specified	Specified
Reduced Swing Tx voltage with noTxEq	V-TX-RS-NO-EQ	Specified	Specified
Min swing during EIEOS for full swing	V-TX-EIEOS-FS	Specified	Specified
Min swing during EIEOS for reduced swing	V-TX-EIEOS-RS	Specified	Specified
Pseudo package loss Root device	ps21TXRootdevice	Specified	Specified
Pseudo package loss AIC device	ps21TXAICdevice	Specified	Specified

Table continued...

Parameter	DPOJET measurement	8.0 GT/s, Rev 3.0	16.0 GT/s, Rev 1.0
Tx uncorrelated total Jitter	T-TX-UTJ	Specified	Specified
Tx uncorrelated deterministic jitter	T-TX-UDJDD	Specified	Specified
Data dependent jitter	T-TX-DDJ	Specified	Specified
Total uncorrelated PWJ	T-TX-UPW-TJ	Specified	Specified
Deterministic DjDD uncorrelated PWJ	T-TX-UPW-DJDD	Specified	Specified
Maximum Boost voltage ratio for full swing	V-TX-FS-BOOST	Specified	Specified
Maximum Boost voltage ratio for reduced swing	V-TX-RS-BOOST	Specified	Specified
Tx DC peak-peak common mode voltage	VTX_DC_CM	Specified	NA
Absolute Delta of DC Common Mode Voltage between D+ and D-	VTX_CM_DC_LINE_DELTA	Specified	NA
Electrical Idle Differential Peak Output Voltage	VTX_IDLE_DIFF_AC_p	Specified	NA
DC Electrical Idle Differential Output Voltage	VTX_IDLE_DIFF_DC	Specified	NA

Supported PCI Express 5.0 Base Transmitter measurements

Parameter	DPOJET measurement	32.0 GT/s, Rev 5.0
Tx uncorrelated total Jitter	T-TX-UTJ	6.25 ps (max)
Tx uncorrelated deterministic Jitter	T-TX-UDJDD	3.125 ps (max)
Data dependent Jitter	T-TX-DDJ	NA
Total uncorrelated PWJ	T-TX-UPW-TJ	6.25 ps (max)
Total Random Jitter (informative)	T-TX-RJ	0.23-0.45 ps rms
Deterministic DjDD uncorrelated PWJ	T-TX-UPW-DJDD	2.5 ps (max)
RMS RefClk jitter for common RefClk architecture	T-RMSCC-RCLK	0.25 ps (max)
IR RefClk jitter	IR32GBPS	NA
Pseudo Package Loss	ps21Tx	(max) 8.5dB
Boost ratio	VTX-BOOST	8.0 (min) dB
EIEOS	VTX-EIEOS	250 mV
TX Differential Peak to Peak	VTX-DIFF-PP	800 mV (max) 1300mV
Unit Interval	UI	31.246875 (min) 31.253125 (max)

Differential transmitter (Tx) output measurements

Parameter	Symbol(s)	2.5 GT/s Rev 1.1/2.0	5 GT/s Rev 2.0
Clock Recovery	NA	Specified	Specified
Unit Interval	UI	Specified	Specified

Table continued...

Parameter	Symbol(s)	2.5 GT/s Rev 1.1/2.0	5 GT/s Rev 2.0
Differential Peak-to-Peak Tx Voltage Swing	$V_{TX-DIFF-P-P}$ $V_{TX-SWING}$ $V_{TX-EYE-FULL}$	Specified	Specified
Low-power Differential Peak-to-Peak Tx Voltage Swing	$V_{TX-SWING-LOW}$ $V_{TX-EYE-HALF}$	Specified	Specified
De-emphasized Output Voltage Ratio	$V_{TX-DE-RATIO}$	Not Specified	Specified
Instantaneous Lane Pulse Width	$T_{MIN-PULSE}$	Not Specified	Specified
Transmitter Eye including All Jitter Sources	T_{TX-EYE} $T_{TX-EYE-TJ}$	Specified	Specified
Maximum Time between the Jitter Median and Maximum Deviation from the Median	$T_{TX-EYEMEDIAN-to-MAXJITTER}$	Specified	Specified
Deterministic Jitter	$T_{TX-DJ-DD}$	Not Specified	Specified
Tx RMS Jitter <1.5 MHz	$T_{TX-LF-RMS}$	Not Specified	Specified
D+/D– Tx Output Rise/Fall Time	$T_{TX-RISE}$ $T_{TX-FALL}$	Specified	Specified
Tx Rise/Fall Mismatch	$T_{RF-MISMATCH}$	Not Specified	Specified
AC Peak-to-Peak Common Mode Output Voltage	$V_{TX-CM-AC-PP}$	Not Specified	Specified
AC Peak Common Mode Output Voltage	$V_{TX-CM-AC-P}$	Specified	Specified
Absolute Delta of DC Common Mode Voltage between D+ and D–	$V_{TX-CM-DC-LINE-DELTA}$	Specified	Specified

Supported CEM specification measurements

Add-in Card 8 GT/s transmitter path compliance measurements

Parameter	Symbol
Transition Eye Voltage	PCIe V-TXA
Nontransition Eye Voltage	PCIe V-TXA-d
Eye Width	PCIe T-TXA

Add-in Card transmitter path compliance measurements

Parameter	Symbol(s)	2.5 Gt/s Rev 1.1/2.0	5 GT/s Rev 2.0
Clock Recovery	NA	Specified	Specified
Unit Interval	UI	Specified	Specified
Eye Height of Transition Bits	V_{TXA}	Specified	Specified
Eye Height of Nontransition Bits	V_{TXA_d}	Specified	Specified
Eye Width with Sample Size of 10^6 UI	T_{TXA} in Rev 1.1	Specified	Not Specified
Jitter Eye Opening at BER 10^{-12}	T_{TXA} in Rev 2.0	Specified	Specified
Maximum Median-Max Jitter Outlier with Sample Size of 10^6 UI	$J_{TXA-MEDIAN-to-MAX-JITTER}$	Specified	Not Specified
Total Jitter at BER 10^{-12}	TJ at BER 10^{-12}	Not Specified	Specified
Deterministic Jitter at BER 10^{-12}	Max DJ	Not Specified	Specified

System board transmitter path measurements

Parameter	Symbol(s)	2.5 GT/s Rev 1.1/2.0	5 GT/s Rev 2.0
Clock Recovery	NA	Specified	Specified
Unit Interval	UI	Specified	Specified
Eye Height of Transition Bits	V_{TXS}	Specified	Specified
Eye Height of Nontransition Bits	V_{TXS_d}	Specified	Specified
Eye Width with Sample Size of 10^6 UI	T_{TXS} in Rev 1.1	Specified	Not Specified
Jitter Eye Opening at BER 10^{-12}	T_{TXS} in Rev 2.0	Specified	Specified
Maximum Median-Max Jitter Outlier with Sample Size of 10^6 UI	$J_{TXA-MEDIAN-to-MAX-JITTER}$	Specified	Not Specified
Total Jitter at BER 10^{-12}	TJ at BER 10^{-12}	Not Specified	Specified
Deterministic Jitter at BER 10^{-12}	Max DJ	Not Specified	Specified

Reference clock measurements

Parameter	Symbol	2.5 Gt/s Rev 1.1/2.0
Reference Clock Phase Jitter at BER 10^{-6}	NA	Specified

PCI ExpressModule™ measurements

ExpressModule Add-in Card
transmitter path measurements

Parameter	Symbol	Rev 1.0
Clock Recovery	NA	Specified
Unit Interval	UI	Specified
Eye Height of Transition Bits	V_{TXA}	Specified
Eye Height of Nontransition Bits	V_{TXA_d}	Specified
Eye Width with Sample Size of 10^6 UI	T_{TXA} in Rev 1.1	Specified
Jitter Eye Opening at BER 10^{-12}	NA	Specified
Maximum Median-Max Jitter Outlier with Sample Size of 10^6 UI	$J_{TXA-MEDIAN-to-MAX-JITTER}$	Specified

ExpressModule system board
transmitter path measurements

Parameter	Symbol	Gen 1 Rev 1.0
Clock Recovery	NA	Specified
Unit Interval	UI	Specified
Eye Height of Transition Bits	V_{TXS}	Specified
Eye Height of Nontransition Bits	V_{TXS_d}	Specified
Eye Width with Sample Size of 10^6 UI	T_{TXS}	Specified
Jitter Eye Opening at BER 10^{-12}	NA	Specified
Maximum Median-Max Jitter Outlier with Sample Size of 10^6 UI	$J_{TXA-MEDIAN-to-MAX-JITTER}$	Specified

PCI Express external cabling measurements

External cabling transmitter path
measurements

Parameter	Symbol	Rev 1.0
Clock Recovery	NA	Specified
Unit Interval	UI	Specified
Eye Height of Transition Bits	V_{TXA}	Specified
Eye Height of Nontransition Bits	V_{TXA_d}	Specified
Jitter Eye Opening at BER 10^{-12}	TrxA at BER 10^{-12}	Specified
Eye Width with Sample Size of 10^6 UI	TrxA at 10^6 Samples	Specified

PCMCIA ExpressCard™ measurements

ExpressCard - Module transmitter
path measurements

Parameter	Symbol	Release 1.0
Clock Recovery	NA	Specified
Unit Interval	UI	Specified
Table continued...		

Parameter	Symbol	Release 1.0
Eye Height of Transition Bits	V_{TXA}	Specified
Eye Height of Nontransition Bits	V_{TXA_d}	Specified
Eye Width across any 250 UIs	T_{TXA}	Specified

ExpressCard-Host sys trans path

ExpressCard™ - Host system
transmitter path measurements

Parameter	Symbol	Release 1.0
Clock Recovery	NA	Specified
Unit Interval	UI	Specified
Eye Height of Transition Bits	V_{txS}	Specified
Eye Height of Nontransition Bits	V_{txS_d}	Specified
Eye Width across any 250 UIs	T_{TxS}	Specified

MXM measurements

PCI Express measurements ²

Parameter	Symbol	Release 1.1
Eye Height of Transition Bits	V_{TXS}	Specified
Eye Height of Nontransition Bits	V_{TXS_d}	Specified
Width at BER	T_{TXS}	Specified
Deterministic Jitter	DJ	Specified
Total Jitter	TJ	Specified

² All de-emphasis levels supported

Ordering information

PCE3³ PCI Express Gen 1/2/3 TekExpress Compliance/Debug Automation with DPOJet Measurements Software

New instrument orders	Option PCE3
Product upgrades	DPO-UP Option PCE3
Floating licenses	DPOFL-PCE3

PCE4⁴ PCI Express Gen 4 TekExpress Compliance/Debug Automation with DPOJet Measurements Software
Requires PCE3 option to support PCI Express Gen 1/2/3 TekExpress Compliance/Debug Automation with DPOJet Measurements Software
For CEM System/Host Test⁵

New instrument orders	Option PCE4
Product upgrades	DPO-UP Option PCE4
Floating licenses	DPOFL-PCE4

PCE5 TekExpress PCIe Tx Compliance Solution, supports PCIe Gen 5 (requires Opt. DJA)

New instrument orders	Option PCE5
Product upgrades	DPO-UP Option PCE5
Floating licenses	DPOFL-PCE5

PCE6 TekExpress PCIe Tx Compliance Solution, supports PCIe Gen 6 (requires Opt. DJA and PAMPCIE6)

New instrument orders	Option PCE6
Product upgrades	DPO-UP Option PCE6
Floating licenses	DPOFL-PCE6

SWX-PCE⁶ Switch configurator for PCIe Gen 1/2/3/4/5

New instrument orders	Option SWX-PCE
Floating licenses	DPOFL-SWX-PCE

Recommended DPO/MSO70000 Series Oscilloscopes

2.5 Gb/s (PCI Express 1.0/1.1) DPO/MSO70000 Series (6 GHz or higher bandwidth models required for compliance testing)

³ Requires Option DJA (DPOJET Jitter and Eye Diagram Analysis) and Option SDLA64 (serial Data Link Analysis Visualizer) highly recommended. Option DJA is standard on MSO70000 Series oscilloscopes, and can be ordered for DPO70000 Series oscilloscopes.

⁴ Require option PCE3. For Debug solution DJA and SDLA64 is required. If user need only Automated TekExpress solution then DJA and SDLA64 is optional

⁵ CEM System/Host Test Configuration

- 1 x MSO/DPO72504DX or DPO73304SX Oscilloscope with P76xx probe or DPS73308SX, min BW = 25GHz
- 2 x P7625 or P7633 probe required for MSO/DPO72504DX or DPO73304SX
- 2 x P76CA-292 probe tip required for MSO/DPO72504DX or DPO73304SX

⁶ Requires Option PCE3, 4 or 5

5.0 Gb/s (PCI Express 2.0)	DPO/MSO70000 Series (12.5 GHz or higher bandwidth models)
8.0 Gb/s (PCI Express 3.0)	DPO/MSO70000 Series (12.5 GHz or higher bandwidth models)
16.0 Gb/s (PCI Express 4.0)	DPO/MSO70000 Series (25 GHz or higher bandwidth models)
32.0 Gb/s (PCI Express 5.0)	DPS77004SX Series (50 GHz or higher bandwidth models), DPO/MSO70000 Series (33 GHz or higher bandwidth models for Gen 5 CEM testing)
64.0 Gb/s (PCI Express 6.0)	DPS77004SX Series (50 GHz or higher bandwidth models)

Support for DPO/MSO70000 SX Series oscilloscopes

Supported DPO70000 Series configurations

Model	Description	Option PCE3	Option PCE4	Option PCE5	Option PCE6
DPO72304DX	23 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	✓			
DPO71254DX	12.5 GHz DPO; 4 Ch, 12.5 GHz: 50GS/s or 2 Ch: 12.5 GHz: 100 GS/s	✓			
MSO71254DX	12.5 GHz MSO; 4 Ch, 12.5 GHz: 50GS/s or 2 Ch: 12.5 GHz: 100 GS/s	✓			
DPO71304SX	13 GHz DPO; 4 Ch, 13GHz: 50GS/s or 2 Ch: 13 GHz: 100 GS/s	✓			
MSO71604DX	16 GHz MSO; 4 Ch, 16 GHz: 50GS/s or 2 Ch: 16 GHz: 100 GS/s	✓			
DPO71604DX	16 GHz DPO; 4 Ch, 16GHz: 50GS/s or 2 Ch: 16 GHz: 100 GS/s	✓			
MSO72004DX	20 GHz MSO; 4 Ch, 20 GHz: 50GS/s or 2 Ch: 20 GHz: 100 GS/s	✓			
DPO72004DX	20 GHz DPO; 4 Ch, 20 GHz: 50GS/s or 2 Ch: 20 GHz: 100 GS/s	✓			
MSO72304DX	23 GHz MSO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	✓			
DPO72304DX	23 GHz DPO; 4 Ch, 23 GHz: 50GS/s or 2 Ch: 23 GHz: 100 GS/s	✓			
MSO72504DX	23 GHz MSO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	✓	✓		
DPO72504DX	25 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	✓	✓		
MSO73304DX	33 GHz MSO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	✓	✓	✓ ⁷	
DPO73304DX	33 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	✓	✓	✓ ⁷	
MSO71254DX	12.5 GHz MSO; 4 Ch, 12.5 GHz: 50GS/s or 2 Ch: 12.5 GHz: 100 GS/s	✓			
MSO71304SX	13 GHz DPO; 4 Ch, 13GHz: 50GS/s or 2 Ch: 13 GHz: 100 GS/s	✓			
DPO 72504DX	25 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	✓	✓		
MSO72304DX	23 GHz MSO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	✓			
MSO72504DX	23 GHz MSO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	✓	✓		
MSO73304DX	33 GHz MSO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s	✓	✓	✓	
DPO77002SX	70 GHz ATI; 1 Ch, 70 GHz, 200 GS/s or 2 Ch, 33 GHz, 100 GS/s	✓	✓	✓	

Table continued...

⁷ Except for the Base Gen5

Model	Description	Option PCE3	Option PCE4	Option PCE5	Option PCE6
DPS77004SX	70 GHz ATI System; 2 Ch: 70 GHz: 200 GS/s or 4 Ch: 33 GHz: 100 GS/s	✓	✓	✓	✓
DPO75902SX	59 GHz ATI; 1 Ch, 59 GHz, 200 GS/s or 2 Ch, 33 GHz, 100 GS/s	✓	✓	✓	
DPS75904SX	59 GHz ATI System; 2 Ch: 59 GHz: 200 GS/s or 4 Ch: 33 GHz: 100 GS/s	✓	✓	✓	✓
DPO75002SX	50 GHz ATI; 1 Ch, 50 GHz, 200 GS/s or 2 Ch, 33 GHz, 100 GS/s	✓	✓	✓	
DPS75004SX	50 GHz ATI System; 2 Ch: 50 GHz: 200 GS/s or 4 Ch: 33 GHz: 100 GS/s	✓	✓	✓	✓
DPO73304SX	33 GHz DPO; 2 Ch, 33 GHz, 100 GS/s or 4 Ch, 23 GHz, 50 GS/s	✓	✓	✓	
DPS73308SX	33 GHz DPO System; 4 Ch: 33 GHz: 100 GS/s or 4 Ch: 23 GHz: 50 GS/s	✓	✓	✓	
DPO72304SX	23 GHz DPO; 4 Ch: 23 GHz: 50 GS/s or 2 Ch: 23 GHz: 100 GS/s	✓			
DPO71604SX	16GHz DPO; 4 Ch: 16GHz: 50GS/s or 2 Ch: 16 GHz: 100 GS/s	✓			
DPO71304SX	13GHz DPO; 4 Ch: 13GHz: 50GS/s or 2 Ch: 13 GHz: 100 GS/s	✓			

Accessories

Recommended accessories

P75xx, P76xx, and P77xx Series
(TriMode™ Differential Probes)

P7513, P7513A, P7516, P7520A, P7625, P7630, P7633, P7713, P7716, P7720 with respective tips

PCI Express						
Speed	Minimum oscilloscope bandwidth	TCA-SMA (Max 18 GHz)	TCA-292D (Max 33 GHz)	P7500 (Max 20 GHz)	P7700 (Max 20 GHz)	P7600 (Max 33 GHz)
2.5 GT/s	6 GHz	✓	✓	✓	✓	✓
5.0 GT/s	12.5 GHz	✓	✓	✓	✓	✓
8.0 GT/s	12.5 GHz	✓	✓	✓	✓	✓
16.0 GT/s	25 GHz		✓			✓
32.0 GT/s BASE	50 GHz					
32.0 GT/s CEM	33 GHz		✓			✓
100 MHz RefClk	5 GHz	✓	✓	✓	✓	✓

Option SDLA64

Serial Data Link Analysis Visualizer ⁸

Option SR-PCle

Bus decode support for PCI Express serial busses ⁹

Option PAMPCIE6

Used for Gen 6 Base and CEM

⁸ SDLA is not required for TekExpress automation solutions. It is mandatory for DPOJET PCIE.

⁹ This is required to perform pattern decoding using TekExpress which gives Preset number and Lane number information (Only for Gen 3, currently Gen 4 is not supported).

Recommended for automated DUT control

RF Switch	Keithley System S46T RF Microwave Switch for X12 PCIe Gigatronics RF Switch 26 GHz (8902-L-48TS26) for x16 PCIe Mini Circuits ZTM/ZTM2 40GHz RF switch (Supports x4, x8, x16 configuration)
Tektronix AFG3252	Arbitrary Function Generator
Tektronix AFG3252C	Arbitrary Function Generator
AWG5002B/C	Arbitrary Waveform Generator
AWG5012B/C	Arbitrary Waveform Generator
AWG5014B/C	Arbitrary Waveform Generator
AWG7082B/C	Arbitrary Waveform Generator
AWG7122B/C	Arbitrary Function Generator
AWG70001A	Arbitrary Waveform Generator
AWG70002A	Arbitrary Waveform Generator
AFG31252	Arbitrary Function Generator
AFG31251	Arbitrary Function Generator
AFG3252C	Arbitrary Function Generator
GRL PCIe34 Controller for automatic test pattern toggling and DUT power cycle (for Add-In-Card)	Part number : GRL-PCI34-P1 Contact GRL at support@graniteriverlabs.com for support and quote@graniteriverlabs.com to request for a quote.

Recommended test fixtures, cables, and tools

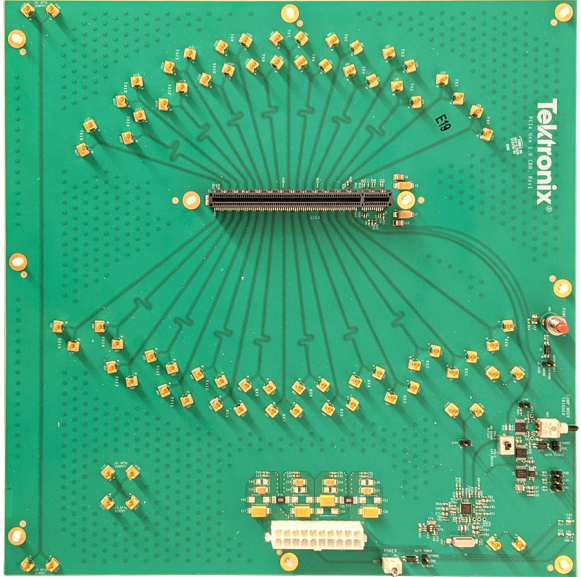
Description	Image
<p>Description PCI Express 5.0 System Board (Tektronix NON-COMPLIANCE)</p> <p>Tektronix PN PCI-SIG fixtures</p> <p>Specifications</p> <ul style="list-style-type: none"> • X16 CEM connector (surface mount) with optimized layout • Megtron 6 low loss material (~1 dB @ 16 GHz) • Microstrip routing (no vias) • MMPx (Huber Suhner) RF connectors for Tx and Rx connections • Tx trace length of 3 in. • Rx trace length of 4 in. • 5.0 Base Specification Reference Clock compliance chip • Power connector (2x10) • Opto-isolator switch for automation of Power, Reset, and Toggle • Insertion loss characterization traces 	

Table continued...

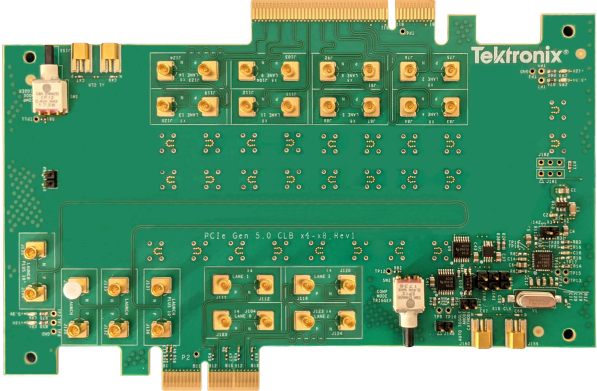
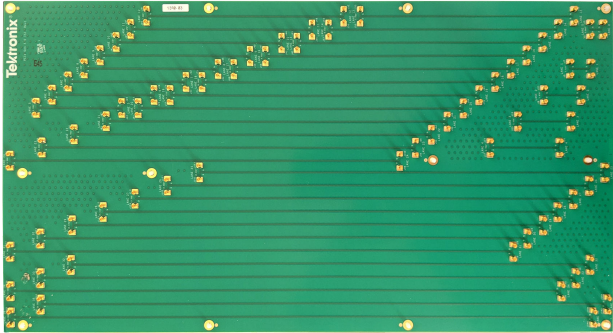
Description	Image
<p>Description PCI Express 5.0 Add-in Card Board (Tektronix NON-COMPLIANCE)</p> <p>Tektronix PN PCI-SIG fixtures</p> <p>Specifications</p> <ul style="list-style-type: none"> • x1/x16 Edge Finger and x4/x8 Edge Finger variants with optimized layout • TF-PCIE5-CEM-X1 comes with X1 and X16 CLB and TF-PCIE5-CEM-X16 comes with X1, X4, X8 and X16 CLB. • Sideband signal RC terminations • Megtron 6 Low Loss Material (~1 dB @ 16 GHz) • Microstrip routing (no vias) • MMPx (Huber Suhner) RF onconnectors for Tx and Rx connections • Tx trace length of 3 in. • Rx trace length of 4 in. • 5.0 Base Specification Reference Clock compliance chip • Compliance toggle circuit (switch between Tx compliance patterns) • Opto-isolator switch for automation of Power, Reset, and Toggle • Insertion loss characterization traces 	
<p>Description PCI Express 5.0 Variable ISI Board (Tektronix NON-COMPLIANCE)</p> <p>Tektronix PN PCI-SIG fixtures</p> <p>Specifications</p> <ul style="list-style-type: none"> • 36 variable length differential pairs (0.5 dB @ 16 GHz step size) • Megtron 6 Low Loss Material (~1 dB @ 16 GHz) • Microstrip routing (no vias) • MMPx (Huber Suhner) RF connectors for Tx and Rx connections 	
<p>Description: [PCI-SIG] PCIe 4.0 CEM Fixture Kit</p> <p>PN: PCIe-CLB-X1X16, PCIe-CLB-X4X8, PCIe-CBB-MAIN, and PCIe-VAR-ISI</p> <p>The PCIe 4.0 CEM Beta fixtures require a VNA based characterization to determine the appropriate Insertion Loss for performing the 16 GT/s Tx Signal Quality Test and the 16 GT/s Rx Link Equalization Test. This characterization will not be performed by the PCI-SIG, but must be performed by the end user after the fixtures are delivered.</p> <p>Quantity: 1</p>	

Table continued...


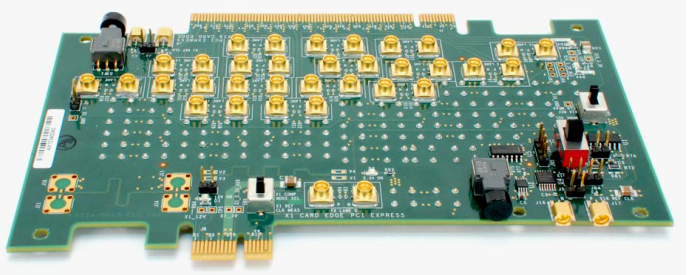

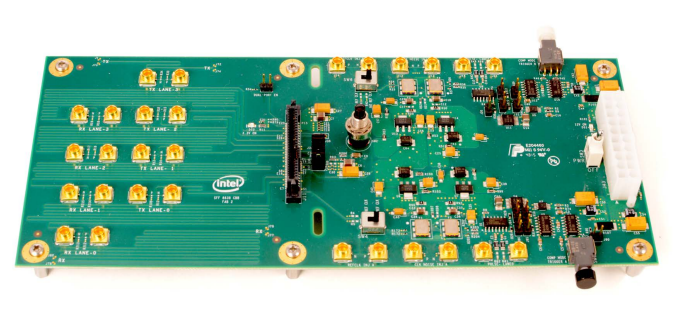
Description	Image
<p>Description: PCI Express Compliance Base Board (CBB) test fixture, revision 3.0. For testing PCI Express add-in cards, x1/x4/x8/x16 PCIe connectors on PCIe devices/add-in cards.</p> <p>Vendor: PCI-SIG www.pcisig.com/specifications/order_form</p> <p>Vendor PN: CBB3</p> <p>Tektronix PN: Only available from PCI-SIG</p> <p>Quantity: 1</p>	
<p>Description: PCI Express Compliance Load Board (CLB3) test fixture, revision 3.0. For testing PCI Express Platforms, x1 and x16 PCIe connectors on PCIe systems/mother boards.</p> <p>Vendor: PCI-SIG www.pcisig.com/specifications/order_form</p> <p>Vendor PN: x1/x16 CLB3</p> <p>Tektronix PN: Only available from PCI-SIG</p> <p>Quantity: 1</p>	
<p>Description: PCI Express Compliance Load Board (CLB3), Revision 3.0. For testing PCI Express Platforms, x4 and x8 PCIe connectors on PCIe systems/mother boards.</p> <p>Vendor: PCI-SIG www.pcisig.com/specifications/order_form</p> <p>Vendor PN: x4/x8 CLB3</p> <p>Tektronix PN: Only available from PCI-SIG</p> <p>Quantity: 1</p>	
<p>Description: PCI Express Compliance Load Board (U.2 CLB3) test fixture, revision 3.0. For testing PCI Express Platforms, x1 and x4 PCIe connectors on PCIe devices/add-in cards.</p> <p>Vendor: PCI-SIG www.pcisig.com/specifications/order_form</p> <p>Vendor PN: U.2 CLB3</p> <p>Tektronix PN: Only available from PCI-SIG</p> <p>Quantity: 1</p> <p>Note: U.2 was formally known as SFF-8639.</p>	

Table continued...

Description	Image
<p>Description: PCI Express Compliance Load Board (U.2 CLB3), Revision 3.0. For testing PCI Express Platforms, x1 and x4 PCIe connectors on PCIe systems/ mother boards.</p> <p>Vendor: PCI-SIG www.pcisig.com/specifications/order_form</p> <p>Vendor PN: U.2 CLB3</p> <p>Tektronix PN: Only available from PCI-SIG</p> <p>Quantity: 1</p> <p>Note: U.2 was formally known as SFF-8639.</p>	
<p>Description: Any ATX PC power supply</p> <p>Vendor: Tektronix recommends "PC Power and Cooling 750 W Silencer MK III Series" or similar.</p> <p>Quantity: 1</p>	
<p>Description: SMP terminator, 50 Ω, limited detent.</p> <p>Vendor: Fairview Microwave www.fairviewmicrowave.com/rf-load-0.25-watts-26.5-ghz-smp-female-st2645-p.aspx</p> <p>Vendor PN: ST2645</p> <p>Tektronix PN: 131-9399-xx</p> <p>Quantity needed per PCIe DUT link width:</p> <ul style="list-style-type: none"> • x1: 0 • x4: 6 • x8: 14 • x16: 30 	
<p>Description: SMA Female to BNC Male adapter.</p> <p>Vendor: Tektronix</p> <p>Tektronix PN: 015-0572-xx www.tek.com</p> <p>Quantity: 2</p>	
Table continued...	

Description	Image
<p>Description: DC Block, SMA, 26 GHz</p> <p>Vendor: Tektronix www.tek.com</p> <p>Tektronix PN: PSPL5500A, PSPL5501A, or PSPL5508</p> <p>Quantity: 2</p> <p>Note: This is an optional accessory and not shown in any of connection diagrams, but can be used if DC offset is encountered in any signal path.</p>	
<p>Description: USB2.0 Cable, Type A Male to Type B Male, 6 foot</p> <p>Vendor: Tektronix www.tek.com</p> <p>Tektronix PN: 174-6053-xx</p> <p>Quantity: 1</p>	
<p>Description: SMA-to-SMA, H+S SF104E Phase Kit (#84077556), Straight, 1' m, 1.5 ps phase-matched.</p> <p>Vendor: Tektronix www.tek.com</p> <p>Tektronix PN: PMCABLE1M</p> <p>Quantity: 1 cable pair per lane</p>	
<p>Description: SMA-to-SMP right-angle cable pair, 102 mm, 1 ps phase-matched.</p> <p>Tektronix PN: 174-6657-xx</p> <p>Quantity: 1 cable pair</p> <p>Note: Applicable only for Gen 3</p>	
<p>Description: SMA-to-SMP right-angle cable pair, 1 m, 1 ps phase-matched (one for AFG to Rx Lane0, one for 100 MHz RefClk for Ch3+4 for System Testing)</p> <p>Tektronix PN: 174-6659-xx</p> <p>Quantity: 1 cable pair</p>	

Table continued...




Description	Image
<p>Description: SMP to SMP right-angle cable pair, 305 mm, 2.5 ps phase-matched set.</p> <p>Tektronix PN: 174-6658-xx</p> <p>Quantity: 1 cable pair</p>	
<p>Description Cables</p> <p>Tektronix PN TF-PCIE5-CEM-X1 or TF-PCIE5-CEM-X16</p> <p>Specifications</p> <ul style="list-style-type: none"> Huber Suhner 24" MMPX PLUG to MMPX PLUG cable PN 174-7327-00 QTY = 4 Huber Suhner 4" MMPX – 2.92 Cable 32024E-29430CR-29092KCR-24PM +/-1 PS-STD PN 174-7326-00 QTY = 4 	
<p>Description: SMA torque wrench, 8.0 in-lbs.</p> <p>Vendor: Fairview Microwave</p> <p>www.fairviewmicrowave.com/sma-fixed-torque-wrench-click-st-sma3-p.aspx</p> <p>Vendor PN: ST-SMA3</p> <p>Tektronix PN: 003-1940-xx</p> <p>Quantity: 1</p>	
<p>Description: SMP right-angle cable extraction tool.</p> <p>Vendor: Fairview Microwave</p> <p>www.fairviewmicrowave.com/undefined-mmtl2682-p.aspx</p> <p>Vendor PN: MMTL2682</p> <p>Tektronix PN: 003-1941-xx</p> <p>Quantity: 1</p>	

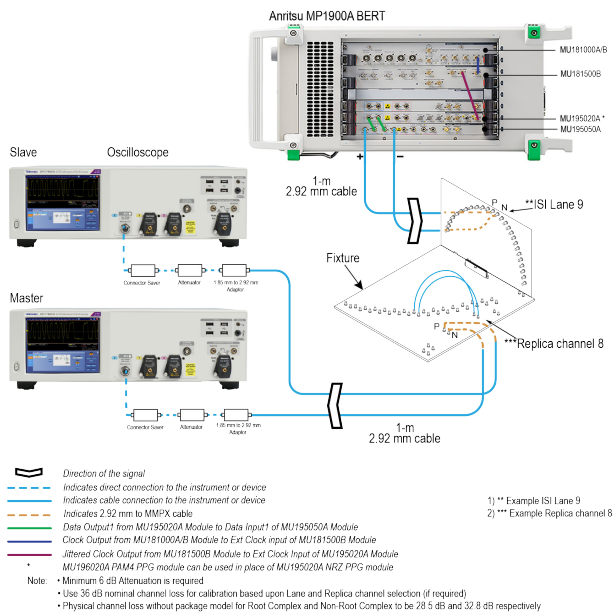
Table continued...

Description	Image
<p>Description: SMP terminator installation/extraction tool.</p> <p>Vendor: Fairview Microwave</p> <p>www.fairviewmicrowave.com/undefined-mm14991-p.aspx</p> <p>Vendor PN: MMTL4991</p> <p>Tektronix PN: 003-1939-xx</p> <p>Quantity: 1</p>	

Additional information

PCI Express receiver testing

Tektronix also offers a complete PCI Express receiver testing solution for Gen 6, Gen 5, and Gen 4 that includes stressed pattern generation as required by PCI-SIG test specifications and support for automated calibration and receiver tests. Automated DUT loopback control simplifies the testing process and reduces the time to test results.



PCIe receiver test setup

Salient features of the Receiver automation software with Tektronix DPO70000SX Series Real-Time Scopes and Anritsu MP1900A BERT are as follows:

- Wizard-based user interface for each step of calibration and test
- Efficient and quick calibration
- Insertion Loss computation powered by Seasim Statistical Simulation Tool
- Tx Link Equalization/Rx Link Equalization
- Jitter Tolerance
- Latest industry tool support (SigTest and Seasim)
- Comprehensive Calibration and test reports
- Automation for PCI Express PLL Bandwidth and Peaking tests (including SJ calibration) for Gen 3/4/5/6



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For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit www.tek.com.

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