Tektronix PCI Express

TekRxTest Suite Datasheet

Calibrate and test PCI Express (PCIe) Receiver (Rx) with confidence. Built for PCIe 7.0 Base at 128 GT/s PAM4, Rx testing should not be the bottleneck standing between your design and shipment. Tektronix TekRxTest automated receiver test software simplifies the most challenging aspects of PCIe validation including stressed-eye TP2/TP3 calibration, Link Equalization (LEQ), and Jitter Tolerance (JTOL) testing for PCIe 6.0 (Base and CEM).

A wizard-guided interface reduces the manual setup complexity that can turn receiver calibration into a multi-day task by cutting setup time dramatically while keeping every parameter within your control when you need to fine-tune for a specific product test cycle. Test flows are continuously updated to align with the latest PCI-SIG specification revisions and ECNs, helping keep your validation environment current with evolving standards.

Beyond compliance validation, TekRxTest scales to validation and debug, providing a single platform for First List submission, early silicon characterization, and channel troubleshooting. The result is a faster path to market and greater confidence that every product meets specification requirements before shipment.

Applications

- Supports latest PCIe 7.0 Base Specification and PCIe 6.0 BASE and CEM Specification testing, and prior generations
- Supports all PCIe data rates: 128 GT/s, 64 GT/s, 32 GT/s, 16 GT/s, 8 GT/s, 5 GT/s and 2.5 GT/s
- Root Complex and Non-Root Complex silicon
- Systems (motherboards and servers), Add-in Cards, Switches, Bridges, and Extension Devices (retimers and redrivers)

Features and benefits

General

- Receiver automation software for Tektronix 7 Series DPO and DPO70000SX Series Real Time Oscilloscopes and Anritsu MP1900A BERT
- Wizard-based user interface for each step of calibration and test
- Pop-up user tips to simplify decision making
- Latest industry tool support (SigTest and Seasim)
- Calibration and test reports

PCIe Gen 7.0 (128 GT/s)

- Base Specification
- TP3: AC/DC Balance, Amplitude, Tx Equalization, Sinusoidal Jitter tones, Random Jitter, and Multi-tone SJ
- TP2: Preset and CTLE Selection, Stressed Eye, DMI, and CMI
- Automated Oscilloscope Noise Compensation for SJ and RJ calibration
- Insertion Loss computation powered by Seasim Statistical Simulation Tool

PCIe 6.0 (64 GT/s), 5.0 (32 GT/s), 4.0 (16 GT/s), 3.0 (8 GT/s)

- Base and CEM
- TP3: AC/DC Balance, Amplitude, Tx Equalization, Sinusoidal Jitter tones, and Random Jitter
- TP2: DMI, CMI, Preset and CTLE Selection, Stressed Eye
- TP1: AC/DC Balance, Amplitude, Tx Equalization, Sinusoidal Jitter tones, and Random Jitter
- Automated Oscilloscope Noise Compensation for SJ and RJ calibration
- Automated loopback through Configuration and Recovery
- Insertion Loss computation powered by Seasim Statistical Simulation Tool
- Rx Link Equalization Test
- Tx Link Equalization Test
- Jitter Tolerance Test
- Advanced debug mode for troubleshooting

PCIe 2.0 (5 GT/s) and PCIe 1.0 (2.5 GT/s)

- TP1 Calibration: Amplitude, De-emphasis, RJ, SJ, SSC Residual, and Multi-tone
- TP2 Calibration: CMI, and Stressed eye calibration
- Jitter Tolerance Test

Add-in Card PLL Bandwidth Test

- Add-in Card PLL Bandwidth and Peaking test automation software for Tektronix DPO70000SX ATI Performance Oscilloscopes and Anritsu MP1900A BERT
- Supports PCIe 3.0, 4.0, 5.0, and 6.0 PLL testing
- Supports Anritsu SI PPG (NRZ) and PAM4 PPG
- Streamlined UI/UX as Receiver test suite
- Supports testing with compliance pattern with any Tx Preset (P0 - P10, or Q0 - Q10 for 64 GT/s) and toggle patterns
- Software CTLE improves accuracy for high loss back channel

Stressed eye calibration

Stressed-eye calibration is often the most time-consuming step and one of the most difficult to correlate across different test benches. TekRxTest automates PCIe 7.0 Base receiver calibration and PCIe 6.0 BASE and CEM receiver testing, orchestrating the BERT, oscilloscope, and channel within a single guided workflow.

The wizard-based interface eliminates much of the manual setup that can turn receiver calibration into a multi-day task, while still providing access to advanced controls. Every stress parameter remains available when you need to customize a test beyond the standard compliance profile for a specific product validation cycle.

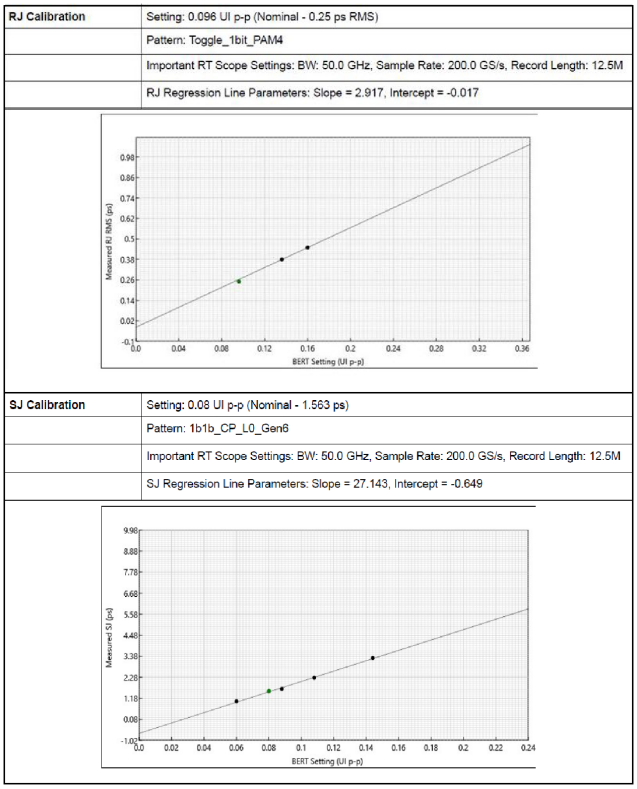
Test workflows are continuously refined and updated to align with the latest PCI-SIG specification revisions and ECNs, helping ensure that your test environment remains aligned with evolving standards.

TP3 calibration

The TP3 (test point at the end of cable from BERT PPG to oscilloscope) calibration is mandatory for all devices to ensure tolerances are met at the defined reference plane. The Tektronix PCIe Rx Test Suite wizard will guide you through all the necessary steps to ensure the pre-channel signal matches the specification requirements to ensure future calibration steps are completed with ease.

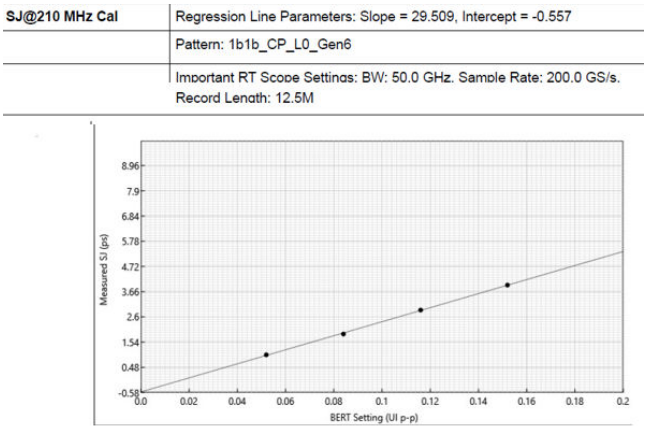
PCIe Gen 7.0 (128 GT/s), Gen 6.0 (64 GT/s) and Gen 5.0 (32 GT/s)

1. AC-DC balance: Small amounts of Tx EQ de-emphasis are enabled to balance low and high-frequency sections of the pattern at a common reference plane.
2. Amplitude: The differential voltage swing is required to be within 720 – 800 mV.
3. Tx Equalization Presets: Calibration of pre-shoot 1, pre-shoot 2 (Gen 6.0 only), and de-emphasis is required to ensure true preset levels are used for testing receivers.
4. IL measurement: Channel insertion loss is calculated using Seasim between TP1 and TP3 (loss before the TP3 reference is computed here for later removal).
5. Random Jitter (RJ): RJ is calibrated to be 0.125 ps [Gen 7.0], 0.25 ps [Gen 6.0], 0.5 ps [Gen 5.0] (RMS value) nominally.
6. Sinusoidal Jitter (SJ): SJ is calibrated to be 0.05 UI at 100 MHz frequency i.e. 0.75 ps for Gen 7.0, 1.5625 ps for Gen 6.0 and 3.125 ps for Gen 5.0.



RJ and SJ calibration for Gen 6.0

7. SJ@210 MHz: This calibration is required for JTOL measurements with some calibrations.



SJ@210 MHz calibration for Gen 6.0

8. Multi-tone SJ: For JTOL measurements where up to maximum 14 frequencies are used, calibration for frequencies other than 100 MHz is required to be performed.

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PCIe7.0 Base Receiver Calibration Report

TP3 Calibration Results

Details	
Unique ID	TP1-13072026
Date/Time	12 July 2026, 23.19
Generated By	Unknown

Additional Comments
No Comments

Test Equipment	
BERT	ANRITSU, MP1900A, 6262199252
BERT FW Version	12.01.01
Rx Test SW Version	6.7.2.8
Analysis SW Version	PAMJET Version 10.11.1.60, Seasim Version 2.0.104e
RT Scope	TEKTRONIX, DPO77002SX, B321505
RT Scope FW Version	10.15.0 Build 3
TekRxService Version	3.1.0.12
DPOJET Version	10.6.3.44

Result Summary	
TP3 Calibration	Unique ID: TP1-13072026
	Balanced De-emphasis: -1.92 dB
	Differential Amplitude: 800.0 mV / Single - Ended Amplitude setting: 688 mV
	SJ Setting: 0.056 UI p-p @ 100 MHz (Nominal SJ 0.75 ps / 0.048 UI p-p)
	RJ Setting: 0.184 UI p-p (Nominal RJ 0.13 ps RMS / 0.113 UI p-p)
	SJ@210 MHz Regression Line Parameters: Slope = 9.756, Intercept = -0.078
	Multi-tone SJ Calibration performed for 5 frequencies

TP3 Calibration Details	
PWJ Calibration	Procedure Type: Measured
	PWJ RJ: 0.116 ps RMS
	PWJ DJ: 0.277 ps
AC-DC Balance	Setting De-emphasis: -1.92 dB
	Pattern: 64ones_64zeros_128bit10_PAM4

Sample calibration report

Automatic characterization and precise calibration of presets, RJ, and SJ along with the important parameters used for calibration like pattern type, oscilloscope, BERT settings, regression line slopes, and intercept for reference.

TP2 calibration

The TP2 (end of channel) calibration is a complex process requiring a deep understanding of the BERT, Real Time Oscilloscope, post-processing tools, and the PCIe specifications. The Tektronix PCIe Rx Test Suite will remove the complexity and ensure the desired results are achieved through user-friendly automation. The time required to complete TP2 calibration is critical, so efficient techniques have been implemented to ensure an accurate stressed eye is achieved within a reasonable time scale. From calibration of DMI (Differential Mode Interference modeling crosstalk) to the fine granularity adjustments to SJ and DMI necessary to find the stressed eye solutions space, our automation software will guide you through this otherwise daunting task.

PCIe Gen 7.0 (128 GT/s), Gen 6.0 (64 GT/s), Gen 5.0 (32 GT/s), Gen 4.0 (16 GT/s), and Gen 3.0 (8 GT/s)

1. DMI: The differential mode interference is required to be calibrated within 0-15 mV (p-p) [Gen 7.0] / 5-25 mV (p-p) [Gen 6.0] / 5-30 mV (p-p) [Gen 5.0] / 10-25 mV (p-p) [Gen 4.0] / 10-100 mV(p-p) [Gen 3.0] by capturing the 2.1 GHz. sinusoidal output for a duration of 40 ns
2. CMI: The common-mode interference is required to be calibrated for a nominal voltage of 75 mV (p-p) [Gen 7.0 and Gen 6.0] / 150 mV (p-p) [Gen 5.0 and Gen 4.0] by capturing the 120 MHz sinusoidal output for a duration of 62.5 us.
3. Channel insertion loss for DMI/CMI and eye diagram measurements computed with Seasim (TP1 to TP2/TP2P for 16 GT/s and TP3 to TP2/TP2P for 32 GT/s, 64 GT/s and 128 GT/s).
4. Channel selection based on optimal Tx EQ Preset and Rx CTLE: Base Specification compliant for Eye Area criteria.
5. Stressed Eye calibration: Fine-tuning of the eye using amplitude, SJ (RJ in case of Gen 3.0), and DMI is utilized to place the stressed eye within allowed tolerances. Automated TP2 calibration plots and stressed eye calibration details along with other important parameters like pattern type, oscilloscope and BERT settings, and regression line slopes and intercept for reference.

Tektronix

PCIe7.0 Base Receiver Calibration Report

Non-Root Complex TP2 Calibration Results

Details	
Unique ID	LFPR
Date/Time	02 July 2026, 12.19
Generated By	Unknown

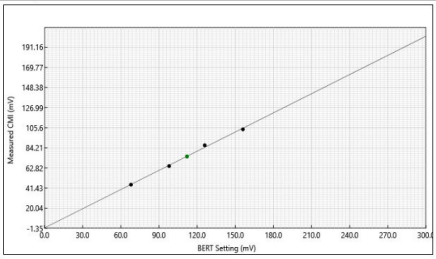
Additional Comments
No Comments

Test Equipment	
BERT	ANRITSU, MP1900A, 6262199252
BERT FW Version	12.01.01
Rx Test SW Version	6.7.1.34
Analysis SW Version	Sigtest Version 6.1.13, Seasim Version 2.0.104d
RT Scope	TEKTRONIX, DPO77002SX, B321505
RT Scope FW Version	10.15.0 Build 3
TekRxService Version	3.1.0.11
DPOJET Version	10.6.3.44

Calibration Summary	
TP2 Calibration	Unique ID: LFPR
	Full Channel Loss: Not Run
	Selected Preset: Q5
	Selected CTLE: 0.0 dB
	ISI Pair: Not Available
	Status: Not Converged
	Final Calibrated EW: 1.7 ps (1.4125 ps ≤ Target EW ≤ 1.7125 ps)
	Final Calibrated EH: 9.0 mV (9.5 mV ≤ Target EH ≤ 10.5 mV)
	Final SJ Stress Level: 1.05 ps / 0.044 UI p-p BERT Setting (0 ps ≤ SJ Sweep ≤ 1.5 ps)
	Final Amplitude Level: 800.0 mV (Differential) / 696 mV (Single-Ended) BERT Setting
	Final DMI Stress Level: 0 / 0 BERT Setting (0 mV ≤ DMI Sweep ≤ 15 mV)
	SJ@210 MHz Setting during JTOL test: 0.036 UI p-p (Calibrated Value of SJ (ps) required to achieve the target stressed eye width minus 0.75 ps)
	Final CMI Stress Level: 75.0 mV / 102 mV BERT Setting

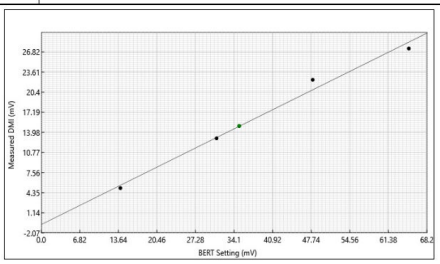
Root complex TP2 calibration sample report

CMI	Setting: 112 mV (Nominal - 75.0 mV)
	Pattern: Electrical_Idle
	Important RT Scope Settings: BW: 33.0 GHz, Sample Rate: 200.0 GS/s, Record Length: 12.5M
	Regression Line Parameters: Slope = 0.68, Intercept = -1.007



AIC CMI calibration result

DMI	Setting: 35 mV @ 2.1 GHz (Nominal - 15.0 mV)
	Pattern: Electrical_Idle
	Important RT Scope Settings: BW: 33.0 GHz, Sample Rate: 200.0 GS/s, Record Length: 8K
	Regression Line Parameters: Slope = 0.448, Intercept = -0.734



AIC DMI calibration result

Stressed Eye Calibration	Final SJ Stress Level: 1.563 ps
	Final DMI Stress Level: 11.0 mV
	Final Amplitude Level: 800.0 mV
	Pattern: Toggle_512bits_PAM4

Index	SJ (ps)	DMI (mV)	Amp (mV)	Eye Width (ps)	Eye Height (mV)
1	1.563	15	800	2.656	4.48
2	1.563	15	800	2.5	4.312
3	1.563	15	800	2.656	4.746
4	1.563	15	800	2.5	3.73
5	1.563	15	800	2.656	4.473
6	1.563	15	800	2.812	4.472
7	1.563	15	800	2.344	4.073
8	1.563	15	800	2.656	4.743
AVERAGE	1.563	15	800	2.598	4.379
9	1.563	13	800	2.969	5.084
10	1.563	13	800	2.812	4.914
11	1.563	13	800	2.969	5.35
12	1.563	13	800	2.656	4.293
13	1.563	13	800	2.969	5.075
14	1.563	13	800	3.281	5.083
15	1.563	13	800	2.656	4.671
16	1.563	13	800	2.969	5.347
AVERAGE	1.563	13	800	2.91	4.977
17	1.563	11	800	3.281	5.677
18	1.563	11	800	3.125	5.505
19	1.563	11	800	3.281	5.944
20	1.563	11	800	2.969	4.898
21	1.563	11	800	3.281	5.708
22	1.563	11	800	3.438	5.685
23	1.563	11	800	2.969	5.259
24	1.563	11	800	3.281	5.939
AVERAGE	1.563	11	800	3.203	5.577
SELECTED	1.563	11	800	3.203	5.577

Stressed eye calibration result

6. Stressed eye calibration supported using Sigtest (Gen 3.0/Gen 4.0/ Gen 5.0) and Seasim (Gen 5.0/Gen 6.0/Gen 7.0).
7. Eye height
   - 10 ± 0.5 mV @ BER E-6 [Gen 7.0]
   - 6 ± 0.5 mV @ BER E-6 [Gen 6.0]
   - 15 ± 1.5 mV @ BER E-12 [Gen 5.0 and Gen 4.0]
   - 47.5 ± 2.5 mV @ BER E-12 [Gen 3.0 System]
   - 43.5 ± 2.5 mV @ BER E-12 [Gen 3.0 AIC]
8. Eye Width
   - 1.5625 ± 0.15 ps @ BER E-6 [Gen 7.0]
   - 3.125 ± 0.3 ps @ BER E-6 [Gen 6.0]
   - 9.375 ± 0.5 ps @ BER E-12 [Gen 5.0]
   - 18.75 ± 0.5 ps @ BER E-12 [Gen 4.0]
   - 44 ± 1 ps @ BER E-12 [Gen 3.0 System]
   - 40.25 ± 1 ps @ BER E-12 [Gen 3.0 AIC]

PCIe Gen 2.0 (5 GT/s) and Gen 1.0 (2.5 GT/s)

The TP2 calibration panel allows you to manually perform calibration for the equipment and save the results. TP2 Calibration is carried out for CMI, and Stressed Eye. This procedure sets SJ, and Amplitude levels to achieve target eye opening. You must perform TP1 calibration before you start performing the calibration for TP2.

The PCIe 2.0 & PCIe 1.0 (BASE / CEM) TekRx test application calibrates the following at TP2:

1. CMI: It is needed to be configured in the settings panel. CMI is only applicable when the user is running Base calibration and test.
2. Stressed Eye calibration: As per the specification, various signal parameters and stress levels are computed to generate a signal that meets the Stressed Eye targets.

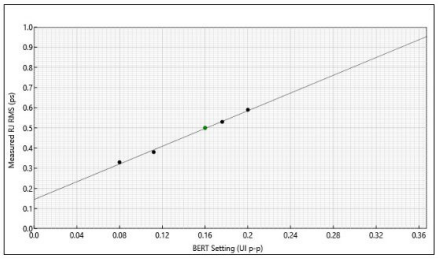
TP1 calibration

PCIe Gen 4.0 (16 GT/s) and Gen 3.0 (8 GT/s)

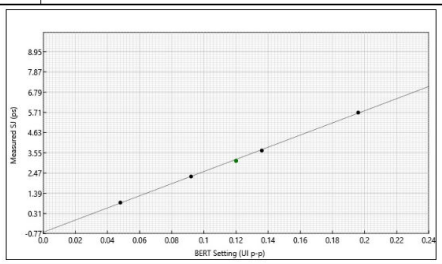
The TP1 (point after cable from BERT PPG to oscilloscope) calibration is mandatory for all devices to ensure tolerances are met at the defined reference plane. The Tektronix PCIe Receiver Test Suite wizard guides users through all the necessary steps to ensure that the pre-channel signal conforms to specification requirements, enabling subsequent calibration steps to be completed efficiently.

1. AC-DC balance: Small amounts of Tx EQ de-emphasis are enabled to balance low and high-frequency sections of the pattern at a common reference plane.
2. Amplitude: The differential voltage swing is required to be within 720 – 800 mV.
3. Tx Equalization Presets: Calibration of pre-shoot and de-emphasis is required to ensure true preset levels are used for testing receivers.
4. Random Jitter (RJ): RJ is calibrated to be 1 ps (RMS) for Gen 4.0 and 1.5 ps (RMS) for Gen 3.0 nominally.

RJ Calibration	Setting: 0.16 UI p-p (Nominal - 0.5 ps RMS)
	Pattern: Toggle_1bit
	Important RT Scope Settings: BW: 50.0 GHz, Sample Rate: 200.0 GS/s, Record Length: 12.5M
	RJ Regression Line Parameters: Slope = 2.2, Intercept = 0.145



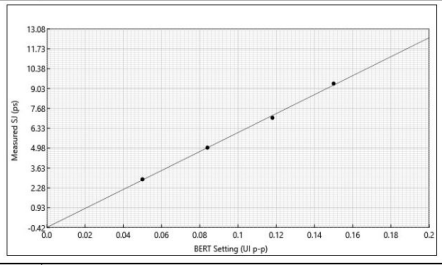
SJ Calibration	Setting: 0.12 UI p-p (Nominal - 3.125 ps)
	Pattern: 128b130b_CP_L0_Gen5_P7
	Important RT Scope Settings: BW: 50.0 GHz, Sample Rate: 200.0 GS/s, Record Length: 12.5M
	SJ Regression Line Parameters: Slope = 32.433, Intercept = -0.687



RJ and SJ calibration for Gen 4.0

5. Sinusoidal Jitter (SJ): SJ is calibrated over the required range of 5-10 ps (p-p) including the nominal SJ specification of 0.1 UI (or 6.25 ps for Gen 4.0 and 12.5 ps for Gen 3.0) at 100 MHz frequency.
6. SJ@210 MHz: This calibration is required for JTOL measurements with some calibrations (only for Gen 4.0).

SJ@210 MHz Cal	Regression Line Parameters: Slope = 64.404, Intercept = -0.4
	Pattern: 128b130b_CP_L0_Gen4_P7
	Important RT Scope Settings: BW: 25.0 GHz, Sample Rate: 100.0 GS/s, Record Length: 12500000



SJ@210 MHz calibration for Gen 4.0

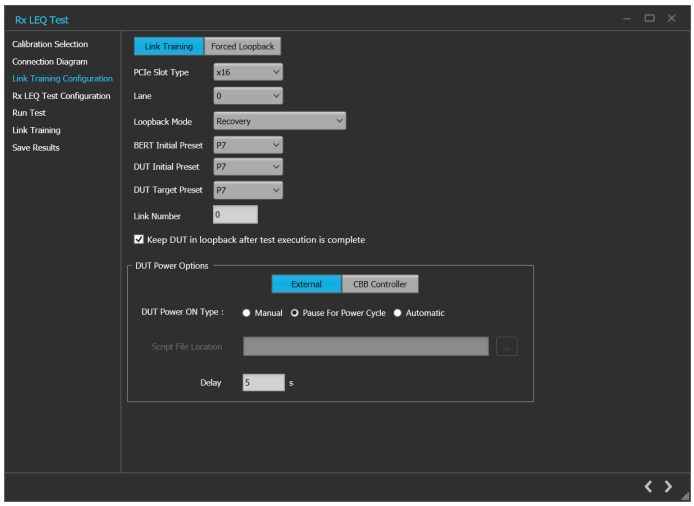
7. Multi-tone SJ: For JTOL measurements where up to maximum of 14 frequencies are used, calibration for frequencies other than 100 MHz is required to be performed.

PCIe Gen 2.0 (5 GT/s) and Gen 1.0 (2.5 GT/s)

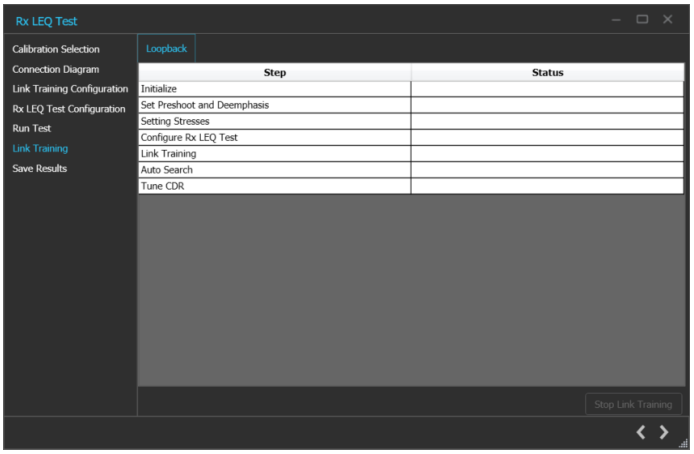
1. Amplitude: The differential voltage swing is required to be within 720 - 800 mV. This is done only after the transition and non-transition bit levels are made equal using de-emphasis.
2. De-emphasis: For PCIe 1.0, the calibration of de-emphasis value -3.5 dB is required. For PCIe 2.0, The calibration of de-emphasis value -3.5 dB is required.
3. RJ: It is calibrated to be 3.4 ps RMS for 2.5 GT/s.
4. SJ: For PCIe 1.0, the SJ is calibrated over the desired value of 150 ps for 2.5 GT/s. For PCIe 2.0, The SJ is calibrated over the desired value of 75 ps for 5 GT/s.
5. SSC Residual: 33 KHz SSC residual for common clock is required for 5 GT/s. This is applicable only for PCIe 2.0.
6. Multi-tone: It is calibrated over a specific range for multiple user-defined frequencies.

Link training

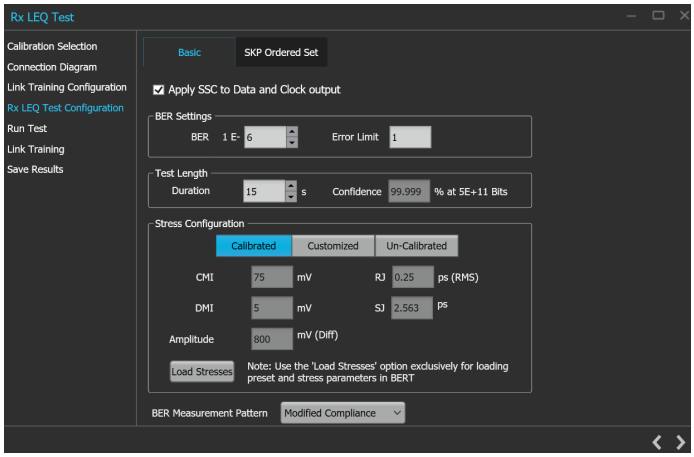
Prior to receiver testing, the Device-Under-Test (DUT) must be placed into loopback, where the signal digitized at the Rx latch is re-transmitted by the corresponding Tx giving visibility into a possible bit or burst errors. Entering the loopback test mode requires a complex dance through the Link Training Status State Machine (LTSSM) between the BERT and DUT. The Tektronix PCIe Receiver Test Suite automates this sequence allowing loopback through configuration (short path) and loopback through recovery (full training of the link Tx and Rx) for different levels of receiver testing. Relevant parameters are exposed to allow user control over this process without unnecessary complexity.



Link training configuration



Flexible link training and loopback control



Rx LEQ test configuration

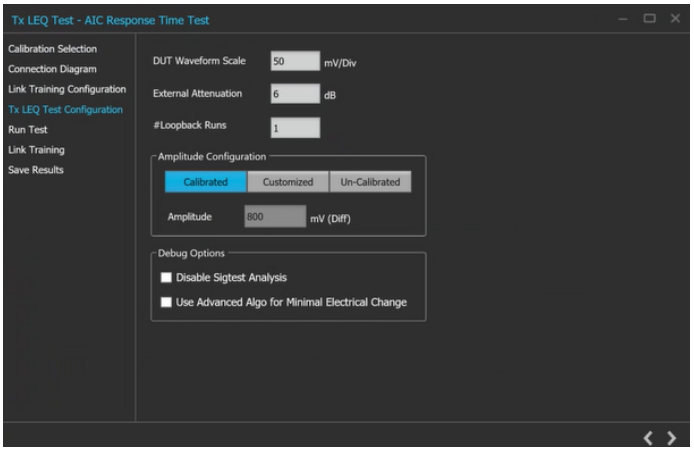
Receiver and transmitter link equalization testing

PCIe compliance at 128 GT/s, 64 GT/s, 32 GT/s, 16 GT/s, and 8 GT/s requires performing a Receiver Link Equalization test (checking analog Rx performance with a stressed signal after full link training) and a Transmitter Link Equalization test (ensuring key digital timing limits are achieved when an Rx makes Tx change requests to its link partner).

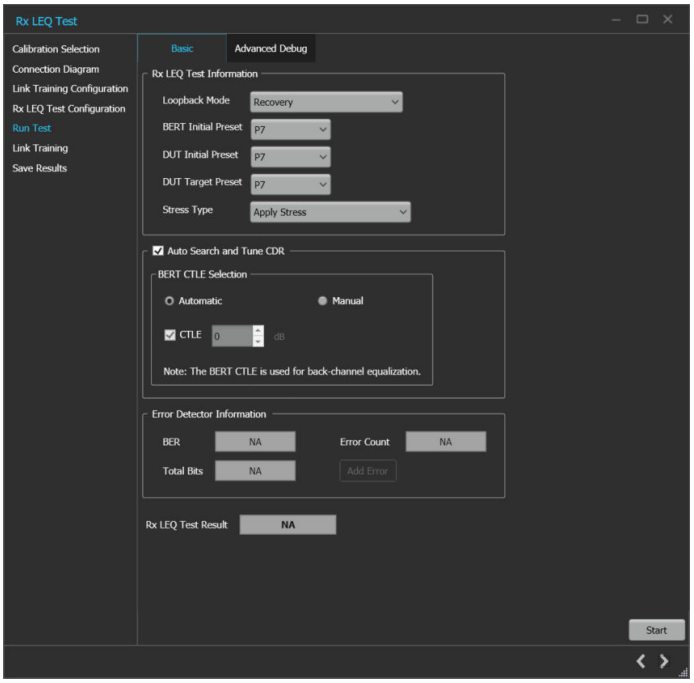
The Tektronix PCIe Receiver Test Suite controls the BERT and Real Time Oscilloscope during these required tests to provide efficient test results with minimal overhead and control only where needed.

The advanced debug mode provides additional troubleshooting capability for LEQ tests, allowing customized stressors, Tx presets, custom patterns, auto-search CTLE, and CDR tuning.

Tx LEQ - Run Test



Tx LEQ test configuration



Rx LEQ- Run Test

Tektronix

PCIe6.0 CEM Receiver Test Report

AIC LEQ Response Time Test Results

Details	
Unique ID	Demo
Date/Time	14 October 2024, 4:24 PM
Generated By	TEK

Additional Comments
Q0,Q1,Q2,Q3,Q5

Test Equipment	
BERT	ANRITSU, MP1900A, 6272608792
BERT FW Version	10.03.04
Rx Test SW Version	6.4.3.19
Analysis SW Version	Sigtest Version 6.1.06
RT Scope	TEKTRONIX, DPO77002SX, B321740
RT Scope FW Version	10.14.0 Build 15

TP3 Calibration Summary	
Unique ID	TP3Cal_13102024
Balanced De-emphasis	-0.6 dB
Differential Amplitude	800.0 mV / Single - Ended Amplitude setting: 624 mV

Test Results

DUT Initial Preset	Target Preset/Coeff		Preshoot2 (dB)	Preshoot1 (dB)	De-Emph (dB)	Boost (dB) (Informative)	Electrical Response Time (ns)	DUT Reported Coefficients	Result
Q2	Q0	Preset	0	0	0	0	136.4	(0,0,32,0)	PASS
Q2		Coeff	0	0	0	0	62.53	-	PASS
Q2	Q1	Preset	0.029	1.346	0.090	1.269	138.4	(0,2,30,0)	PASS
Q2		Coeff	0.095	1.442	0.420	1.088	112.7	-	PASS
Q0	Q2	Preset	-0.20	3.625	0.356	3.392	98.60	(0,5,27,0)	PASS
Q0		Coeff	-0.01	3.052	-0.00	3.054	74.84	-	PASS
Q2	Q3	Preset	-0.12	0.369	-1.13	1.459	146.6	(0,0,30,2)	PASS
Q2		Coeff	-0.20	-0.46	-1.49	1.105	100.3	-	PASS

Tx LEQ AIC response time test results

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PCIe6.0 CEM Receiver Test Report

AIC Rx LEQ Test Results

Details	
Unique ID	Demo
Date/Time	07 June 2024, 9:12 AM
Generated By	Tek

Additional Comments
Rx LEQ Pass 1.9 E11

Test Equipment	
BERT	ANRITSU, MP1900A, 6272594808
BERT FW Version	10.02.50.01
Rx Test SW Version	6.4.3.7

Calibration Summary	
TP2 Calibration	Unique ID: 06_03_24_DB
	Full Channel Loss: Not Run
	ISI Pair: 0 & 27
	Status: Converged
	Final Calibrated EW: 3.1 ps (2.825 ps ≤ Target EW ≤ 3.425 ps)
	Final Calibrated EH: 6.0 mV (5.5 mV ≤ Target EH ≤ 6.5 mV)
	Final SJ Stress Level: 1.563 ps / 0.08 UI p-p BERT Setting (1 ps ≤ SJ Sweep ≤ 3 ps)
	Final Amplitude Level: 800.0 mV (Differential) / 542 mV (Single-Ended) BERT Setting
	Final DMI Stress Level: 9.0 mV / 21 mV BERT Setting (5 mV ≤ DMI Sweep ≤ 25 mV)
	Final CMI Stress Level: 75.0 mV / 112 mV BERT Setting
TP3 Calibration	Unique ID: TP3_FYI_Gen6_Final
	Differential Amplitude: 800.0 mV / Single - Ended Amplitude setting: 542 mV
	SJ Setting: 0.08 UI p-p @ 100 MHz (Nominal SJ 1.563 ps / 0.05 UI p-p)
	RJ Setting: 0.096 UI p-p (Nominal RJ 0.25 ps RMS / 0.113 UI p-p)
Rx LEQ Test	Loopback Configuration: Link Training
	Loopback Mode: Recovery Full EQ
	Clock Architecture: Common
	Apply SSC to Data and Clock Output: OFF
	BERT Initial Preset: Q2
	DUT Initial Preset: Q1
	DUT Target Preset: Q1
	Link #: 0 , Lane #: 0
	CTLE: Disabled
	BER Measurement Pattern: Modified Compliance
	BER: 1E-06
	Test Duration: 3.00 s
	Test Confidence: 100.00% at 1E+11 Bits
	Stress Configuration: Calibrated
	Stress Type: Apply Stress
	RJ: 0.25 ps (RMS)
	SJ: 1.563 ps
	DMI: 9.00 mV
	CMI: 75.00 mV
	Amplitude: 800.00 mV

Rx LEQ Test Results	
Status	PASS
BER	7.1293E-07
Error Count	135564
Initial BERT Preset	Q2
Final BERT Preset	-------
Final BERT Coefficients	(-------, -------, -------, -------)

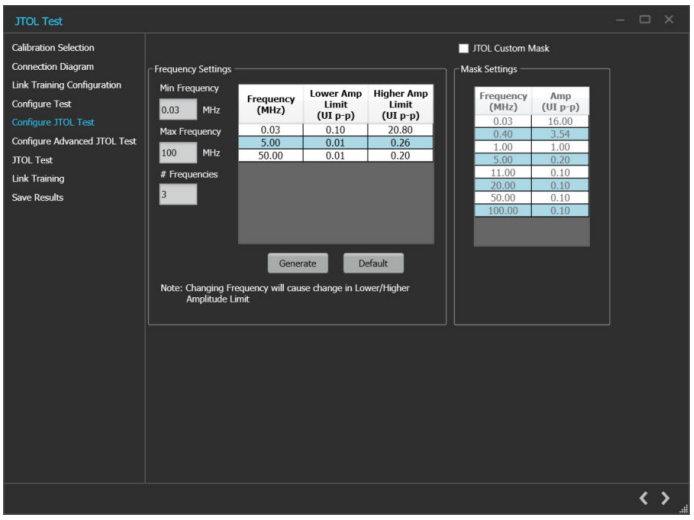
AIC Rx LEQ test results

Remote control protocol

The test software can be operated remotely through SCPI commands, allowing seamless integration into custom test flows.

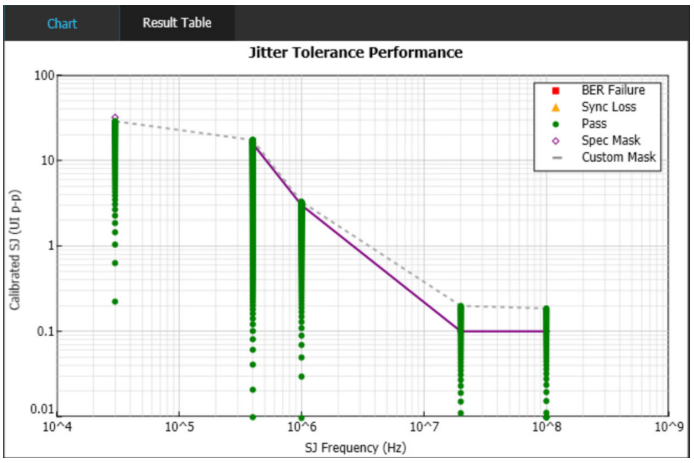
Jitter Tolerance (JTOL) test

Jitter Tolerance (JTOL) testing requires sweeping numerous calibrated SJ tones from low to high amplitude to see how the receiver-under-test CDR tracks the stress (typically in the presence of other noise & jitter sources). Custom JTOL pass/fail masks can be configured while testing with different search algorithms (upward linear, logarithmic, etc.). The Tektronix PCIe Receiver Test Suite allows engineers minimal setup with quick and descriptive test reports.

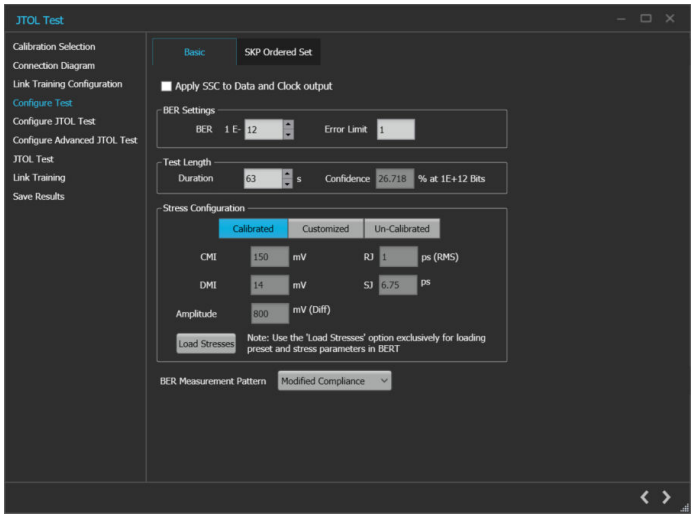


JTOL test configuration settings

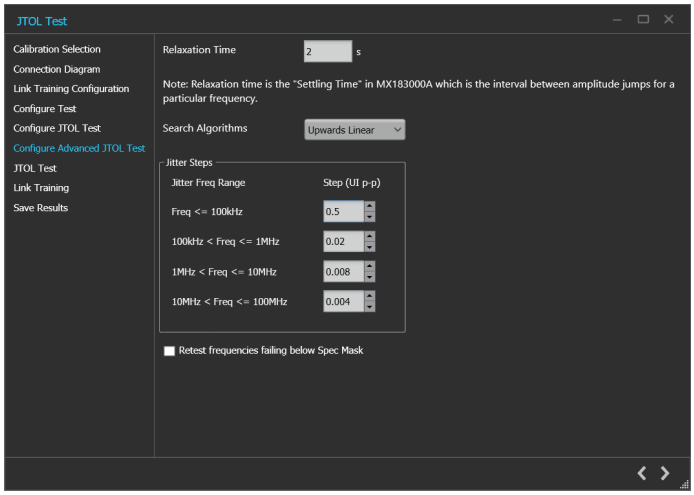
Both the custom mask and the specification mask (except Gen 1.0 & Gen 2.0) are provided in the JTOL test to have a better understanding of the DUT performance, especially at the design stage. The Receiver solution performs an automatic back-channel equalization and sampling-point optimization to ensure the best conditions for the DUT transmitted data traffic to be accurately comprehended at the BERT receiver ensuring the correct determination of BER performance.



JTOL test result with specification



Error detector and stress settings for JTOL



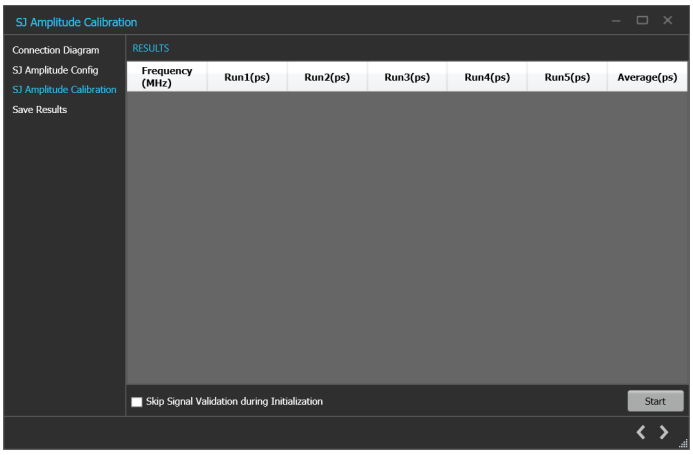
Different margin search algorithm settings for JTOL test

PCIe PLL bandwidth and peaking

This test verifies that the Add-In Card Tx PLL has the correct bandwidth and peaking. Providing a 100 MHz reference clock to the DUT with a calibrated amount of SJ allows us to measure how much SJ passes through the DUT's Tx PLL for a certain SJ tone. Performing this process across multiple tones allows the construction of the PLL frequency response to measure both bandwidth and peaking.

SJ Amplitude Calibration for Gen 6.0/5.0/4.0/3.0

- Calibration of SJ amplitude to modulate the 100 MHz Refclk used by DUT Tx PLL
- Adjustable SJ amplitude
- User-controlled SJ frequency selection to ensure adequate resolution at peaking & 3 dB point
- Increased averaging can be used to minimize variation (5 recommended)
- Software CTLE ensures support for higher loss channels and various DUT Tx patterns



SJ amplitude calibration

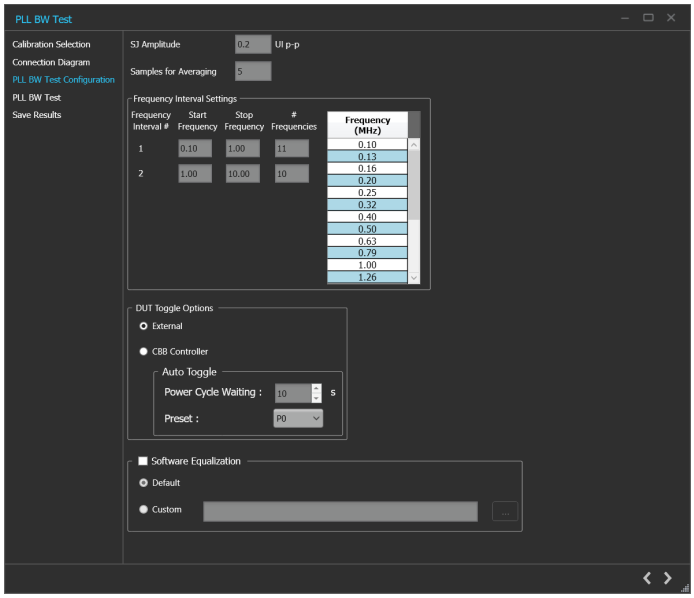
Result Summary	
SJ Amplitude Cal	SJ Amplitude: 0.2 UI p-p
	Samples for averaging: 5

Frequency (MHz)	Run1 (ps)	Run2 (ps)	Run3 (ps)	Run4 (ps)	Run5 (ps)	Average (ps)
0.10	6.446	6.445	6.376	6.006	6.209	6.296
0.13	6.348	6.159	6.198	6.171	6.32	6.239
0.16	6	6.45	6.546	6.296	6.367	6.332
0.20	6.228	5.983	6.576	5.831	6.538	6.231
0.25	6.177	6.398	6.27	6.362	6.273	6.296
0.32	6.553	6.447	6.254	6.268	6.287	6.362
0.40	6.325	6.386	6.438	6.342	6.248	6.348
0.50	6.184	6.343	6.192	6.288	6.395	6.28
0.63	6.239	6.345	6.296	6.337	6.426	6.329
0.79	6.28	6.299	6.263	6.267	6.263	6.274
1.00	6.261	6.276	6.177	6.455	6.338	6.301
1.26	6.374	6.255	6.293	6.38	6.374	6.335
1.58	6.35	6.248	6.245	6.367	6.317	6.305
2.00	6.198	6.404	6.186	6.398	6.262	6.29
2.51	6.327	6.268	6.242	6.217	6.281	6.267
3.16	6.264	6.295	6.262	6.295	6.242	6.272
3.98	6.354	6.255	6.264	6.31	6.326	6.302
5.01	6.328	6.217	6.245	6.228	6.258	6.255
6.31	6.23	6.254	6.346	6.31	6.221	6.272
7.94	6.207	6.199	6.234	6.281	6.282	6.241
10.00	6.21	6.222	6.25	6.192	6.271	6.229

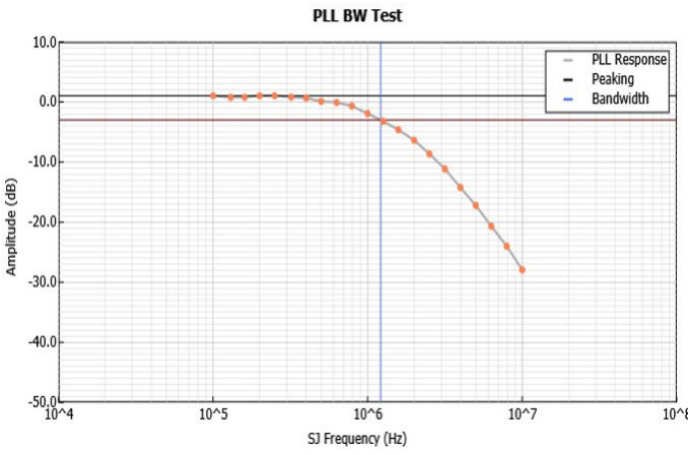
Result summary for SJ Amplitude calibration

PLL bandwidth and peaking measurements

- Bandwidth and peaking reported for selected data rates
- DUT Tx can transmit compliance patterns or jitter measurement (toggle) patterns
- Consistent DSP algorithm used for SJ calibration and DUT testing
- Test report with PLL bandwidth, peaking, frequency response plot, and individual measurements



PLL bandwidth test



Test results

Ordering information

PCIe Gen 7.0 BASE software options

Item	Description	Type
RXSW-FLP-PCIE7	License; PCI Gen 7.0 Rx BASE automation software for TEK scopes and Anritsu BERT; Floating Permanent	Software
RXSW-NLP-PCIE7	License; PCI Gen 7.0 Rx BASE automation software for TEK scopes and Anritsu BERT; Node-Locked Permanent	Software

PCIe Gen 6.0 BASE and CEM software options

Item	Description	Type
RXSW-FL1-PCIE6	License; PCI Gen 6.0 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Floating 1-Year Subscription	Software
RXSW-FLP-PCIE6BC	License; PCI Gen 6.0 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Canned; Electronically Downloaded; Floating; Permanent	Software
RXSW-NL1-PCIE6	License; PCI Gen 6.0 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Node-Locked 1-Year Subscription	Software
RXSW-NLP-PCIE6BC	License; PCI Gen 6.0 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Canned; Electronically Downloaded; Node-Locked Permanent	Software

PCIe Gen 5.0 BASE and CEM software options

Item	Description	Type
RXSW-NL1-PCIE5	License; PCI Gen 5.0 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Node-Locked 1-Year Subscription	Software
RXSW-NLP-PCIE5BC	License; PCI Gen 5.0 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Canned; Electronically Downloaded; Node-Locked Permanent	Software
RXSW-FL1-PCIE5	License; PCI Gen 5.0 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Floating 1-Year Subscription	Software
RXSW-FLP-PCIE5BC	License; PCI Gen 5.0 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Canned; Electronically Downloaded; Floating Permanent	Software

PCIe Gen 1.0 – 4.0 BASE and CEM software options

Item	Description	Type
RXSW-NL1-PCIE4C	License; PCI Gen 3.0, Gen 4.0 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Node-Locked 1-Year Subscription	Software
RXSW-NLP-PCIE4	License; PCI Gen 3.0, Gen 4.0 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Node-Locked Permanent	Software

Item	Description	Type
RXSW-FL1-PCIE4C	License; PCI Gen 3.0, Gen 4.0 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Floating 1-Year Subscription	Software
RXSW-FLP-PCIE4	License; PCI Gen 3.0, Gen 4.0 Rx BASE and CEM Automation Software for Tektronix oscilloscopes and Anritsu BERT; Floating Permanent	Software

NOTE: Gen 1.0 and Gen 2.0 are supported only on DPO70000 Series oscilloscopes.

PCIe PLL BW software options

Item	Description	Type
RXSW-NLP-PLLBW-PCIE	License; PCIe PLL BW Gen 6.0/5.0/4.0/3.0 Rx Automation Software for Tektronix oscilloscopes and Anritsu BERT; Canned; Electronically Downloaded; Node-Locked Permanent	Software
RXSW-NL1-PLLBW-PCEG5	License; PCIe PLL BW Gen 6.0/5.0/4.0/3.0 Rx automation software for Tektronix oscilloscopes and Anritsu BERT; 1-year subscription; Node-Locked	Software
RXSW-FLP-PLLBW-PCIE	License; PCIe PLL BW Gen 6.0/5.0/4.0/3.0 Rx Automation Software for Tektronix oscilloscopes and Anritsu BERT; Canned; Electronically Downloaded; Floating Permanent	Software
RXSW-FL1-PLLBW-PCEG5	License; PCIe PLL BW Gen 6.0/5.0/4.0/3.0 Rx automation software for Tektronix oscilloscopes and Anritsu BERT; 1-year subscription; Floating	Software

Overall Setup list:

PCIe Gen 7.0 BASE

Item	Vendor	Type	Requirement	Quantity	Description	Notes
MP1900A	Anritsu	Equipment	Required	1	BERT with Gen 7.0 PAM4 PPG (model #MU196020C)	Customer to work with Anritsu to get the exact BERT configuration and quote
DPS77004SX + sync cable	Tektronix	Equipment	Required	1	Dual-Stack 70GHz SX Scope	65GHz or higher bandwidth. Backwards compatible with PCIE 1.0/2.0/3.0/4.0/5.0/6.0
PAMPCIE7	Tektronix	Software	Required	1	PAMPCIe7: PAM Analysis (PAMJET) - PCIe Electrical	PAMPCIe7: PAM Analysis (PAMJET) - PCIe Electrical
PAMJET-E	Tektronix	Software	Required	1	PAMJET-E: PAM Analysis (PAMJET) - Electrical	PAMJET-E: PAM Analysis (PAMJET) - Electrical
DPO7AFP	Tektronix	Equipment	Optional	1	Auxiliary Front Panel	
DPO7RFK2	Tektronix	Tektronix Accessory	Required	2	Attenuator Kit	Attenuator kit + DC Blocks + V-K adapters
DJA	Tektronix	Software	Required	1	DPOJET Advanced option	DPOJET advanced Jitter, Eye & Timing Analysis SW option (Used for Multi-tone SJ calibration for PCIe 4.0/5.0/6.0, PLL BW measurements)

Item	Vendor	Type	Requirement	Quantity	Description	Notes
SDLA64	Tektronix	Software	Recommended	1	Serial Data Link Analysis Software	Embedding/De-embedding/s-parameter filter generation/ Receiver Virtualization & Analysis Software
174-6659-01	Tektronix	Tektronix Accessory	Required	1	Cable; SMA-to-SMP, Right Angle, 1ps phase-matched, 1000mm, 20GHz	Refclk connection between DUT & BERT
1.85 Cable Kit	PCI-SIG	Accessory	Required	1	1.85mm cable kit from PCI-SIG	1.85mm Female to MMPX Male adapter (x4) 1.85mm Male to MMPX Female adapter (x4) SF570E - MMPX Male to 1.85mm Male 36 inch length (1 pair) SF570E - 1.85mm Male to 1.85mm Male 36 inch length (1 pair) SF570E - MMPX Male to MMPX Male 12 inches length (Qty 2) MF86HE - MMPX Male to 1.85mm Female 4 inches length (Qty 2) SF570E - MMPX Male to MMPX Male 24 inches length (Qty 2) MinibendL - SMP Female to SMA Female 2.5 inches length (Qty 2)
PCIe 7.0 Base Fixture	PCI-SIG	Test Fixtures	Required	1	Gen 7.0 Base Test Fixtures	Reach out to PCI-SIG for availability information
RXSW-NLP-PCIE7	Tektronix	Software	Required	1	License; PCI Gen 7.0 Rx BASE automation software for TEK scopes and Anritsu BERT;Node-Locked Permanent	BERT stress calibration
RXSW-FLP-PCIE7					License; PCI Gen 7.0 Rx BASE automation software for TEK scopes and Anritsu BERT;Floating Permanent	

PCIe Gen 6.0 CEM

Item	Vendor	Type	Requirement	Quantity	Description	Notes
MP1900A	Anritsu	Equipment	Required	1	≥32Gb/s BERT with PAM4 PPG (MU196020A), PAM4 ED (MU196040B), and CDR (MU196060A)	Cables required for connection between BERT modules shall be included by the 3rd party vendor. Configuration for BERT provided by Anritsu. NRZ or PAM4 Config can be used for Gen3.0/4.0/5.0. Customer to work with Anritsu to get the exact BERT configuration and quote.
DPS75004SX	Tektronix	Equipment	Required	1	Dual-Stack 50GHz Sx Scope	50G or better. Backward compatible to PCIe Gen1.0/2.0/3.0/4.0/5.0. Depending on the bench locations for the DUT, scope and BERT the user can either go with 2pr - PMCABLE1M and 1pr 174-6663-01, OR, 3pr - PMCABLE1M.
DPO7AFP	Tektronix	Equipment	Optional	1	Auxiliary Front Panel	-
DPO7RFK2	Tektronix	Tektronix Accessory	Required	2	Attenuator Kit	Attenuator kit + DC Blocks + V-K adapters
C7239	CentricRF	3rd Party	Optional	2	2.92mm Female to 2.4mm Female Adapter Right Angle VSWR 1.15 40Ghz	Optional adapters to reduce the protrusion distance of the ATI SX scope front end. FMAD1227 from Fairview Microwave can be another option.
DJA	Tektronix	Option	Required	1	DPOJET Advanced option	DPOJET advanced Jitter, Eye & Timing Analysis SW option (Used for Multi-tone SJ calibration for PCIe 4.0/5.0/6.0, PLL BW measurements)
SDLA64	Tektronix	Option	Recommended	1	Serial Data Link Analysis Software	Embedding/De-embedding/s-parameter filter generation/ Receiver Virtualization & Analysis Software
PMCABLE1M	Tektronix	Tektronix Accessory	Required	2 or 3	Cable pair; 2.92-to-2.92mm, Straight, 1.5ps matched, 1000mm, 40GHz	Equipment connection to fixtures and DUT
174-6663-01	Tektronix	Tektronix Accessory	Optional	0 or 1	Cable pair; 2.92-to-2.92mm, Straight, 1.5ps matched, 500mm, 40GHz	Signal Connection between scope and BERT for Tx LEQ
174-6666-01	Tektronix	Tektronix Accessory	Required	1	Cable; SMA-to-SMA, Right Angle-Right Angle, 500mm	Signal Connection between scope and BERT for Tx LEQ AUX Trigger

Item	Vendor	Type	Requirement	Quantity	Description	Notes
174-6659-01	Tektronix	Tektronix Accessory	Required	1	Cable pair; SMA-to-SMP, Right Angle, 1ps phase-matched, 1000mm, 20GHz	Refclk connection between DUT & BERT
MPR40M	Fairview Microwave	3rd Party	Required	2	2-Way Power Divider 2.92mm Connectors, 40 GHz	Split signal from DUT Tx to the scope and Error Detector
C7035	CentricRF	3rd Party	Optional	4	Right Angle Male-Female 2.92mm adapter	Cable management
C7049	CentricRF	3rd Party	Required	2	2.92mm Male to 2.92mm Male Adaptor	Power divider output to scope input
ZTM2	Mini-circuits	Equipment	Optional	1 to 2	40GHz RF switch for automated multi-lane testing	Contact Tektronix for model and configuration assistance
PowerUSB - Basic	PowerUSB	3rd Party	Optional	1	Power USB Power Strip	Automate DUT power cycle
PCIe 6.0 CEM Test Fixture	PCI-SIG	Test Fixtures	Required	1	Gen 6.0 CEM Test Fixtures	PCI-SIG
RXSW-NLP-PCIE6BC	Tektronix	Software	Required	1	PCI Gen 6.0 Rx BASE and CEM automation software for Tektronix oscilloscopes and Anritsu BERT	Node-Locked Permanent
RXSW-NL1-PCIE6						Node-Locked - 1-Year Subscription
RXSW-FLP-PCIE6BC						Floating Permanent
RXSW-FL1-PCIE6						Floating - 1-Year Subscription

NOTE: Another matched pair of cables (e.g. 174-6663-01) will be required if the Active redriver is used for Rx or Tx LEQ.

NOTE: Gen 6.0 CEM Test Fixtures are not backwards compatible for Gen 3.0 & Gen 4.0 CEM Rx.

NOTE: It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit.

PCIe Gen 6.0 Base

Item	Vendor	Type	Requirement	Quantity	Description	Notes
DPS75004SX	Tektronix	Equipment	Required	1	Dual-Stack 50 GHz Sx oscilloscope	50 GHz or better
DPO7RFK2	Tektronix	Tektronix accessory	Required	2	Attenuator kit	Attenuator kit + DC blocks
103047400	Tektronix	Tektronix accessory	Required	2	Connector savers (1.85 mm)	1.85 mm oscilloscope channel input connection
Anritsu MP1900A **NOTE:** Configuration for BERT provided by 3rd party vendor.	Anritsu	3rd party equipment	Required	1	Bit Error Rate Tester (BERT)	Configuration provided by 3rd party

Item	Vendor	Type	Requirement	Quantity	Description	Notes
DJA	Tektronix	Equipment SW option	Required	1	DPOJET advanced option	DPOJET advanced Jitter, Eye and Timing Analysis SW option
PAMJET-E	Tektronix	Equipment SW option	Required	1	PAM4 tool	PCIe Gen 6.0 PAM4 measurement
PAMJET PCIe Option	Tektronix	Equipment SW option	Required	1	PAMJET PCIe Option	
Gen 5.0 Base Test Fixture Set	PCI-SIG	Test fixtures	Required	1	Gen 5.0 Base Rev3 Test Fixtures **NOTE:** Gen 5.0 BaseTest Fixtures are not backwards compatible for Gen3 & Gen4 Base Rx	Rev3 is Meg6 material with MMPX connectors **NOTE:** It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit
PMCABLE1M	Tektronix	Tektronix accessory	Required	2	Cable pair; 2.92-to-2.92 mm, Straight, 1.5 ps phase-matched, 40 GHz	Equipment connections to fixtures and DUT
174-6659-01	Tektronix	Tektronix accessory	Required	1	Cable pair; SMA - SMP cable pair	Refclk connection between DUT and BERT
C7035	CentricRF	3rd party	Optional	4	Right Angle Male-Female 2.92 mm adapter	Cable management
RXSW-FL1-PCIE6	Tektronix	SW option	Required	1	PCI Gen 6.0 Rx BASE automation software for Tektronix oscilloscopes and Anritsu BERT License	Floating 1-Year Subscription
RXSW-FLP-PCIE6BC						Floating Permanent
RXSW-NL1-PCIE6						Node-Locked 1-Year Subscription
RXSW-NLP-PCIE6BC						Node-Locked Permanent

PCIe Gen 5.0 CEM

Item	Vendor	Type	Requirement	Quantity	Description	Notes
DPS75004SX	Tektronix	Equipment	Required	1	Dual-Stack 50 GHz Sx oscilloscope	50 G or better **NOTE:** If ATI channels will be used for refclk measurements they will need Option Key 4 (50 XL)
DPO7RFK2	Tektronix	Tektronix accessory	Required	2	Attenuator kit	Attenuator kit + DC blocks
103047400	Tektronix	Tektronix accessory	Required	2	Connector savers (1.85 mm)	1.85 mm oscilloscope channel input connection

Item	Vendor	Type	Requirement	Quantity	Description	Notes
Anritsu MP1900A **NOTE:** Configuration for BERT provided by 3rd party vendor.	Anritsu	3rd party equipment	Required	1	Bit Error Rate Tester (BERT) **NOTE:** Cables required for connection between BERT modules shall be included for the 3rd party vendor.	Configuration provided by 3rd party
DJA	Tektronix	Equipment SW option	Required	1	DPOJET advanced option	DPOJET advanced option
SDLA64	Tektronix	Equipment SW option	Required	1	Serial Data Link Analysis (SDLA) software	Serial Data Link Analysis (SDLA) software
PMCABLE1M	Tektronix	Tektronix accessory	Required	2 pr	Cable; 2.92-to-2.92 mm, straight, 1.5 ps phase-matched, 40 GHz	Equipment connection to fixtures and DUT
174-6663-01	Tektronix	Tektronix accessory	Required	1 pr	Cable; 2.92-to-2.92 mm, straight, 1.5 ps phase-matched, 500 mm, 40 GHz	Signal connection between oscilloscope and BERT for Tx LEQ
174-6666-01	Tektronix	Tektronix accessory	Required	2 pr	Cable; SMA-to-SMA, Right Angle-Right Angle, 500 mm	Signal connection between oscilloscope and BERT for Tx LEQ & Trigger
174-6659-01	Tektronix	Tektronix accessory	Required	1 pr	Cable; SMA - SMP cable pair	Refclk connection between DUT & BERT
MPR40M	Fairview Microwave	3rd party	Required	2	Power divider	Split signal from DUT Tx to the oscilloscope and Error Detector
C7035	CentricRF	3rd party	Optional	4	Right Angle Male-Female 2.92 mm adapter	Cable management
C7049	CentricRF	3rd party	Required	3	2.92 mm Male to 2.92 mm Male adaptor	Power divider output to oscilloscope input
Redriver	3rd party	3rd party equipment	Optional	1	Active Gen5 Redriver (back channel equalization) **NOTE:** Another matched pair of cables (e.g. 174-6663-xx) will be required if the Active redriver is used for Rx or Tx LEQ	High loss back channels (DUT Tx to Error Detector) may need EQ
PowerUSB - Basic	PowerUSB	3rd party	Optional	1	Power USB Power Strip	Automate DUT power cycle
TF-PCIE5-CEM-X16	PCI-SIG	Test fixtures	Required	1	Gen 5.0 CEM Test fixtures **NOTE:** Gen 5.0 CEM Test Fixtures are not backwards compatible for Gen3 & Gen4 CEM Rx	Tektronix fixtures are not officially approved by PCI-SIG **NOTE:** It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit

Item	Vendor	Type	Requirement	Quantity	Description	Notes
RXSW-NLP-PCIE5BC	Tektronix	Software	Required	1	PCIe Gen 5.0 Rx BASE and CEM automation software for Tektronix oscilloscopes and Anritsu BERT	Node-Locked; Permanent
RXSW-NL1-PCIE5						Node-Locked, Time Based, 1 year subscription
RXSW-FLP-PCIE5BC						Floating; Permanent
RXSW-FL1-PCIE5						Floating, Time Based, 1-year subscription

PCIe Gen 5.0 Base

Item	Vendor	Type	Requirement	Quantity	Description	Notes
DPS75004SX	Tektronix	Equipment	Required	1	Dual-Stack 50 GHz Sx Oscilloscope	50 G or better **NOTE:** If ATI channels will be used for refclk measurements they will need Option Key 4 (50 XL)
DPO7RFK2	Tektronix	Tektronix accessory	Required	2	Attenuator kit	Attenuator kit + DC blocks
103047400	Tektronix	Tektronix accessory	Required	2	Connector savers (1.85 mm)	1.85 mm oscilloscope channel input connection
Anritsu MP1900A **NOTE:** Configuration for BERT provided by 3rd party vendor.	Anritsu	3rd party equipment	Required	1	Bit Error Rate Tester (BERT) **NOTE:** Cables required for connection between BERT modules shall be included for the 3rd party vendor	Configuration provided by 3rd party
DJA	Tektronix	Equipment SW option	Required	1	DPOJET advanced option	DPOJET advanced option
SDLA64	Tektronix	Equipment SW option	Required	1	Serial Data Link Analysis (SDLA) Software	Serial Data Link Analysis (SDLA) Software
174-6659-01	Tektronix	Tektronix accessory	Required	1 pr	Cable; SMA - SMP cable pair	Refclk connection between DUT & BERT
PMCABLE1M	Tektronix	Tektronix accessory	Required	2 pr	Cable; 2.92-to-2.92 mm, Straight, 1.5 ps phase-matched, 40 GHz	Equipment connections to replica channel & DUT
Gen 5.0 Base Test Fixture Set	PCI-SIG	Test fixtures	Required	1	Gen 5.0 Base Rev3 Test Fixtures **NOTE:** Gen 5.0 BaseTest Fixtures are not backwards compatible for Gen3 & Gen4 Base Rx	Rev3 is Meg6 material with MMPX connectors **NOTE:** It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit

Item	Vendor	Type	Requirement	Quantity	Description	Notes
RXSW-NLP-PCIE5BC	Tektronix	Software	Required	1	PCIe Gen 5.0 Rx BASE and CEM automation software for Tektronix oscilloscopes and Anritsu BERT	Node-Locked; Permanent
RXSW-NL1-PCIE5						Node-Locked, Time Based, 1-year subscription
RXSW-FLP-PCIE5BC						Floating; Permanent
RXSW-FL1-PCIE5						Floating, Time Based, 1-year subscription

PCIe Gen 4.0 CEM

Item	Vendor	Type	Requirement	Quantity	Description	Notes
DPO72504DX, DPO73304SX, 7 Series DPO	Tektronix	Equipment	Required	1	≥25 GHz minimum bandwidth oscilloscope	
DJA	Tektronix	Option	Required	1	DPOJET Advanced option	DPOJET advanced Jitter, Eye & Timing Analysis SW option
MP1900A	Anritsu	Equipment	Required	Pick 1	Anritsu ≥16 Gb/s BERT, add RXSW-XXX-PCIE4C RX software	NRZ or PAM4 Config can be used for Gen 3.0/4.0/5.0
BSX240	Tektronix				Tektronix 24 Gb/s BERT, options TXEQ, STR, add BSXSICOMB and BSXPCI4CEM software	
174-6659-00	Tektronix	Tek Accessories	Required	1	Cable pair; 2.92 mm-to-SMP, Right Angle, 1ps matched, 1000 mm, 20 GHz	PCIe refclk from BSX to CBB (AIC) or Pcie refclk out of CLB to BSX refclk input (rear).
174-6663-01	Tektronix	Tek Accessories	Required	0 or 1	Cable pair; 2.92 mm to 2.92 mm, Straight, 1.5 ps matched, 500 mm, 40 GHz	Power divider out to Error Detector in
174-6665-00	Tektronix	Tek Accessories	Required	1	Cable; 2.92 mm to 2.92 mm, Right Angle-Right Angle, 300 mm, 20 GHz	BSX Subrate clock out to BSX Error Detector clock in.
174-6666-01	Tektronix	Tek Accessories	Required	1	Cable; SMA-to-SMA, Right Angle-Right Angle, 500 mm, 20 GHz	BSX Pattern Trigger out to TekScope Aux input
PMCABLE1M	Tektronix	Tek Accessories	Required	2 or 3	Cable pair; 2.92 mm to 2.92 mm, Straight, 1.5 ps matched, 1000 mm, 40 GHz	BSX TX out to DUT RX in and DUT TX out to Power Divider input.

Item	Vendor	Type	Requirement	Quantity	Description	Notes
SMP Terminator	Fairview Microwave	3rd Party	Required	Depends	50 Ohm (Female)	Quantity depends on the number of unused lane. x1 = Qty 0, x4 = Qty 6, x8 = Qty 14, x16 = Qty 30.
MPR40-2	Fairview Microwave	3rd Party	Required	2	2-Way Power Divider 2.92 mm Connectors, 40 GHz	Or equivalent
SM3242	Fairview Microwave	3rd Party	Required	2	Adapter, 2.92 mm Male to 2.92 mm Male	Power divider output to TekScope input
SD3473	Fairview Microwave	3rd Party	Required	2	DC Block, 26.5 GHz	Or equivalent
ATX Power supply	Corsair	3rd Party	Required	1	ATX power supply for System board power	As required for DUT power. Any vendor ATX power supply will work.
PCIe Gen 4.0 Test Fixtures	PCI-SIG	3rd Party	Required	1	Gen 4.0 CBB, CLB and Variable ISI board	Available only from PCI-SIG directly
SMP-SMP Cables	PCI-SIG	3rd Party	Required	4	SMP-SMP cables	
SMA-SMP (2.6")	PCI-SIG	3rd Party	Required	4	SMP-SMP cables	
Power USB – Basic	Power USB	3rd Party	Optional	1	Power USB power strip	For DUT reset automation. Not compatible with 240 VAC systems.
AH54192A	Anritsu	3rd Party	Optional	1	PCIe Gen 4.0 Active Redriver (back channel equalization)	High loss back channels (DUT Tx to Error Detector) may need Active Equalization.
C7035	Centric RF	3rd Party	Recommended	6	Adapter; 2.92 mm Right Angle Male-Female	BERT I/O and Power Divider output to BSX Error Detector
RXSW-NLP-PCIE4	Tektronix	Software	Required	1	PCIe Gen 4.0 Receiver Software	Gen 3.0 and Gen 4.0 RX CEM and BASE test software - Node-Locked, Permanent
RXSW-NL1-PCIE4C						Gen 3.0 and Gen 4.0 RX CEM and BASE test software - Node-Locked, Time Based, 1-year subscription
RXSW-FLP-PCIE4						Gen 3.0 and Gen 4.0 RX CEM and BASE test software - Floating, Permanent
RXSW-FL1-PCIE4C						Gen 3.0 and Gen 4.0 RX CEM and BASE test software - Floating, Time Based, 1-year subscription

PCIe Gen 4.0 Base

Item	Vendor	Type	Requirement	Quantity	Description	Notes
DPO/MSO70K DX/SX, 7 Series DPO	Tektronix	Equipment	Required	1	Bandwidth >=25 GHz Oscilloscope	25 G or better
Anritsu MP1900A	Anritsu	3rd party equipment	Required	1	Bit Error Rate Tester (BERT)	Configuration provided by 3rd party
DJA	Tektronix	Equipment SW option	Required	1	DPOJET advanced option	DPOJET advanced option
174-6659-01	Tektronix	Tektronix accessory	Required	1 pr	Cable; SMA - SMP cable pair	Refclk connection between DUT & BERT
PMCABLE1M	Tektronix	Tektronix accessory	Required	2 pr	Cable; 2.92-to-2.92 mm, Straight, 1.5 ps phase-matched, 40 GHz	Equipment connections to replica channel & DUT
Gen4 Base Test Fixture Set	PCI-SIG	Test fixtures	Required	1	Gen 4.0 Base Rev3 Test Fixtures	Provided by PCI-SIG
RXSW-NLP-PCIE4	Tektronix	Software	Required	1	PCIe Gen 4.0 Receiver Software	Gen 3.0 and Gen 4.0 RX CEM and BASE test software - Node-Locked, Permanent
RXSW-NL1-PCIE4C						Gen 3.0 and Gen 4.0 RX CEM and BASE test software - Node-Locked, Time Based, 1-year subscription
RXSW-FLP-PCIE4						Gen 3.0 and Gen 4.0 RX CEM and BASE test software - Floating, Permanent
RXSW-FL1-PCIE4C						Gen 3.0 and Gen 4.0 RX CEM and BASE test software - Floating, Time Based, 1-year subscription

PCIe Gen 3.0 Base/CEM

Item	Vendor	Requirement	Quantity	Description	Notes
MP1900A	Anritsu	Required	1	≥16 Gb/s BERT	NRZ or PAM4 Configuration can be used for Gen 3.0/4.0/5.0 **NOTE:** Configuration and Cables are required for connection between BERT modules are included by the 3rd party vendor.
DPO/MSO70K DX/SX, 7 Series DPO	Tektronix	Required	1	Bandwidth >= 12 GHz, 4-channel oscilloscope	
DJA	Tektronix	Required	1	DPOJET Advanced option	DPOJET advanced Jitter, Eye and Timing Analysis SW option

Item	Vendor	Requirement	Quantity	Description	Notes
MP1900A	Anritsu	Required	1	≥16 Gb/s BERT	NRZ or PAM4 Configuration can be used for Gen 3.0/4.0/5.0 **NOTE:** Configuration and Cables are required for connection between BERT modules are included by the 3rd party vendor.
174-6659-01	Tektronix	Required	1	1-m Cable pair (2.92 mm SMA Male - SMP)	DUT-BERT Ref clock
PMCABLE1M	Tektronix	Required	2	1 m Cable pair (2.92 mm M-M, Straight, 1.5 ps phase-matched, 40 GHz)	Equipment connection to fixtures and DUT
174-6663-01	Tektronix	Required	1	0.5 m Cable pair (2.92 mm M-M, Straight, 1.5 ps phase-matched, 40 GHz)	Signal Connection between oscilloscope and BERT for Tx LEQ
174-6666-01	Tektronix	Required	2	0.5 m Cable pair (SMA M-M, Right Angle - Right Angle)	Connection between oscilloscope and BERT for Tx LEQ and Trigger
MPR40M	Fairview Microwave	Required	1	Power Divider pair (2 way 2.92 mm F-F-M)	Split signal from DUT Tx to the oscilloscope and Error detector
Power USB Power Strip	Power USB	Required		Power USB – Basic	Automate DUT power cycle
SMP 50 Ohm Terminator	Any	Required		50 ohms (Female)	
ATX Power Supply for System Board Power	Any	Required	1	Any	
PCI-SIG	PCI-SIG	Required	1	Gen 3.0 BASE / CEM Test Fixtures	
RXSW-NLP-PCIE4	Tektronix	Required	1	PCIe Gen 3.0 Receiver software	Gen 3.0 BASE / CEM Rx test software - Node-Locked; Permanent
RXSW-NL1-PCIE4C					Gen 3.0 Base / CEM Rx test software - Node-Locked, Time Based, 1-year subscription
RXSW-FLP-PCIE4					Gen 3.0 BASE / CEM Rx test software - Floating; Permanent
RXSW-FL1-PCIE4C					Gen 3.0 BASE / CEM Rx test software - Floating, Time Based, 1-year subscription

PCIe Gen 2.0, Gen 1.0 Base and CEM Rx

Item	Vendor	Requirement	Quantity	Description	Notes
MP1900A	Anritsu	Required	1	>=2.5Gb/s BERT	
DPO/MSO70K DX/SX	Tektronix	Required	1	≥6 GHz, 4-channel oscilloscope (Gen 1) >=12.5GHz, 4-channel oscilloscope (Gen 2)	
DJA	Tektronix	Required	1	DPOJET Advanced option	DPOJET Advanced Jitter, Eye and Timing Analysis SW option
174-6659-01	Tektronix	Required	1	1-m Cable pair, 2.92 mm SMA Male - SMP	DUT-BERT Ref clock
PMCABLE1M	Tektronix	Required	2	1 m Cable pair, 2.92 mm M-M, Straight, 1.5 ps	Equipment connection in fixtures and DUT
174-6663-01	Tektronix	Required	1	0.5 m Cable pair, 2.92 mm M-M, Straight	Signal Connection between oscilloscope and BERT for Tx LEQ
174-6666-01	Tektronix	Required	2	0.5 m Cable pair, SMA-MH, Right Angle	Connection between oscilloscope and BERT for Tx IFQ and Trigger
MPR40M	Fairview Microwave	Required	1	Power Divider (2 way 2.92 mm F-F-M)	Split signal from DUT Tx to the oscilloscope and Error Detector
Power USB Power Strip	Power USB	Required	1	Power USB – Basic	Automate DUT power cycle
SMP 50 Ohm Terminator	Any	Required		50 ohms (Female)	
ATX Power Supply for System Board Power	Any	Required	1	Any	
PCI-SIG Fixture	PCI-SIG	Required	1	Gen 4.0/5.0 test fixtures OR Variable ISI board	
RXSW-NLP-PCIE4	Tektronix	Software	Pick 1	PCIe Gen 3.0 Receiver software	Gen 4.0 CEM & Base Rx test software - Node-Locked; Permanent
RXSW-NL1-PCIE4C					Gen 4.0 CEM & Base Rx test software - Node-Locked, Time Based, 1-year subscription
RXSW-FLP-PCIE4					Gen 4.0 CEM & Base Rx test software - Floating; Permanent
RXSW-FL1-PCIE4C					Gen 4.0 CEM & Base Rx test software - Floating, Time Based, 1-year subscription

PCI PLL Bandwidth (Gen 6.0/5.0/4.0/3.0)

Item	Vendor	Type	Requirement	Quantity	Description
MP1900A	Anritsu	Equipment	Required	1	≥32 Gb/s BERT
DPS73304SX	Tektronix	Equipment	Required	1	Single Stack 33 GHz or better (e.g. Dual-Stack 50 GHz SX oscilloscope)
DPO7AFP	Tektronix	Equipment	Optional	1	Auxiliary Front Panel
DPO7RFK2	Tektronix	Tektronix Accessory	Required	2	Attenuator Kit
PMCABLE1M	Tektronix	Tektronix Accessory	Required	2	Cable pair; 2.92-to-2.92 mm, Straight, 1.5 ps matched, 1000 mm, 40 GHz
DJA	Tektronix	Option	Required	1	DPOJET Advanced option
TF-PCIE5-CEM-X1 **NOTE:** It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit.	PCI-SIG	Test Fixtures	Required	1	Gen 5.0 CEM Test Fixtures
TF-PCIE5-CEM-X16 **NOTE:** It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit.	PCI-SIG	Test Fixtures	Required		
RXSW-NLP-PLLBW-PCIE	Tektronix	Software	Required	1	PCIe Gen 6.0/5.0/4.0/3.0 PLL BW automation software for Tektronix oscilloscopes and Anritsu BERT- Node-Locked; Permanent
RXSW-NL1-PLLBW-PCEG5					PCIe Gen 6.0/5.0/4.0/3.0 PLL BW automation software for Tektronix oscilloscopes and Anritsu BERT; Perpetual; Node-Locked, Time Based, 1-year subscription
RXSW-FLP-PLLBW-PCIE					PCIe Gen 6.0/5.0/4.0/3.0 PLL BW automation software for Tektronix oscilloscopes and Anritsu BERT- Floating; Permanent
RXSW-FL1-PLLBW-PCEG5					PCIe Gen 6.0/5.0/4.0/3.0 PLL BW automation software for Tektronix oscilloscopes and Anritsu BERT; Perpetual; Floating Time Based, 1-year subscription

Host system software requirements

- Microsoft Windows 10
- Microsoft Windows 11

Tektronix is registered to ISO 9001:2015 and ISO 14001:2015.

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