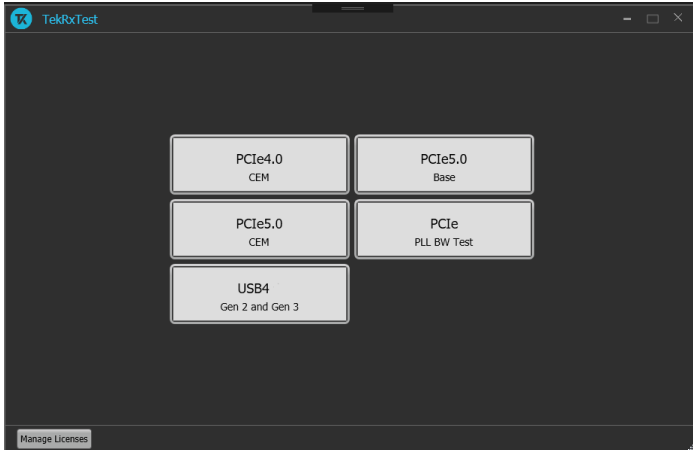


## Tektronix PCI Express

### PCI Express Receiver Test Suite Datasheet



Improve accuracy and precision of PCI Express Gen5 Receiver Stressed Eye Calibration, Receiver & Transmitter Link Equalization testing, and Receiver Jitter Tolerance with Tektronix automation software. Remove the complexity of receiver testing with a step-by-step user interface designed by industry leaders engaged in the standards bodies to drive the latest specifications to maturity. Industry engagement ensures our software will evolve in-step with the technology. Achieving the correct balance of simplicity and user control has been at the forefront of the design team to ensure your device can complete link training with the correct calibrated stress and be efficiently tested with optimized PHY settings.

#### Applications

- PCI Express Gen5 (32 GT/s) & Gen4 (16 GT/s)
- Gen5 Base Specification (silicon validation) & Gen5 and Gen5 CEM Specification (system verification & compliance)
- Root Complex & Non-Root Complex silicon
- Systems (motherboards & servers), Add-in Cards, Switches & Bridges, Extension Devices (retimers & redrivers)

#### Features and benefits

##### PCI Express Gen5 (32 GT/s)

- Receiver automation software for Tektronix DPO70000SX Series Real Time Scopes & Anritsu MP1900A BERT
- Wizard based user interface for each step of calibration and test
- Pop-up user tips to simplify decision making
- Stressed Eye Calibration (32 GT/s) &
  - Base & CEM
  - TP3 – AC/DC Balance, Amplitude, Tx Equalization, Sinusoidal Jitter tones, & Random Jitter

- TP2 – DMI, CMI, Preset & CTLE Selection, Stressed Eye, Automated loopback through Configuration & Recovery
- Insertions Loss computation powered by Seasim Statistical Simulation Tool
- Rx Link Equalization (32 GT/s)
- Tx Link Equalization (32 GT/s)
- Jitter Tolerance (32 GT/s)
- Latest industry tool support (SigTest & Seasim)
- Calibration and test reports

##### PCI Express Gen4 (16 GT/s)

- Receiver automation software for Tektronix DPO70000SX Series Real Time Scopes & Anritsu MP1900A BERT
- Wizard based user interface for each step of calibration and test
- Pop-up user tips to simplify decision making
- Stressed Eye Calibration (32 GT/s)
  - CEM
    - TP1 – AC/DC Balance, Amplitude, Tx Equalization, Sinusoidal Jitter tones, & Random Jitter
  - TP2 – DMI, CMI, Preset & CTLE Selection, Stressed Eye, Automated loopback through Configuration & Recovery
- Insertions Loss computation powered by Seasim Statistical Simulation Tool
- Rx Link Equalization (16 GT/s)
- Tx Link Equalization (16 GT/s)
- Jitter Tolerance (16 GT/s)
- Latest industry tool support (SigTest & Seasim)
- Calibration and test reports

#### Stressed Eye Calibration

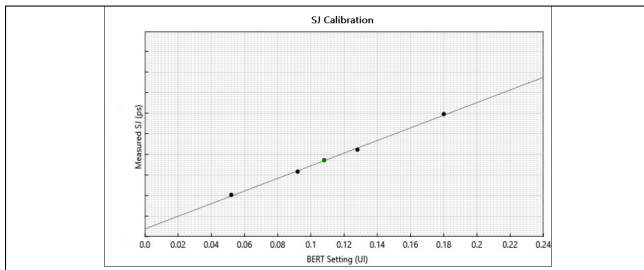
Calibration of the stressed eye signal, generated by the BERT's PPG, is important to ensure the receiver is tested in alignment with the PCI-SIG specifications with the proper amount of impairments. New challenges at 32 GT/s demand the fully automated approach taken by the Tektronix PCI Express Receiver Test Suite to avoid alternative tedious and error-prone approaches. Let the domain expertise and experience of the Tektronix engineers guide you through the steps of calibration starting with accurate TP3 measurements and ending with an end of channel eye diagram easily obtained within the tolerances required. Engineers will spend less time calibrating and more time collecting meaningful data on receiver performance and margin.

## TP3 calibration

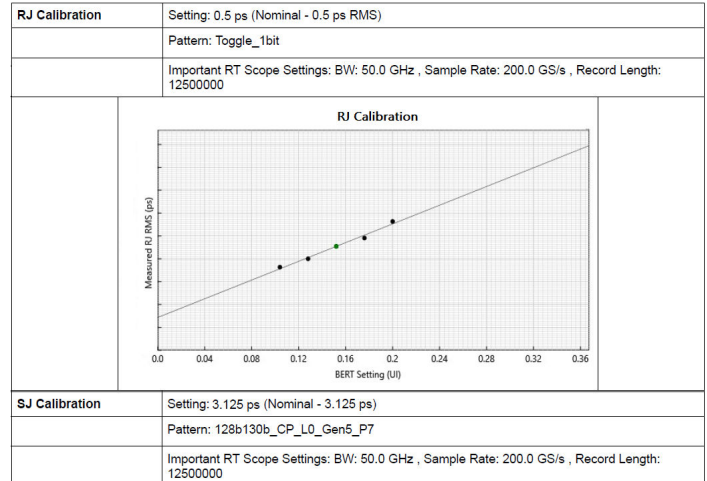
### PCI Express Gen5 (32 GT/s)

The TP3 (cable from BERT PPG to scope) is mandatory for all devices to ensure tolerances are met at the defined reference plane. Tektronix PCI Express Receiver Test Suite wizard will guide the user through all the necessary steps to pre-channel signal is true to the specification requirements to ensure future calibration steps complete with ease.

1. AC-DC Balance – Small amounts of Tx EQ de-emphasis are enabled to balance low and high-frequency sections of the pattern at a common reference plane.
2. Amplitude – The differential voltage swing is required to be within 720 – 800 mV.
3. Tx Equalization Presets – Calibration of pre-shoot and de-emphasis is required to ensure true preset level are used for testing receivers.
4. IL Measurement – Channel insertion loss is calculated using Seasim between TP3 and TP1 (loss before the TP3 reference is computed here for later removal).
5. RJ – Random Jitter (RJ) is calibrated to be 0.5 ps (RMS value) nominally.
6. SJ – Sinusoidal Jitter (SJ) is calibrated over the required range of 1-5 ps (p-p) including the nominal SJ specification of 0.1 UI (or 3.125 ps) at 100 MHz frequency.
7. SJ@210 MHz – This calibration is required for JTOL measurements with some calibrations



8. Multi-tone SJ – For JTOL measurements where up to maximum 14 frequencies are used, calibration for frequencies other than 100 MHz are required to be performed.



#### RJ/SJ calibration

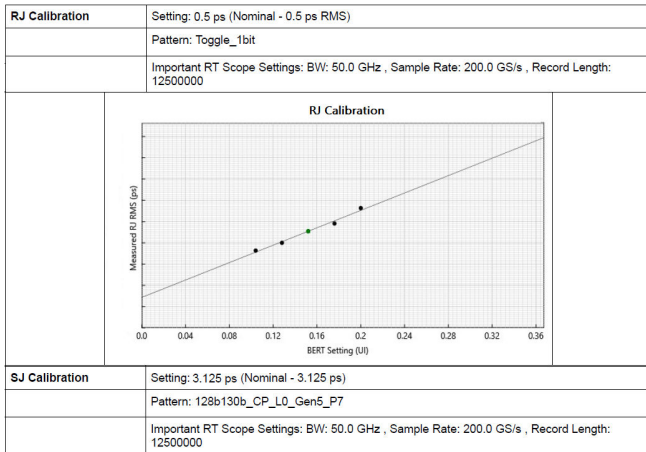
Automatic characterization and precise calibration of presets, RJ, and SJ along with the important parameters used for calibration like pattern type, scope, BERT settings, regression line slopes, and intercept for reference.

## TP1 calibration

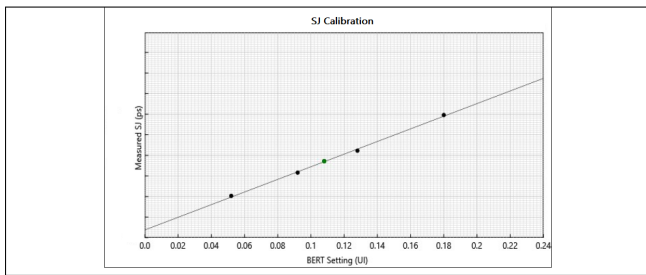
### PCI Express Gen4 (16 GT/s)

The TP1 (cable from BERT PPG to scope) is mandatory for all devices to ensure tolerances are met at the defined reference plane. Tektronix PCI Express Receiver Test Suite wizard will guide the user through all the necessary steps to pre-channel signal is true to the specification requirements to ensure future calibration steps complete with ease.

1. AC-DC Balance – Small amounts of Tx EQ de-emphasis are enabled to balance low and high-frequency sections of the pattern at a common reference plane.
2. Amplitude – The differential voltage swing is required to be within 720 – 800 mV.
3. Tx Equalization Presets – Calibration of pre-shoot and de-emphasis is required to ensure true preset level are used for testing receivers.
4. IL Measurement – Channel insertion loss is calculated using Seasim between TP3 and TP1 (loss before the TP3 reference is computed here for later removal).



5. RJ – Random Jitter (RJ) is calibrated to be 1 ps (RMS value) nominally.
6. SJ – Sinusoidal Jitter (SJ) is calibrated over the required range of 5-10 ps (p-p) including the nominal SJ specification of 0.1 UI (or 6.25 ps) at 100 MHz frequency.
7. SJ@210 MHz – This calibration is required for JTOL measurements with some calibrations.



8. Multi-tone SJ – For JTOL measurements where up to maximum 14 frequencies are used, calibration for frequencies other than 100 MHz are required to be performed.

<div>Tektronix</div> <div>PCIe5.0 CEM Receiver Calibration Report</div> <div>TP1 Calibration Results</div>	
Test Details	
Unique ID	[Example_TP1_Calibration]
Date/Time	05 October 2020, 11:56 PM
Generated By	Tektronix
Additional Comments	
No Comments	
Test Equipment	
BERT	ANRITSU, MP1900A, 6261788378
Rx Test SW Version	6.0.1.28
RT Scope	TEKTRONIX, DPO77002SX, B321456
RT Scope FW Version	10.11.0 Build 30
TekRxService Version	2.8.0.8
DPOJET Version	10.2.0.17
Result Summary	
TP1 Calibration	Unique ID: [Example_TP1_Calibration]
	Balanced De-emphasis: -1.8 dB
	Differential Amplitude: 800.0 mV
	SJ Setting: 0.1 UI p-p @ 100 MHz (Nominal SJ 3.125 ps / 0.1 UI p-p )
	RJ Setting: 0.16 UI p-p (Nominal RJ 0.5 ps RMS / 0.016 UI p-p )
	SJ@210 MHz Regression Line Parameters: Slope = - / Intercept = -
	Multi-tone SJ Calibration performed for 7 frequencies
TP1 Calibration Details	
AC-DC Balance	Setting De-emphasis: -1.8 dB
	Pattern: 64ones_64zeros_128bit10
	Important RT Scope Settings: BW: 50.0 GHz , Sample Rate: 200.0 GS/s , Record Length: 5000
Amplitude Calibration	Pattern: 64ones_64zeros_128bit10
Preset Calibration	Pattern: 64ones_64zeros_128bit10
	Important RT Scope Settings: BW: 50.0 GHz , Sample Rate: 200.0 GS/s , Record Length: 5000

#### Example Report:

Automatic characterization and precise calibration of presets, RJ, and SJ along with the important parameters used for calibration like pattern type, scope, BERT settings, regression line slopes, and intercept for reference.

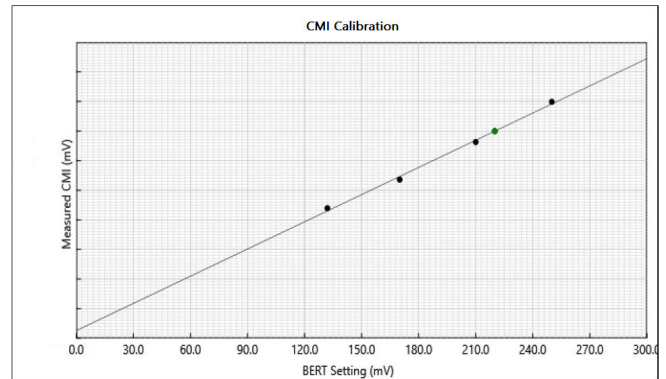
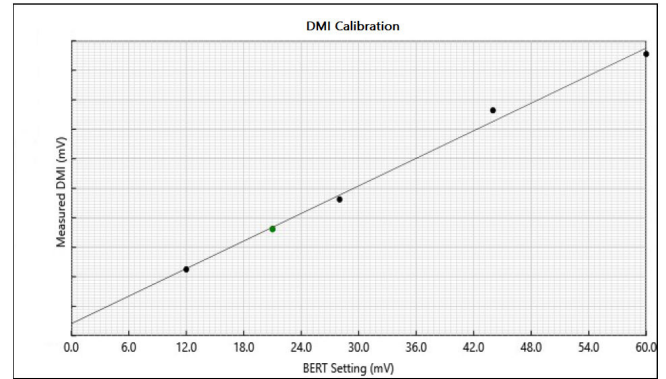
## TP2 calibration

### PCI Express Gen5 (32 GT/s) & Gen4 (16GT/s)

The TP2 (end of the channel) calibration is a complex process requiring a deep understanding of the BERT, Real Time Oscilloscope, post-processing tools, and the PCIe specifications. The Tektronix PCI Express Receiver Test Suite will remove the complexity and ensure the desired results are achieved through user-friendly automation. Time to TP2 completion is critical, so efficient techniques have been Implemented to ensure an accurate stressed eye is achieved within a reasonable time scale. From calibration of DMI (differential mode interference modeling cross-talk) to the fine granularity adjustments to SJ and DMI necessary to find the stressed eye solutions space, our automation software will guide you through this otherwise daunting task.

1. DMI– The differential mode interference is required to be calibrated within 5-30 mV (p-p) [Gen5] / 10-25 mV (p-p) [Gen4] by capturing the 2.1 GHz sinusoidal output for a duration of 40 ns.
2. CMI – The common-mode interference is required to be calibrated for a nominal voltage of 150 mV (p-p) by capturing the 120 MHz sinusoidal output for a duration of 62.5 us.
3. Channel insertion loss for DMI/CMI & eye diagram measurements computed with Seasim (TP1 to TP2/TP2P for 16GT/s & TP3 to TP2/TP2P for 32GT/s).
4. Channel Selection based on optimal Tx EQ Preset and Rx CTLE – Base Specification compliant for Eye Area criteria and tie breaker rules.
5. Stressed-Eye calibration – Fine-tuning of the eye using amplitude, SJ, & DMI is utilized to place the stressed eye within allowed tolerances.

<b>Tektronix</b> <b>PCIe5.0 CEM Receiver Calibration Report</b> <b>AIC TP2 Calibration Results</b>	
Test Details	
Unique ID	[Example_TP2_AIC_Calibration]
Date/Time	26 September 2020, 7:13 AM
Generated By	Tektronix
Additional Comments	
No Comments	
Test Equipment	
BERT	ANRITSU, MP1900A, 6261788378
Rx Test SW Version	6.0.1.18
RT Scope	TEKTRONIX, DPO77002SX, B321456
RT Scope FW Version	10.11.0 Build 30
TekRxService Version	2.8.0.8
Calibration Summary	
TP2 Calibration	Unique ID: [Example_TP2_AIC_Calibration]
	Full Channel Loss: 36 dB
	Selected Preset: P6
	Selected CTLE Index: 3.0
	Status: Converged
	Final Calibrated EW: 9.375 ps (8.875 ps ≤ Target EW ≤ 9.875 ps)
	Final Calibrated EH: 15.5 mV (13.5 mV ≤ Target EH ≤ 16.5 mV)
	Final SJ Stress Level: 3.125 ps (1 ps ≤ SJ Sweep ≤ 5 ps)
	Final DMI Stress Level: 10 mV (5 mV ≤ DMI Sweep ≤ 30 mV)
	Final Amplitude Level: 800 mV (Differential)
	SJ@210 MHz Setting during JTOL test: 0 UI p-p (Calibrated Value of SJ (ps) required to achieve the target stressed eye width minus 3.125 ps)
	Final CMI Stress Level: 150.0 mV
DMI	Pattern: Electrical_Idle
	Important RT Scope Settings: BW: 5.0 GHz , Sample Rate: 200.0 GS/s , Record Length: 8000
CMI	Pattern: Electrical_Idle
	Important RT Scope Settings: BW: 5.0 GHz , Sample Rate: 200.0 GS/s , Record Length: 12500000



AIC TP2 calibration results

Stressed Eye Calibration		Final Amplitude Level: 800.0 mV			
		Pattern: Toggle_512bits			
Index	SJ (ps)	DMI (mV)	Amp (mV)	Eye Width (ps)	Eye Height (mV)
1	3.125	10	800	14.468	23.836
2	3.125	10	800	14.652	24.434
3	3.125	10	800	14.747	23.925
4	3.125	10	800	14.416	23.455
5	3.125	10	800	14.531	23.912
6	3.125	10	800	14.375	24.374
7	3.125	10	800	14.408	23.983
8	3.125	10	800	14.583	24.183
AVERAGE	3.125	10	800	14.522	24.013

AVERAGE	3.125	27.5	800	10.26	16.183
73	3.375	27.5	800	9.882	15.575
74	3.375	27.5	800	10.049	16.18
75	3.375	27.5	800	10.096	15.675
76	3.375	27.5	800	9.801	15.192
77	3.375	27.5	800	9.912	15.655
78	3.375	27.5	800	9.943	16.09
79	3.375	27.5	800	9.824	15.717
80	3.375	27.5	800	10.07	15.882
AVERAGE	3.375	27.5	800	9.947	15.746
82	3.625	27.5	800	9.726	15.341
83	3.625	27.5	800	9.893	15.934
84	3.625	27.5	800	9.94	15.482
85	3.625	27.5	800	9.644	14.928
86	3.625	27.5	800	9.756	15.484
87	3.625	27.5	800	9.786	15.879
88	3.625	27.5	800	9.668	15.448
89	3.625	27.5	800	9.913	15.689
AVERAGE	3.625	27.5	800	9.791	15.523
SELECTED	3.625	27.5	800	9.791	15.523

Stressed eye calibration result

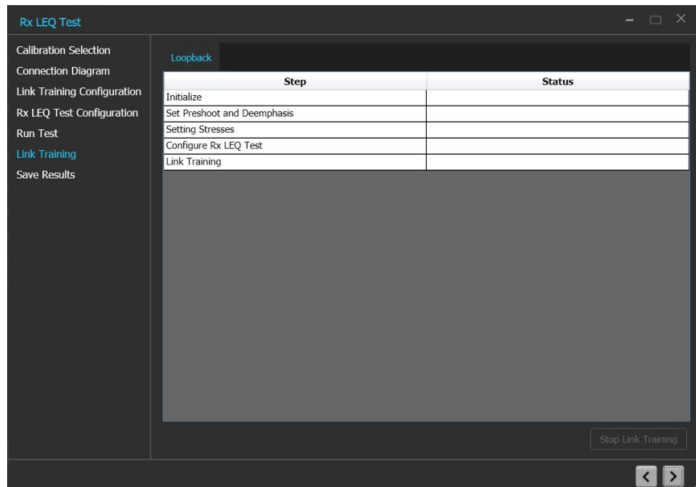
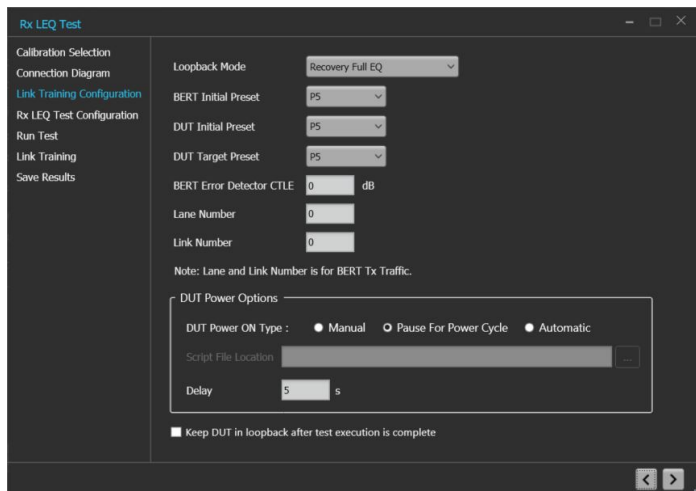
Automated TP2 calibration plots and stressed eye calibration details along with other important parameters like pattern type, scope and BERT settings and regression line slopes and intercept for reference.

6. Eye height 15 +/- 1.5 mV [Gen5 & Gen4] and

- Eye width 9.375 +/- 0.5ps [Gen5]
- Eye width 18.75 +/- 0.55ps [Gen4]

## Link training

Prior to receiver testing, the device-under-test (DUT) must be placed into loopback, where the data digitized at the Rx latch is re-transmitted by the corresponding Tx giving visibility into a possible bit or burst errors. Entering the loopback test mode requires a complex dance through the Link Training Status State Machine (LTSSM) between the BERT and DUT. The Tektronix PCI Express Receiver Test Suite automates this sequence allowing loopback through configuration (short path) and loopback through recovery (full training of the link Tx & Rx) for different levels of receiver testing. Relevant parameters are exposed to allow user control over this process without unnecessary complexity.

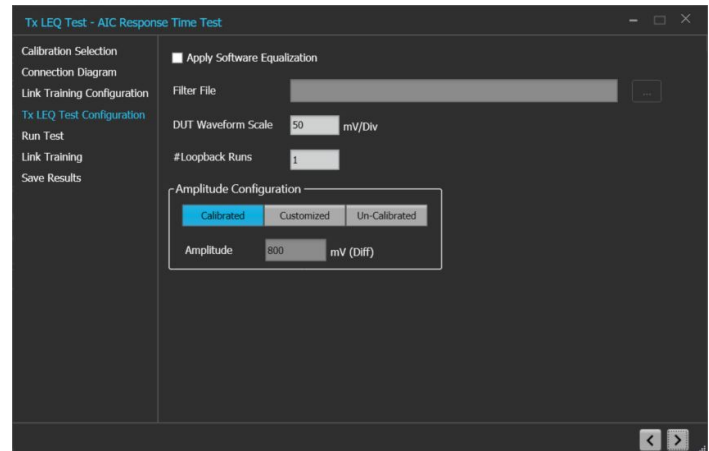


Flexible link training and loopback control

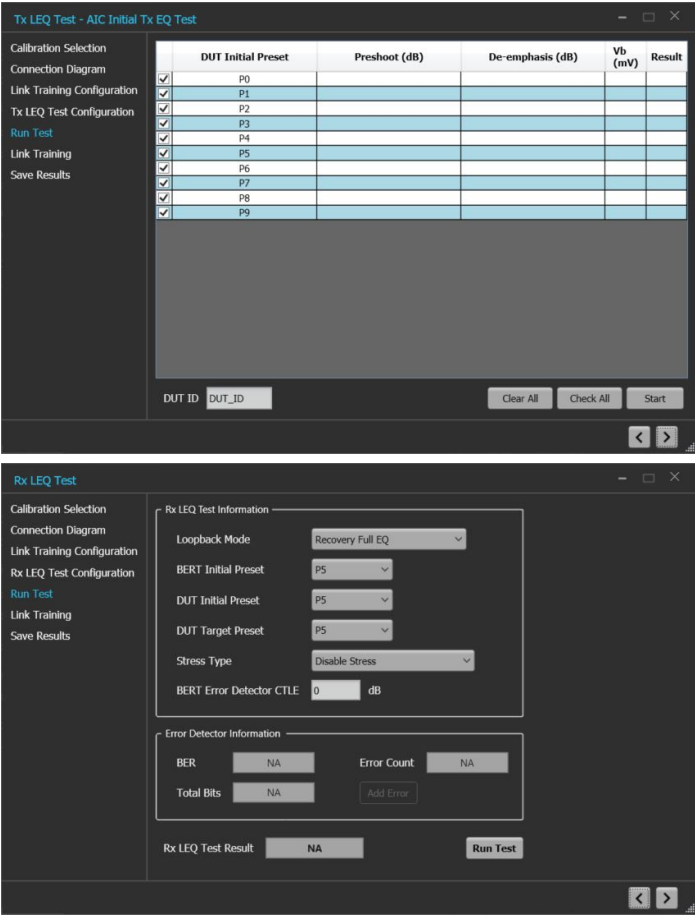
## Receiver and transmitter link equalization testing

PCI Express compliance at 32 GT/s & 16 GT/s requires performing a Receiver Link Equalization test (checking analog Rx performance with a stressed signal after full link training) and a Transmitter Link Equalization test (ensuring key digital timing limits are achieved when an Rx makes Tx change requests to its link partner).

The Tektronix PCI Express Receiver Test Suite controls the BERT and RT Oscilloscope during these required tests to provide efficient test results with minimal overhead and control only where needed.



Tx-LEQ and Rx-LEQ test configuration



Tx-LEQ and Rx-LEQ execution page

Tektronix									
CEM Receiver Compliance Test Report									
AIC LEQ Response Time Test Results									
Test Details									
Unique ID	TxLEQResponse_Run2								
Date/Time	11 December 2020, 1:06 PM								
Generated By	SQE								
Additional Comments									
NA									
Test Equipment									
BERT	ANRITSU, MP1900A, 6261788378								
BERT FW Version	4.09.41								
Rx Test SW Version	6.0.1.142								
RT Scope	TEKTRONIX, DPO77002SX, B321456								
RT Scope FW Version	10.12.0 Build 1								
Test Results									
DUT Initial Preset	Target Preset/Coeff	Preshoot (dB)	De-Emph (dB)	Vb (mV) (Informative)	Electrical Response Time (ns)	Protocol Response Time (ns) (Informative)	DUT Reported Coefficients	Result	
P4	P0	Preset	0.000	-5.95	206.4	55.49	166.6	(0.47,16)	Pass
P4		Coeff	0.000	-5.96	206.4	85.55	143.4	-	Pass
P4	P1	Preset	0.000	-3.54	272.7	97.94	155.2	(0.52,11)	Pass
P4		Coeff	0.000	-3.56	272.1	89.05	161.1	-	Pass
P4	P2	Preset	0.000	-4.37	247.7	62.48	165.4	(0.50,13)	Pass
P4		Coeff	0.000	-4.39	247.2	82.64	151.9	-	Pass
P7	P3	Preset	0.000	-2.38	311.6	119.0	161.6	(0.55,8)	Pass
P7		Coeff	0.000	-2.38	311.4	97.28	146.3	-	Pass
P7	P4	Preset	0.000	0.000	409.9	107.7	154.2	(0.63,0)	Pass
P7		Coeff	0.000	0.000	410.1	98.04	144.7	-	Pass
P7	P5	Preset	1.708	0.000	336.7	121.2	155.6	(6.57,0)	Pass
P7		Coeff	1.712	0.000	336.7	99.07	156.0	-	Pass
P7	P6	Preset	2.380	0.000	311.6	110.6	164.6	(8.55,0)	Pass
P7		Coeff	2.396	0.000	311.2	106.0	148.4	-	Pass
P4	P7	Preset	3.130	-5.79	172.7	95.89	166.6	(7.45,11)	Pass
P4		Coeff	3.094	-5.77	173.1	58.44	154.9	-	Pass
P4	P8	Preset	3.694	-3.69	203.6	96.18	162.6	(8.47,8)	Pass
P4		Coeff	3.725	-3.71	202.8	93.49	152.7	-	Pass
P7	P9	Preset	3.540	0.000	272.7	117.5	158.6	(11.52,0)	Pass
P7		Coeff	3.551	0.000	272.4	99.82	149.7	-	Pass

Tx-LEQ AIC Response time test results

<b>Tektronix</b> <b>PCIe5.0 CEM Receiver Compliance Test Report</b> <b>System Rx LEQ Test Results</b>	
Test Details	
Unique ID	RxLEQ_Pattern
Date/Time	19 October 2020, 3:10 AM
Generated By	SQE
Additional Comments	
ClockPattern	
Test Equipment	
BERT	ANRTSU, MP1900A, 6261788378
BERT FW Version	4.03.13
Rx Test SW Version	6.0.1.62
Calibration Summary	
<b>TP2 Calibration</b>	Unique ID: [Example_TP2_AIC_Calibration]
	Full Channel Loss: 36 dB
	Status: Converged
	Final Calibrated EW: 9.375 ps (8.875 ps ≤ Target EW ≤ 9.875 ps)
	Final Calibrated EH: 15.5 mV (13.5 mV ≤ Target EH ≤ 16.5 mV)
	Final SJ Stress Level: 3.125 ps (1 ps ≤ SJ Sweep ≤ 5 ps)
	Final DMI Stress Level: 10 mV (5 mV ≤ DMI Sweep ≤ 30 mV)
	Final Amplitude Level: 800 mV (Differential)
	Final CMI Stress Level: 150.0 mV
<b>TP1 Calibration</b>	Unique ID: [Example_TP1_Calibration]
	Differential Amplitude: 800.0 mV
	SJ Setting: 0.1 UI p-p @ 100 MHz (Nominal SJ 3.125 ps / 0.1 UI p-p)
	RJ Setting: 0.16 UI p-p (Nominal RJ 0.5 ps RMS / 0.016 UI p-p)
Test Configuration	
<b>Rx LEQ Test</b>	Loopback Type: Recovery Full EQ
	Link Training Status: Successful
	BERT Initial Preset: P6
	DUT Initial Preset: P9
	DUT Target Preset: P9
	Link #: 0, Lane #: 0
	CTLE @ ED: 0 dB
	BERT Measurement Pattern: RxLEQ_Pattern
	Error Limit: 1
	Test Duration: 125 s
	Test Confidence: 26.42% at 0E+00 Bits
	Stress Configuration: Un-calibrated
	Stress Type: Apply Stress
	RJ: 0.03 UI
	SJ: 0.030 UI
	DMI: 2.00 mV
	CMI: 2.00 mV
	Amplitude: 800.0 mV
Rx LEQ Test Results	
Status	PASS
BER	0.0000E-11
Error Count	0
Initial BERT Preset	P6
Final BERT Preset	P5
Final BERT Coefficients	(2, 22, 0)

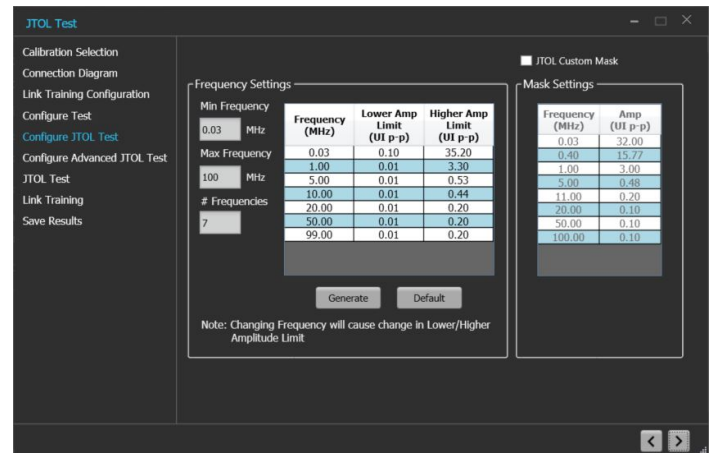
AIC Rx LEQ test results

## Remote control protocol

The test software can be operated remotely through ASCII commands sent through TCP/IP, giving engineers further flexibility in designing “Beyond Compliance” tests.

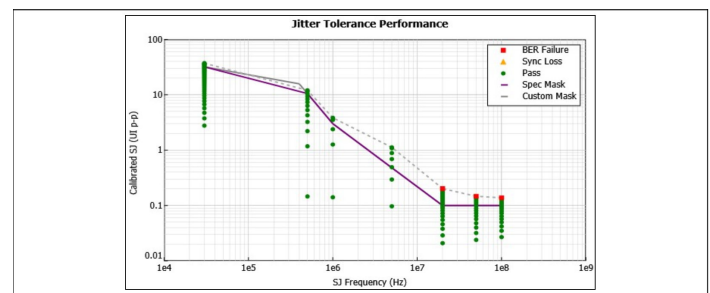
## Jitter Tolerance (JTOL) test

Jitter tolerance (JTOL) testing requires sweeping numerous calibrated SJ tones from low to high amplitude to see how the receiver-under-test CDR tracks the stress (typically in the presence of other noise & jitter sources). Custom JTOL pass/fail masks can be configured while testing with different search algorithms (upward linear, logarithmic, etc. ...). The Tektronix PCI Express Receiver Test Suite allows engineers minimal setup with quick and descriptive test reports.



JTOL test configuration settings

Both the custom mask and the specification mask are provided in the JTOL test to have a better understanding of the DUT performance, especially at the design stage. The Receiver solution performs an automatic back channel equalization and sampling point optimization ensures to ensure the best conditions for the DUT transmitted data traffic to be accurately comprehended at the BERT receiver to ensure the correct determination of BER performance.



JTOL test result with specification

JTOL Test

Calibration Selection

Connection Diagram

Link Training Configuration

Configure Test

Configure JTOL Test

Configure Advanced JTOL Test

JTOL Test

Link Training

Save Results

BER Settings

BER 1 E- 12Error Limit 1

Test Length

Duration 31.25 sConfidence 26.424 % at 1E+12 Bits

Stress Configuration

CalibratedCustomizedUn-Calibrated

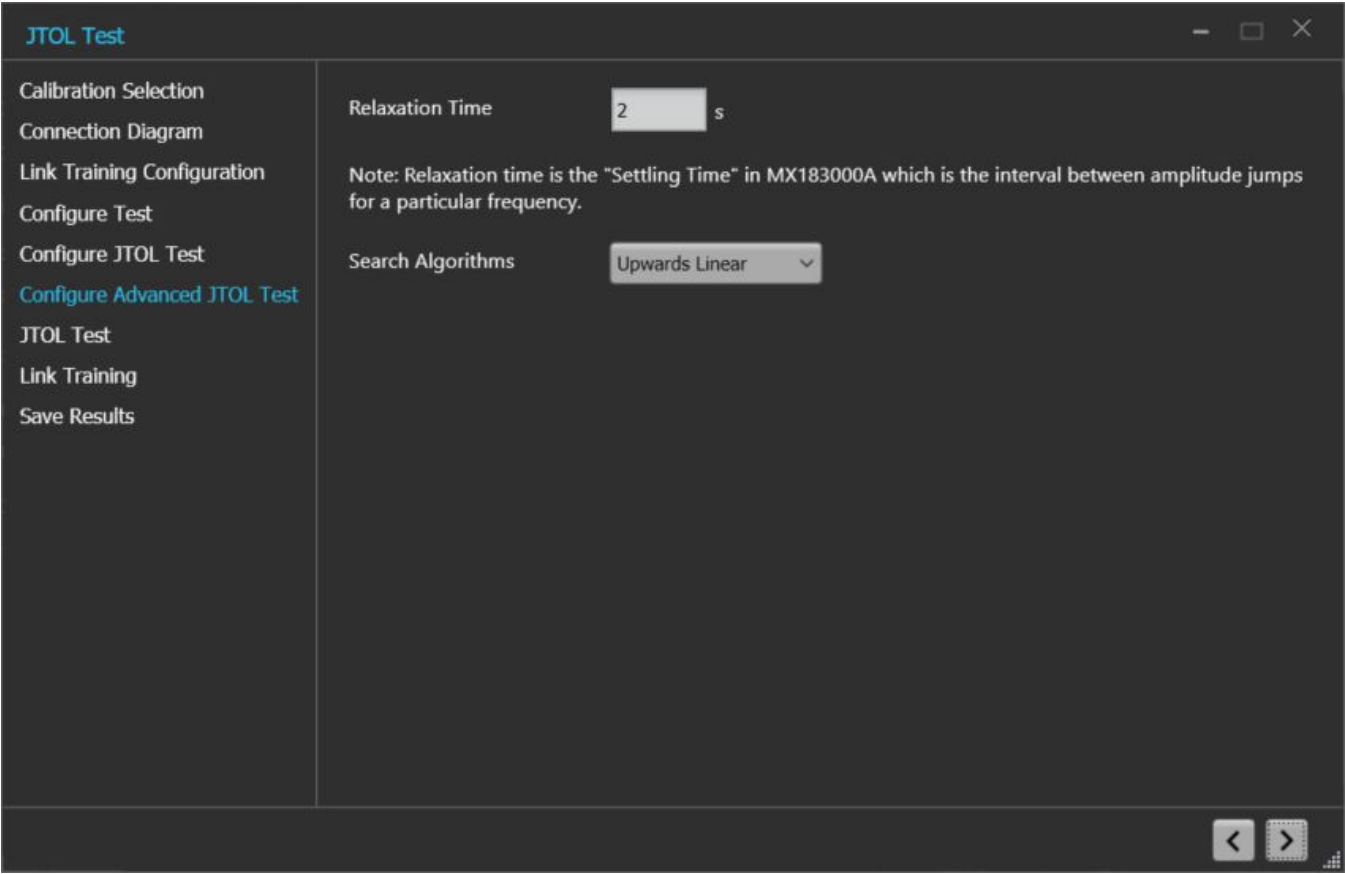
CMI 150 mVRJ 0.5 ps (RMS)

DMI 27.5 mVSJ 3.625 ps

Amplitude 800 mV (Diff)

BER Measurement Pattern Compliance

Error detector and stress settings for JTOL



Different margin search algorithm settings for JTOL test

## Ordering information

### PCIe Gen5 Base and CEM Software Options

Table 1: Models - SX >= 50 GHz DPS + DPO

Item	Description	Type
RXSW-NL1-PCIE5	License; PCI Gen 5 Rx CEM and BASE automation software for TEK scopes and Anritsu BERT; Node-Locked 1-Year Subscription	Software
RXSW-NLP-PCIE5	License; PCI Gen 5 Rx CEM and BASE automation software for TEK scopes and Anritsu BERT; Node-Locked Perpetual	Software
RXSW-FL1-PCIE5	License; PCI Gen 5 Rx CEM and BASE automation software for TEK scopes and Anritsu BERT; Floating 1-Year Subscription	Software
RXSW-FLP-PCIE5	License; PCI Gen 5 Rx CEM and BASE automation software for TEK scopes and Anritsu BERT; Floating Perpetual	Software

### PCIe Gen5 Pre-compliance Fixture Options

Item	Description	Type
TF-PCIE5-CEM-X16	PCIe Gen5 X1/X4/X8/X16 Electrical Test Fixture, Supports X1/X4/X8/X16 configuration includes ISS Board, CBB (System Board), CLB X1-X16, CLB X4-X8, 4 MMPX cables, and 4 MMPX to 2.92 mm cables	Fixture
TF-PCIE5-CEM-X1	PCIe Gen5 X1/X16 Electrical Test Fixture, Supports X1/X16 configuration includes ISS Board, CBB (System Board), CLB X1-X16, 4 MMPX cables, and 4 MMPX to 2.92 mm cables	Fixture

### PCIe Gen4 CEM Software Options

Table 2: Models >= 24 GHz and Above (DPO72504DX, DPO73304DX, DPO70KDX)

Item	Description	Type
RXSW-NL1-PCIE4C	License; PCI Gen 4 Rx CEM automation software for TEK scopes and Anritsu BERT; Node-Locked 1-Year Subscription	Software
RXSW-NLP-PCIE4C	License; PCI Gen 4 Rx CEM automation software for TEK scopes and Anritsu BERT; Node-Locked Perpetual	Software
RXSW-FL1-PCIE4C	License; PCI Gen 4 Rx CEM automation software for TEK scopes and Anritsu BERT; Floating 1-Year Subscription	Software
RXSW-FLP-PCIE4C	License; PCI Gen 5 Rx CEM automation software for TEK scopes and Anritsu BERT; Floating Perpetual	Software

**Overall Setup list:****Table 3: PCIe Gen5 Base Rx**

Item	Vendor	Type	R/O	Qty	Description	Notes
DPS75004SX	Tektronix	Equipment	Required	1	Dual-Stack 50 GHz Sx Scope	50 G or better <sup>1</sup>
DPO7RFBK2	Tektronix	Tek accessory	Required	2	Attenuator kit	Attenuator kit + DC blocks
103047400	Tektronix	Tek accessory	Required	2	Connector savers (1.85 mm)	1.85 mm scope channel input connection
Anritsu MP1900A <sup>5</sup>	Anritsu	3 <sup>rd</sup> party equipment	Required	1	Bit Error Rate Tester (BERT) <sup>2</sup>	Configuration provided by 3 <sup>rd</sup> party
DJA	Tektronix	Equipment SW option	Required	1	DPOJET advanced option	DPOJET advanced option
SDLA64	Tektronix	Equipment SW option	Required	1	Serial Data Link Analysis (SDLA) Software	Serial Data Link Analysis (SDLA) Software
174-6659-01	Tektronix	Tek accessory	Required	1 pr	Cable; SMA - SMP cable pair	Refclk connection between DUT & BERT
PMCABLE1M	Swiftbridge	Tek accessory	Required	2 pr	Cable; 2.92-to-2.92 mm, Straight, 1.5 ps phase-matched, 40 GHz	Equipment connections to relca channel & DUT
Gen5 Base Test Fixture Set	PCI-SIG	Test fixtures	Required	1	Gen 5 Base Rev3 Test Fixtures <sup>3</sup>	Rev3 is Meg6 material with MMPX connectors <sup>4</sup>
RXSW-XXX-PCI5	Tektronix	SW option	Required	1	PCIe Gen5 Receiver Software	Select from Node locked Perpetual /1 year subscription

**Table 4: PCIe Gen5 CEM LEQ**

Item	Vendor	Type	R/O	Qty	Description	Notes
DPS75004SX	Tektronix	Equipment	Required	1	Dual Stack 50 GHz Sx scope	50 G or better <sup>1</sup>
DPO7RFBK2	Tektronix	Tek accessory	Required	2	Attenuator kit	Attenuator kit + DC blocks
103047400	Tektronix	Tek accessory	Required	2	Connector savers (1.85 mm)	1.85 mm scope channel input connection
Anritsu MP1900A <sup>5</sup>	Anritsu	3 <sup>rd</sup> party equipment	Required	1	Bit Error Rate Tester (BERT) <sup>2</sup>	Configuration provided by 3 <sup>rd</sup> party
DJA	Tektronix	Equipment SW option	Required	1	DPOJET advanced option	DPOJET advanced option
SDLA64	Tektronix	Equipment SW option	Required	1	Serial Data Link Analysis (SDLA) software	Serial Data Link Analysis (SDLA) software
PMCABLE1M	Tektronix	Tek accessory	Required	2 pr	Cable; 2.92-to-2.92 mm, straight, 1.5 ps phase-matched, 40 GHz	Equipment connection to fixtures and DUT

Table continued...

<sup>1</sup> If ATI channels will be used for refclk measurements they will need Option Key 4 (50 XL)<sup>2</sup> Cables required for connection between BERT modules shall be included for the 3<sup>rd</sup> party vendor<sup>3</sup> Gen5 BaseTest Fixtures are not backwards compatible for Gen3 & Gen4 Base Rx<sup>4</sup> It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit<sup>5</sup> Configuration for BERT provided by 3<sup>rd</sup> party vendor

Item	Vendor	Type	R/O	Qty	Description	Notes
174-6663-01	Tektronix	Tek accessory	Required	1 pr	Cable; 2.92-to-2.92 mm, straight, 1.5 ps phase-matched, 500 mm, 40 GHz	Signal connection between scope and BERT for Tx LEQ
174-6666-01	Tektronix	Tek accessory	Required	2 pr	Cable; SMA-to-SMA, Right Angle-Right Angle, 500 mm	Signal connection between scope and BERT for Tx LEQ & Trigger
174-6659-01	Tektronix	Tek accessory	Required	1 pr	Cable; SMA - SMP cable pair	Refclk connection between DUT & BERT
MPR40M	Fairview Microwave	3 <sup>rd</sup> party	Required	2	Power divider	Split signal from DUT Tx to the scope and Error Detector
C7035	CentricRF	3 <sup>rd</sup> party	Optional	4	Right Angle Male-Female 2.92 mm adapter	Cable management
C7049	CentricRF	3 <sup>rd</sup> party	Required	3	2.92 mm Male to 2.92 mm Male adaptor	Power divider output to scope input
Redriver	3 <sup>rd</sup> party	3 <sup>rd</sup> party equipment	Optional	1	Active Gen5 Redriver (back channel equalization) <sup>6</sup>	High loss back channels (DUT Tx to Error Detector) may need EQ
PowerUSB - Basic	PowerUSB	3 <sup>rd</sup> party	Optional	1	Power USB Power Strip	Automate DUT power cycle
TF-PCIE5-CEM-X16	Tektronix or PCI-SIG	Test fixtures	Required	1	Gen 5 CEM Test fixtures <sup>7</sup>	Tektronix fixtures are not officially approved by PCI-SIG <sup>4</sup>
RXSW-XXX-PCI5	Tektronix	SW option	Required	1	PCIe Gen5 Receiver software	Select from Node locked Perpetual /1 year subscription

Table 5: PCIe Gen4 CEM

Equipment	Details	Qty	Vender
Bit Error Rate Tester (BERT)	Part Number provided by 3 <sup>rd</sup> Party	1	Anritsu
Real Time Oscilloscope > 24 GHz	DPO72504DX, DPO73304DX, DPO70KDX	1	Tektronix
DPOJET Advanced option	DJA (Scope SW option)	1	Tektronix
1-m Cable pair (2.92 mm SMA Male - SMP )	174-6659-01 (DUT-BERT Ref clock)	1 pair	Tektronix
1 m Cable (2.92 mm M-M, Straight, 1.5 ps phase - matched, 40 GHz)	PMCABLE1M (Equipment connection to fixtures and DUT)	2 pairs	Tektronix
0.5 m Cable (2.92 mm M-M, Straight, 1.5 ps phase - matched, 40 GHz)	174-6663-01 (Signal Connection between scope and BERT for Tx LEQ)	1 pair	Tektronix
0.5 m Cable (SMA M-M, Right Angle - Right Angle)	174-6666-01 (Connection between scope and BERT for Tx LEQ & Trigger)	2 pairs	Tektronix
Power Divider (2 way 2.92mm F-F-M)	MPR40M (Split signal from DUT Tx to the scope and Error Detector)	1 pair	Fairview Microwave
Power USB Power Strip	PowerUSB – Basic (Automate DUT power cycle)		PowerUSB
SMP 50 Ohm Terminator	50 ohms (Female)	**	Any
ATX Power Supply for System Board Power	Any	1	Any
Gen 4 CEM Test Fixtures	PCI-SIG	1	PCI-SIG

Table continued...

<sup>6</sup> Another matched pair of cables (e.g. 174-6663-xx) will be required if the Active redriver is used for Rx or Tx LEQ<sup>7</sup> Gen5 CEM Test Fixtures are not backwards compatible for Gen3 & Gen4 CEM Rx

Equipment	Details	Qty	Vender
Equalizer	BSXPCI4EQ	2	Tektronix
<b>Optional Items</b>			
Right Angle M-F 2.92 mm adapter	C7035 (Cable management)	4	CentricRF
Active Gen4 Redriver (Back channel equalization)	-	1	Texas Instrument

#### Host system software requirements

Microsoft Windows 10

CE Marking Not Applicable.

Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.



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