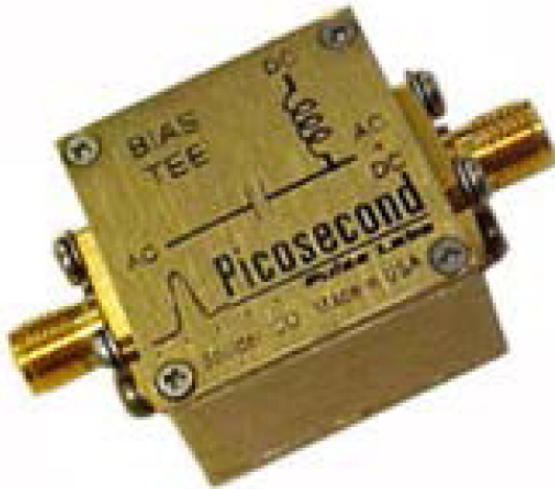


20 GHz Bias Tee

PSPL5545 Datasheet



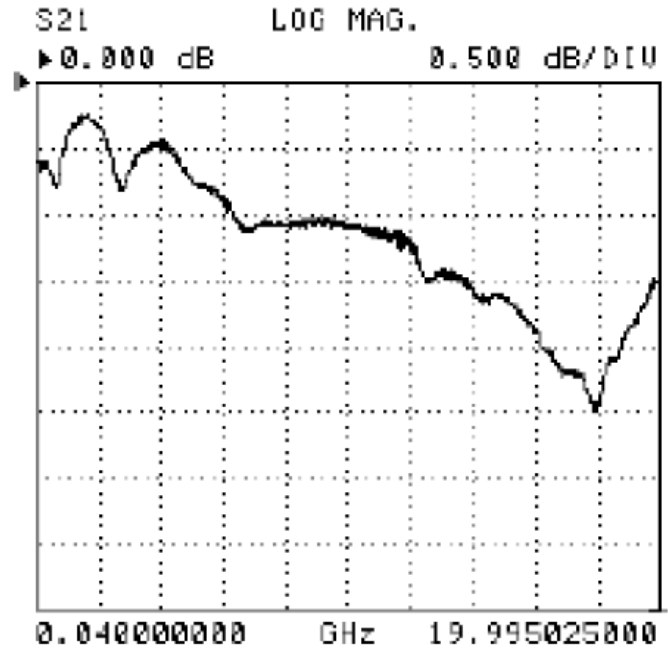
The PSPL5545 Bias Tee and DC Block is a broadband, coaxial bias insertion tee and DC blocking capacitor. It passes fast rise pulses with a minimum of waveform distortion. The rise time is 12 ps. The frequency response is flat over many decades, and the -3 dB bandwidth extends from 65 kHz to 20 GHz.

Key performance specifications

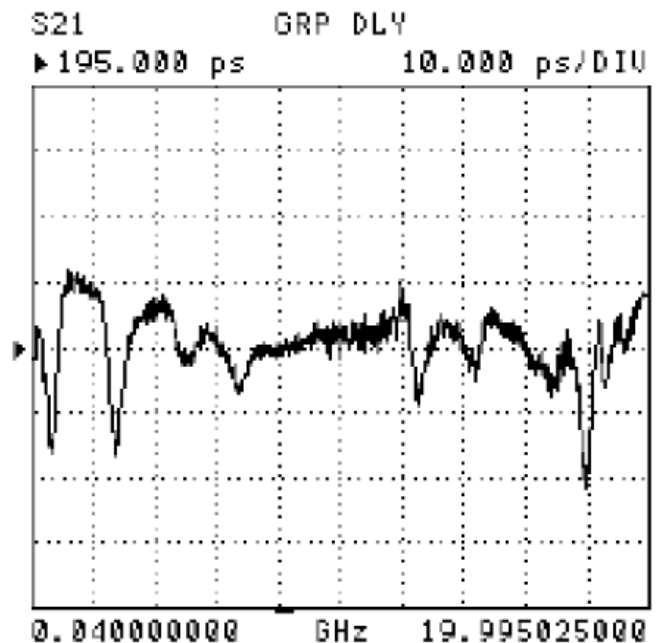
- 65 kHz to 20 GHz
- 12 ps rise time
- 100 V, 500 mA

Typical performance

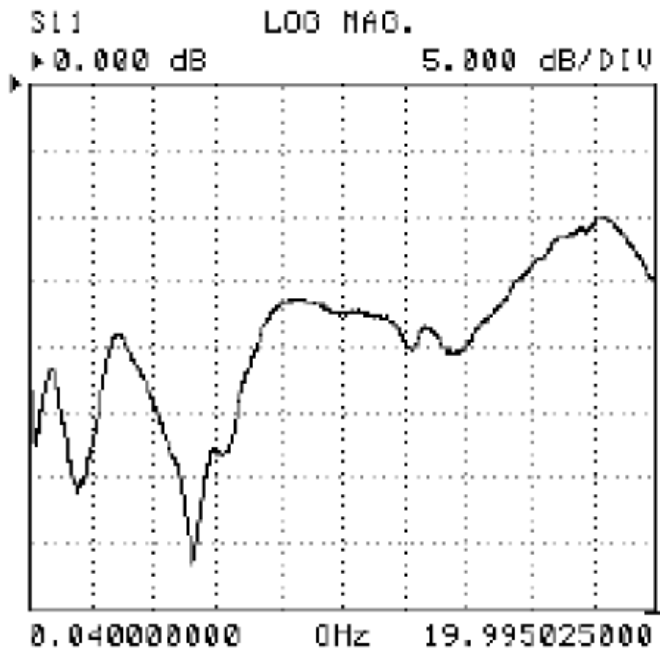
The following figure shows the S21 insertion loss at 0.5 dB/div.



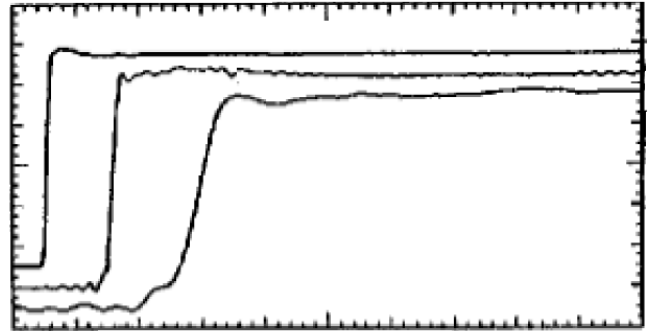
The following figure shows the S21 group delay at 10 ps/div.



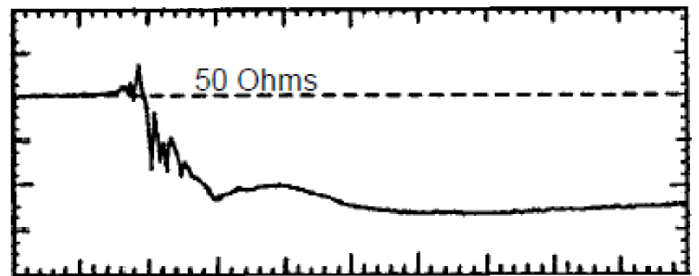
The following figure shows the S11 return loss at 5 dB/div.



The following figures show the linear sweep from 40 MHz to 20 GHz at 2 GHz/div.



500 ps/div, 100 ps/div, and 20 ps/div, 10 ps Step Response

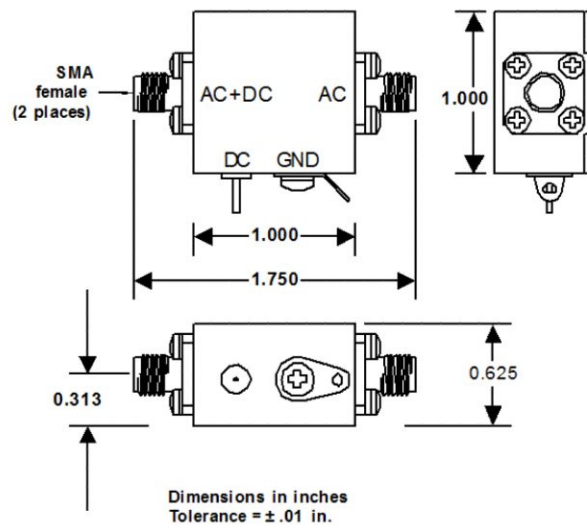


2.5% rho/div and 500 ps/div, 35 ps TDR

Specifications

Parameter	Symbol	Units	Minimum	Typical	Maximum	Comments
Impedance	Z	ohms		50		
Upper 3 dB frequency	$f_{c,h}$	GHz		$>20^1$		
Lower 3 dB frequency	$f_{c,l}$	kHz		65		
Rise time	t_r	ps		12		10 – 90%
Insertion loss	S_{21}	dB		0.7 1 1.5		$f < 5$ GHz $f < 12$ GHz
Input (AC) Return Loss	S_{11}	dB		23 >20 >12		$f = 100$ MHz $f < 6$ GHz $f < 14$ GHz
Refl. Coefficient (35 ps TDR)	Γ	%		-7		$t > 1$ ns
DC voltage	V	V			50	
DC current	I	mA			500	
Capacitance	C	μ F		0.03		$\pm 20\%$
Inductance	L	μ H		340		$\pm 20\%$
Resistance	R	ohms		1.1		
RF power	P	W			2	Average power
Isolation	S_{13}	dB		>25		
DC path bandwidth	$f_{c,DC}$	kHz		37		
Delay	T_d	ps		195		
RF Connectors	SMA jacks (f)					
DC Connector	Solder pin					
Warranty	One year					

Mechanical dimensions



¹ Not recommended for freq. domain applications above 15 GHz due to higher order mode resonances.

Ordering information

Models

PSPL5545

BIAS TEE, 20 GHz, 50 V

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