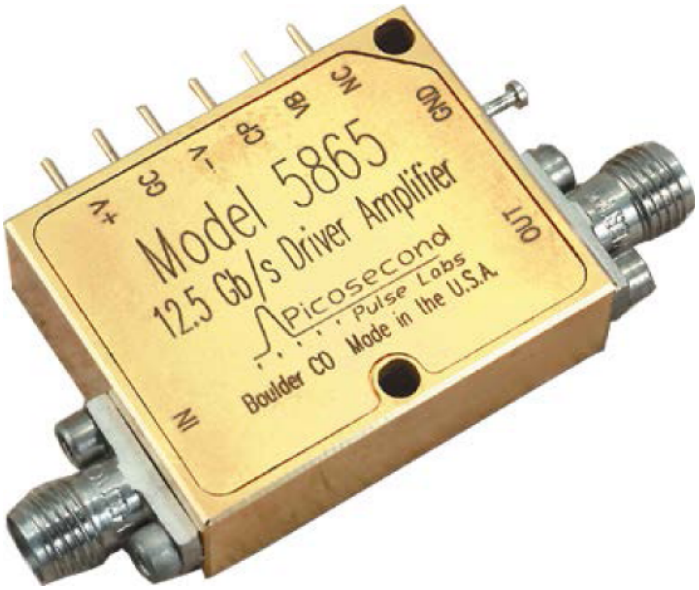
12.5 Gb/s Driver Amplifier

PSPL5865 Datasheet

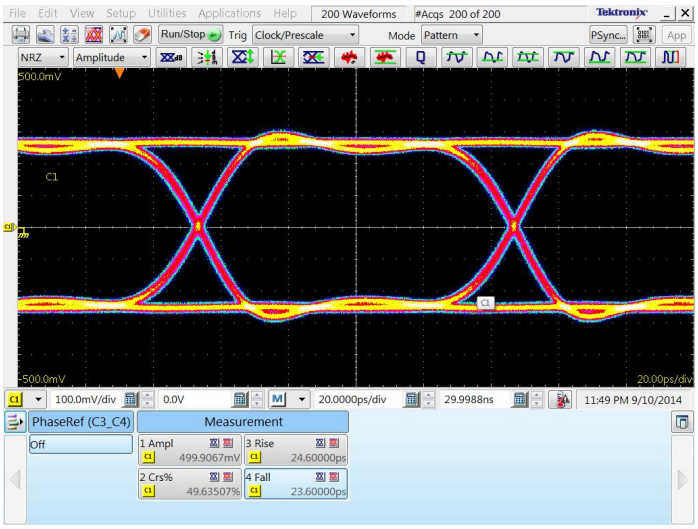


The Model PSPL5865 Driver Amplifier is intended for use driving Lithium Niobate modulators or as a linear amplifier. This device includes internal temperature compensation for excellent output stability over temperature, and exhibits both high output and low power dissipation. It also incorporates internal sequencing circuitry, making it insensitive to power supply application sequence.

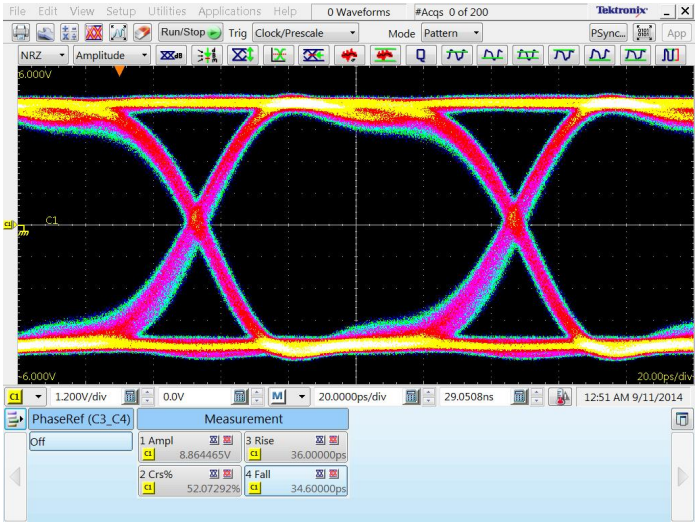
Key performance specifications

- 7.5 V output amplitude 12.5 Gb/s Modulator Driver
- Linear amplifier with 26 dB gain
- 30 kHz to 12 GHz bandwidth
- Temperature compensated design for output stability
- Includes bias network, crossing point control & adjustable output voltage

Typical 10.66 Gb/s eye measurements



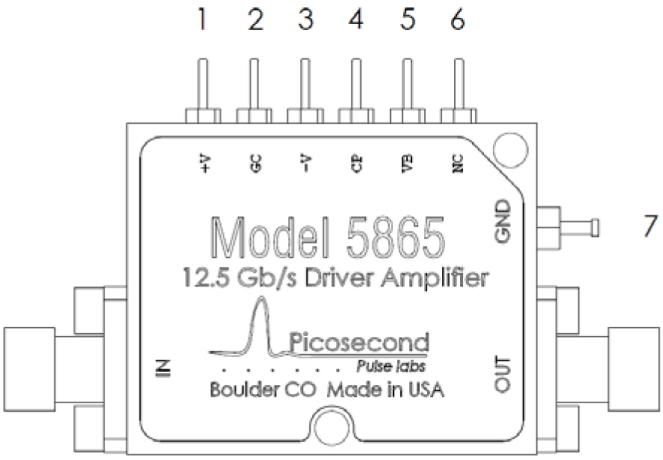
Input from Tektronix PPG1601, PRBS=2^{23}–1, 500 mv



Output amplitude > 8 V

Instructions for use

The PSPL5865 12.5 Gb/s modulator driver can be operated using only three of the available 7 pins. The DC pins required for operation are 1, 3, and 7. The connectors and pins are shown in the following diagram and table. **Warning:** To prevent damage to the PSPL5865, a ground connection is required at pin 7 before applying voltage to the PSPL5865.



Pin #	Pin Lable	Description
	IN	SMA, signal input, $V_{amp} \leq$ 1.5 V (damage threshold)
1	+V	Positive DC voltage supply, 8 V () [1] [2]
2	GC	V_{gc}, Variable output control, -15 V$\leq V_{gc} \leq$ 0 V [3]
3	-V	Negative DC voltage supply, -5.25 V ≤ V ≤ -4.75 V [4]
4	CP	Crossing point adjust, -5 V ≤ V_{cp} 5 V [5]
5	VB	DC Voltage bias, -17 ≤ VB +33 [6]
6	NC	No connection / Not used
7	GND	Ground connection
	OUT	SMA, signal output

1 At 8V, approximately 2.3 W is dissipated.

2 No power sequencing is necessary. Voltages may be applied in any order **after** ground is applied.

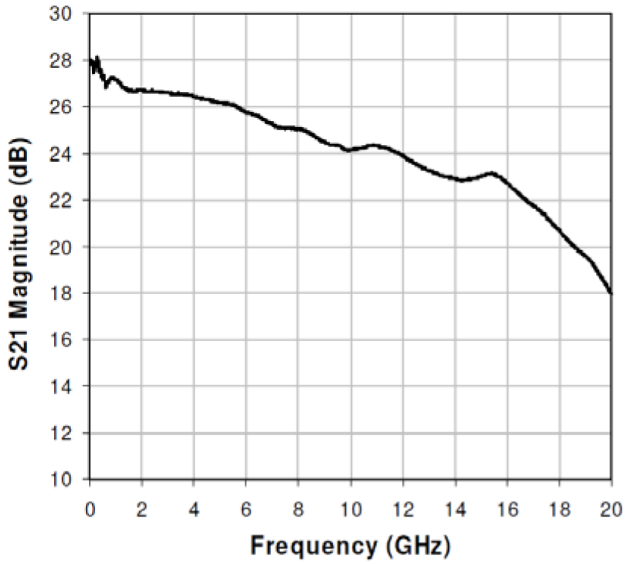
3 Output Control: With VGC at 0 V, or left floating (disconnected), the driver will provide maximum gain and maximum output voltage. The user may decrease VGC to decrease the RF signal gain when the driver is operating in the linear regime, or to reduce the output voltage level when the driver is operated in saturation (this will also reduce the power dissipated).

4 No power sequencing is necessary. Voltages can be applied in any order after ground is applied.

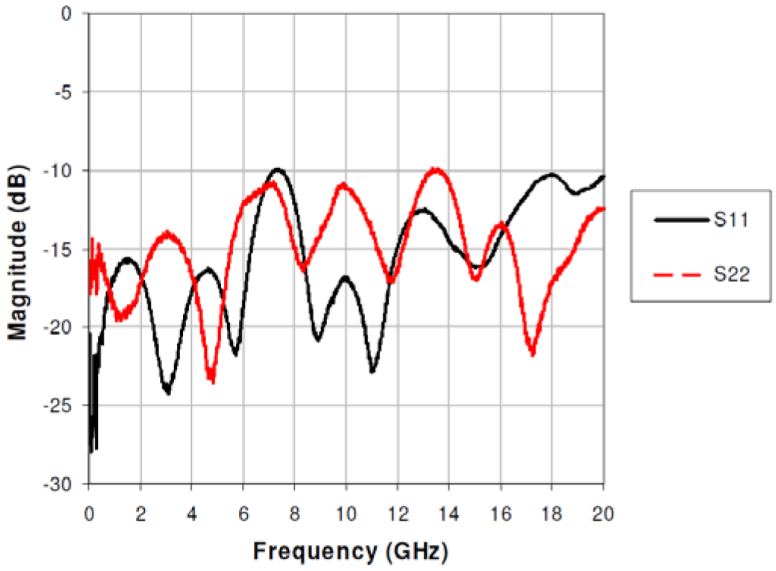
5 The crossing point may vary until unit achieves thermal equilibrium. VCP > 0 V will lower the output crossing point and increase power dissipation. Care must be taken to ensure that the positive supply current does not exceed 320 mA.

6 Voltage Bias: The VB pin allows the user to apply a low current (less than 3.5 mA) DC offset to the Signal Output for biasing electro-optic modulators through a 2.5 kΩ resistor.

Typical performance

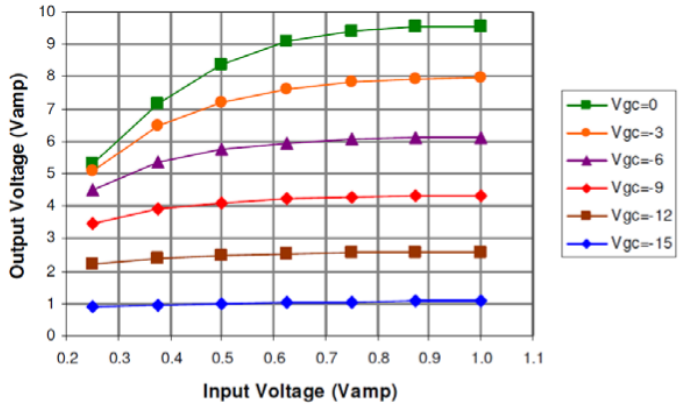


Typical Small Signal S_{21}
(measured at –20 dBm input power)

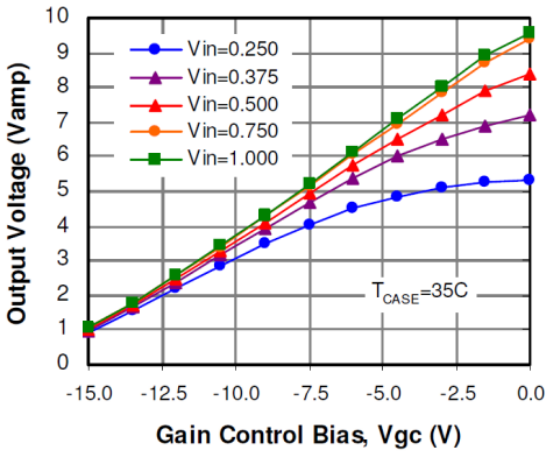


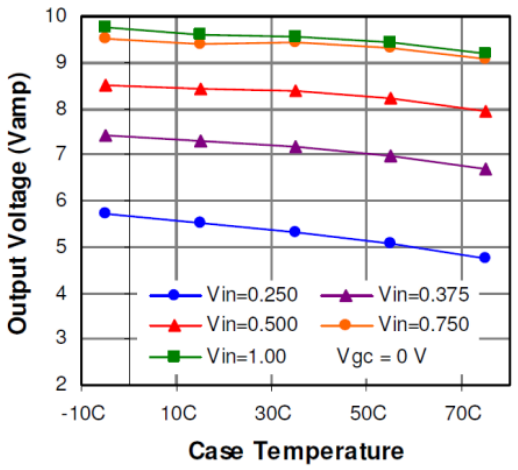
Typical Small Signal S_{11} and S_{22}
(measured at –20 dBm input power)

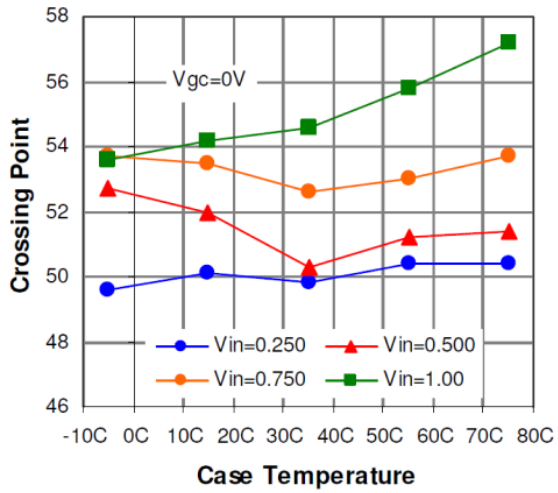
Typical performance plots

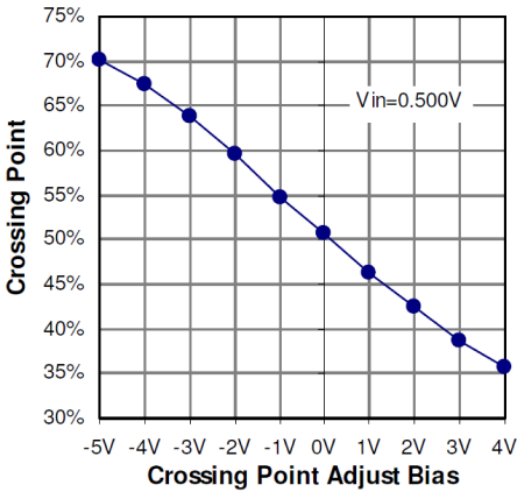


Typical Output Voltage versus Input Voltage
(Gain Control Bias = Vgc, T_{CASE} = 35C)









Specifications

Parameter	Symbol	Units	Minimum	Typical	Maximum	Comments
Impedance	Z	Ohms		50		
Upper 3 dB freq.	$f_{c,h}$	GHz		12		Relative to gain at 2 GHz
Lower 3 dB freq.	$f_{c,l}$	kHz		30		Relative to gain at 2 GHz
Small signal gain	S_{21}	dB		26.5		Measured at 2 GHz
Max Power Out (-1 dB gain comp)	$P_{1\ dB}$	dBm		23.5		Measured at 2 GHz
Output Eye Voltage with VGC = 0 V	V_{OUT}	V_{amp}	7.0	7.5		V_{in} = 0.5 V_{amp}, 12.5 Gb/s PRBS
Output Eye Voltage with VGC = -15 V	V_{OUT}	V_{amp}		1.0	2.0	V_{in} = 0.5 V_{amp}, 12.5 Gb/s PRBS
Return Loss, Input and Output	S_{11} S_{22}	dB		-14 -11	-12 -9	50 MHz < f < 5 GHz 5 GHz ≤ f < 12 GHz
Rise Time	t_r	ps		22	28	20-80%, V_{in} = 0.5 V_{amp}, 12.5 Gb/s PRBS
Fall Time	t_f	ps		24	30	
Additive Jitter RMS Peak-to-Peak		 ps ps_{pp}		 0.7 4	 2.0 8	V_{in} = 0.5 V_{amp}, 12.5 Gb/s PRBS, measured at crossing point
Overshoot		%		5		12.5 Gb/s PRBS
Undershoot		%		5		12.5 Gb/s PRBS
Eff. Input RMS Noise Voltage		µV rms		120		
Noise Figure	NF	dB		5.75	6.5	f = 1 GHz
Output Eye Voltage Variation	Δ V_{OUT}	%		+/-3	+/-5	V_{gc} = 0 V, V_{in} = 0.5 V $_{amp}$, T_{CASE} = -5 to 75 °C
Crossing Point Adjust		%	+/- 15	+/- 20		+/- 5 V input at V_{cp}, V_{in} = 0.5 V_{amp}
Crossing Point Variation		%		+/- 1.0	+/- 2.0	V_{in} = 0.5 V_{amp}, 12.5 Gb/s PRBS, T_{CASE} = -5 to 75 °C
Polarity	Non-Inverting					
Coupling	AC, input and output					
RF Connectors	SMA jacks (f)					
DC Connector	Solder pins					
Voltage Supply (+)	$+V_{DC}$	V	8	8	8.25	
Voltage Supply (-)	$-V_{DC}$	V	-5.25	-5	-4.75	
Supply Current (+)	$+I_{DC}$	mA		275		V_{out} = 7.5 V_{amp} [7]
Supply Current (-)	$-I_{DC}$	mA		20		
Power Dissipation	P_{diss}	W		2.3	2.6	V_{out} = 7.5 V_{amp} [8]
Max Allowed Input		V_{amp}			1.5	Input damage threshold
Output Voltage Bias	V_{bias}	V_{DC}	-17	0	33	No connection required [9]
Gain Control Bias	V_{gc}	V_{DC}	-15	0	0	No connection required

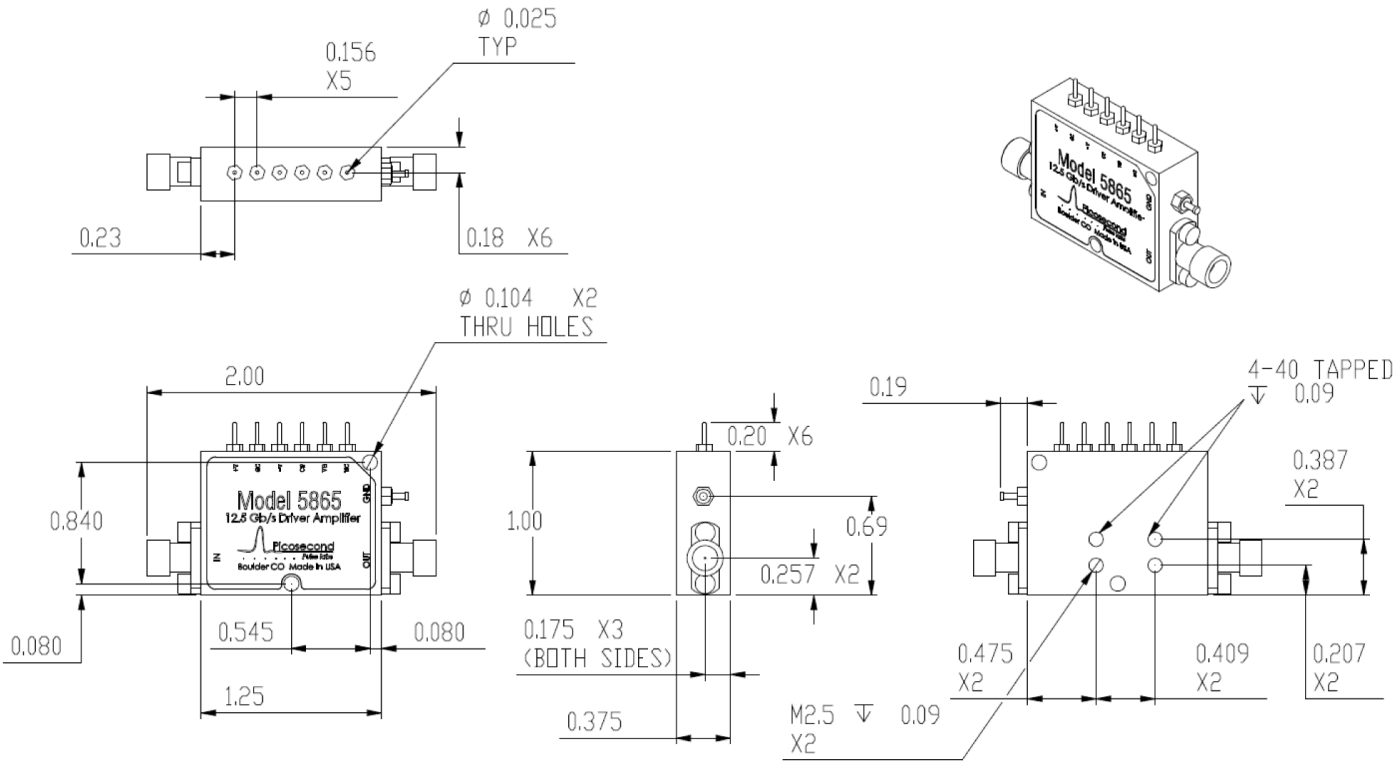
7 The PSPL5865 may be damaged by excessive heat that is produced when driving low duty cycle positive pulses. To ensure the amplifier will not be damaged by overheating, it is recommended the positive supply voltage has its current limit set to 320 mA.

8 Vgc may be utilized to lower the output level and power dissipated. Vcp > 0 V will lower the crossing point and increase the power dissipated.

9 A 2.5 kΩ resistor is connected to the output from the Vbias pin for adding a low current (≤ 3.5 mA) DC bias

Parameter	Symbol	Units	Minimum	Typical	Maximum	Comments
Crossing Point Bias	V_{cp}	V_{DC}	-5	0	5	No connection required
Operating Temp	T_{CASE}	Deg C	-5		75	Case temperature
Storage Temp	T_{stor}	Deg C	-40		125	
Warranty	One Year					

Mechanical dimensions



Ordering information

Models

PSPL5865	Driver Amplifier, 12.5 Gb/s

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