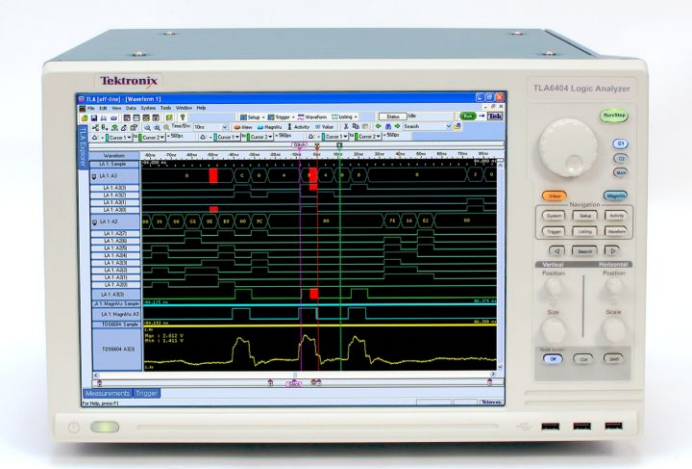
Tektronix Logic Analyzers

TLA6400 Series Datasheet



Tektronix TLA6400 Series logic analyzers provide a significant price-performance breakthrough for digital debug.

Notice to EU customers

This product is not updated to comply with the RoHS 2 Directive 2011/65/EU and will not be shipped to the EU. Customers may be able to purchase products from inventory that were placed on the EU market prior to July 22, 2017 until supplies are depleted. Tektronix is committed to helping you with your solution needs. Please contact your local sales representative for further assistance or to determine if alternative product(s) are available. Tektronix will continue service to the end of worldwide support life.

Features and benefits

- Performance and ease of use to debug, validate, and optimize digital systems
  - 40 ps resolution MagniVu™ Acquisition to accurately see signal relationships in your system
  - State Speed - Sample your fastest synchronous buses with clock rates up to 667 MHz and data rates up to 1333 Mb/s
  - 15 in. display, with optional touch screen to see more of your data and navigate efficiently through your data
  - 4 models with 34/68/102/136 channels and up to 64 Mb record length offer flexible solutions to fit any budget
  - Drag-and-Drop Triggering - Simply drag any one of eight different trigger types from a table to the waveform and the TLA will automatically set up the trigger conditions. Eliminates errors, improves repeatability, and saves time.
  - Drag-and-Drop measurements - Simply drag an icon from the measurement toolbar and drop it on your signal of interest and get a table of results. Saves time, removes complexity, and reduces measurement uncertainty.
- Comprehensive set of signal integrity tools that allow you to quickly isolate, identify, and debug complex signal integrity issues
  - Glitch Trigger and Storage - Allows you to trigger on and highlight potential signal integrity problems. Not only can the TLA6400 Series trigger on the problem, but by highlighting suspected problems in red, you will easily determine which signals you need to investigate further.
  - iCapture -Route the suspected signal to the analog output of the TLA6400 Series using the exclusive Tektronix iCapture feature. This eliminates the need to double-probe with an oscilloscope probe, reducing time to debug.
  - iView - Time-correlated view of both logic analyzer and oscilloscope data to trace the SI problem across the digital and analog domain.

Applications

- Digital hardware validation and debug
- Monitoring, measurement, and optimization of digital hardware performance
- Embedded software integration, debug, and verification

Efficiently debug and validate your digital system at a price you will like!

The affordable TLA6400 Series logic analyzers offer the performance needed to debug, validate, and optimize the functionality of your digital system. The TLA6400 Series provides a comprehensive set of signal integrity debug tools that allow you quickly isolate, identify, and characterize elusive and hard-to-find problems. Add a broad range of support for today's applications, and you have the ideal tool to help you meet all of the debug challenges of today's digital designs.

The TLA6400 Series allows you to effectively validate and debug the functionality of your digital designs:

- Use the patented 25 GHz MagniVu technology to accurately measure timing relationships. The single, integrated acquisition architecture of the TLA6400 Series eliminates the timing skew problems inherent in other logic analyzer architectures.
- Capture buses with clock rates up to 667 MHz and data rates up to 1333 Mb/s.
- Buy the capability you need now and upgrade as your measurement needs grow.
- Quickly isolate events through a simple and intuitive drag-and-drop trigger setup.
- Easily summarize your design's performance with sophisticated drag-and-drop measurements such as frequency, period, pulse width, duty cycle, and edge count.
- View data in a variety of time-correlated formats including waveform, listing, graph, disassembly, source code, or compare.

Oscilloscope integration

The TLA6400 seamlessly integrates with Tektronix oscilloscopes to make it easy to find problems that cross between the digital and analog portions of a design.

Probing

The TLA6400 with iCapture can be used as flexible and convenient probe system for your oscilloscope. It allows you to use one probe for both your logic analyzer and your oscilloscope eliminating the need to double-probe signals. With a single probe, you can view both the digital and analog characteristics of the signal.

You can route up to four analog signals through the TLA6400's 2 GHz analog mux to your oscilloscope and change the signals you are viewing with just a mouse click. This eliminates the need to physically move an oscilloscope probe to make a new measurement

Display and triggering

In addition to integrated probing, iView allows time-correlated logic analyzer and oscilloscope waveforms to be integrated into a single TLA6400 waveform window simplifying viewing and analysis. You can also trigger the oscilloscope from the logic analyzer or have the oscilloscope trigger the logic analyzer.

The connection between the TLA6400 and the oscilloscope consists of two BNC cables for cross triggering and a data connection to transfer data between the instruments. The data connection can be GPIB, USB, or a LAN connection.

This seamless integration not only helps you troubleshoot functional issues in your design, but also helps you find signal integrity problems caused by crosstalk, termination mismatches, ground bounce, and other issues.

Use the TLA6400's glitch trigger to monitor selected signals in your design and trigger when a signal integrity problem is found on any one of these signals. Signals with suspected signal integrity problems can also be tagged allowing you to quickly identify the signals of interest.

The analog nature of the suspected signals can then be routed to an oscilloscope using the exclusive iCapture functionality and viewed in the TLA6400 using iView.

DDR2/DDR3 and LPDDR2 memory validation

A complete DDR2/DDR3 and LPDDR2 protocol debug and validation solution is available for the TLA6400. This tool set consist of everything embedded engineers - even those who are not DDR experts - need to validate and debug the operation of memory sub-systems in their designs.

Support consists of a set of tools designed to provide visibility to all address, data, and control signals and consists of:

- Memory chip and PoP (Package-on-Package) interposers that provide a convenient way of probing embedded DDR memory systems and eliminates the need to design in probe access points. These interposers work with the unique iCapture Analog Mux feature of the TLA6400 to provide a single probing solution for both the logic analyzer and oscilloscope, saving time and minimizing setup complexity.
- Setup software to configure the TLA6400 to accurately sample the DDR signals.
- Protocol decode software that shows all of the DDR transactions as well as providing triggering on DDR events.
- Optional protocol violation software that finds and reports any violation of the JEDEC-defined DDR protocol.

The DDR protocol debug and validation solution supports:

- x4, x8, and x16 DDR2 devices up to speeds of DDR2-1333.
- x4, x8, and x16 DDR3 devices with speeds up to DDR3-1333.
- LPDDR2 PoP devices with speeds up to LPDDR2-1333.

DDR2/DDR3 protocol debug and validation solutions

	DDR2 memory **Up to DDR2-1333 (667 MHz clock) state measurements on Addr/Cmd/Data.** [1]	**DDR3 memory** **Up to DDR3-1333 (667 MHz clock) state measurements on Addr/Cmd/Data.** [1]
x4/x8 Configurations	Requires 68 channel model or higher (Option 1T required for DDR2-800, DDR2-1067, and DDR2-1333)	Requires 68 channel model or higher (Option 1T required for DDR3-800, DDR3-1067, and DDR3-1333)
	Memory Chip Interposer [2]: NEX-DDR2MP60BLASK (socketed) or NEX-DDR2MP60BLA (non-socketed)	Memory Chip Interposer [3]: NEX-DDR3MP78BLASK (socketed) or NEX-DDR3MP78BLA (non-socketed)
	NEX-PRB1XL64 (requires 2) NEX-PRB1XL64 (requires 2)	NEX-PRB1XL64 (requires 2).
	(Optional) Protocol software: NEX-DDR-PROTOCOL	(Optional) Protocol software: NEX-MCATLA-DDR3-SWL
x16 Configurations	Requires 68 channel model or higher (Option 1T required for DDR2-800, DDR2-1067, and DDR2-1333)	Requires 68 channel model or higher (Option 1T required for DDR3-800, DDR3-1067, and DDR3-1333)
	Memory Chip Interposer [2]: NEX-DDR2MP84BLASK (socketed) or NEX-DDR2MP84BLA (non-socketed)	Memory Chip Interposer [3]: NEX-DDR3MP96BLASK (socketed) or NEX-DDR3MP96BLA (non-socketed)
	NEX-PRB1XL64 (requires 2)	NEX-PRB1XL64 (requires 2)
	(Optional) Protocol software: NEX-DDR-PROTOCOL (must be ordered directly from Nexus)	(Optional) Protocol software: NEX-MCATLA-DDR3-SWL

LPDDR2 protocol debug and validation solutions

	LPDDR2 Memory **Up to DDR2-1333 (667 MHz clock) state measurements on Addr/Cmd/Data.** [4]
168 Ball Package on Package (x32 Data Width)	Requires 68 channel model or higher (Option 1T required for LPDDR2-800, LPDDR2-1067, and LPDDR2-1333)
	Memory Chip Interposer: NEX-LP2POP168BLASK [5] (Socketed)
	NEX-PRB1XL64 (requires 2)
	(Optional) Protocol software: NEX-MCATLA-LP2-SWL
216 Ball Package on Package (2x32 Data Width)	Requires 68 channel model or higher (Option 1T required for LPDDR2-800, LPDDR2-1067, and LPDDR2-1333)
	Memory Chip Interposer: NEX-LP2POP216BLASK [5] (Socketed)
	NEX-PRB1XL64 (requires 2)
	(Optional) Protocol software: NEX-MCATLA-LP2-SWL

1 All configurations support simultaneous capture of Read and Write data.

2 DDR2 Memory Chip Interposers include Sample Point Analyzer Tool (SPA), Logic Analyzer configuration files, and DDR Protocol Decoder and Triggering Support.

3 DDR3 Memory Chip Interposers include Sample Point Analyzer Tool (SPA), ICIS Software, Logic Analyzer configuration files, and DDR Protocol Decoder and Triggering Support.

4 All configurations support simultaneous capture of Read and Write data.

5 DDR2 Memory Chip Interposers include Sample Point Analyzer Tool (SPA), Logic Analyzer configuration files, and DDR Protocol Decoder and Triggering Support.

Specifications

All specifications are guaranteed unless noted otherwise. All specifications apply to all models unless noted otherwise.

TLA6400 selection guide

Characteristic	TLA6401	TLA6402	TLA6403	TLA6404
Channels	34	68	102	136
High-speed timing	25 GHz (40 ps) with 128 Kb record length			
Maximum timing sample rate (Half/ Full channel)	3.2 GHz / 1.6 GHz			
Maximum State clock rate	333 MHz (standard) 667 MHz (with Option 1T)			
Maximum State data rate	667 Mb/s (standard) 1333 Mb/s (with Option 1T)			
Maximum record length	2 Mb (standard) 4 Mb (Option 1S) 8 Mb (Option 2S) 16 Mb (Option 3S) 32 Mb (Option 4S) 64 Mb (Option 5S)			
Analog Mux	4 fixed channels (standard) Any signal (user selectable) may be routed to 4 output BNCs with Option AM			
Probing options (order separately)	P5910 - 17-channel General-purpose probe P5934 - 34-channel Mictor probe P5960 - 34-channel D-MAX probe			

General characteristics

Number of channels (all channels are acquired including clocks)

TLA6401	34 channels (2 are clock channels). Clock channels can also be used as qualifiers.
TLA6402	68 channels (4 are clock channels). Clock channels can also be used as qualifiers.
TLA6403	102 channels (4 are clock and 2 are qualifier channels). Clock channels can also be used as qualifiers.
TLA6404	136 channels (4 are clock and 4 are qualifier channels). Clock channels can also be used as qualifiers.
Channel grouping	No limit to number of groups or number of channels per group (all channels can be reused in multiple groups).
Time stamp	54 bits at 20 ps resolution (>4 days duration)
Clocking/acquisition modes	Asynchronous/Synchronous; 25 GHz MagniVu high-speed timing is available simultaneous with all modes.

PC characteristics

Operating system	Microsoft® Windows® 7 Ultimate, 64-bit
Processor	Intel® Core i3-2120, 3.3 GHz, 3M Cache
Chipset	Intel® Q67 chipset
Memory	2 × 2 GB DIMM, 4 GB Total DDR3, 1066 MHZ, PC3-8500
Sound	Line In, Line Out, and Mic In connectors
	3.5 in., ≥500 GB Serial ATA, 7200 RPM
Optical drive	Internal 4.7 GB DVD±R/RW
External display port type	One (1) DVI connector and one (1) VGA connector
External display resolution	Up to 1920 × 1200 noninterlaced at 32-bit color, each for both primary and secondary displays
Network port	Two (2) 10/100/1000 LAN with RJ-45 connector
USB port	Five (5) USB 2.0 ports and two (2) USB 3.0 ports. USB ports can be disabled in BIOS.

Integral controls

Front panel display	Size: 15 in. (38.1 cm) diagonal Type: Active-matrix color TFT LCD with backlight Resolution: 1024 × 768
Simultaneous display capability	Both the front-panel and one external display can be used simultaneously at 1024 × 768 resolution
Front panel	General-purpose knob with dedicated hotkeys and knobs for horizontal and vertical scaling and scrolling
Touch screen	Available with Option 18. Can be enabled/disabled with a front-panel button.

Integrated View (iView™) capability

TLA mainframe configuration requirements	GPIB-iView™ (Opt. 1C) USB-iView™ (Opt. 2C)
Number of Tektronix oscilloscopes that can be connected to a TLA system	1
External oscilloscopes supported	More than 100. For a complete listing of current supported oscilloscopes, please visit our website http://www.tek.com/iview.
TLA connections	USB, Trigger In, Trigger Out, Clock Out
Oscilloscope connections	
GPIB-iView™ (Opt. 1C)	GPIB, Trigger In, Trigger Out, Clock In (when available)
USB-iView™ (Opt. 2C)	USB Device Port, Trigger In, Trigger Out

Integrated View (iView™) capability

Setup	iView™ external oscilloscope wizard automates setup.
Data correlation	After oscilloscope acquisition is complete, the data is automatically transferred to the TLA and time correlated with the TLA acquisition data.
Deskew	The oscilloscope and TLA data is automatically deskewed and time correlated when using the iView™ external oscilloscope cable.
GPIB-iView™ (Opt. 1C) External oscilloscope cable length	2 m (6.6 ft.)
USB-iView™ (Opt. 2C) External oscilloscope cable length	2 m (6 ft.)

Symbolic support

Number of symbols/ranges	Unlimited (limited only by amount of virtual memory available on TLA)
Object file formats supported	IEEE695, OMF 51, OMF 86, OMF 166, OMF 286, OMF 386, COFF, Elf/Dwarf 1 and 2, Elf/Stabs, TSF (If your software development tools do not generate output in one of the above formats, TSF, or the Tektronix symbol file, a generic ASCII file format is supported. The generic ASCII file format is documented in the TLA online help). If a format is not listed, please contact your local Tektronix representative.

External instrumentation interface

System Trigger output	Asserted whenever a system trigger occurs (TTL-compatible output, back-terminated into 50 Ω)
System Trigger input	Forces a system trigger when asserted (adjustable threshold between 0.5 V and 1.5 V, edge sensitive, falling-edge latched)
External Signal output	Can be used to drive external circuitry from a module's trigger mechanism (TTL-compatible output, back-terminated into 50 Ω)
External Signal input	Can be used to provide an external signal to arm or trigger any or all modules (adjustable threshold between 0.5 V and 1.5 V, level sensitive)

Power

Voltage range/frequency	90-264 VAC at 47-63 Hz
Power consumption	400 W maximum

Environmental

Temperature	
Operating	+5 °C to +40 °C
Nonoperating	-20 °C to +60 °C
Humidity	Max wet bulb temperature: +29 °C
Operating	20% to 80% relative humidity noncondensing
Nonoperating	8% to 80% relative humidity noncondensing
Altitude	
Operating	To 3,000 meters (10,000 ft.), derate maximum operating temperature by 1 °C per 300 meters above 1,500 meters altitude
Nonoperating	To 12,000 meters (40,000 ft.)
Safety	UL61010-1:2004, CAN/CSA-C22.2 No. 61010-1:2004, EN61010-1:2001, and IEC61010-1:2001

Physical characteristics

Dimensions	
Height	297 mm (11.7 in.)
Width	437 mm (17.2 in.)
Depth	387 mm (15.2 in.)
Net weight	
TLA6401	13.5 kg (29 lb. 13 oz.)
TLA6402	13.9 kg (30 lb. 10 oz.)
TLA6403	14.3 kg (31 lb. 8 oz.)
TLA6404	14.7 kg (32 lb. 5 oz.)
Shipping weight	
TLA6401	20.5 kg (45 lb. 2 oz.)
TLA6402	20.9 kg (46 lb. 1 oz.)
TLA6403	21.3 kg (47 lb.)
TLA6404	21.7 kg (47 lb. 8 oz.)

Input characteristics

Threshold selection range	From -2.0 V to +4.5 V in 5 mV increments Threshold presets include TTL (1.5 V), CMOS (1.65 V), ECL (-1.3 V), PECL (3.7 V), LVPECL (2.0 V), LVCMOS 1.5 V (0.75 V), LVCMOS 1.8 V (0.9 V), LVCMOS 2.5 V (1.25 V), LVCMOS 3.3 V (1.65 V), LVDS (0 V), and user defined.
Threshold selection channel granularity	Separate selection for each channel
Threshold accuracy	
23 °C ±5 °C	±(50 mV + 1% of threshold voltage setting) of threshold voltage setting
Full range	±(80 mV + 2%)
Input voltage range	
Operating	-2.5 V to 5.0 V
Nondestructive	-4.5 V to +13 V
Minimum input voltage swing	300 mV (P5910 and P5960)

State acquisition system

Maximum State clock rate	333 MHz (standard) 667 MHz (optional)
Maximum data rate	667 Mb/s (standard) 1333 Mb/s (optional)
State record length with time stamps	2 Mb, 4 Mb, 8 Mb, 16 Mb, 32 Mb, 64 Mb
Setup and hold selection range	From 15 ns before, to 7.5 ns after clock edge in 20 ps increments

State acquisition system

Setup and hold window	
Single channel	260 ps typical (P5910 and P5960)
Minimum clock pulse width	250 ps (P5910 and P5960)

Timing acquisition system

MagniVu™ timing	40 ps, adjustments to 80 ps, 160 ps, 320 ps, and 640 ps
MagniVu timing record length	128 Kb per channel, with adjustable trigger position
Deep timing resolution (half/full channel)	312.5 ps / 625 ps to 50 ms
Deep timing resolution with glitch storage enabled	1.25 ns to 50 ms
Deep timing record length (half/full channels with time stamps and with or without transitional storage)	4/2 Mb, 8/4 Mb, 16/8 Mb, 32/16 Mb, 64/32 Mb, 128/64 Mb per channel
Deep timing record length with glitch storage enabled	Half of default main memory depth
Channel-to-channel skew	160 ps typical (P5910 and P5960)
Minimum recognizable pulse/glitch width (single channel)	250 ps (P5910 and P5960)
Minimum detectable setup/hold violation	80 ps
Minimum recognizable multichannel Trigger event	Sample period + channel-to-channel skew

Analog acquisition system

Bandwidth	2 GHz typical (P5910 and P5960)
Attenuation	10X or 5X
Offset and Gain (accuracy)	±80 mV, ±2% of signal amplitude
Run/Stop requirements	None, analog outputs are always active
iCapture™ Analog outputs	Compatible with any supported Tektronix oscilloscope
iCapture Analog output BNC cable	4; Low loss, 10X, 36 in. Basic Analog Multiplexer functionality is offered standard on all TLA6400 models. This routes 4 fixed channels to the iCapture Analog Output BNCs. The outputs cannot be switched to other logic analyzer channels. Option AM enables full analog multiplexer control and allows the routing of any 4 logic analyzer channels to the iCapture Analog Output BNCs.

Trigger system

Independent Trigger states	16
Maximum idependent If/Then clauses per state	16
Maximum numger of events per If/ Then clause	8
Maximum number of actions per If/ Then clause	8
Maximum number of Trigger events	26 (2 counters/timers plus any 24 other resources)
Number of word recognizers	24
Number of transition recognizers	24
Number of range recognizers	8
Number of counters/timers	
Trigger event types	Word, Group, Channel, Transition, Range, Anything, Counter Value, Timer Value, Signal, Glitch, Setup-and-Hold Violation, Snapshot
Trigger action types	Trigger Module, Trigger All Modules, Trigger Main, Trigger MagniVu, Store, Don't Store, Store Sample, Increment Counter, Decrement Counter, Reset Counter, Start Timer, Stop Timer, Reset Timer, Snapshot Current Sample, Goto State, Set/Clear Signal, Do Nothing
Maximum triggerable data rate	1333 Mb/s
Trigger machine sequence rate	DC to 800 MHz (1.25 ns)
Counter/timer range	48 bits each (~4 days at 1.25 ns)
Counter rate	DC to 800 MHz (1.25 ns)
Timer clock rate	800 MHz (1.25 ns)
Counter/timer test latency	0 ns
Range recognizers	Double bounded (136 channel max). Can be as wide as any group, must be grouped according to specified order of significance.
Setup-and-hold violation recognizer setup time range	From 7.5 ns before, to 7.5 ns after clock edge in 20 ps increments. This range may be shifted toward the positive region by 0 ns, 2.5 ns, 5 ns, or 7.5 ns.
Setup-and-hold violation recognizer hold time range	From 7.5 ns before, to 7.5 ns after clock edge in 20 ps increments. This range may be shifted toward the positive region by 0 ns, 2.5 ns, 5 ns, or 7.5 ns.
Trigger position	Any data sample
MagniVu trigger postion	MagniVu position can be set from 0% to 60% centered around the MagniVu trigger
Storage control (data qualification)	Global (conditional), by state (start/stop), block, by trigger action, or transitional. Also force main prefill selection available.

P5900 series probes

General

Characteristic	P5910	P5934	P5960
Probe type	Single-ended data Single-ended clock (General Purpose)	Single-ended data Single-ended clock (Mictor 34-channel)	Single-ended data Single-ended clock (D-Max® Probing technology)
Number of channels	17	34	34
Recommended usage	Most general-purpose applications	Applications requiring many channels to be connected quickly in a small footprint	High-performance applications requiring many channels to be connected quickly in a small footprint
Attachment to target system	Fits both 0.100 in. and 2 mm square pin configuration	Amp Mictor 34-channel connector	D-Max probing technology
Probe load AC/DC	1.3 pF/20 kΩ to 0 V	2 pF/20 kΩ to 0 V	0.8 pF/20 kΩ to 0 V
Input range	-2.5 V to +5 V		
Maximum voltage (nondestruct)	-4.5 V to +13 V		
Cable length	1.5 m (5 ft.)	1.2 m (4 ft.)	1.5 m (5 ft.)

Ordering information

TLA6400 series

TLA6401	34-channel Logic Analyzer module, 25 GHz timing, 333 MHz state, 2 Mb record length. Options for up to 64 Mb record length and/or up to 667 MHz state.
TLA6402	68-channel Logic Analyzer module, 25 GHz timing, 333 MHz state, 2 Mb record length. Options for up to 64 Mb record length and/or up to 667 MHz state.
TLA6403	102-channel Logic Analyzer module, 25 GHz timing, 333 MHz state, 2 Mb record length. Options for up to 64 Mb record length and/or up to 667 MHz state.
TLA6404	136-channel Logic Analyzer module, 25 GHz timing, 333 MHz state, 2 Mb record length. Options for up to 64 Mb record length and/or up to 667 MHz state.
All include:	Mini Keyboard (119-7275-xx), Optical Wheel Mouse (119-7054-xx), Front-panel cover (200-4939-xx), TLA Application Software CD (063-3881-xx), Certificate of Traceable Calibration.
Note:	Please specify probe, power, language, and service options when ordering.

Instrument options

Option	Description
1S	Increase to 4 Mb record length
2S	Increase to 8 Mb record length
3S	Increase to 16 Mb record length
4S	Increase to 32 Mb record length
5S	Increase to 64 Mb record length
1T	Increase state speed to 667 MHz
AM	Add full analog mux control
18	Add touch screen
1C	Add GPIB-iView™ external oscilloscope cable kit
2C	Add USB-iView™ external oscilloscope cable kit
PO	Add accessory pouch

Power cord options

Opt. A0	North America power plug (115 V, 60 Hz)
Opt. A1	Universal Euro power plug (220 V, 50 Hz)
Opt. A2	United Kingdom power plug (240 V, 50 Hz)
Opt. A3	Australia power plug (240 V, 50 Hz)
Opt. A4	North America power plug (240 V, 50 Hz)
Opt. A5	Switzerland power plug (220 V, 50 Hz)
Opt. A6	Japan power plug (100 V, 50/60 Hz)
Opt. A10	China power plug (50 Hz)
Opt. A11	India power plug (50 Hz)
Opt. A12	Brazil power plug (60 Hz)
Opt. A99	No power cord

Language options

Opt. L0	English manual
Opt. L5	Japanese manual
Opt. L10	Russian manual
Opt. L99	No manual

Service options

Opt. C3	Calibration Service 3 Years
Opt. C5	Calibration Service 5 Years
Opt. D1	Calibration Data Report
Opt. D3	Calibration Data Report 3 Years (with Opt. C3)
Opt. D5	Calibration Data Report 5 Years (with Opt. C5)
Opt. R3	Repair Service 3 Years (including warranty)
Opt. R3DW	Repair Service Coverage 3 Years (includes product warranty period). 3-year period starts at time of instrument purchase
Opt. R5	Repair Service 5 Years (including warranty)
Opt. R5DW	Repair Service Coverage 5 Years (includes product warranty period). 5-year period starts at time of instrument purchase

Upgrade options

The TLA6400 can easily be upgraded after the initial purchase. To increase the state speed, memory depth, or add full analog multiplexer capability to an existing TLA6400, order the appropriate upgrade kit and an option listed below. Example: TLA64F03 Option 01. Please refer to the TLA Family Upgrade Guide for further details.

Upgrade kits

TLA64F01	PowerFlex Field Kit for TLA6401
TLA64F02	PowerFlex Field Kit for TLA6402
TLA64F03	PowerFlex Field Kit for TLA6403
TLA64F04	PowerFlex Field Kit for TLA6404

Memory upgrades

Opt. 01	Increase from 2 Mb Record Length to 4 Mb Record Length
Opt. 02	Increase from 2 Mb Record Length to 8 Mb Record Length
Opt. 03	Increase from 2 Mb Record Length to 16 Mb Record Length
Opt. 04	Increase from 2 Mb Record Length to 32 Mb Record Length
Opt. 05	Increase from 2 Mb Record Length to 64 Mb Record Length
Opt. 06	Increase from 4 Mb Record Length to 8 Mb Record Length
Opt. 07	Increase from 4 Mb Record Length to 16 Mb Record Length
Opt. 08	Increase from 4 Mb Record Length to 32 Mb Record Length
Opt. 09	Increase from 4 Mb Record Length to 64 Mb Record Length
Opt. 10	Increase from 8 Mb Record Length to 16 Mb Record Length
Opt. 11	Increase from 8 Mb Record Length to 32 Mb Record Length

Opt. 12	Increase from 8 Mb Record Length to 64 Mb Record Length
Opt. 13	Increase from 16 Mb Record Length to 32 Mb Record Length
Opt. 14	Increase from 16 Mb Record Length to 64 Mb Record Length
Opt. 15	Increase from 32 Mb Record Length to 64 Mb Record Length

State speed upgrade

Opt. 1T	Increase from 333 MHz State Clock to 667 MHz State Clock

Analog Mux upgrade

Opt. AM	Enable full control of Analog Mux

Recommended accessories

Accessory	Description	
Logic analyzer cart		
	LACART	2-shelf Cart
	K4000	3-shelf Cart
016-1522-xx	Wheeled transport case	
020-2664-xx	Rackmount kit	
650-4815-xx	Additional removable hard disk drive assembly; no software	

P5900 probes

Model	Description
P5910	17-channel general-purpose probe with single-ended Data/Clock, separable podlets, and accessories
	Includes: podlet holders, IC grabbers, ground leads, ground tips, extension ground tips, probe labels
P5934	34-channel high-density Mictor probe with single-ended Data/Clock and accessories
	Includes: latch housing assembly (edge-mount), latch housing assembly (vertical), probe labels
P5960	34-channel high-density D-Max® probing technology probe with single-ended Data/Clock and accessories
	Includes: probe head protective cover, probe retention kit for D-Max® probing technology, probe labels

Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.

Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

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