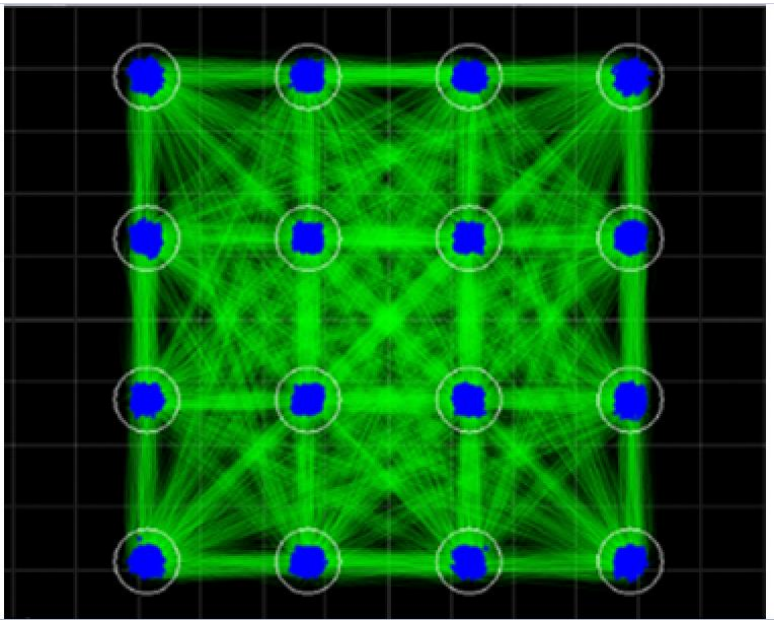
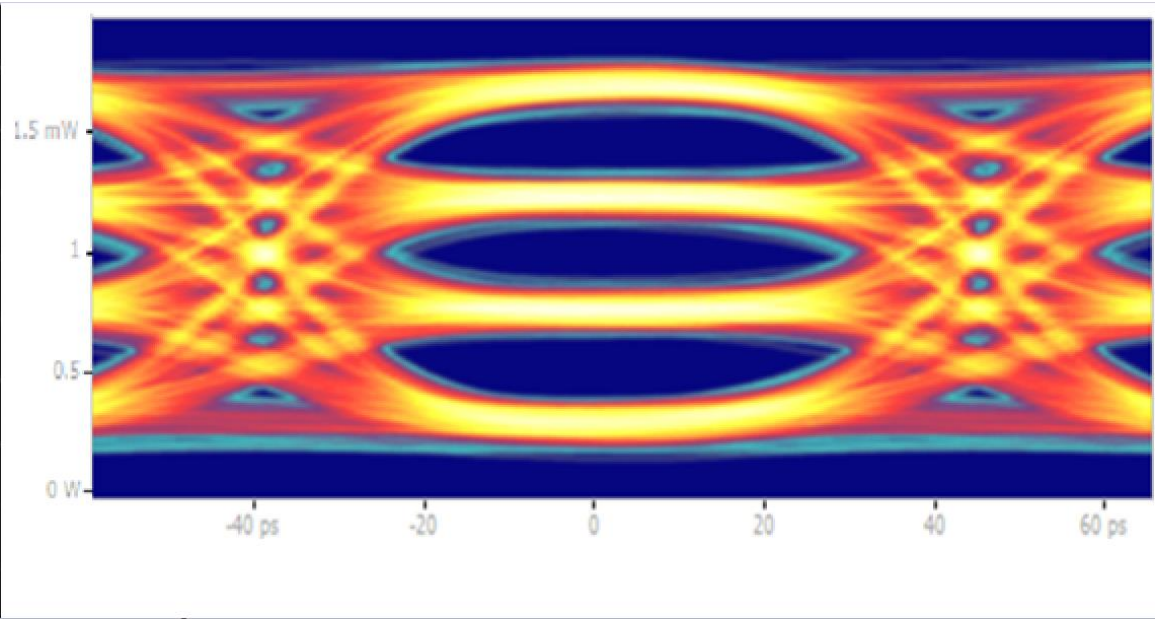
100G and 400G Ethernet and general DataCom roadmap/Challenge/solution





王宏军
FAE/Tektronix China

Tektronix®

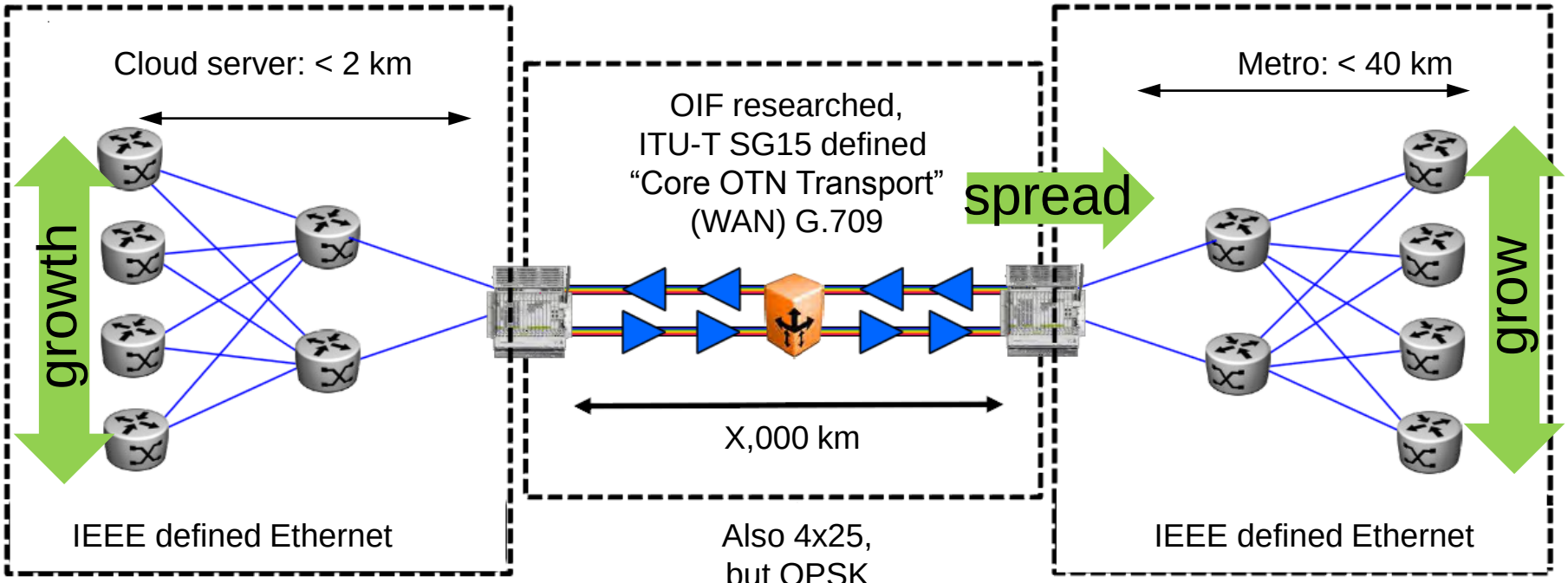
Nov, 2015

Agenda: **100G and 400G Ethernet and general DataCom roadmap and testing needs**

- Overview
  - 100G and 400G futures
  - Transitional from 100G to 400G.
- 100G-400G Design Challenges
  - Channel Loss –vs- Higher order modulation
  - Excerpts from 400G Specs that cause pain
- TX Signal Acquisition for 100G/400G
  - Real Time Signal Acquisition
  - Equivalent Time Signal Acquisition
- RX Signal Generation for 100G/400G
  - PAM-4 modulation and demodulation for error detection.
- Coherent optical Introduction

Communication world past 100G/400G

- Emerging 100G/400G industry, leverages an assortment of standards and technologies to support the broad set of **Submarine -> Continental** -> Metro -> Campus -> Data-Center -> Back-Plane -> **Chip to Chip** requirements.



Graphics after OIF CEI / Chris Cole, Finisar

The top-to-bottom *100G* standards

(Main actors only, not a comprehensive table)

Distance	Standard	Modulation/signaling	e.g.
X,000 km…40 km	OIF, OTN, ITU	Complex optical	DP-QPSK
10, 40 km	Ethernet	NRZ SM	100GBASE-ER4/LR4
2 km	*MSA "CLR4"*	NRZ SM	100G-CLR4
500 m	*MSA "PSM4"*	NRZ SM	100G PSM4
100 m	Ethernet	NRZ MM	100GBASE-SR4
~100 m	Infiniband (IB)	NRZ over active cable; or interconnect	"CAUI-4" going
10 m	Ethernet, IB	NRZ on passive Cu cable	100GBASE-CR4
Backplane < 1m	Ethernet, OIF CEI	NRZ	100GBASE-KR4, CEI LR
		PAM4	100GBASE-KP4
Interconnect module to chip, chip to chip	OIF CEI, Ethernet	NRZ	VSR CAUI-4

100G across the stack

The top-to-bottom *400G* standards

(Main actors only, not a comprehensive table)

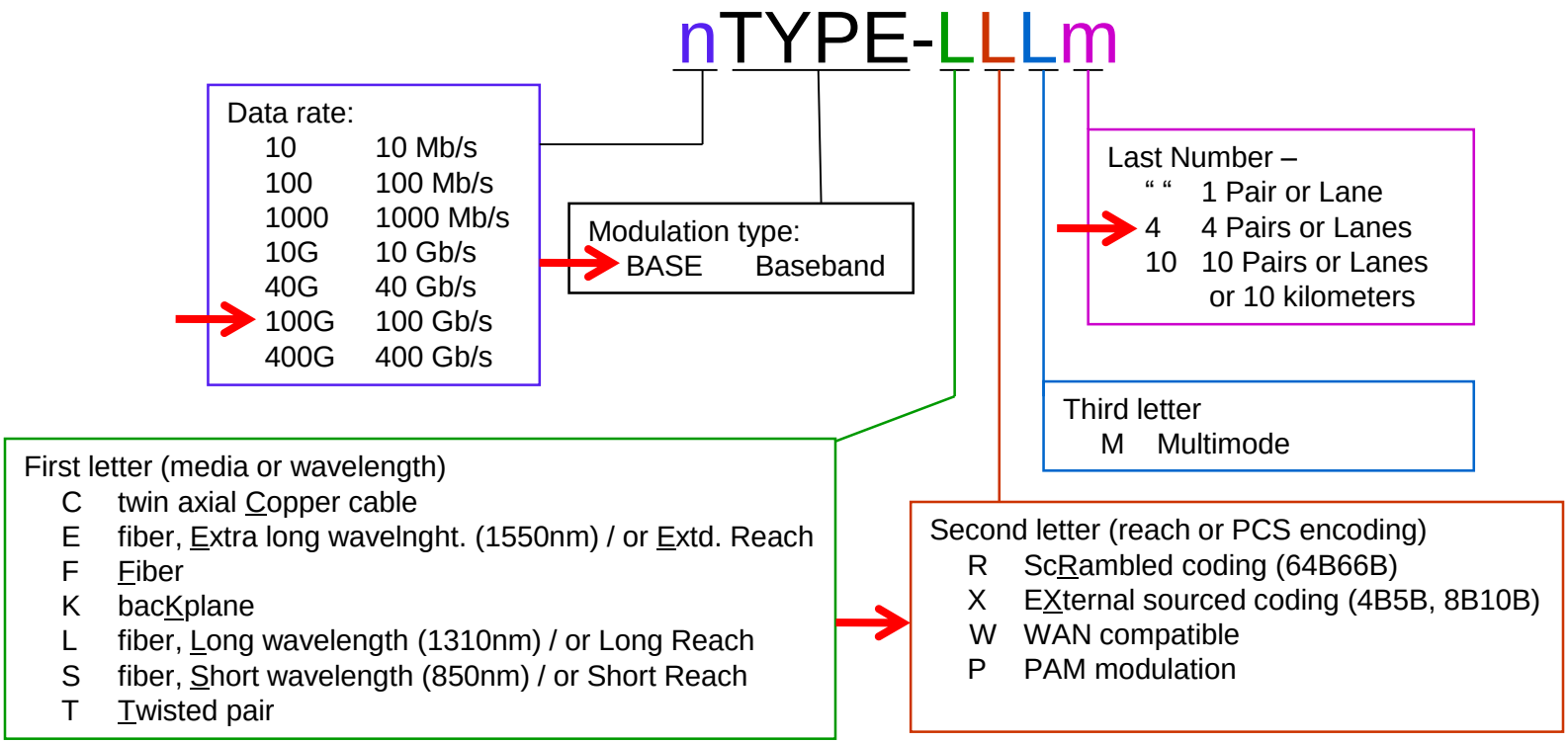
Distance	Standard	Modulation/signaling	e.g.
X,000 km	OIF, OTN, ITU	Complex optical	DP-QPSK Multi?
10 km	Ethernet	PAM4 at 25 GBd	400GBASE-LR8
2 km	Ethernet	PAM4 at 25 GBd	400GBASE-FR8
500 m	Ethernet	PAM4 at 50 GBd	400GBASE-DR4
Backplane < 1m	OIF CEI	PAM4 at 25 GBd	CEI LR
Interconnect module to chip, chip to chip	Ethernet OIF CEI	NRZ PAM4	CDAUI-16, CDAUI-8 CEI VSR

To 400G across the stack

Ethernet Nomenclature

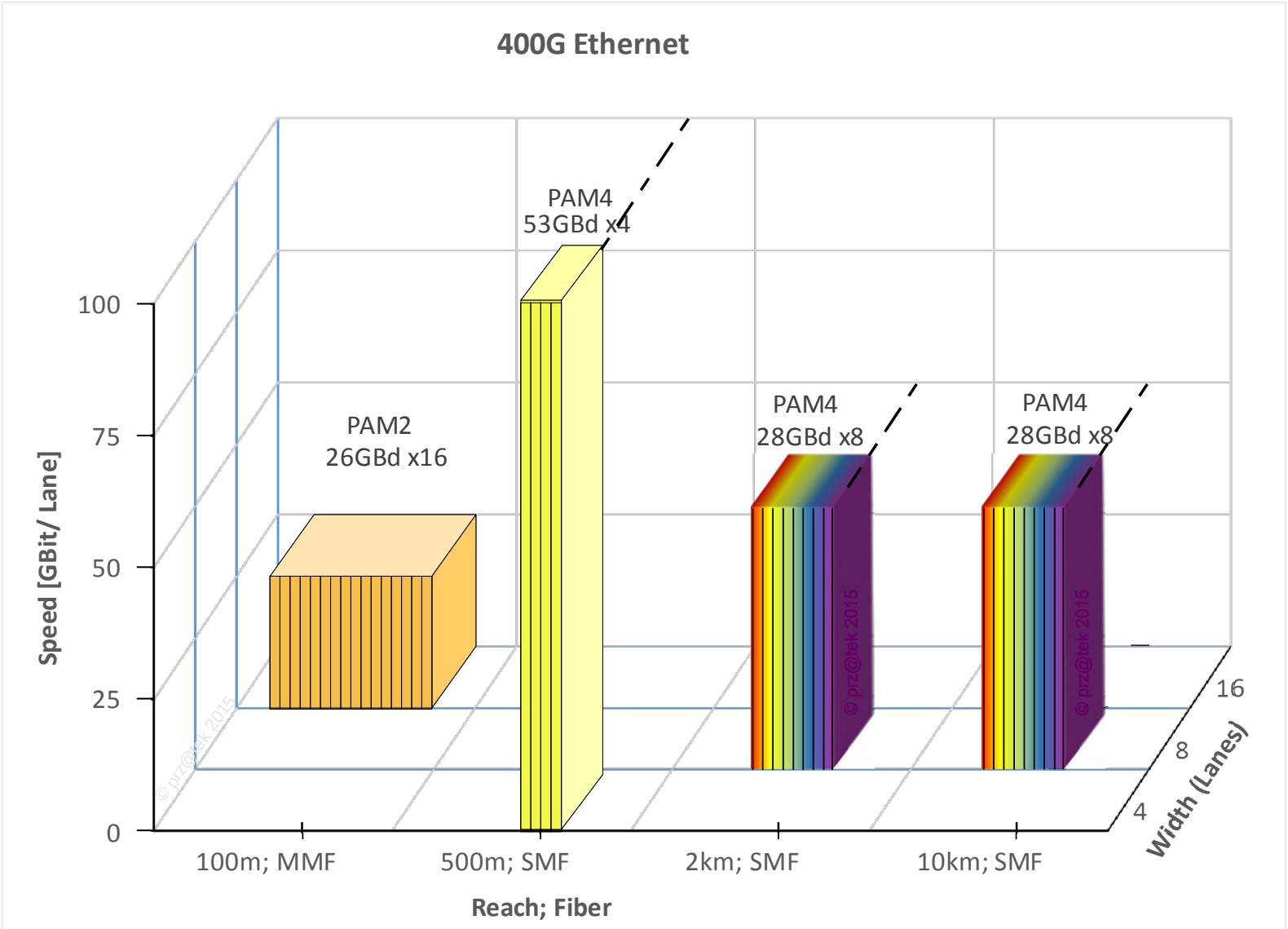
(based on an Ethernet Alliance slide by Scott Kipp, with Tektronix extensions)

- Common interpretation* is as follows:
- Example: 100GBASE-KP4



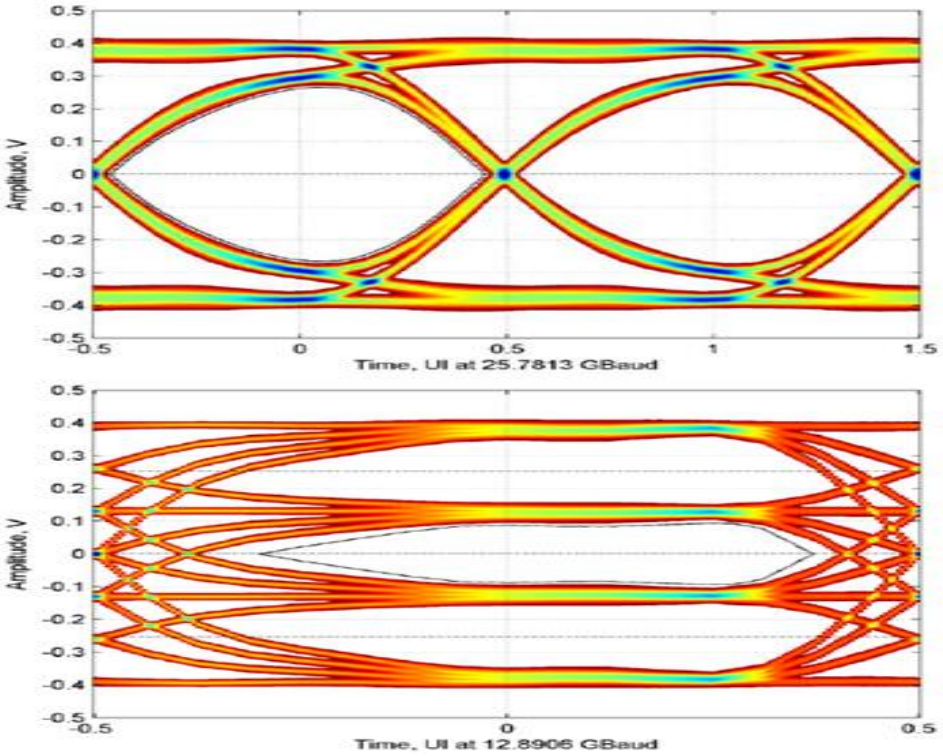
- The IEEE does not specify the meanings of the letters, rather it simply identifies PHYs by combinations of letters. There is no guarantee that in the future these interpretations will retain whatever meaning they presently have.

Driver is Optical Ethernet at 400G
Interconnect electrical at 25 GBd x8 PAM4



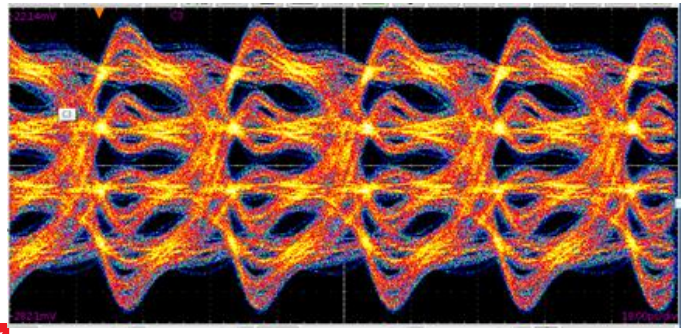
Design and Test Challenges in the 100G-400G transition

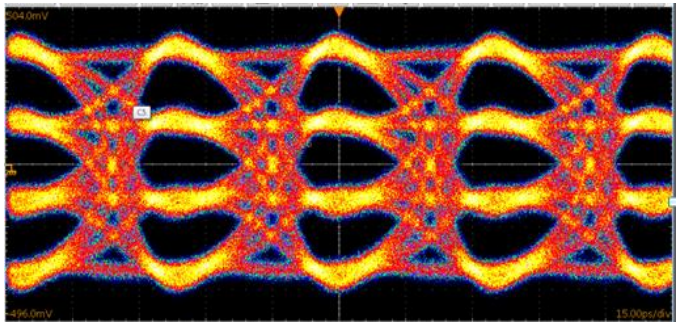
- "Copper is out of gas" at 56Gbps.
  - Higher order modulation (PAMn) is one means of combating incredibly high channel losses.
  - Multiple bits/symbols results in a reduced overall symbol rate and fundamental transmission frequency. 14GHz rather than 28GHz.



Design and Test Challenges in the 100G-400G transition

- Higher order modulation (PAM4) signals are more sensitive to ISI as they involve multiple transitions between multiple levels.
  - *This results in smaller horizontal eye openings.*
- The signal transitions between each level are also smaller
  - *This results in smaller vertical eye openings, higher sensitivity to noise.*
- Forward Error Correction (FEC) is needed to improve BER performance of the link.
- Tx pre-emphasis and Rx CTLE/DFE may be used to somewhat compensate for the channel induced ISI
- Gray coding may be used to limit certain multi-level transitions and also reduce ISI





Design and Test Challenges in the 100G-400G transition

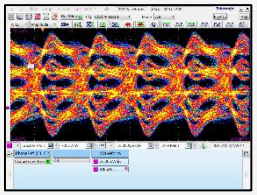
- High data rate for Pattern generator
- Low instrument intrinsic jitter <350fs for Pattern generator
- Jitter injection support for stress testing
- High sensitivity error detector
- Low instrument intrinsic jitter <150fs for Scope
- High bandwidth electrical/optical measurement
- CDR support

Tektronix 100/400G Test Solutions

Industry's only complete solution for comprehensive Tx and Rx testing

Signal Generation

PAM4 PPG with pre-emphasized remote head



Device Under Test

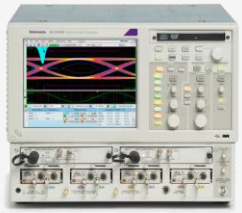
ASIC/FPGA SERDES, transceivers, physical layer ICs

Signal Acquisition

PAM4 PED with decoder remote head

DPO70000SX ATI Real Time Oscilloscope

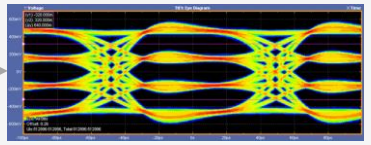
DSA8300 Sampling Oscilloscope



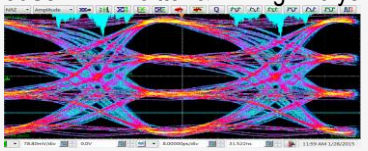
Analysis Software

PAM4 BERT control and analysis

DPOJET RT Jitter & Timing Analysis



80SJNB ET Jitter & Timing Analysis



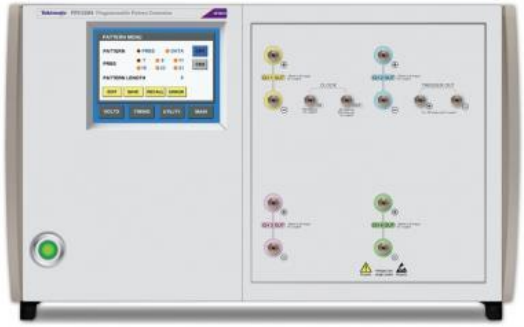
PPG and PED instruments

Options and configurations

PPG Base Instruments

- **PPG1251** 12.5Gb/s PPG
  - Jitter insertion (LF+HF)
- **PPG1600x/300X** 16&30Gb/s PPG
  - 1/2/4 Channel
  - LF jitter insertion
  - HF jitter insertion
- **PPG320X** 32Gb/s PPG
  - 1/2/4 Channel
  - Adjustable output
  - LF jitter insertion
  - HF jitter insertion
- **PPG4001** 40Gb/s PPG
  - LF jitter insertion
  - HF jitter insertion

Industry's only 40G PPG with Jitter Insertion



PPG3204 32Gb/s
4 channel PPG

PED3202 32Gb/s
2 channel PED

PED Base Instruments

- **PED320X** 32Gb/s PED
  - 1/2 Channel
  - Full or half rate clock input
  - AC or DC coupled input
- **PPG400X** 40Gb/s PED
  - 1/2 Channel
  - Full or half rate clock input
  - AC or DC coupled input

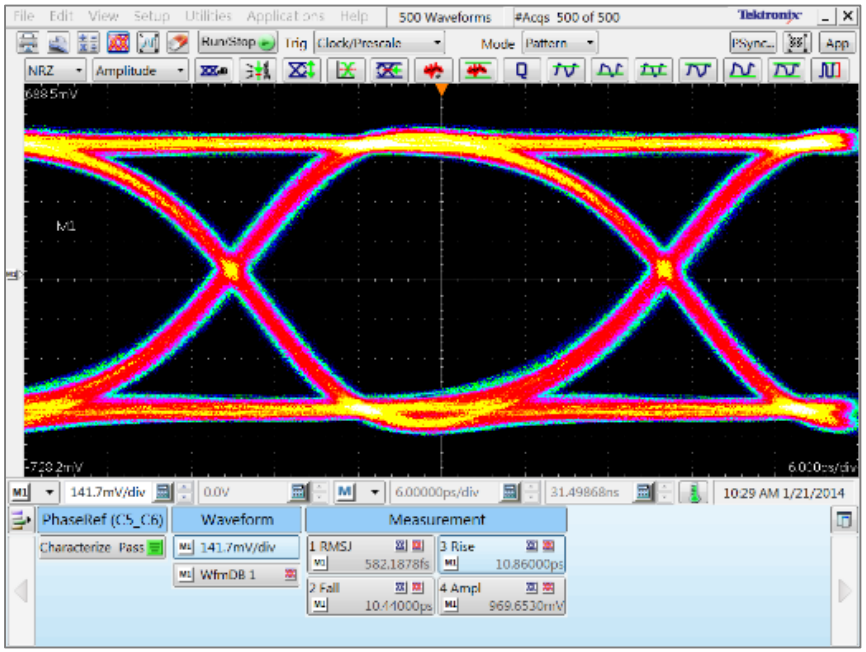
Industry's best PED sensitivity

6mV auto-align and auto-sync

PatternPro competitive advantage

32Gb/s Multi-channel BERT electrical performance

Fast Risetime and Low Jitter



PPG320X 32Gb/s
OPT-ADJ

DSA8300
80E11 sampling plug-in
82A04-60G phase reference

Data Source: MATH1	Data Rate: 32 Gbps	Filter: False
SSC: Off	Pattern: 2047 bits	Channel: False
Phase Reference: 32 GHz	Sample Count: 304.70 k	Equalizer: None

Jitter (Decision Threshold: -11.95 mV)		
Random Jitter		
RJ (RMS)	=	211.36 fs
RJ(h) (RMS)	=	211.20 fs
RJ(v) (RMS)	=	8.39 fs
Deterministic Jitter		
DJ	=	4.94 ps
DDJ	=	3.20 ps
DCD	=	971.00 fs
DDPWS	=	2.77 ps
BUJ(d-d)	=	50.00 fs
PJ	=	718.02 fs
PJ(h)	=	717.99 fs
PJ(v)	=	6.79 fs
NPJ(d-d)	=	50.00 fs
Total Jitter @ BER		
TJ (1E-12)	=	6.76 ps
Eye Opening (1E-12)	=	24.49 ps
Dual Dirac		
RJ(d-d)	=	243.96 fs
DJ(d-d)	=	3.32 ps

Noise (Sampling Phase: 0 UI)		
Random Noise		
RN (RMS)	=	581.45 uV
RN(v) (RMS)	=	567.11 uV
RN(h) (RMS)	=	128.35 uV
Deterministic Noise		
DN	=	149.69 mV
DDN	=	149.22 mV
DDN(level 1)	=	124.94 mV
DDN(level 0)	=	167.15 mV
BUN(d-d)	=	1.74 mV
PN	=	633.25 uV
PN(v)	=	458.95 uV
PN(h)	=	436.33 uV
NPN(d-d)	=	1.70 mV
Total Noise @ BER		
TN (1E-12)	=	157.72 mV
Eye Opening (1E-12)	=	821.79 mV
Eye Amplitude	=	979.51 mV
SSC Modulation		
Magnitude	=	0 ppm
Frequency	=	0 Hz

Industry Best 32Gb/s
Jitter Performance! 211fs

- **Data rate** range = 1.5 to 32 Gb/s
- **Voltage adjustability** = 300mV - 1Vpp single-ended (600mV - 2Vpp diff)
- **Rise/fall time** <11ps (20-80%)
- **Intrinsic Jitter** < 7ps TJ@1E-12

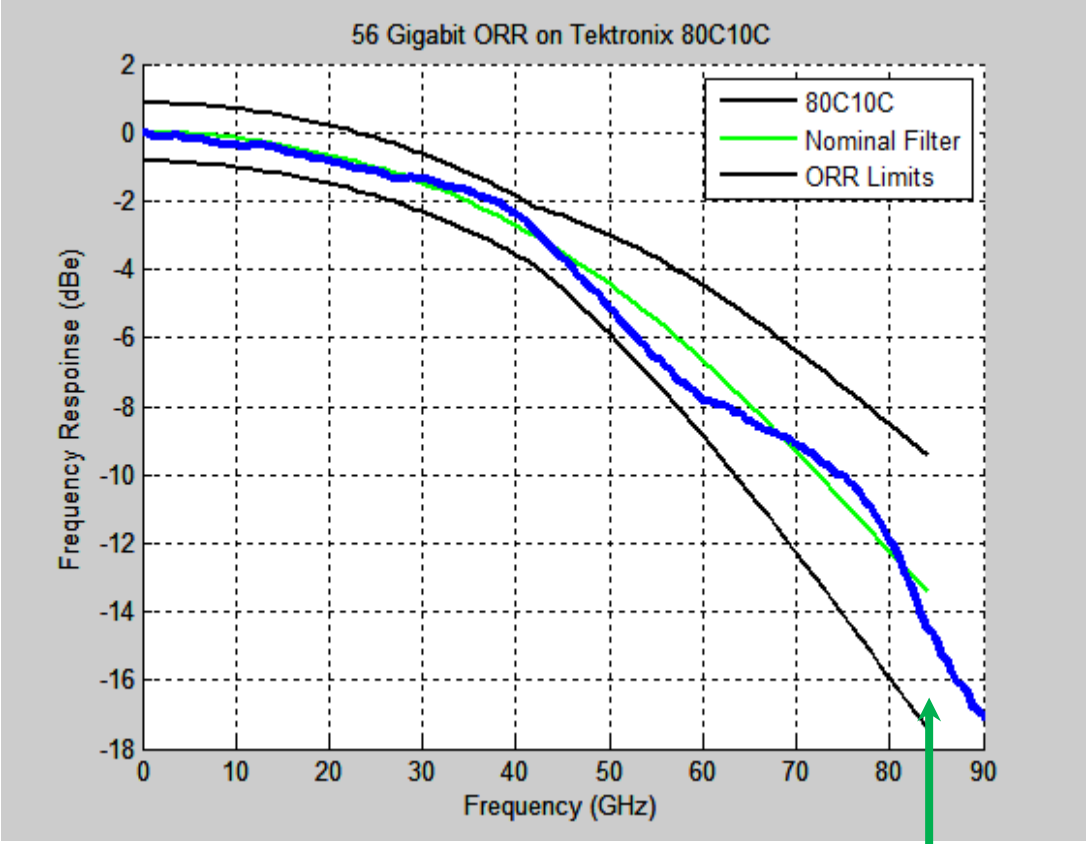
DSA8300 Digital Serial Analyzer
DSA8300 Optical Module Portfolio

Single and Multi-mode, Broad Wavelength (750 - 1650 nm) Modules	
80C07B	Supports standard rates to 2.7 Gb/s, high sensitivity, optional integrated clock recovery
80C08D	Supports all of the 8/10 Gb/s applications, high sensitivity, optional integrated clock recovery, optional Integrated CR
80C12B	Supports standard rates from 155 Mb/s – 11.3 Gb/s, high sensitivity - data pick-off for external CRU e.g. CR125A
80C14	Supports rates from 8.5 Gb/s – 14.063 Gb/s, high sensitivity – data pick-off for external CRU e.g. CR175A
80C15 New	Supports standard rates from 25.73 Gb/s – 28.05 Gb/s (maximum optical bandwidth > 32 GHz)
Single-mode, Long Wavelength (1100 - 1650nm) Modules	
80C11B	Optical bandwidth to 30GHz, supports 10Gbit/s up to14G+ standards, optional Integrated CR
80C10C	Optical bandwidth to 80GHz, supports all 40 and 100 Gb/s (4 x 25 Gb/s) standards, optional CR trigger pickoff for e.g. CR286A CRU, optional high sensitivity photo-receiver for use with external equipment (e.g. for optical BER testing with BERTScope)

56Gbps Optical Reference Receiver on Highest optical Bandwidth oscilloscope

80C10C, 80C10C-CRTP

- High sensitivity with and without CR
- Support for Optical Bessel-Thompson Filter in HW (no DSP, no special pattern needed)
- Electrical Data Out (optional) for:
  - Clock Recovery,
  - Real-time oscilloscope for troubleshooting
  - BER analysis



- Best noise performance at 40G, 56G → best system for PAM4 @ 56 GBd
- **Nearly 100 GHz optical Bandwidth**

Compliant
@ 84 GHz !!!

80C10C
Outstanding Performance and Value

Flexibility:

- Solution to 100GbE (4x25), OC768, G.709 FEC, OTU3+, and 40GbE test in one module
- Solution for 1550 nm and 1310 nm in one module
- Solution to 100G clock recovery, with Option CRTP (clock recovery trigger pickoff), and Tektronix CR286A Clock Recovery Instrument
- Solution to 40G clock recovery, with Option CRTP and 3rd party clock recovery Instrument.

Performance:

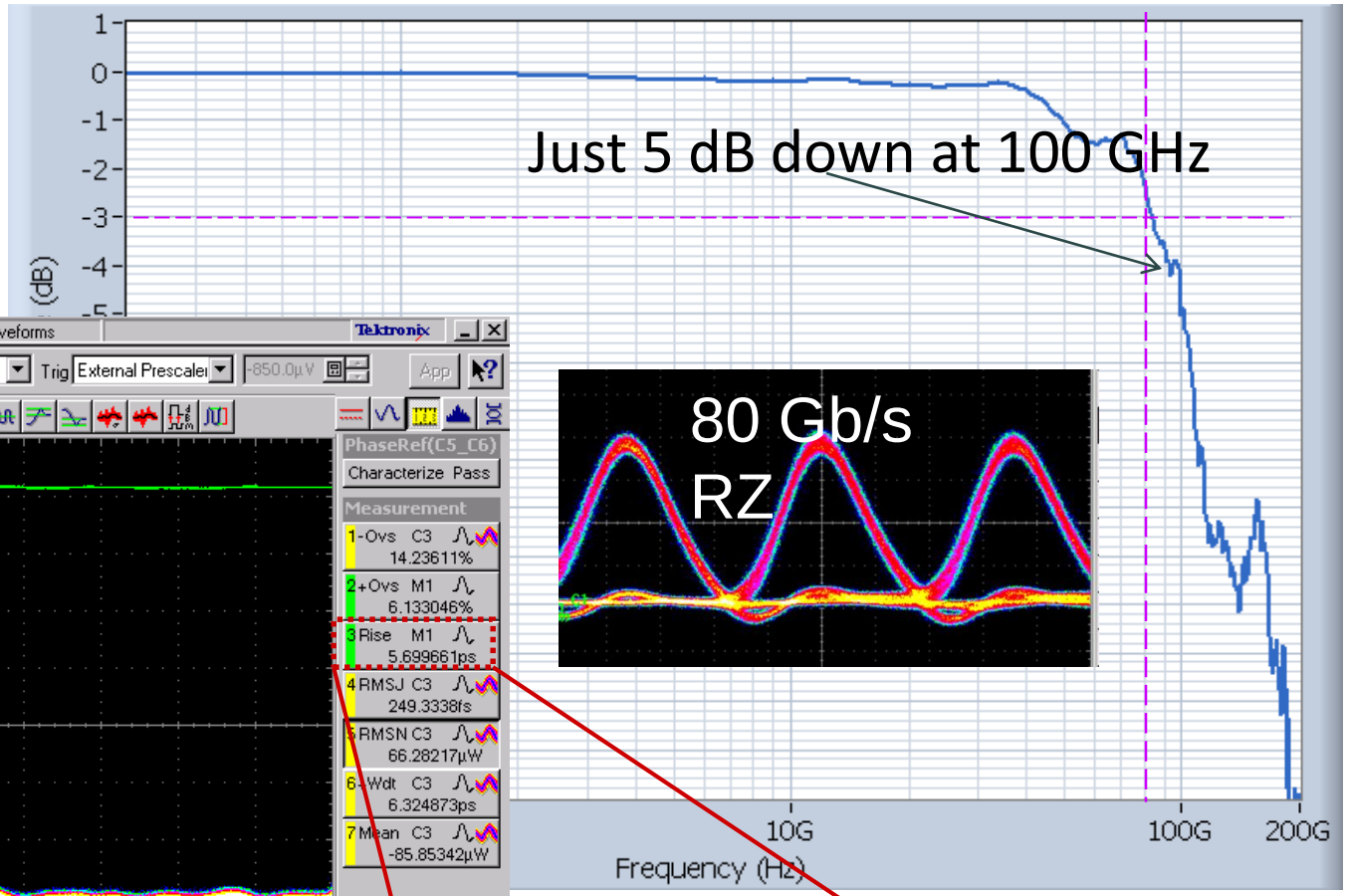
- Up to 80 GHz Optical Bandwidth
- Excellent Noise Performance
- Low Optical Return Loss
- Patented Technology For:
  - ✓ Low Aberrations
  - ✓ Extremely Flat Group Delay
  - ✓ ITU-Compliant OC-768 and G.709 FEC Filters

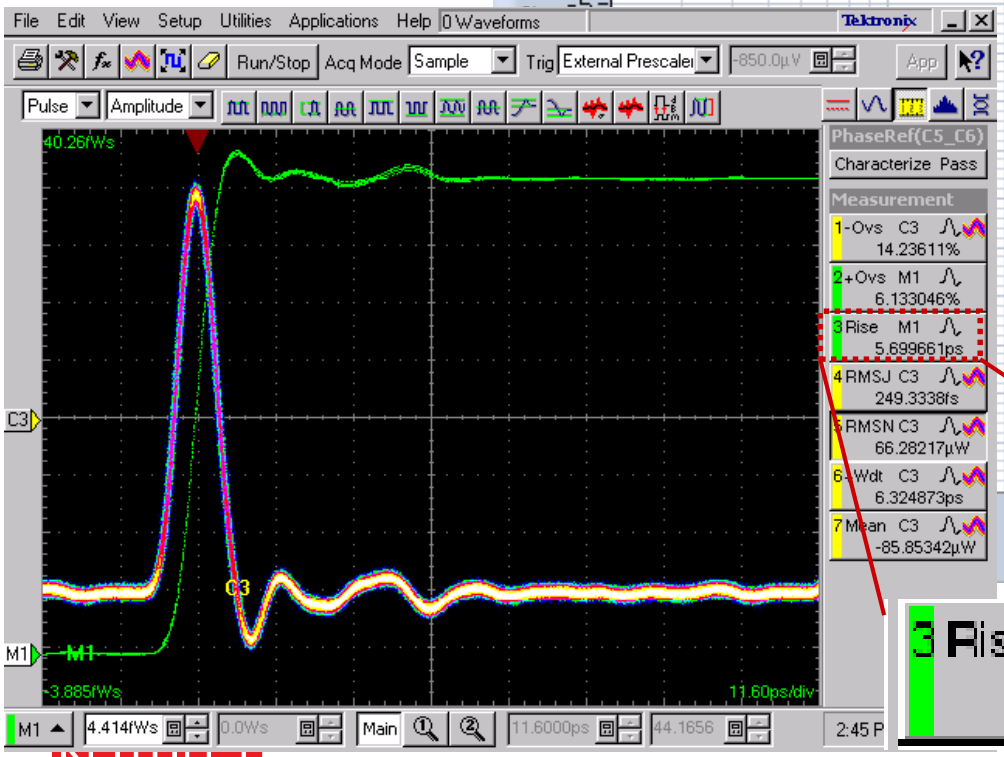
Optical Bandwidth / Integrated ORR	80C10C Opt. F1	80C10C Opt. F2	80C10C Opt. F3
Unfiltered bandwidth	70 GHz	55 GHz	80 GHz
Opt. CRTP available Clock Recovery Trigger Pickoff	✓	✓	✓
40Gbs G.709 FEC Telecom 43.02 Gb/s & 44.5 Gb/s	✓		✓
40GbE Datacom 41.25 Gb/s	✓		✓
OC768 40 GHz Telecom 39.8 Gb/s	✓		✓
OTU4 27.9 Gb/s	✓	✓	
100GbE-4X Datacom 25.7 Gb/s	✓	✓	

Single-mode optical standards (100Gb/s stable since 802.3ba ratified in 2011)

- Current technology satisfies 56 Gb/s as well as current 25 Gb/s

Tek 80C10C optical module:





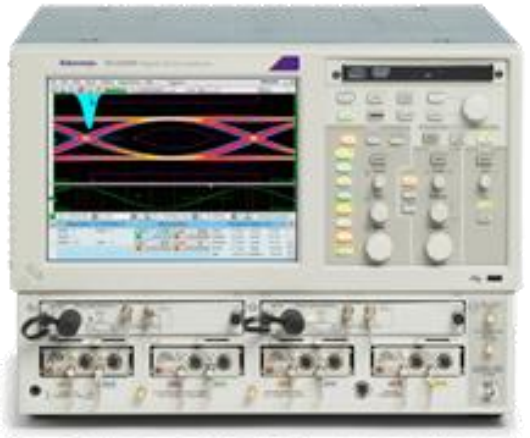
Tektronix 100G/400G Signal Acquisition Systems

Equivalent Time Signal Acquisition • Real Time Signal Acquisition Software Control and Analysis

- **Two world class acquisition systems cover the breadth of any 400G Verification and design needs, with the lowest noise, highest bandwidth in the industry**
  - Real Time (70GHz ATI) single shot acquisition and triggering capabilities are key tools for advanced analysis and debug.
  - Equivalent Time low noise, high sensitivity tools enable the best margin in product and device characterization.

- Real Time
  - 70GHz Analog Bandwidth, 4.3ps rise time (20%-80%)
  - 200GS/s Sample Rate
  - <125fs jitter noise floor
  - ≥25GHz Edge trigger bandwidth
  - Compact 5 ¼" Oscilloscope package

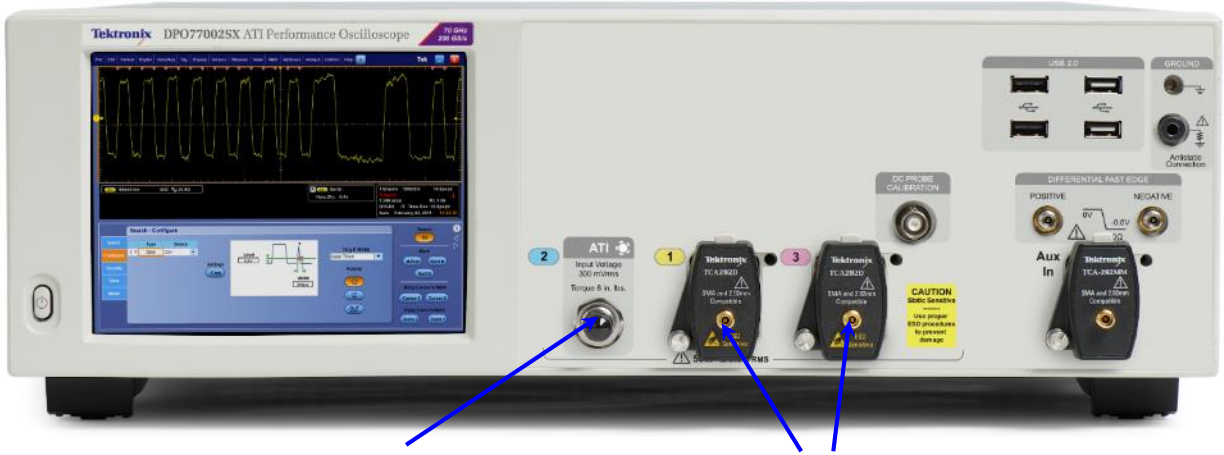
- Equivalent Time
  - 85GHz Optical Bandwidth
  - 70GHz Electrical Bandwidth
  - <100fs jitter noise floor
  - 20nW to .6uW Optical Resolution.
  - Automated test of 80 Industrial Stds.



ATI Performance Oscilloscope

- 70GHz Analog Bandwidth, 4.3ps rise time (20%-80%)
- 200GS/s Sample Rate
- <125fs jitter noise floor
- ≥25GHz Edge trigger bandwidth
- Compact 5 ¼” Oscilloscope package

- ✓ Low-noise ATI architecture
- ✓ Best-in-class signal capture
- ✓ Compact package with precise multi-unit sync



- 1 channel x 70GHz bandwidth
- Single-ended, 100mV$_{fsr}$ to 300mV$_{fsr}$
- 200GS/s sample rate
- Up to 1 Gsamples record length

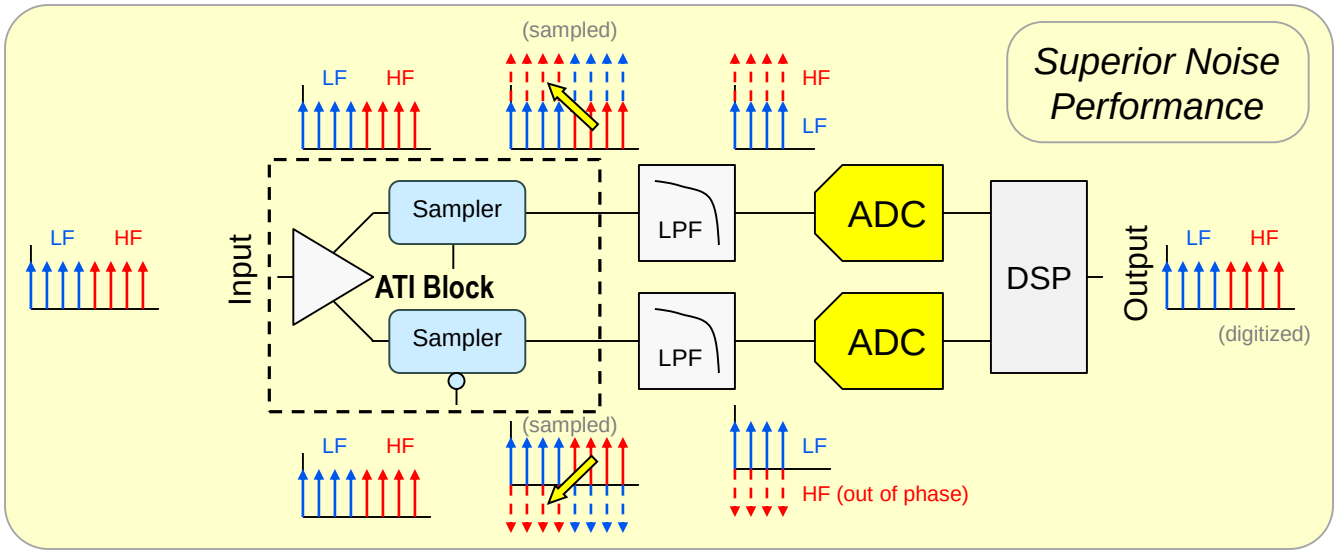
[OR]

- 2 channels x 33GHz bandwidth
- Single-ended, 62.5mV$_{fsr}$ to 6V$_{fsr}$
- 100GS/s sample rate per channel
- Up to 1 Gsamples record per channel

Comparing Methods: Tek Advantage

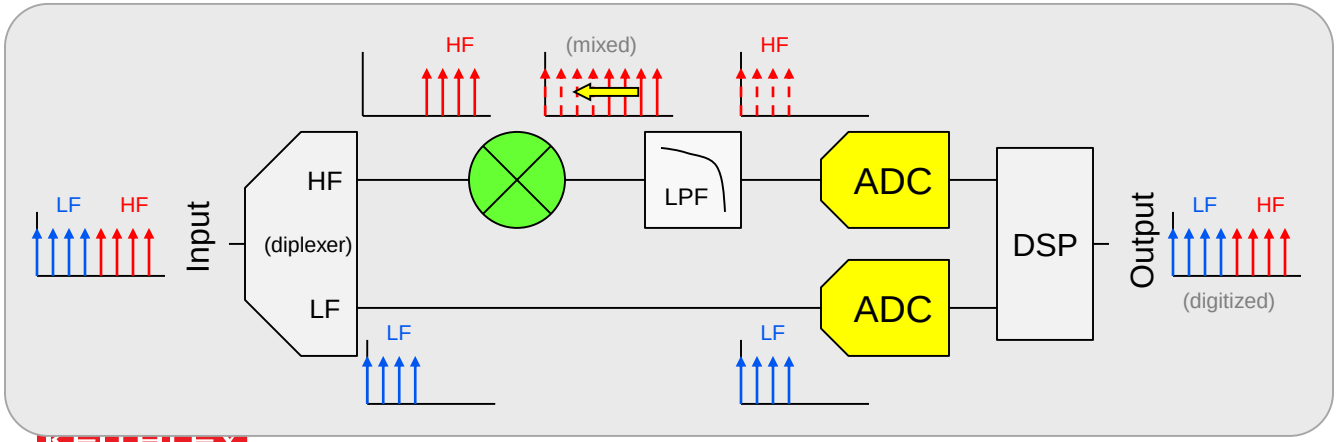
Superior Noise Performance for High-Bandwidth Data Converters

Tektronix Architectural Innovation



- ✓ **Improved SNR**
  - Each ADC sees full spectrum
  - Signal reconstruction involves *averaging* → improves SNR
- ✓ **Signal-path symmetry**
- ✓ **Patented architecture**

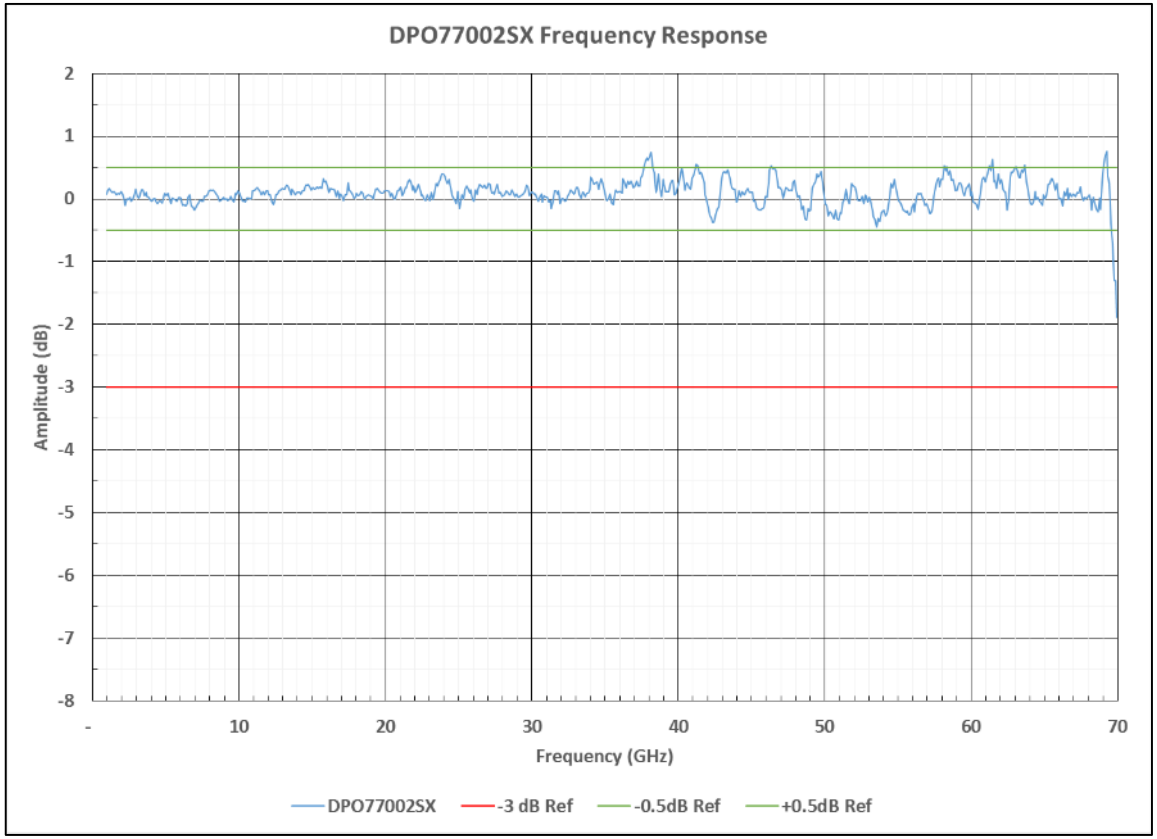
Legacy Frequency Interleaving



- Each ADC sees **half** spectrum
- Signal reconstruction involves *summation* → no improvement in SNR

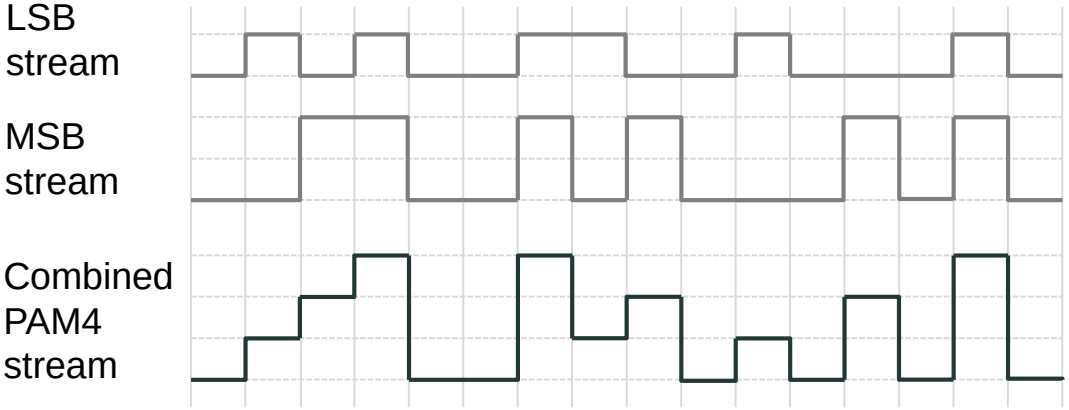
70GHz ATI frequency response Flatness

- Current data shows very good frequency response flatness
- Expect ±0.5dB to 50% and ±1.5dB to 80% of BW (typical)

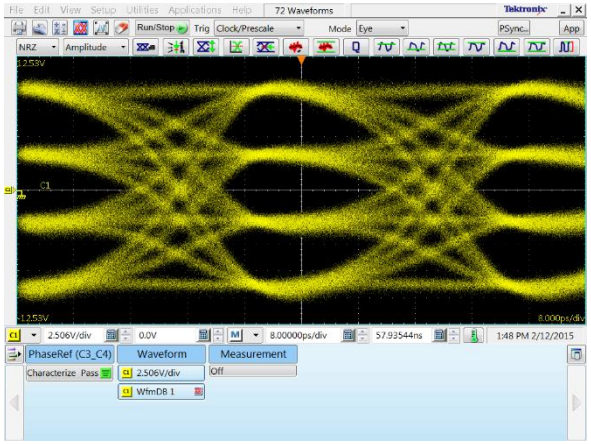


100Gbase-KP4 What is PAM?

- **P**ulse **A**mplitude **M**odulation
  - –PAM4 combines two bit streams and uses 4 levels to encode 2 bits into 1 UI
  - –For Example, 56 Gbit/s PAM4 runs at a symbol rate of 28 GBaud

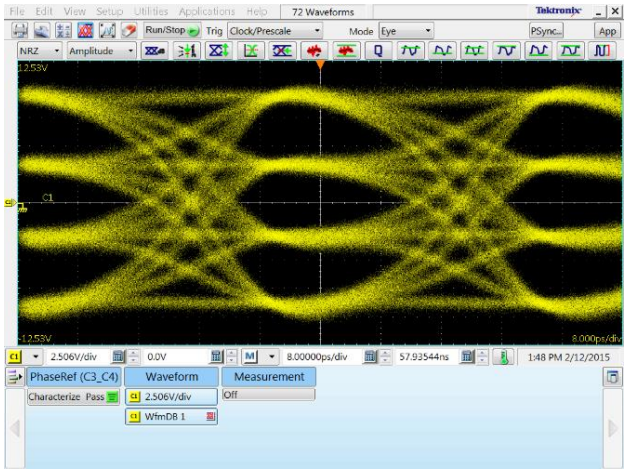


MSB	LSB	PAM4 LEVEL
0	0	0
0	1	1
1	0	2
1	1	3

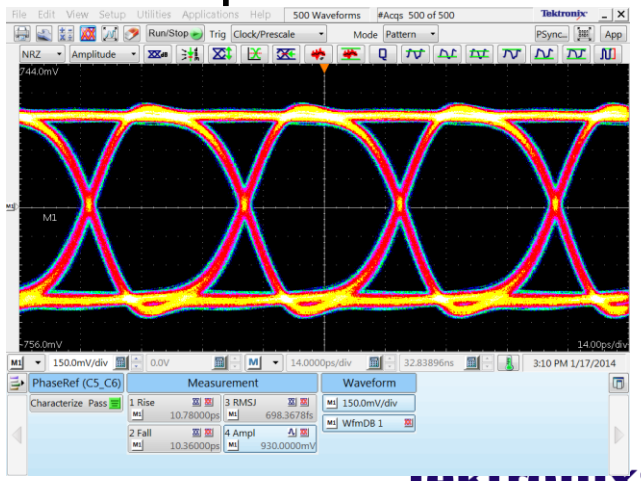


What are the differences between PAM4 and NRZ?

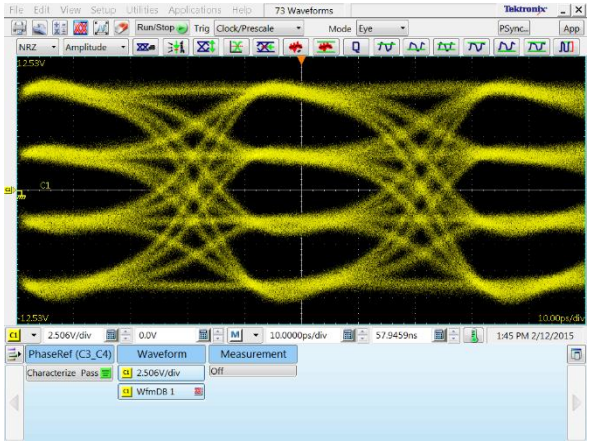
- PAM4
  - 4 Levels -> 3 Eyes
  - Sensitive to SNR (eyes smaller)
  - 2 bits into 1 UI
  - ½ Baud Rate for same data throughput (28 GBaud = 56Gbps)
  - Adds complexity/cost to Tx/Rx



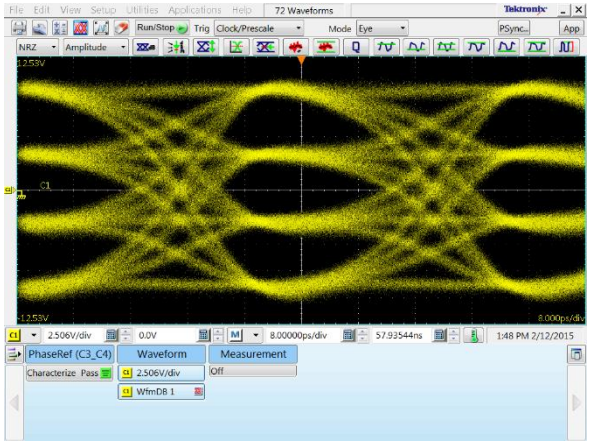
- NRZ
  - 2 Levels -> 1 Eye
  - Less Sensitive to SNR
  - 1 bit in 1 UI
  - 2X Baud Rate for same data throughput (28GBaud = 28Gbps)
  - Less expensive Tx/Rx



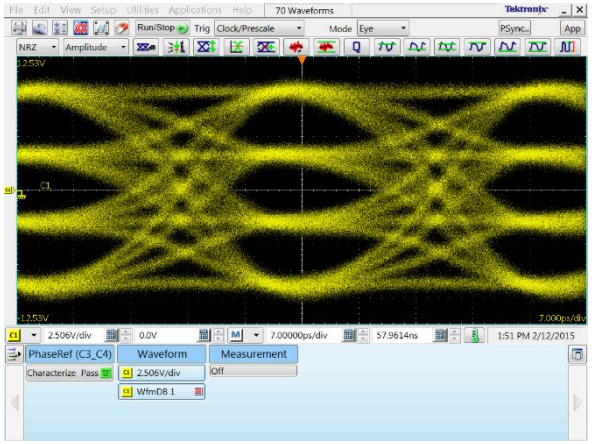
Tektronix PAM4 Signal Generation Performance



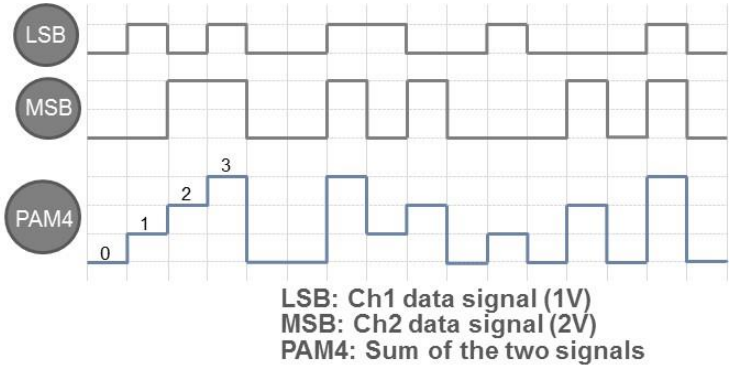
25Gbaud

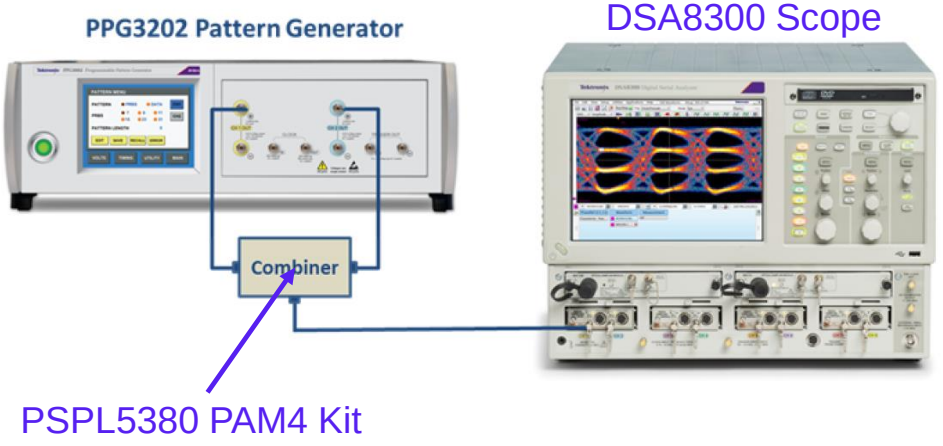


28Gbaud



32Gbaud





Tektronix 100G/400G BERT Signal Generation System

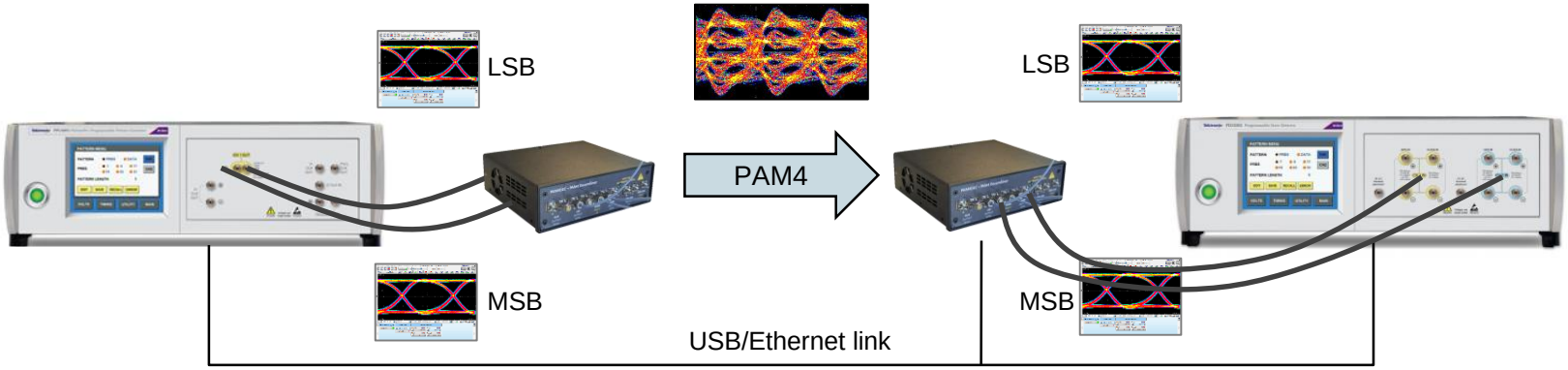
Signal generation • Signal Acquisition • Software Control and Analysis

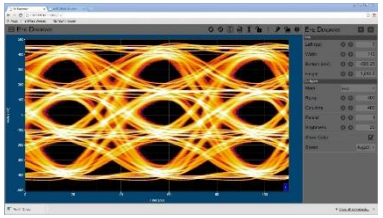
PAM4 signal generation

- Programmable Tx pre-emphasis for device and channel loss compensation
- Independent programming of LSB and MSB data
- PRBS31 and user data patterns

PAM4 signal acquisition

- Auto-alignment of PAM4 signal at decoder
- Integrated clock recovery
- True hardware BER measurement of all LSB and MSB data
- PRBS31 and user data patterns





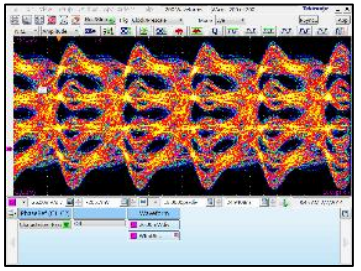
PAM4 control software

- Full GUI with PAM4 eye display at decoder input
- Signal generation and analysis control from a single software console
  - Full pattern and pre-emphasis control
  - Measurement point alignment and control
  - BER measurement and analysis

Tektronix 100G/400G BERT System

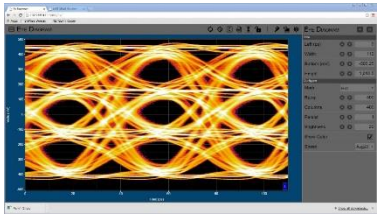
Signal generation • Signal Acquisition • Software Control and Analysis

- **Only dedicated PAM4 BERT system in the industry**
  - True PAM4 signal generation, acquisition, measurement, and system control
  - Equipment and software designed specifically for PAM4 testing
- Signal Generation
  - Remote head with programmable pre-emphasis
    - Independent control of LSB and MSB amplitude and pre-emphasis levels
    - Re-timing of signal at remote head to minimize PAM4 signal DDJ from long cables
  - Independent control of LSB and MSB data
    - Built-in PRBS and programmable user data
    - Independent patterns on LSB/MSB or split between LSB/MSB



Pre-emphasized PAM4 Signal

- Signal Acquisition
  - Remote head with true PAM4 eye measurement and decoding
    - PAM4 diagnostic eye measured directly at decoder input
    - Separate, full adjustment of PAM4 sample points (threshold, time)
    - Re-timing of signal at remote head to minimize PAM4 signal DDJ from long cables
  - Integrated clock recovery
  - Hardware decoding of LSB and MSB data

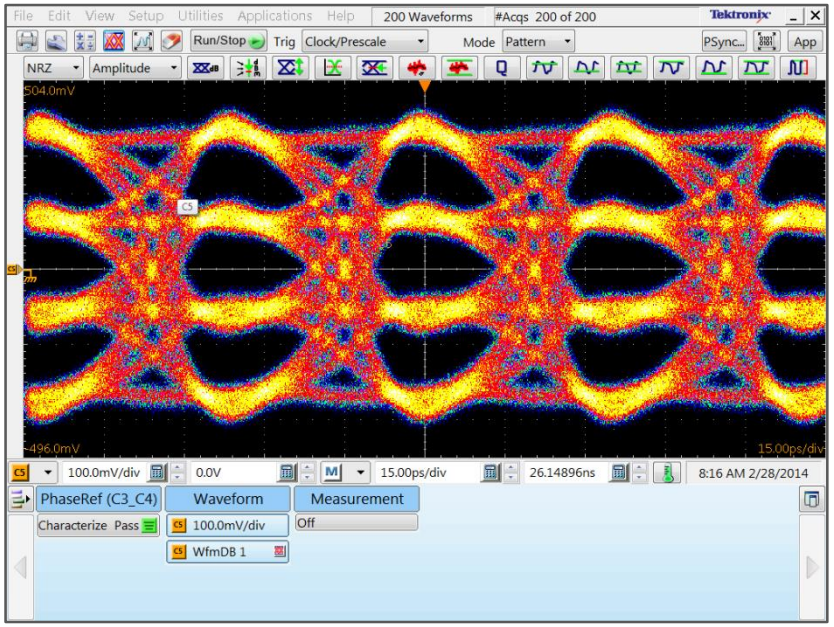


Diagnostic PAM4 Eye Diagram and System Analysis/Control

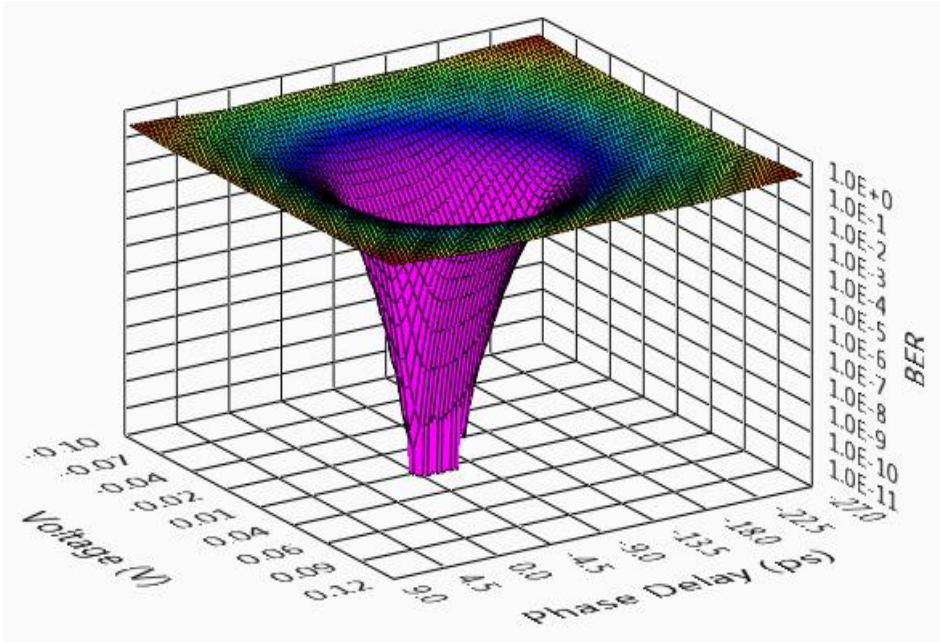
- Software Control and Analysis: Single console for full control of PAM4 BERT system
  - Signal generation and acquisition (patterns, pre-emphasis, sample points)
  - Signal analysis (diagnostic eye, LSB/MSB BER, bathtub curves, etc.)

Example data with PPG3202 2 channel 32Gb/s generator and external combiner:

28G PAM4 PRBS23/31 Eye Diagram and Contour Plot



Eye diagram measured with 60GHz sampler and precision timebase. PRBS23 pattern on LSB and PRBS31 pattern on MSB.



Contour plot measured with error detector and PatternPro software.

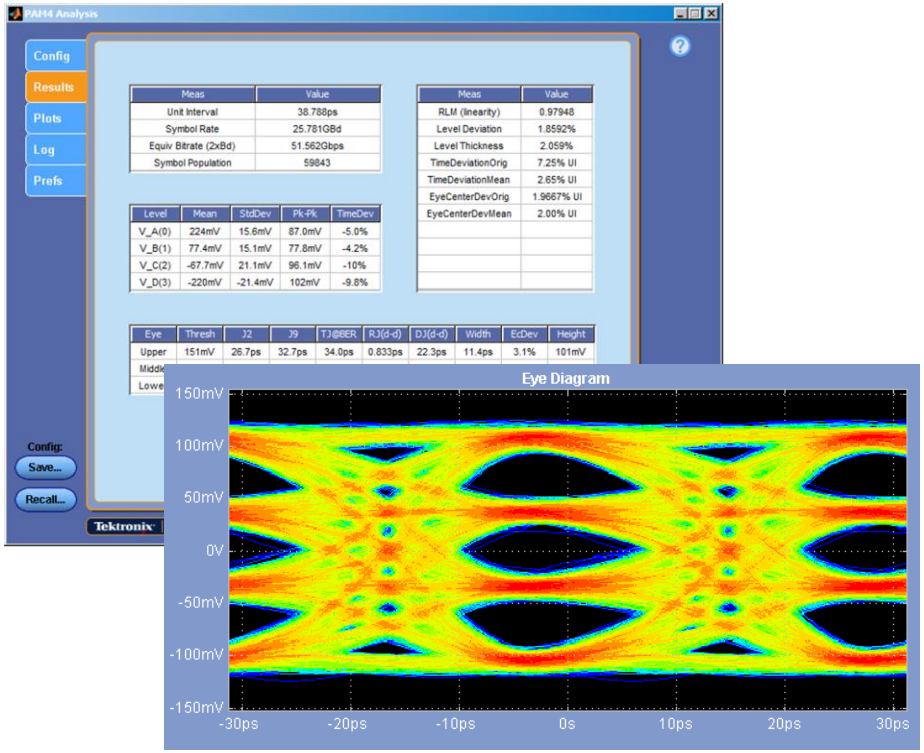
Eye opening is reduced from NRZ eye by PAM4 added deterministic jitter. Contour slope is steep due to low RJ. Small changes in cables/etc have large impact on BER floor due to slim DJ margins at 28G.

PAM4 Transmitter Solution on Real time scope

- PAM4 Clock Recovery
- CTLE/DFE Equalization
- Channel Embedding/De-Embedding

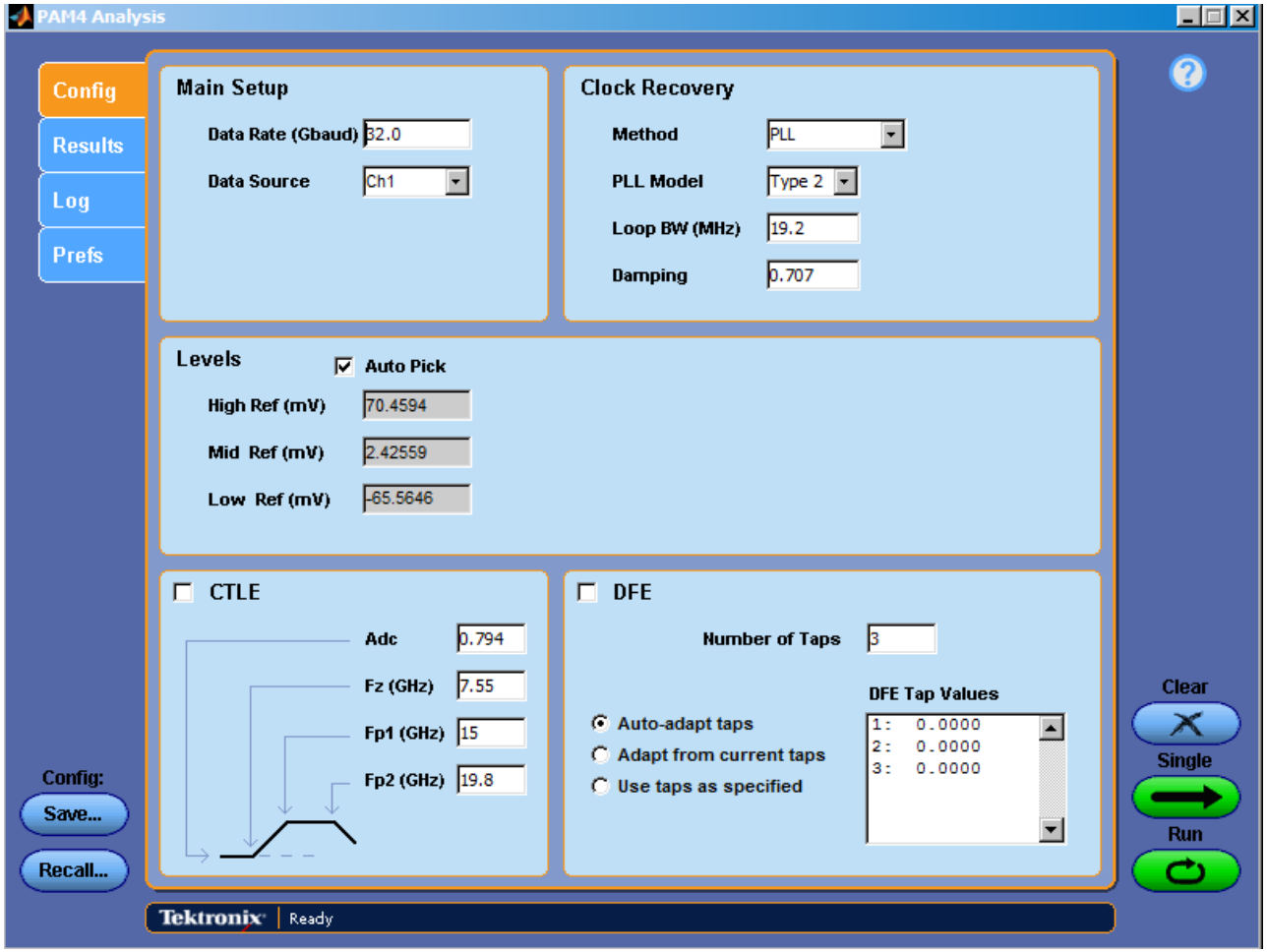
- Comprehensive Measurements
  - Level separation mismatch - R_{LM}
  - Time and Level Deviation
  - Level Thickness
  - Jitter (RJdd, DJdd, TJ, J2, J9)
  - Eye Height
  - Eye Width
  - Noise Analysis (Phase 2)

- DPO70000SX/DX/C
  - PAM4 Analysis with Jitter and Noise
    - Opt. PAM4, DJA, DJAN
  - Channel Embedding/De-Embedding and Equalization
    - Opt. SDLA64

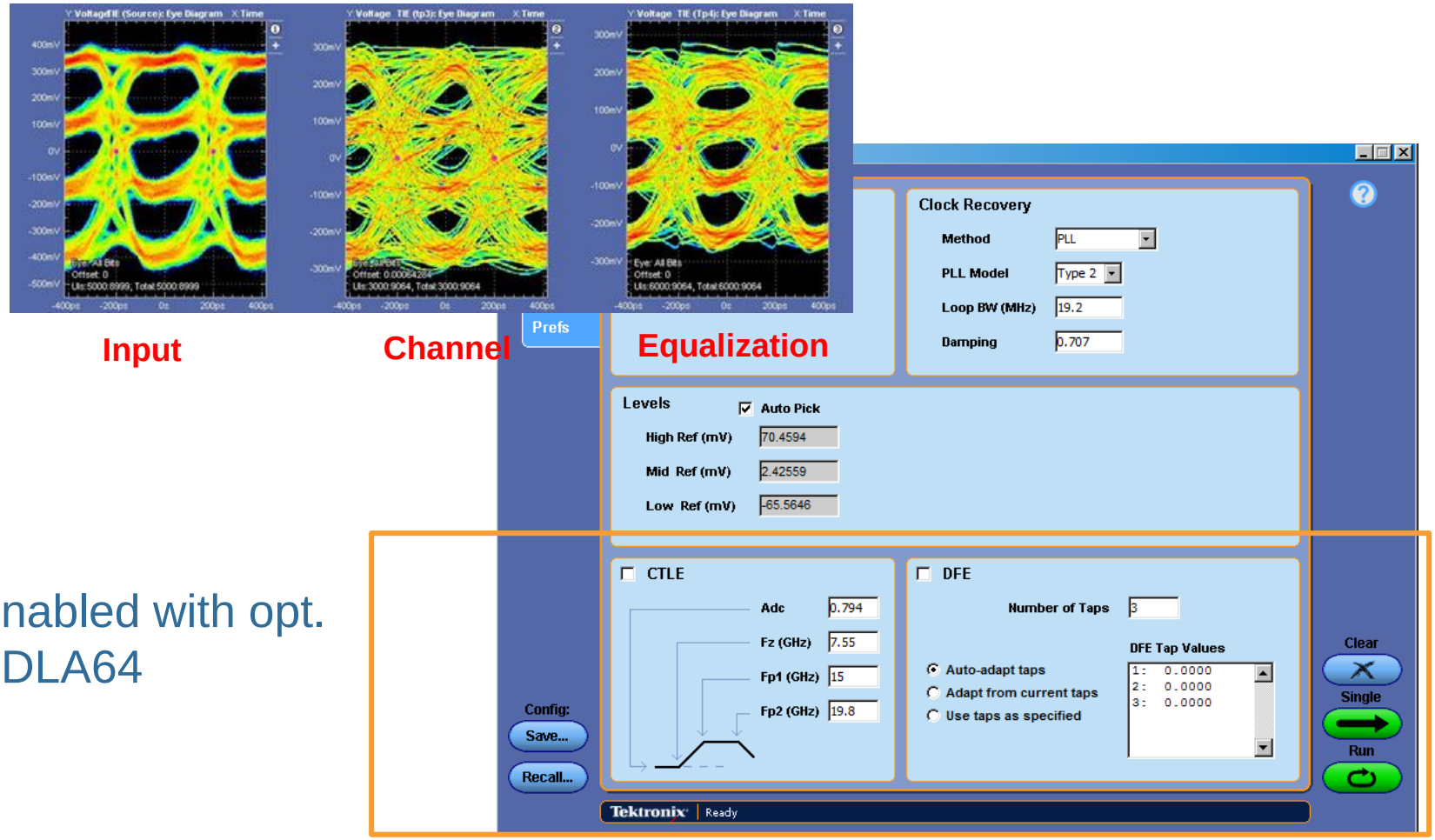


Clock Recovery

- New Clock Recovery for PAM
  - PLL- Type 1 and 2
  - Explicit Clock

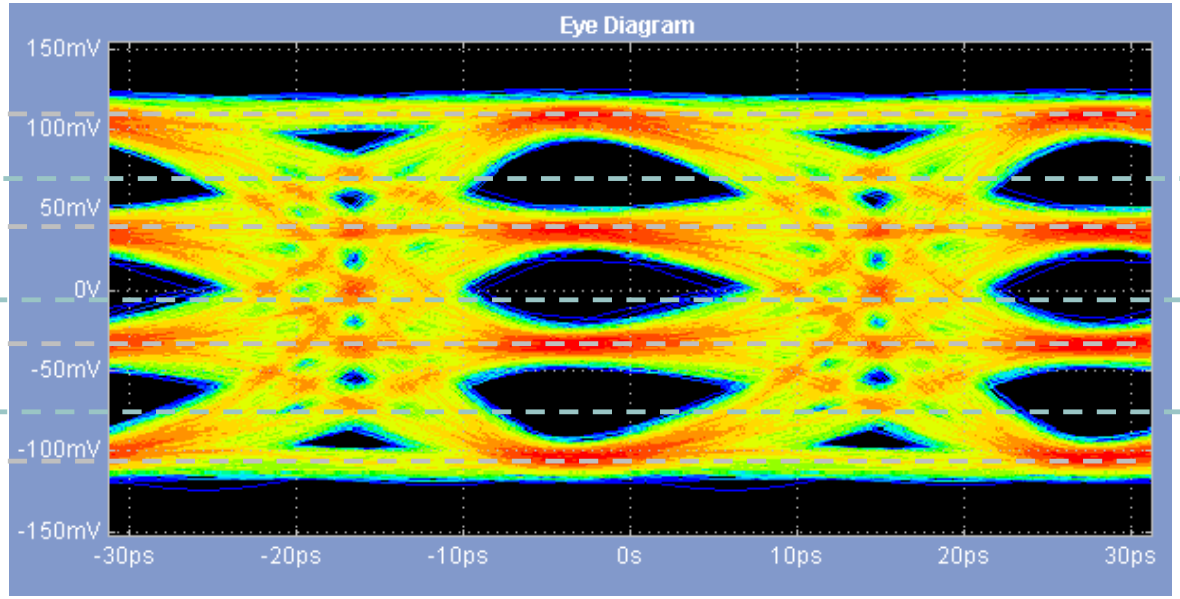


CTLE / DFE Equalization



Enabled with opt. SDLA64

TX Measurements
PAM4 Levels and Thresholds



Level 3

Level 2

Level 1

Level 0

Threshold 2 - 3

Threshold 1 - 2

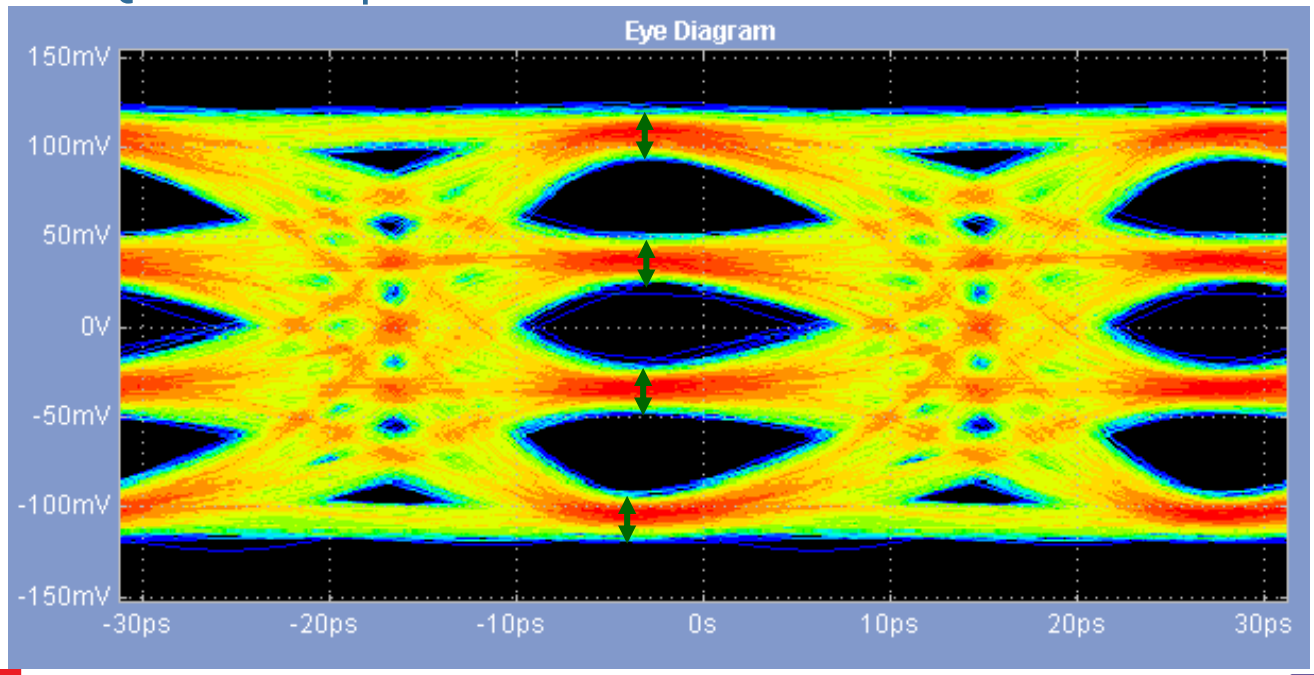
Threshold 0 - 1

Levels are used for determining the thresholds, calculating noise, linearity, time deviation
Thresholds are used to calculate jitter, eye centers and other eye parameters

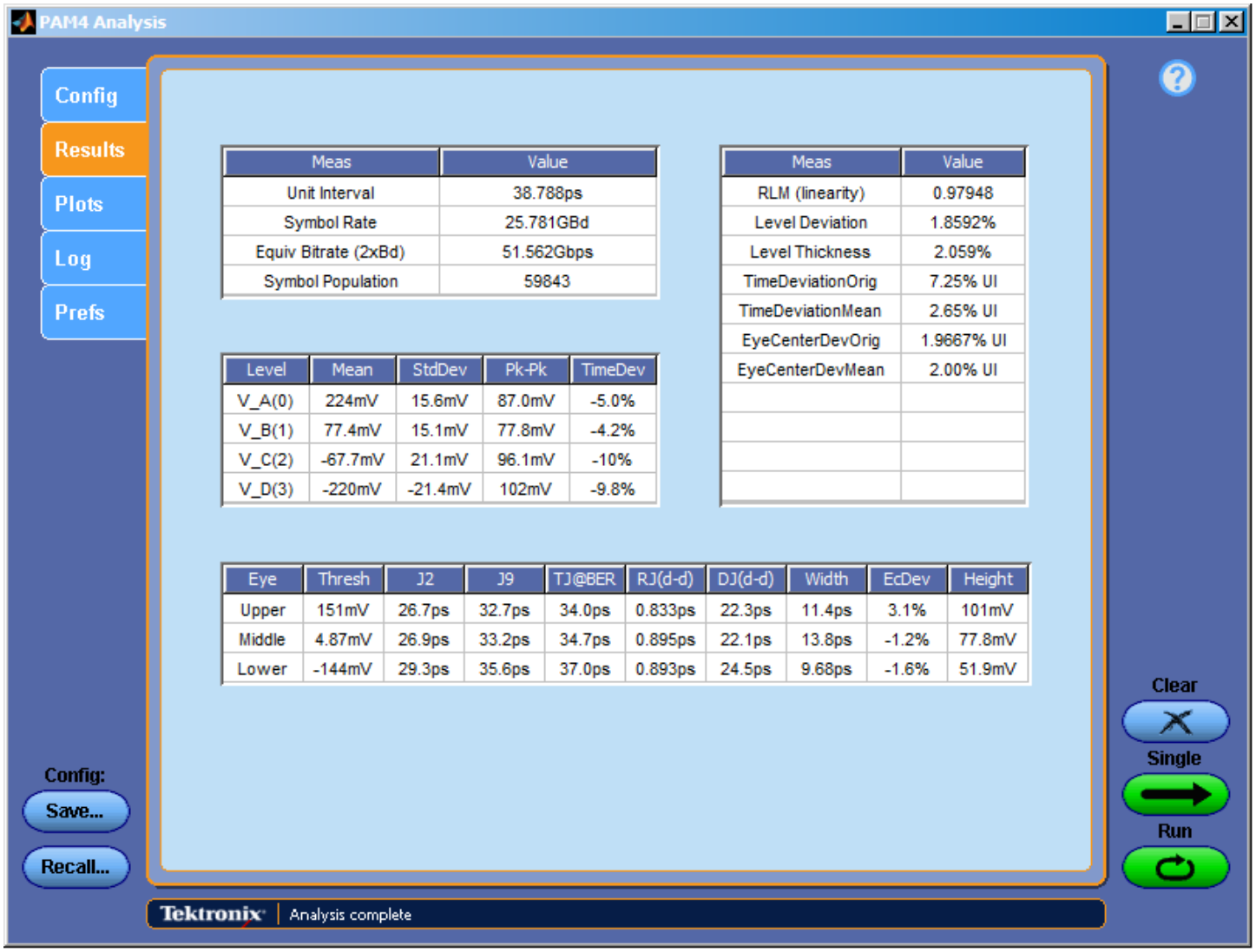
Levels and Thresholds are automatically detected or can be manually configured

TX Measurements
Level Thickness and Deviation

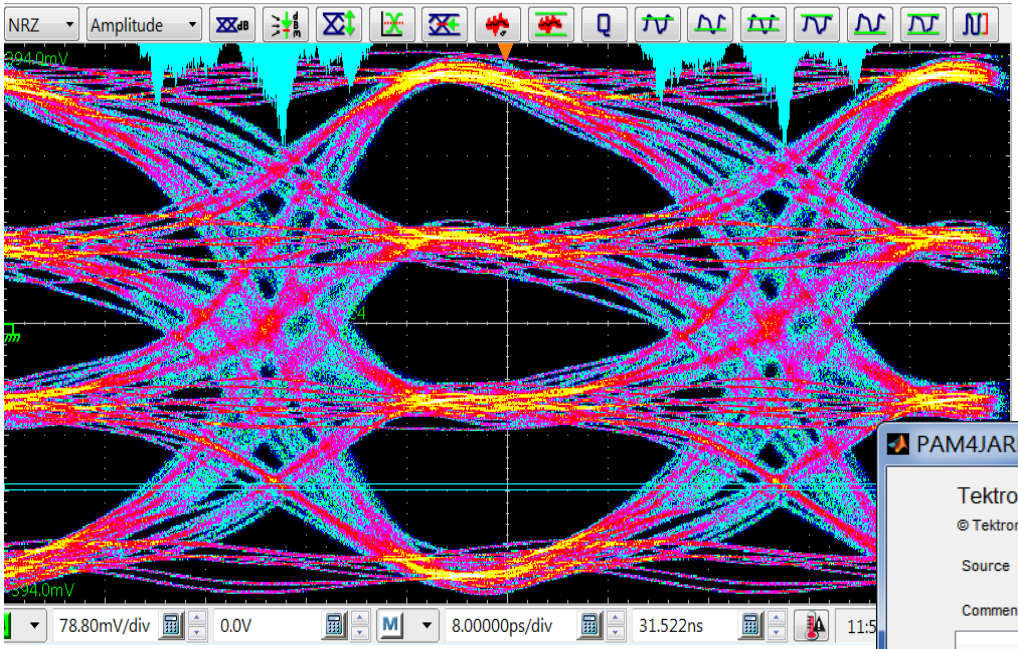
- Thickness- Measures thickness of each symbol level
- Deviation
  - Characterize timing properties of the signal and non-linear artifacts in the driver
  - Look at the skew between the narrowest point on each level
- Done on QPRBS13 pattern



DPOJET PAM4 (Real Time)



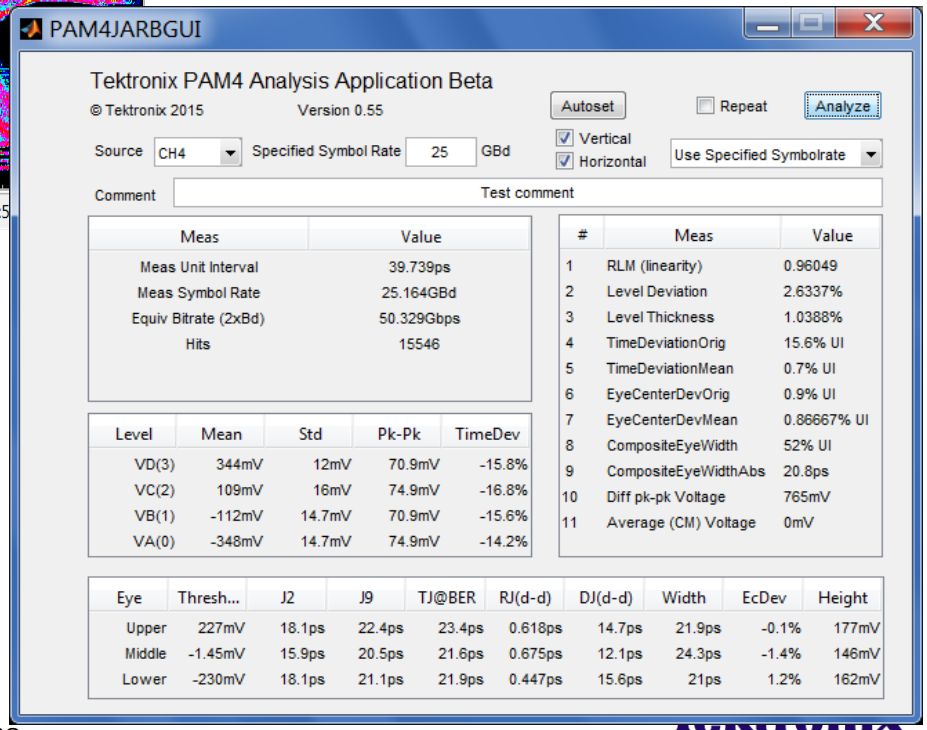
Tektronix 400G PAM TX Analysis on Sampling scope



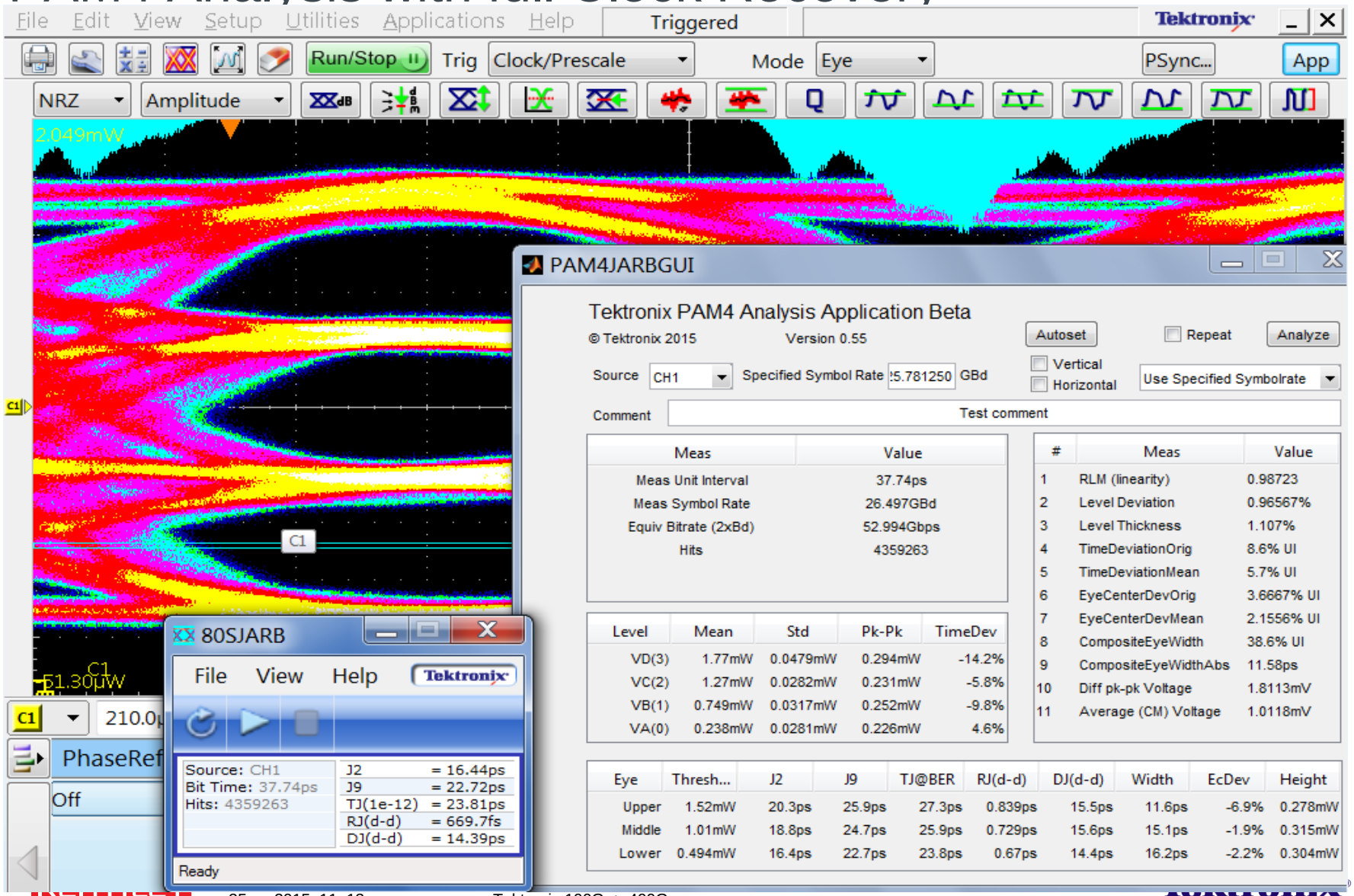
DSA8300 Sampling Oscilloscope

- Software Opt. JNB02 and ADVTRIG
- 80E09B 60 GHz Electrical Sampling Module
- 82A04B Phase Reference Module
- Optical I/O - add one of the following:
  - 80C14 for Multi-mode PAM to 16 Gbps
  - 80C15 for Multi-mode PAM to 28 Gbps
  - 80C10C for Single mode PAM

- Available Measurements (O/E)
  - Level separation mismatch - R_{LM}
  - Time and Level Deviation
  - Level Thickness
  - Eye Center Deviations
  - Composite Eye Width
  - Jitter
  - Eye Height and Width



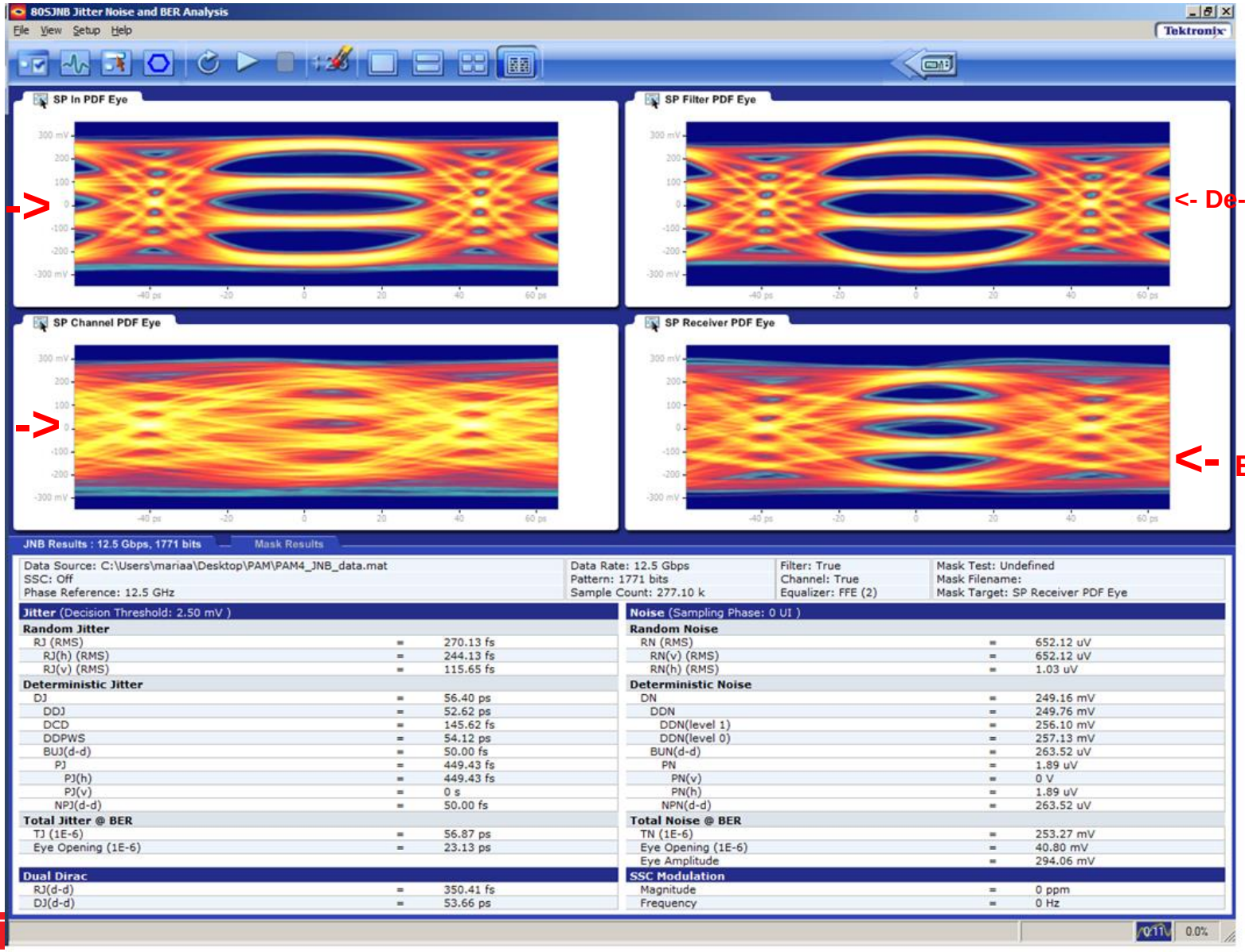
DSA8300 Sampling Oscilloscope, Optical 56GBaud PAM4 Analysis with full Clock Recovery



PAM4 signal path compensation and CTLE

Input ->

Channel ->

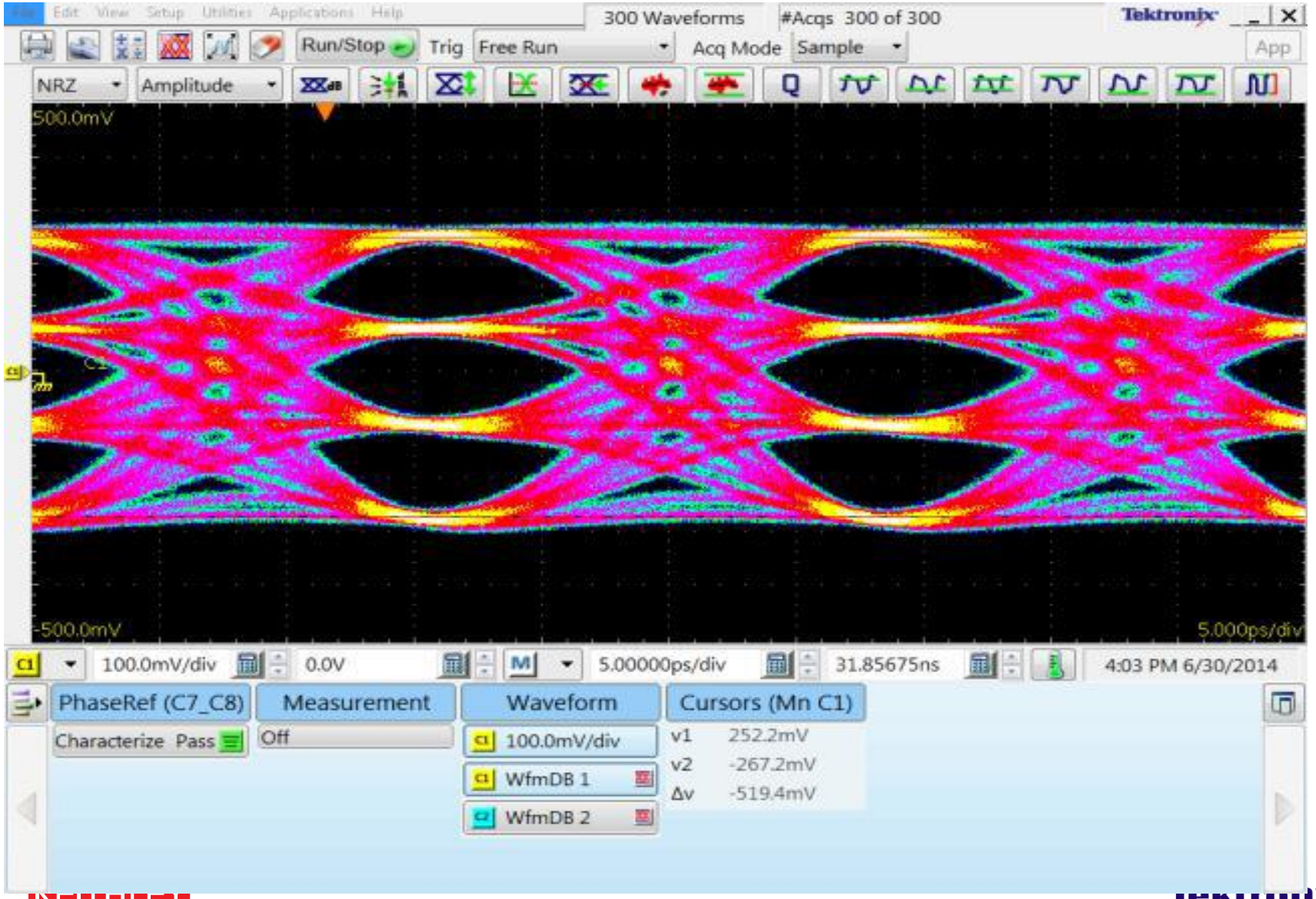


<- De-embedded

<- Equalized

KEI
A Tek

56 GBaud *Yes that is* PAM-4 at 112 Gbit!



Tektronix 100GBASE-SR4 Test Solutions

Tektronix®

What is 100GBASE-SR4?

- IEEE 802.3bm 100G standard, defining 4 x 25Gb/s interconnects over multi-mode fiber (MMF), with a range of up to 100m
- RS-FEC is mandatory for 100GBASE-SR4
- Supports CFP2, CFP4, and QSFP-28 transceivers

Tx Test

SR4 Tx Measurements

Table 95–6—100GBASE-SR4 transmit characteristics

Description	Value	Unit	Supported by Tek Tx measurement tools
Signaling rate, each lane (range)	25.78125 ± 100 ppm	GBd	✓
Center wavelength (range)	840 to 860	nm	
RMS spectral width[a] (max)	0.6	nm	
Average launch power, each lane (max)	2.4	dBm	✓
Average launch power, each lane (min)	–8.4	dBm	✓
Optical Modulation Amplitude (OMA), each lane (max)	3	dBm	✓
Optical Modulation Amplitude (OMA), each lane (min)[b]	–6.4	dBm	✓
Launch power in OMA minus TDEC (min)	–7.3	dBm	✓
Transmitter and dispersion eye closure (TDEC), each lane (max)	4.3	dB	✓
Average launch power of OFF transmitter, each lane (max)	–30	dBm	✓
Extinction ratio (min)	2	dB	✓
Optical return loss tolerance (max)	12	dB	
Encircled flux[c]	≥ 86% at 19 μm ≤ 30% at 4.5 μm		
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 1.5×10^{-3} hits per sample	{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}		✓

Notes

- Full TDEC Tek test solution currently in process, using Tek Tx instruments in currently in place
- Center wavelength, RMS spectral width, Optical Return Loss, and Encircled Flux supported by alternate instruments

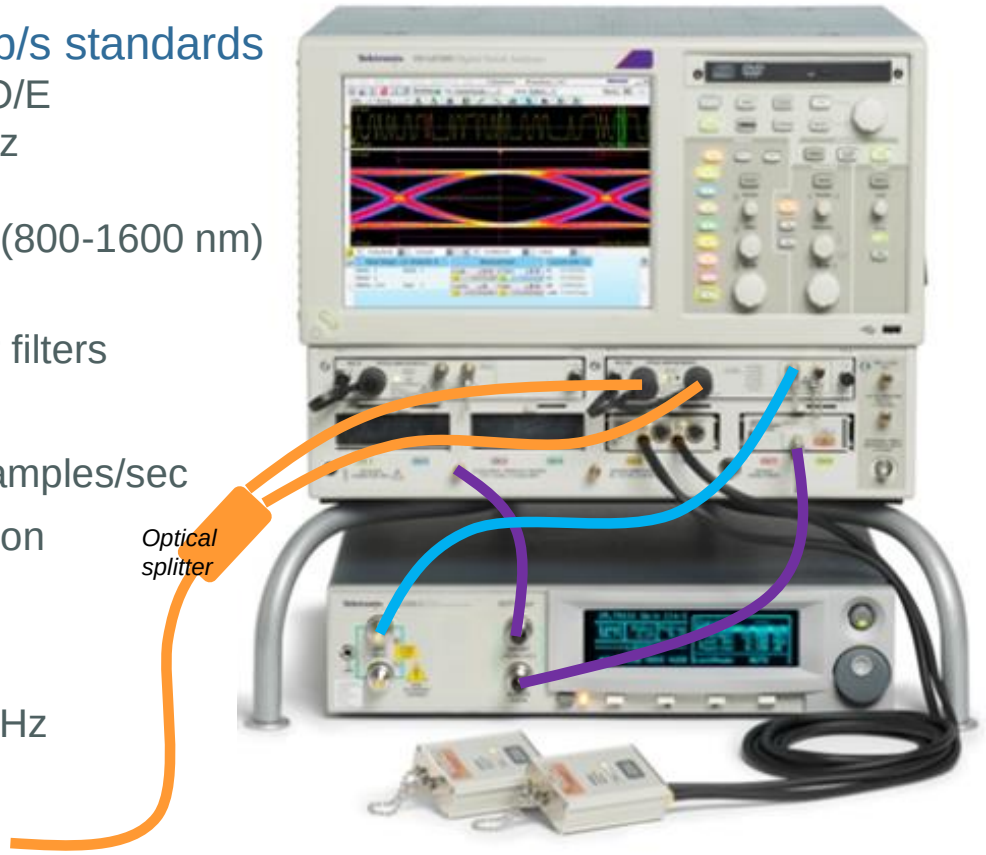
Tx Test
SR4 Transmitter Test Configuration

Item	Description	Qty
DSA8300/ADVTRIG/JNB02	Sampling scope mainframe	1
82A04B	Phase reference module	1
CR286A/HS/XLBW	Clock Recovery module	1
80C15 with option CRTP	Optical plugin for DSA8300 with CRTP option	1
80A08	Accessory kit	1

Sampling Scope System

Optical CDR, MM or SM Fiber, 28.6Gb/s

- CDR for optical MM & SM 25-28.5Gb/s standards
  - Optical head with dedicated Trigger O/E
  - Un-filtered Optical Bandwidth >35GHz
  - 62.5/125 µm Multi-Mode Fiber Input
  - Short and Long Wavelength Support (800-1600 nm)
  - Trigger O/E -15dBm sensitivity
- 100Gbase-LR4/ER4/SR4 optical receiver filters
- Best optical MM sensitivity to -9dBm
- Highest acquisition throughput @ 180kSamples/sec
- Jitter and noise analysis and decomposition
- CTLE filter application
- Embedding and de-embedding
- TDR, insertion, and return loss up to 50GHz
- RIN & RINxOMA support

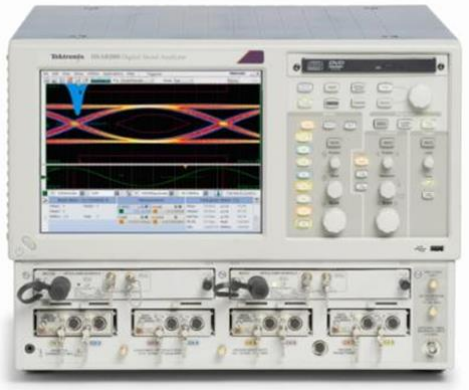


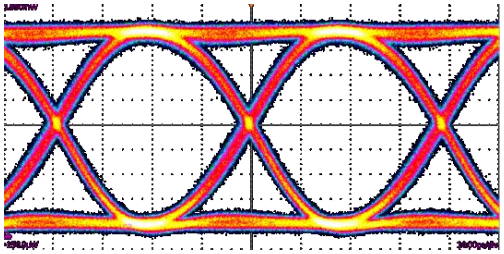
Tektronix 80C15 Optical Sampling Module Highlights

NEW

80C15

- Single-Channel Optical Plug-in Module for DSA8300
- Unfiltered Optical Bandwidth >32 GHz
- 62.5/125 µm Multi-Mode Fiber Input
- Short- and Long-Wavelength Support 780-1650 nm
- 200 kS/s Acquisition Rate
- Jitter Floor <150 fs_{RMS} (with 82A04B)
- Reference Receiver Filters:
  - ✓ 32G FibreChannel (28.05 Gb/s)
  - ✓ OTU4 (27.95 Gb/s)
  - ✓ 100Gbase-LR4/ER4/SR4 (25.78 Gb/s)
  - ✓ 26G EDR Infiniband (25.78 Gb/s)





26 Gb/s

Tx Test

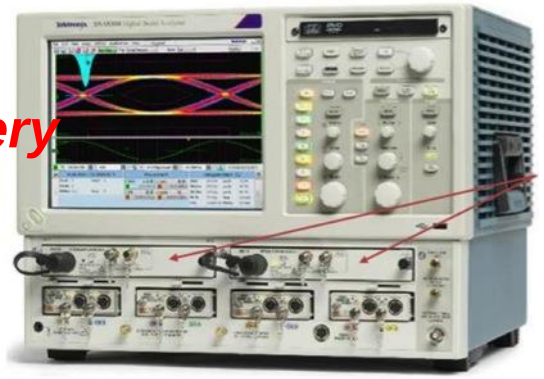
80C15: Tektronix Optical portfolio with unmatched accuracy, noise performance, and flexibility

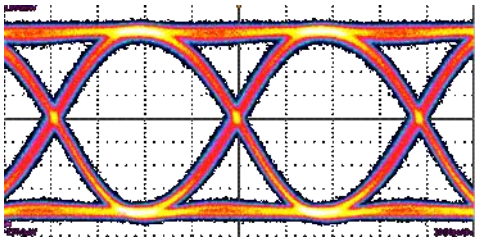
Feature / Specification	80C15
Input Fiber Type	SMF + MMF 9, 50, 62.5 µm
Wavelength Range	780nm-1650nm
Unfiltered Optical Bandwidth	32+ GHz
Unfiltered Risetime, typ	14 ps
Filter Rates	25.78 – 28.05 Gb/s
26 Gb/s Mask Test Sensitivity AOP @ 1310nm	*-9 dBm*
Usable Electrical Out	*32 Gb/s*

Tektronix 80C15 module, optional CRTP (Electrical Out)

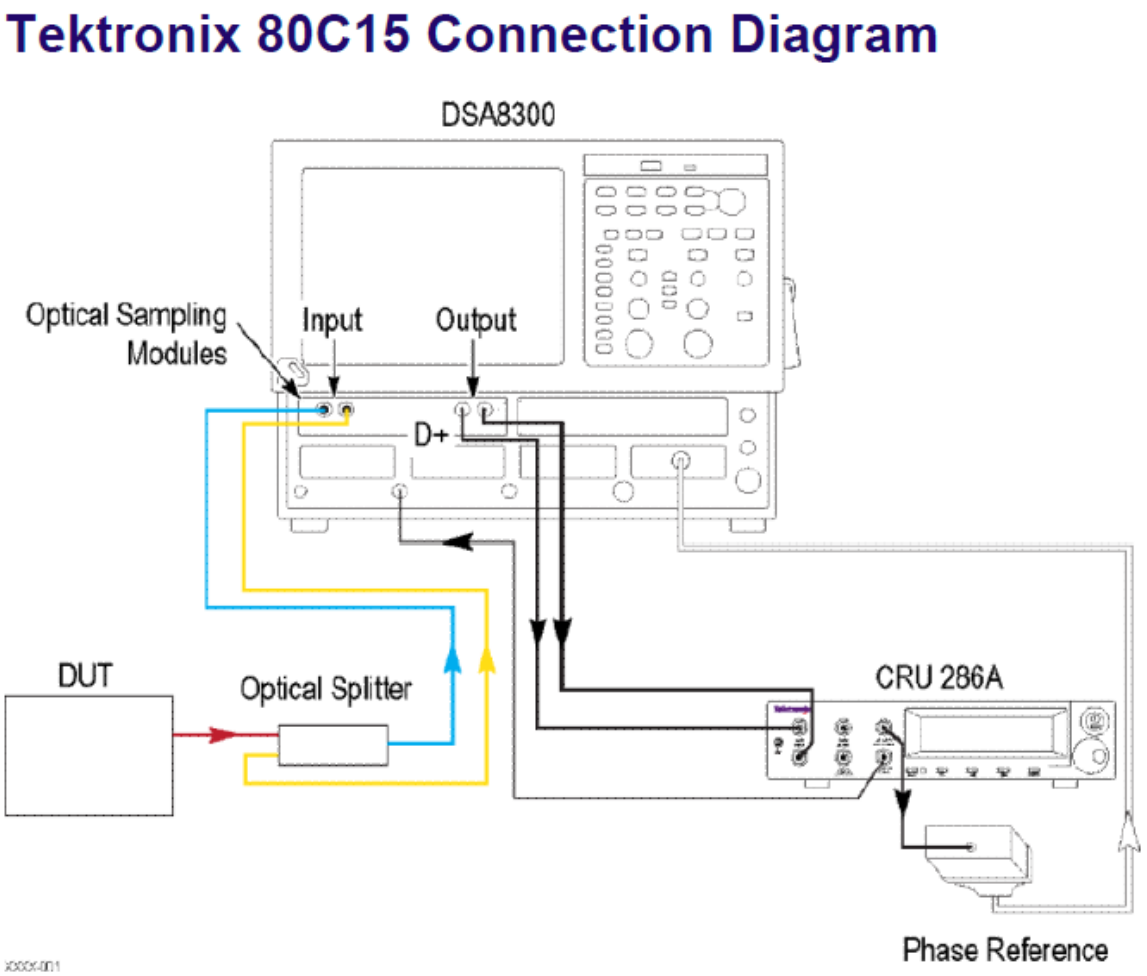
80C15 CRTP

- Single-Channel Optical Plug-in Module for DSA8300 *with optional* ***Electrical Clock Recovery Trigger Pickoff (CRTP)***
- Unfiltered Optical Bandwidth >32GHz
- 62.5/125 µm **Multi-Mode** Fiber Input
- **Short-** and Long-Wavelength Support (800 -1600 nm)
- 200 kS/s Acquisition Rate
- **Jitter Floor <150 fs RMS (with 82A04B)**
- Optical Receiver Filters:
  - **32G Fibre Channel (28.05 Gb/s)**
  - OTU-4 (4 x 27.95 Gb/s)
  - 100Gbase-LR4/ER4/SR4 (25.78 Gb/s)
  - 26G EDR Infiniband (25.78 Gb/s)





Connection for 80C15



Rx Test
SR4 Receiver Test Specifications and Algorithm

Table 95–7—100GBASE-SR4 receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm	GBd
Center wavelength (range)	840 to 860	nm
Damage threshold[a] (min)	3.4	dBm
Average receive power, each lane (max)	2.4	dBm
Average receive power, each lane[b] (min)	–10.3	dBm
Receive power, each lane (OMA) (max)	3	dBm
Receiver reflectance (max)	–12	dB
Stressed receiver sensitivity (OMA), each lane[c] (max)	–5.2	dBm
Conditions of stressed receiver sensitivity test:[d]		
Stressed eye closure (SEC), lane under test	4.3	dB
Stressed eye J2 Jitter, lane under test	0.39	UI
Stressed eye J4 Jitter, lane under test (max)	0.53	UI
OMA of each aggressor lane	3	dBm
Stressed receiver eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5×10^{-5} hits per sample	{0.28, 0.5, 0.5, 0.33, 0.33, 0.4}	

Supported by Tek Rx measurement tools

Notes
- Center wavelength and receiver reflectance supported by alternate instruments

100 GBASE-SR4 and TDEC

- 100GBASE-LR4, ER4 and PSM4 and CLR4 are all supported by 80C15 and 80C10C
- 100GBASE-SR4 bring MM; 80C15 can handle all of that
- What are the new measurement in SR4?

95.8.5.1 TDEC conformance test set-up

A block diagram for the TDEC conformance test is shown in Figure 95–3. Other measurement implementations may be used with suitable calibration.

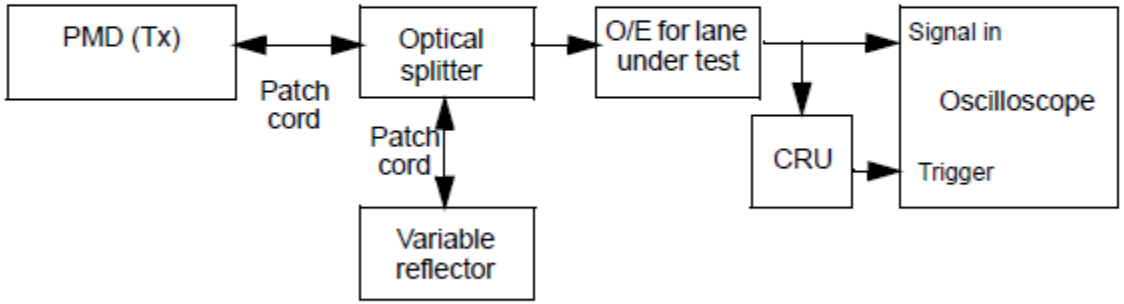


Figure 95–3—TDEC conformance test block diagram

TDEC measurement process

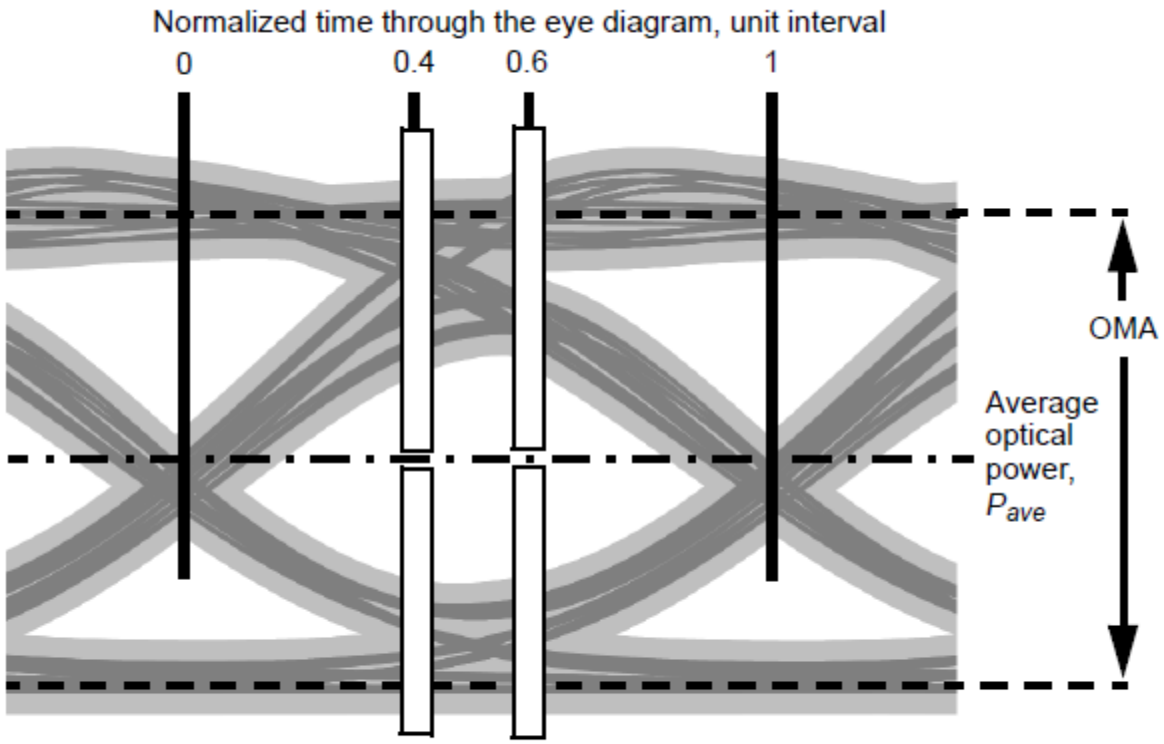


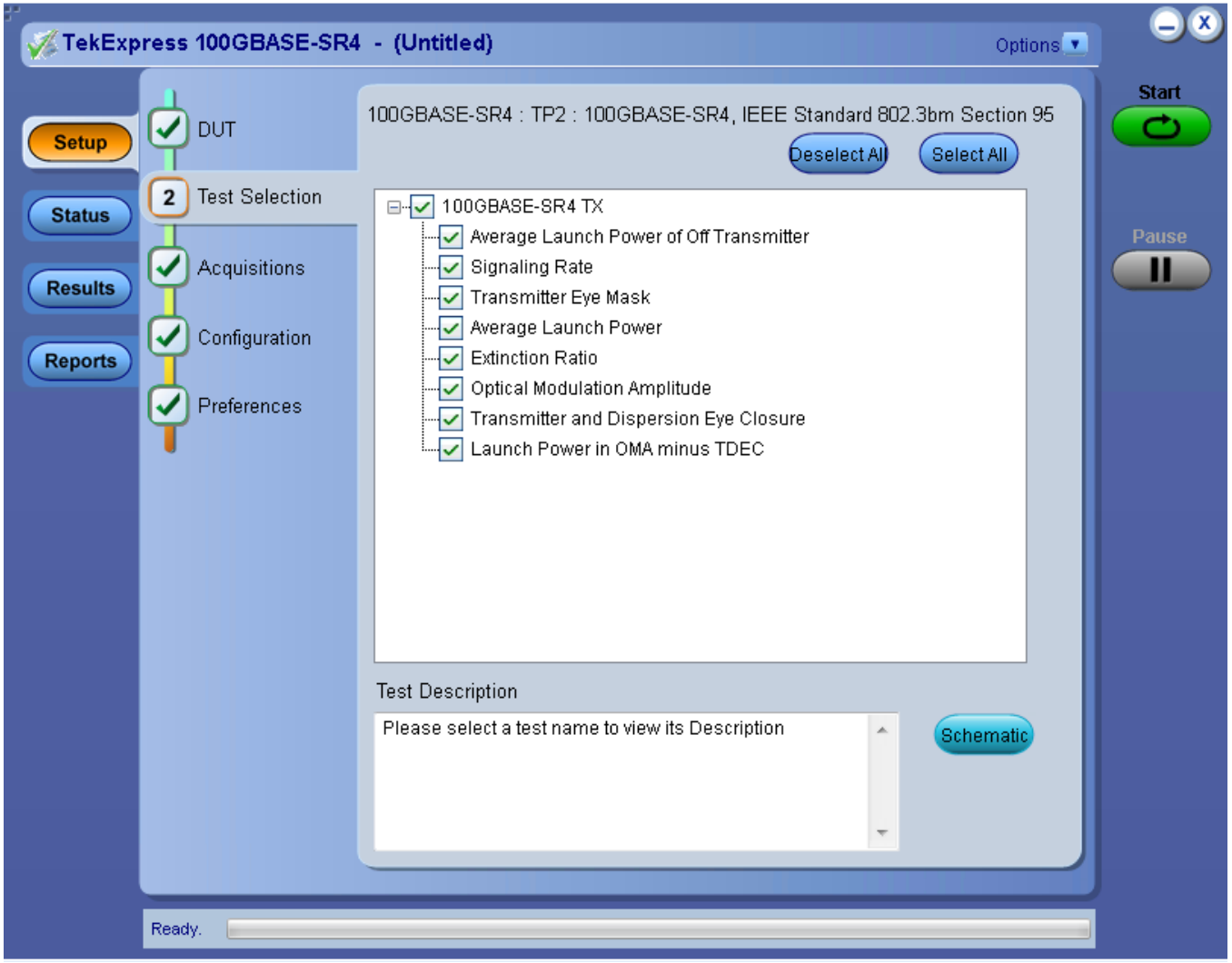
Figure 95–4—Illustration of the TDEC measurement

- Relatively complicated processing of several histograms
- Transmitter and dispersion eye closure(<4.3dB)

TDEC is given by Equation (95–6).

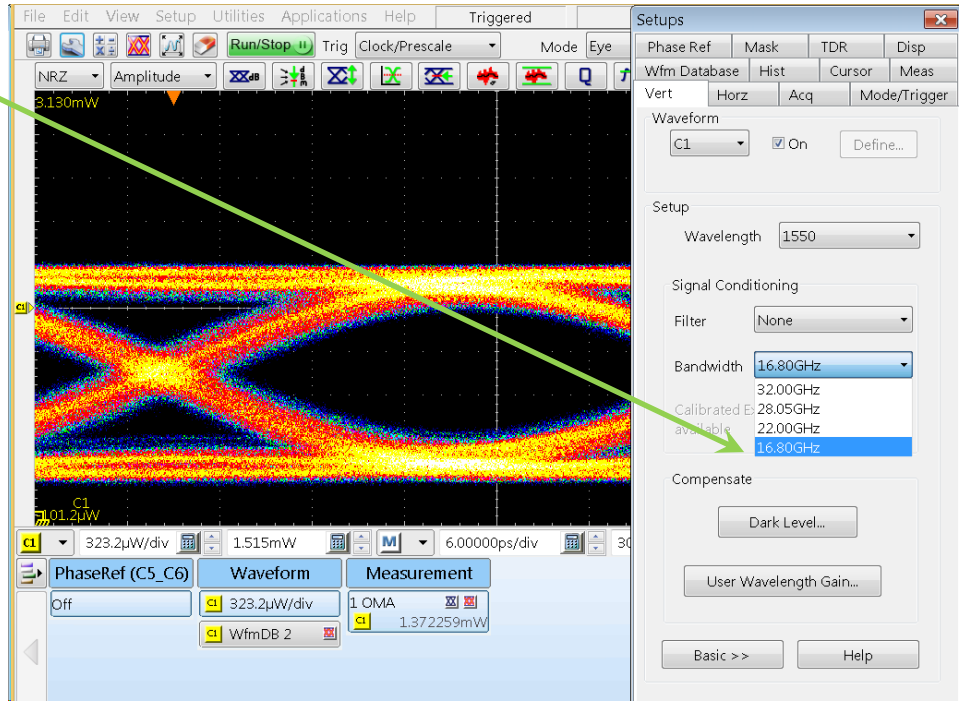
$$TDEC = \left|10\log_{10}\left(\frac{OMA}{2} \times \frac{1}{3.8906R}\right)\right|$$

100GBASE-SR4 and TDEC measurement automated with TekExpress



TDEC (Transmitter and dispersion eye closure) a penalty of an optical Transmitter

- TDEC is at best 0 dB (i.e. no penalty – the TX is IDEAL)
- Standards set the highest TDEC (highest penalty) allowable
- TDEC for Multi Mode fiber uses special BW limiting in the module:
- Discussion on SR4 and TDEC



Rx Test
SR4 Receiver Test Algorithm

Recommended SR4 RX test algorithm:

- Configure setup per slide 11
- Measure SEC, J2, and J4 using DSA8300
- Iteratively adjust SI insertion from AFG and RJ insertion from PPG until Table 95-7 specs for SEC, J2, and J4 are simultaneously met

Notes:

- Tektronix SR4 Solution requires E/O and O/E test components
  - 80C15 can be used with DSA300 for O/E
  - Recommended external E/O options available upon request

SR4 Stressed Receiver Block Diagram

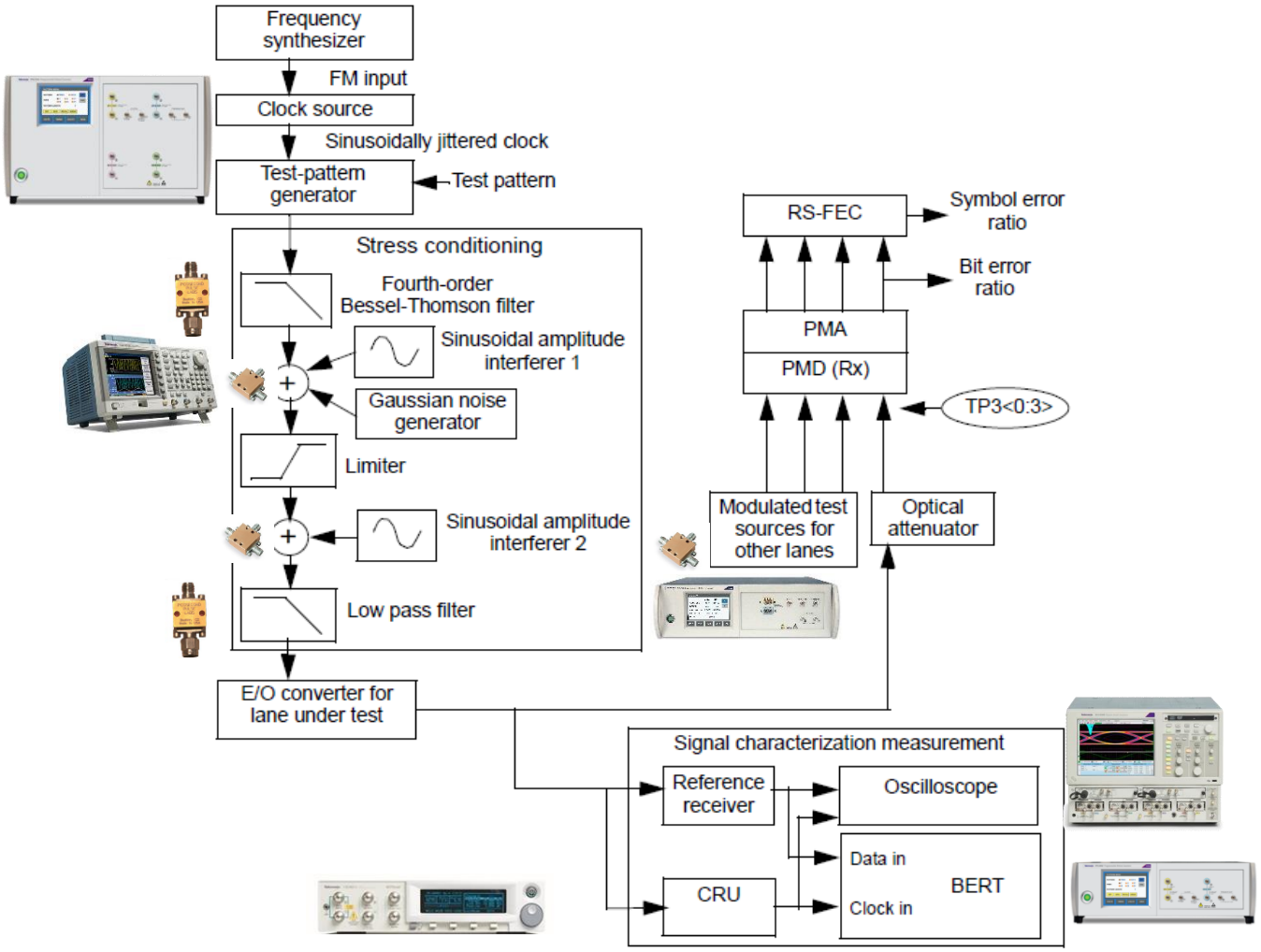


Figure 95–5—Stressed receiver conformance test block diagram

SR4 Receiver Test Configuration

Item	Description	Qty
PPG3204/HFJ/ADJ	4-ch 32Gb/s PPG w/ jitter insertion	1
PED3202	2-ch 32Gb/s error detector	2
DSA8300/ADVTRIG/JNB02	Sampling scope mainframe	1
80C15	Optical plugin for DSA8300	1
PPG3002, crosstalk generator	2CH 30G PPG	1
PSPL5333, crosstalk generation	1:2 power splitter	2
AFG325C	240 MHz function generator	1
CR268A	Clock recovery module	1
PSPL5361	40GHz pick off T	2
80A08	Accessory kit	1

Rx Test
SR4 Pattern Requirements

Table 95–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 ones, 8 zeros)	83.5.10
3	PRBS31	83.5.10
4	PRBS9	83.5.10
5[a]	RS-FEC encoded scrambled idle	82.2.10[a]

[a]The pattern defined in 82.2.10 as encoded by Clause 91 RS-FEC for 100GBASE-SR4

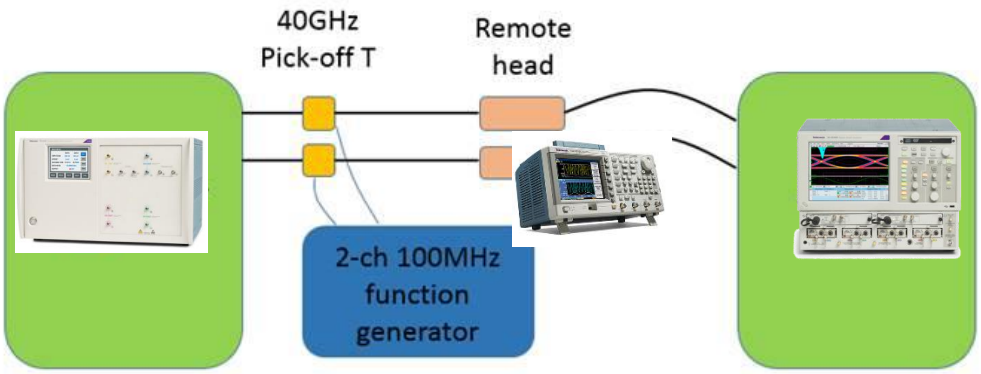
- SR4 test requires both user pattern and PRBS generation
- PatternPro PPG and PED can generate full suite of PRBS patterns, as well as any user patterns up to 2Mb memory depth
  - ➢ Solution for square wave and RS-FEC encoded scrambled idle patterns
- Each channel of PPG3204 can be programmed with an individual user pattern with channel-specific skew
  - ➢ Solution for emulating FEC-striping across four lanes

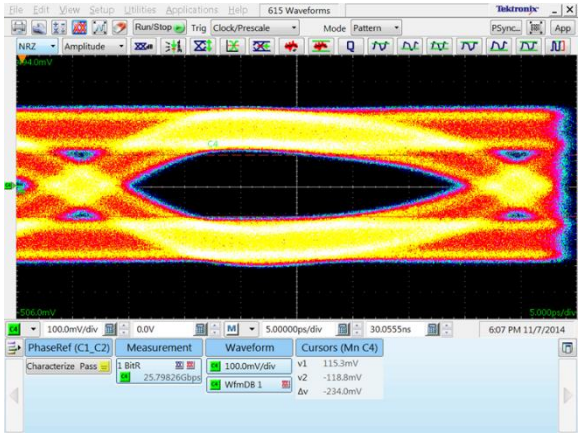
Rx Test

Sinusoidal Interference Receiver Configuration and Calibration

The target values from Table 97-5 of **IEEE802.3bm** Spec.

Description	Value
Stressed eye closure (SEC), lane under test	4.3dB
Stressed eye J2 Jitter, lane under test	0.39UI
Stressed eye J4 Jitter, lane under test (max)	0.53UI



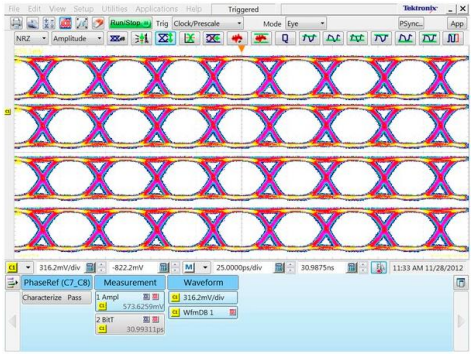


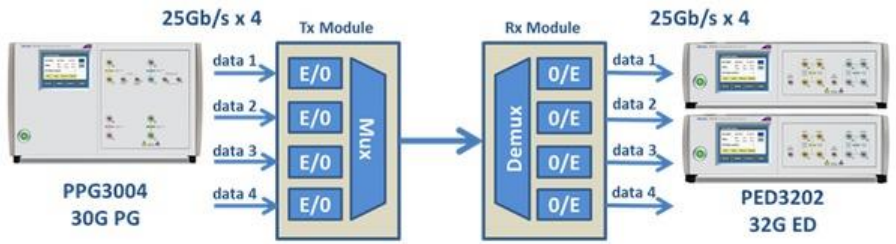
BERT running at 25.78Gb/s, PRBS11 pattern. 40GHz pick-off T connected to BERT output (through path) and 100MHz function generator (pick-off path). Function generator provides sinusoidal CMI to both P and N, closing the eye.

Rx Test
BERT System

Stressed Receiver Sensitivity

- Multi channel 32Gb/s pattern generator
  - Low inherent jitter <250fsec RMS
  - ~10psec rise/fall time (20-80%)
  - RJ, SJ, and BUJ jitter stress
  - Full rate or half rate clock output
  - DC coupled outputs
  - PRBS or custom patterns
  - Adjustable channel phase delay
- 1/2-ch 32Gb/s error detector
  - Best in class sensitivity @ 6mV
  - Auto or manual voltage adjust
  - Auto-sync to input pattern
  - PC GUI SW that provides:
    - Remote instrument control
    - Bathtub and Contour Analysis
    - JTOL measurements
    - J2/J9 measurements





Low instrument intrinsic jitter is critical for SR4

- Tektronix PPG3204:
  - Support for rates through 32G
  - Low intrinsic jitter across data ra

Data Source: CH7	Data Rate: 25 Gbps	Filter: False
SSC: Off	Pattern: 2047 bits	Channel: False
Phase Reference: 25 GHz	Sample Count: 304.70 k	Equalizer: None

Jitter (Decision Threshold: -1.28 mV)			Noise (Sampling Phase: 0 UI)		
Random Jitter			**Random Noise**		
RJ (RMS)	=	280.65 fs	RN (RMS)	=	488.96 uV
RJ(h) (RMS)	=	280.15 fs	RN(v) (RMS)	=	482.66 uV
RJ(v) (RMS)	=	10.00 fs	RN(h) (RMS)	=	78.26 uV

PPG3204
Measured Results @ 25G

Data Source: CH7	Data Rate: 32 Gbps	Filter: False
SSC: Off	Pattern: 2047 bits	Channel: False
Phase Reference: 32 GHz	Sample Count: 304.70 k	Equalizer: None

Jitter (Decision Threshold: -2.48 mV)			Noise (Sampling Phase: 0 UI)		
Random Jitter			**Random Noise**		
RJ (RMS)	=	229.47 fs	RN (RMS)	=	297.00 uV
RJ(h) (RMS)	=	229.24 fs	RN(v) (RMS)	=	297.00 uV
RJ(v) (RMS)	=	10.00 fs	RN(h) (RMS)	=	1.09 uV

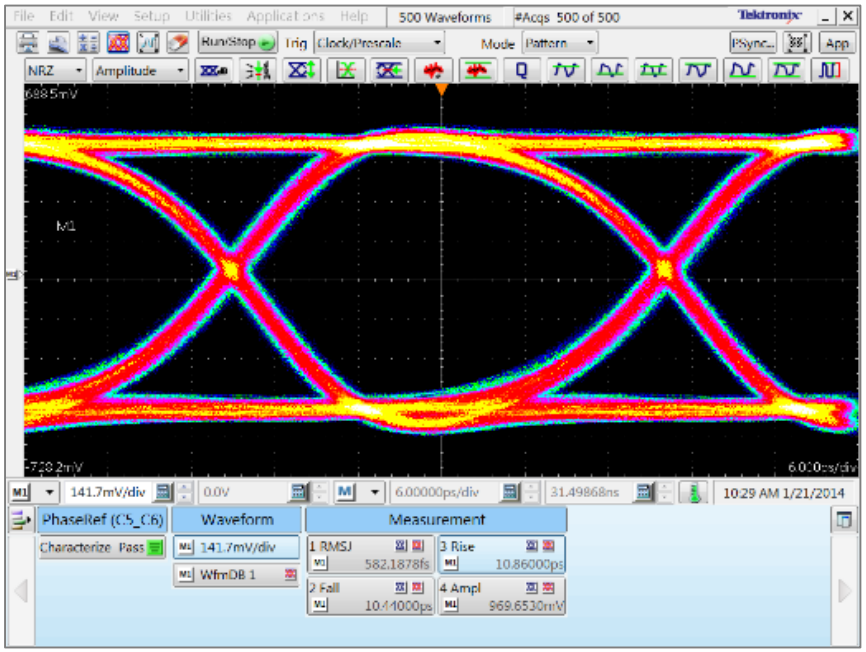
PPG3204
Measured Results @ 32G

	100GBase-*R4	100GBase-*R4 (FEC)	CEI
Rate	25.7813	27.7390	28.0500
I UI (period)	38.7879	36.0500	35.6500
Allocated Rj (UI)	0.13	0.13	0.13
Rj in fs RMS	360.2	334.8	331.0

Key 100G
Electrical Specs

Rx Test

32Gb/s Multi-channel BERT electrical performance



PPG320X 32Gb/s
OPT-ADJ

DSA8300
80E11 sampling plug-in
82A04-60G phase reference

Data Source: MATH1	Data Rate: 32 Gbps	Filter: False
SSC: Off	Pattern: 2047 bits	Channel: False
Phase Reference: 32 GHz	Sample Count: 304.70 k	Equalizer: None

Jitter (Decision Threshold: -11.95 mV)			**Noise** (Sampling Phase: 0 UI)		
Random Jitter			**Random Noise**		
RJ (RMS)	=	211.36 fs	RN (RMS)	=	581.45 uV
RJ(h) (RMS)	=	211.20 fs	RN(v) (RMS)	=	567.11 uV
RJ(v) (RMS)	=	8.39 fs	RN(h) (RMS)	=	128.35 uV
Deterministic Jitter			**Deterministic Noise**		
DJ	=	4.94 ps	DN	=	149.69 mV
DDJ	=	3.20 ps	DDN	=	149.22 mV
DCD	=	971.00 fs	DDN(level 1)	=	124.94 mV
DDPWS	=	2.77 ps	DDN(level 0)	=	167.15 mV
BUJ(d-d)	=	50.00 fs	BUN(d-d)	=	1.74 mV
PJ	=	718.02 fs	PN	=	633.25 uV
PJ(h)	=	717.99 fs	PN(v)	=	458.95 uV
PJ(v)	=	6.79 fs	PN(h)	=	436.33 uV
NPJ(d-d)	=	50.00 fs	NPN(d-d)	=	1.70 mV
Total Jitter @ BER			**Total Noise @ BER**		
TJ (1E-12)		6.76 ps	TN (1E-12)	=	157.72 mV
Eye Opening (1E-12)	=	24.49 ps	Eye Opening (1E-12)	=	821.79 mV
			Eye Amplitude	=	979.51 mV
Dual Dirac			**SSC Modulation**		
RJ(d-d)	=	243.96 fs	Magnitude	=	0 ppm
DJ(d-d)	=	3.32 ps	Frequency	=	0 Hz

Industry Best 32Gb/s Jitter Performance!

- **Data rate** range = 1.5 to 32 Gb/s
- **Voltage adjustability** = 300mV - 1Vpp single-ended (600mV - 2Vpp diff)
- **Rise/fall time** <11ps (20-80%)
- **Intrinsic Jitter** < 7ps TJ@1E-12

Rx Test
DSA8300 SJNB SJ Measurements

Data Source: MATH1	Data Rate: 28 Gbps	Filter: False
SSC: Off	Pattern: 2047 bits	Channel: False
Phase Reference: 28 GHz	Sample Count: 304.70 k	Equalizer: None

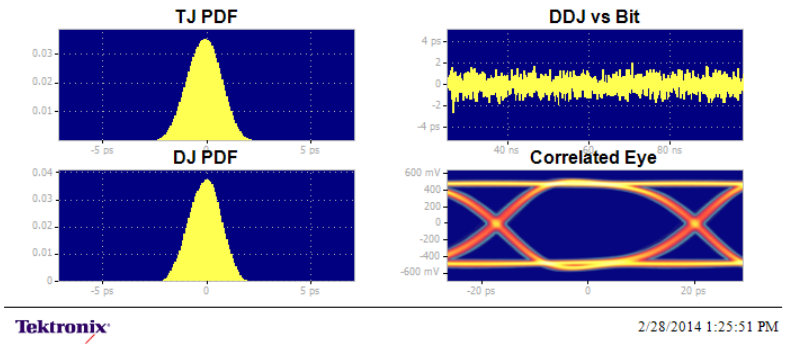
Jitter (Decision Threshold: -11.25 mV)			**Noise** (Sampling Phase: 0 UI)		
Random Jitter			**Random Noise**		
RJ (RMS)	=	281.96 fs	RN (RMS)	=	1.49 mV
RJ(h) (RMS)	=	281.13 fs	RN(v) (RMS)	=	1.48 mV
RJ(v) (RMS)	=	21.52 fs	RN(h) (RMS)	=	180.06 uV
Deterministic Jitter			**Deterministic Noise**		
DJ	=	5.94 ps	DN	=	118.85 mV
DDJ	=	4.38 ps	DDN	=	118.95 mV
DCD	=	108.39 fs	DDN(level 1)	=	95.82 mV
DDPWS	=	3.07 ps	DDN(level 0)	=	134.44 mV
BUJ(d-d)	=	50.00 fs	BUN(d-d)	=	4.72 mV
PJ	=	1.08 ps	PN	=	938.47 uV
PJ(h)	=	1.08 ps	PN(v)	=	636.68 uV
PJ(v)	=	9.27 fs	PN(h)	=	689.46 uV
NPJ(d-d)	=	50.00 fs	NPN(d-d)	=	3.36 mV
Total Jitter @ BER			**Total Noise @ BER**		
TJ (1E-12)	=	8.12 ps	TN (1E-12)	=	141.44 mV
Eye Opening (1E-12)	=	27.59 ps	Eye Opening (1E-12)	=	833.75 mV
			Eye Amplitude	=	975.20 mV
Dual Dirac			**SSC Modulation**		
RJ(d-d)	=	331.07 fs	Magnitude	=	0 ppm
DJ(d-d)	=	3.45 ps	Frequency	=	0 Hz

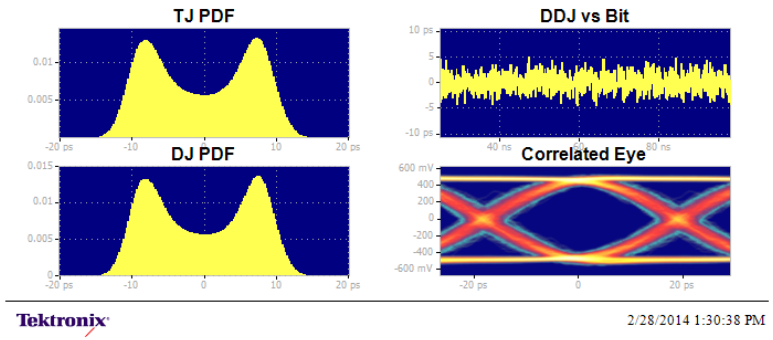
Data Source: MATH1	Data Rate: 28 Gbps	Filter: False
SSC: Off	Pattern: 2047 bits	Channel: False
Phase Reference: 28 GHz	Sample Count: 304.70 k	Equalizer: None

Jitter (Decision Threshold: -11.13 mV)			**Noise** (Sampling Phase: 0 UI)		
Random Jitter			**Random Noise**		
RJ (RMS)	=	554.31 fs	RN (RMS)	=	4.72 mV
RJ(h) (RMS)	=	549.00 fs	RN(v) (RMS)	=	4.72 mV
RJ(v) (RMS)	=	76.51 fs	RN(h) (RMS)	=	26.12 uV
Deterministic Jitter			**Deterministic Noise**		
DJ	=	31.59 ps	DN	=	304.15 mV
DDJ	=	9.40 ps	DDN	=	158.76 mV
DCD	=	143.24 fs	DDN(level 1)	=	130.66 mV
DDPWS	=	7.53 ps	DDN(level 0)	=	170.94 mV
BUJ(d-d)	=	21.22 ps	BUN(d-d)	=	281.32 mV
PJ	=	19.78 ps	PN	=	143.00 mV
PJ(h)	=	17.46 ps	PN(v)	=	143.00 mV
PJ(v)	=	2.32 ps	PN(h)	=	934.91 uV
NPJ(d-d)	=	50.00 fs	NPN(d-d)	=	925.72 uV
Total Jitter @ BER			**Total Noise @ BER**		
TJ (1E-12)	=	35.71 ps	TN (1E-12)	=	497.01 mV
Eye Opening (1E-12)	=	0 s	Eye Opening (1E-12)	=	432.26 mV
			Eye Amplitude	=	929.28 mV
Dual Dirac			**SSC Modulation**		
RJ(d-d)	=	649.90 fs	Magnitude	=	0 ppm
DJ(d-d)	=	28.61 ps	Frequency	=	0 Hz

28G Jitter Baseline
0ps added SJ
1ps measured PJ

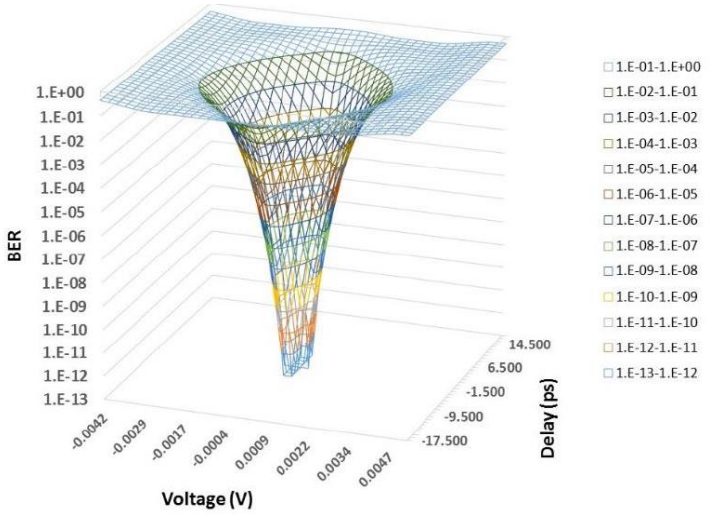
28G Jitter with
20ps added SJ at 10MHz
20ps measured PJ





Rx Test
Best in class PED Sensitivity

- PED can measure input data signals of 6-750mVpp
- With 6mVpp, PED properly center voltage & phase sampling point and synchronizes to input pattern
- Contour plot below measured at 28Gb/s with 6mVpp input signal
- **Highly sensitive PED allows for very precise BER measurements at low input power levels**



Transceiver Test
Tektronix 100GBASE-SR4 Test Solutions

PPG3204 32G PPG

4x25G electrical

E/O
E/O
E/O
E/O

MUX

DUT, eg CFP4 SR4 XCVR

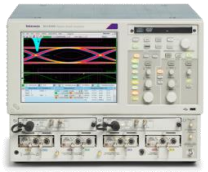
DEMUX

O/E
O/E
O/E
O/E

4x25G electrical

CR286A Clock Recovery

PED3202 32G PED



DSA8300 with 80E10B and 80C15 plug-ins

SR4 Optical Test Solutions

PPG3204 32G PPG

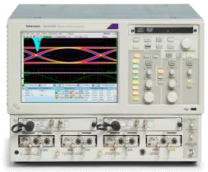
4x25G electrical

DUT, eg chip-to-module

4x25G electrical loopback

CR286A Clock Recovery

PED3202 32G PED

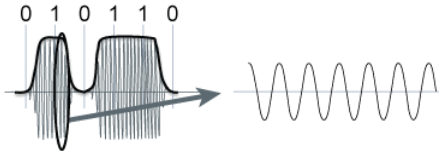


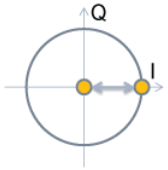
DSA8300 with 80E10B plug-ins

SR4 Electrical Test Solutions

What is Coherent Optical Modulation?

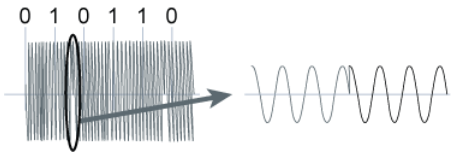
Traditional 10G transmissions modulate the amplitude of the light, a.k.a. or on-off keying (OOK). Direct detection is used in the receiver.

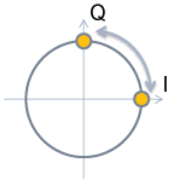




OOK
On-Off Keying
1 bit/Baud (symbol)

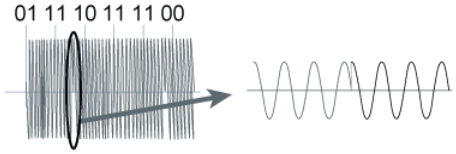
Coherent transmissions modulate the phase of the light, the simplest case is phase shift keying.

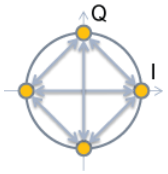




PSK
Phase Shift Keying
1 bit/Baud (symbol)

By doubling the number of phase states, the bit/Baud rate is also doubled.

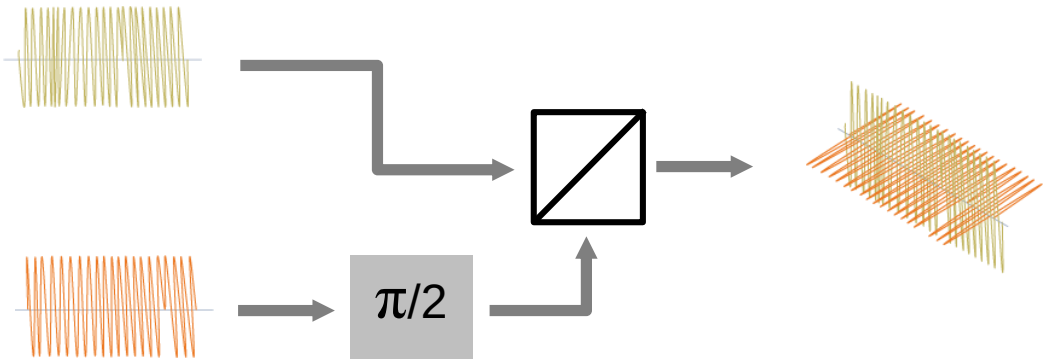




QPSK
Quadrature Phase Shift Keying
2 bits/Baud (symbol)

What is Coherent Optical Modulation?

Rotating the polarization of one QPSK signal, and combining it with a second QPSK signal, doubles the bits/Baud rate again.



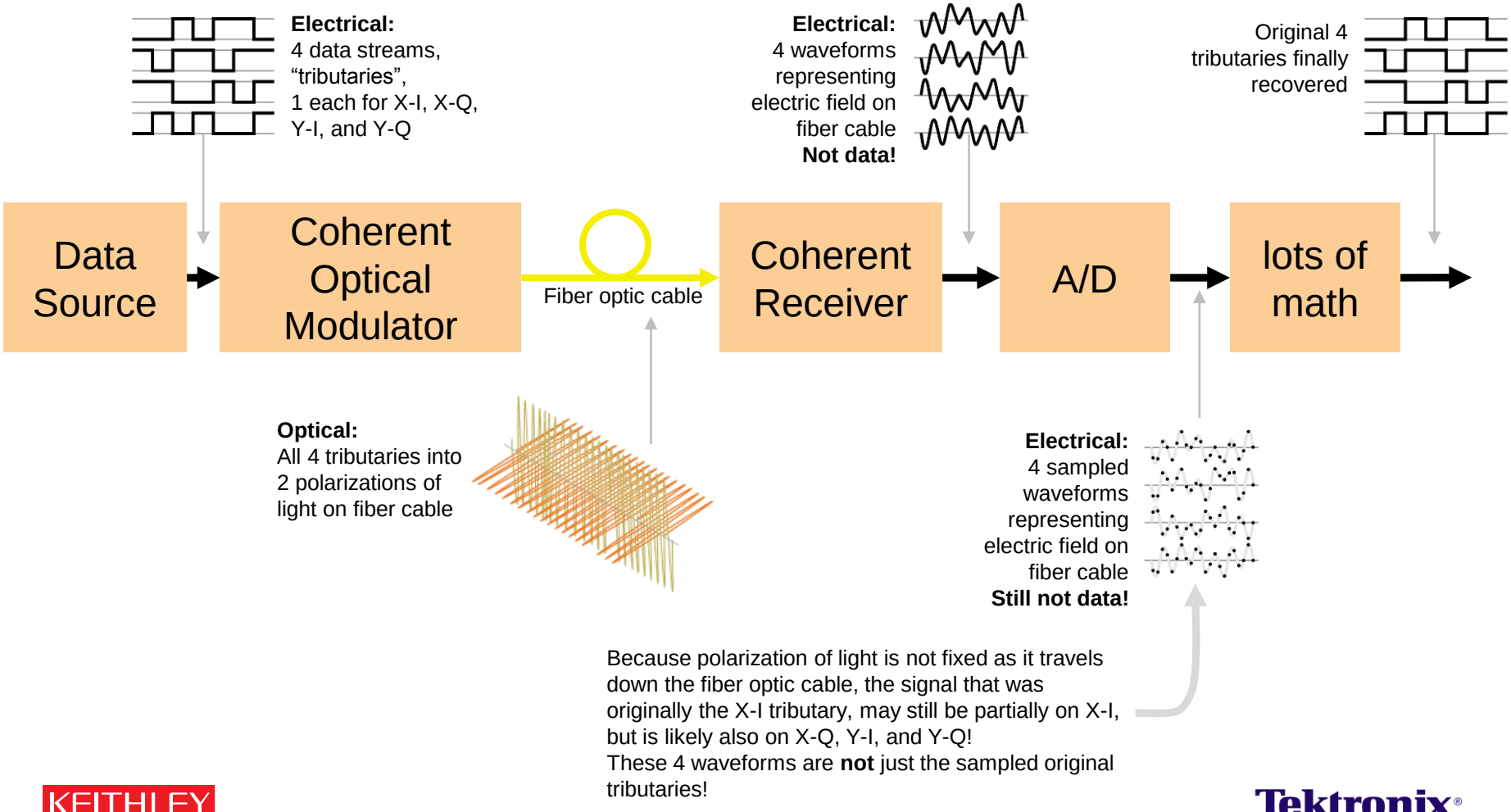
DP-QPSK
Dual-Polarization QPSK
4 bits/Baud (symbol)

Common Modulation Formats

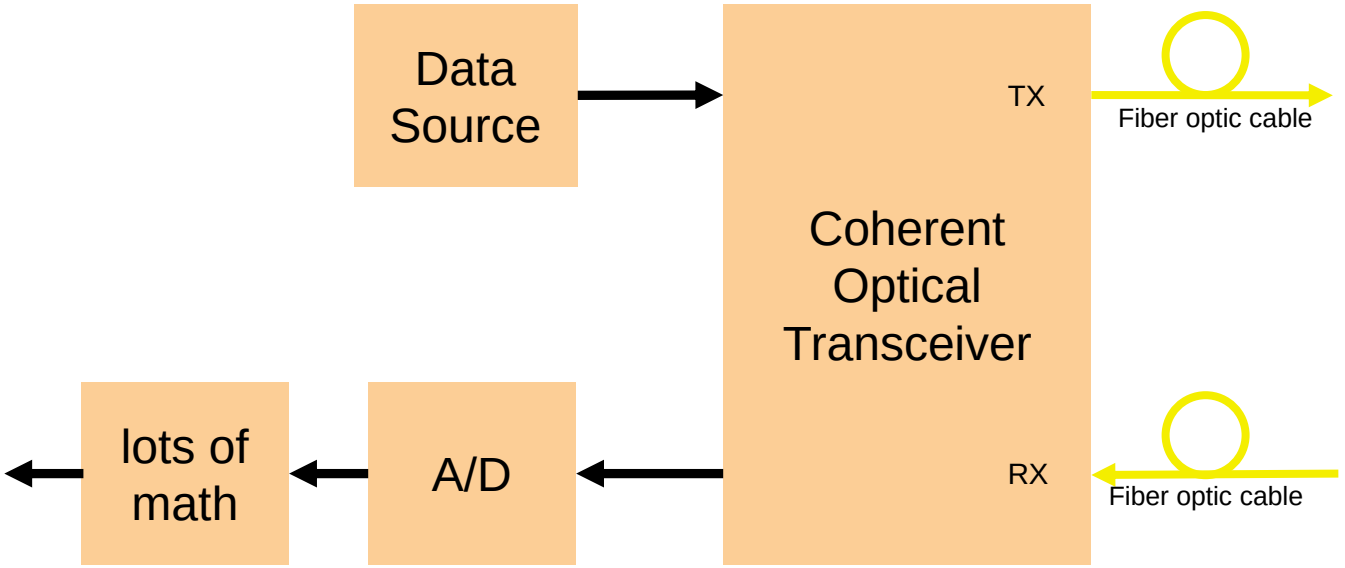
		28 GBaud	32 GBaud	40 GBaud	46 GBaud	56 GBaud	64 GBaud
NRZ/PAM2 1 bit per Baud (symbol)	Single Polarization	28 Gb/s	32 Gb/s	40 Gb/s	46 Gb/s	56 Gb/s	64 Gb/s
BPSK 1 bit per Baud (symbol) per polarization	Single Polarization	28 Gb/s	32 Gb/s	40 Gb/s	46 Gb/s	56 Gb/s	64 Gb/s
	Dual Polarization	56 Gb/s	64 Gb/s	80 Gb/s	92 Gb/s	112 Gb/s	128 Gb/s
PAM4 2 bits per Baud (symbol)	Single Polarization	56 Gb/s	64 Gb/s	80 Gb/s	92 Gb/s	112 Gb/s	128 Gb/s
QPSK 2 bits per Baud (symbol) per polarization	Single Polarization	56 Gb/s	64 Gb/s	80 Gb/s	92 Gb/s	112 Gb/s	128 Gb/s
	Dual Polarization	112 Gb/s	128 Gb/s	160 Gb/s	184 Gb/s	224 Gb/s	256 Gb/s
8PSK 3 bits per Baud (symbol) per polarization	Single Polarization	84 Gb/s	96 Gb/s	120 Gb/s	138 Gb/s	168 Gb/s	192 Gb/s
	Dual Polarization	168 Gb/s	192 Gb/s	240 Gb/s	276 Gb/s	336 Gb/s	384 Gb/s

		28 GBaud	32 GBaud	40 GBaud	46 GBaud	56 GBaud	64 GBaud
8QAM 3 bits per Baud (symbol) per polarization	Single Polarization	84 Gb/s	96 Gb/s	120 Gb/s	138 Gb/s	168 Gb/s	192 Gb/s
	Dual Polarization	168 Gb/s	192 Gb/s	240 Gb/s	276 Gb/s	336 Gb/s	384 Gb/s
16QAM 4 bits per Baud (symbol) per polarization	Single Polarization	112 Gb/s	128 Gb/s	160 Gb/s	184 Gb/s	224 Gb/s	256 Gb/s
	Dual Polarization	224 Gb/s	256 Gb/s	320 Gb/s	368 Gb/s	448 Gb/s	512 Gb/s
32QAM 5 bits per Baud (symbol) per polarization	Single Polarization	140 Gb/s	160 Gb/s	200 Gb/s	230 Gb/s	280 Gb/s	320 Gb/s
	Dual Polarization	280 Gb/s	320 Gb/s	400 Gb/s	460 Gb/s	560 Gb/s	640 Gb/s
64QAM 6 bits per Baud (symbol) per polarization	Single Polarization	168 Gb/s	192 Gb/s	240 Gb/s	276 Gb/s	336 Gb/s	384 Gb/s
	Dual Polarization	336 Gb/s	384 Gb/s	480 Gb/s	552 Gb/s	672 Gb/s	768 Gb/s

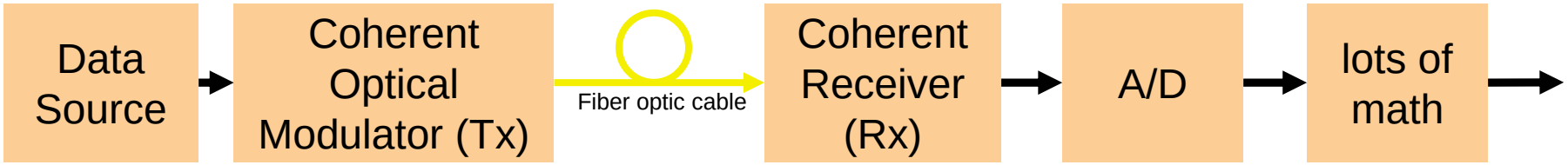
Coherent System Building Blocks

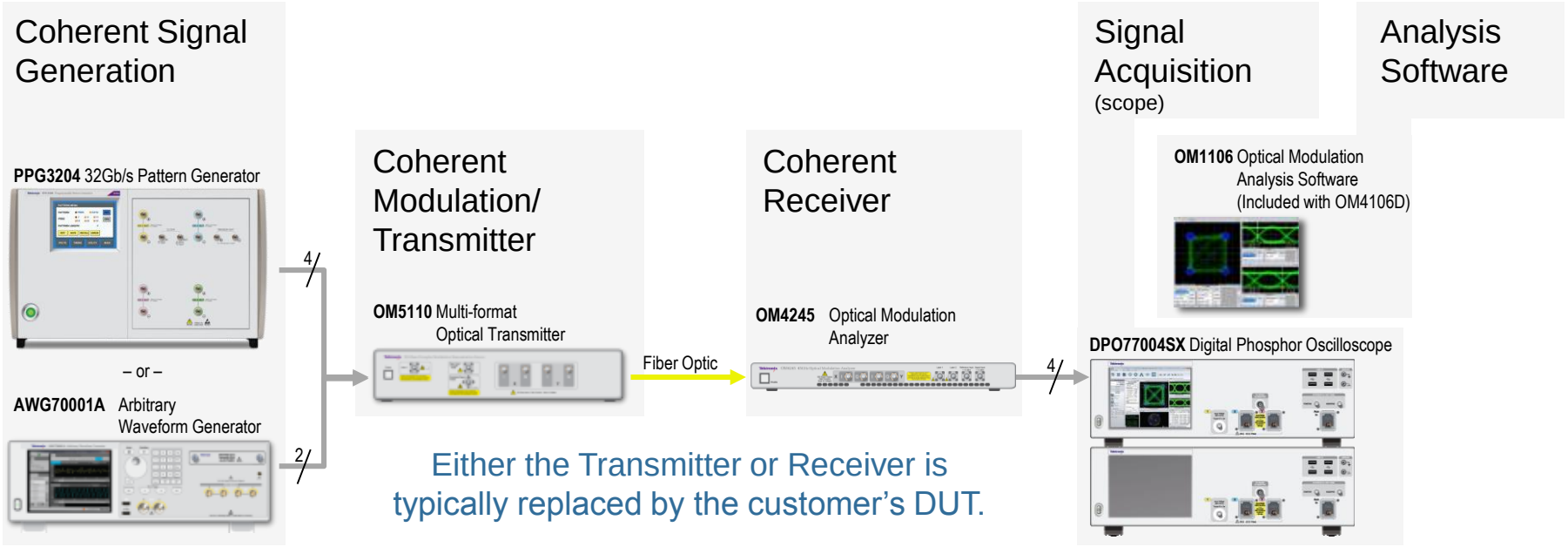


Coherent System Building Blocks



Coherent Test System Building Blocks



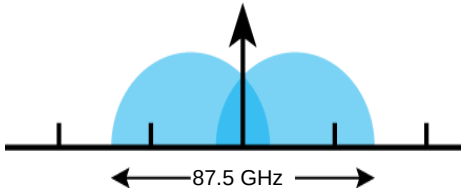


Example Industry Approaches to 400G and Beyond

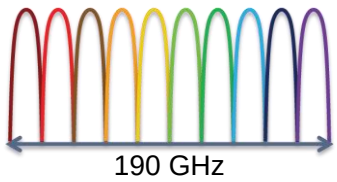
- No industry consensus on how to build super-channels – no one architecture fits all requirements.
- Vendors differ on characteristics as basic as carrier count and carrier spacing to what modulation format should be used.

system rate	# of carriers	modulation format
400 Gb/s[1]	2	DP-16QAM
500 Gb/s[2]	5	DP-QPSK
500 Gb/s[3]	10	DP-QPSK
1.0 Tb/s[4]	10	DP-QPSK
1.5 Tb/s[5]	8	DP-16QAM

400 Gb/s, 2 carriers

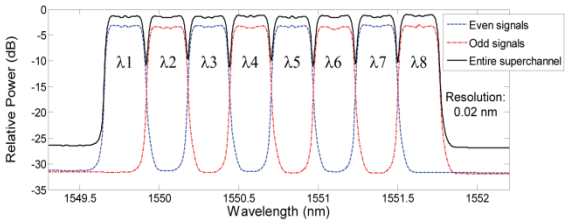


500 Gb/s, 10 carriers



1.0 Tb/s, 10 carriers

1.5 Tb/s, 8 carriers



Sources:
[1]Beyond 100G, copyright 2012, Fujitsu Network Communications, Inc.
[2]Dawn of the Terabit Age , copyright 2011, Infinera Corporation
[3]Coherent Super-Channel Technologies, OSA Webinar , copyright 2011, Infinera Corporation
[4]Super-Channels: DWDM Transmission at100Gb/s and Beyond, copyright 2012, Infinera Corporation
[5]1.5-Tb/s Guard-Banded Superchannel Transmission over 56 × 100-km (5600-km) ULAF Using 30-Gbaud Pilot-Free OFDM-16QAM Signals with 5.75-b/s/Hz Net Spectral Efficiency, Alcatel-Lucent, Bell Labs

Thank you ！ ！ ！