100G and 400G Ethernet and general DataCom roadmap/Challenge/solution

王宏军
FAE/Tektronix China

Nov, 2015
Agenda: 100G and 400G Ethernet and general DataCom roadmap and testing needs

- Overview
  - 100G and 400G futures
  - Transitional from 100G to 400G.

- 100G-400G Design Challenges
  - Channel Loss vs Higher order modulation
  - Excerpts from 400G Specs that cause pain

- TX Signal Acquisition for 100G/400G
  - Real Time Signal Acquisition
  - Equivalent Time Signal Acquisition

- RX Signal Generation for 100G/400G
  - PAM-4 modulation and demodulation for error detection.

- Coherent optical Introduction
Emerging 100G/400G industry, leverages an assortment of standards and technologies to support the broad set of **Submarine -> Continental** -> Metro -> Campus -> Data-Center -> Back-Plane -> **Chip to Chip** requirements.

- OIF researched, ITU-T SG15 defined “Core OTN Transport” (WAN) G.709
- Also 4x25, but QPSK
- Graphics after OIF CEI / Chris Cole, Finisar

Cloud server: < 2 km

IEEE defined Ethernet

4x25 PAM2 (NRZ)

Metro: < 40 km

IEEE defined Ethernet

4x25 PAM2 (NRZ)

X,000 km

spread

grow

growth

IEEE defined Ethernet

4x25 PAM2 (NRZ)
The top-to-bottom 100G standards
(Main actors only, not a comprehensive table)

<table>
<thead>
<tr>
<th>Distance</th>
<th>Standard</th>
<th>Modulation/signaling</th>
<th>e.g.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X,000 km…40 km</td>
<td>OIF, OTN, ITU</td>
<td>Complex optical</td>
<td>DP-QPSK</td>
</tr>
<tr>
<td>10, 40 km</td>
<td>Ethernet</td>
<td>NRZ SM</td>
<td>100GBASE-ER4/LR4</td>
</tr>
<tr>
<td>2 km</td>
<td>MSA “CLR4”</td>
<td>NRZ SM</td>
<td>100G-CLR4</td>
</tr>
<tr>
<td>500 m</td>
<td>MSA “PSM4”</td>
<td>NRZ SM</td>
<td>100G PSM4</td>
</tr>
<tr>
<td>100 m</td>
<td>Ethernet</td>
<td>NRZ MM</td>
<td>100GBASE-SR4</td>
</tr>
<tr>
<td>~100 m</td>
<td>Infiniband (IB)</td>
<td>NRZ over active cable; or interconnect</td>
<td>“CAUI-4” going</td>
</tr>
<tr>
<td>10 m</td>
<td>Ethernet, IB</td>
<td>NRZ on passive Cu cable</td>
<td>100GBASE-CR4</td>
</tr>
<tr>
<td>Backplane &lt; 1m</td>
<td>Ethernet, OIF CEI</td>
<td>NRZ</td>
<td>100GBASE-KR4, CEI LR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PAM4</td>
<td>100GBASE-KP4</td>
</tr>
<tr>
<td>Interconnect</td>
<td>OIF CEI, Ethernet</td>
<td>NRZ</td>
<td>VSR CAUI-4</td>
</tr>
<tr>
<td>module to chip,</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>chip to chip</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

100G across the stack
The top-to-bottom 400G standards
(Main actors only, not a comprehensive table)

<table>
<thead>
<tr>
<th>Distance</th>
<th>Standard</th>
<th>Modulation/signaling</th>
<th>e.g.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X,000 km</td>
<td>OIF, OTN, ITU</td>
<td>Complex optical</td>
<td>DP-QPSK Multi?</td>
</tr>
<tr>
<td>10 km</td>
<td>Ethernet</td>
<td>PAM4 at 25 G Bd</td>
<td>400GBASE-LR8</td>
</tr>
<tr>
<td>2 km</td>
<td>Ethernet</td>
<td>PAM4 at 25 G Bd</td>
<td>400GBASE-FR8</td>
</tr>
<tr>
<td>500 m</td>
<td>Ethernet</td>
<td>PAM4 at 50 G Bd</td>
<td>400GBASE-DR4</td>
</tr>
<tr>
<td>Backplane &lt; 1 m</td>
<td>OIF CEI</td>
<td>PAM4 at 25 G Bd</td>
<td>CEI LR</td>
</tr>
<tr>
<td></td>
<td>Interconnect module to chip, chip to chip</td>
<td>Ethernet OIF CEI</td>
<td>NRZ CDAUI-16, CDAUI-8 CEI VSR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Ethernet Nomenclature
(based on an Ethernet Alliance slide by Scott Kipp, with Tektronix extensions)

- Common interpretation* is as follows:
- Example: 100GBASE-KP4

- The IEEE does not specify the meanings of the letters, rather it simply identifies PHYs by combinations of letters. There is no guarantee that in the future these interpretations will retain whatever meaning they presently have.
Driver is Optical Ethernet at 400G
Interconnect electrical at 25 GBd x8 PAM4

400G Ethernet

- PAM4 53GBd x4
- PAM4 28GBd x8
- PAM4 28GBd x8
- PAM2 26GBd x16

Reach; Fiber

- 100m; MMF
- 500m; SMF
- 2km; SMF
- 10km; SMF

© prz@tek 2015
Design and Test Challenges in the 100G-400G transition

- “Copper is out of gas” at 56Gbps.
  - Higher order modulation (PAMn) is one means of combating incredibly high channel losses.
  - Multiple bits/symbols results in a reduced overall symbol rate and fundamental transmission frequency. 14GHz rather than 28GHz.
Design and Test Challenges in the 100G-400G transition

- Higher order modulation (PAM4) signals are more sensitive to ISI as they involve multiple transitions between multiple levels.
  - This results in smaller horizontal eye openings.
- The signal transitions between each level are also smaller
  - This results in smaller vertical eye openings, higher sensitivity to noise.
- Forward Error Correction (FEC) is needed to improve BER performance of the link.
- Tx pre-emphasis and Rx CTLE/DFE may be used to somewhat compensate for the channel induced ISI
- Gray coding may be used to limit certain multi-level transitions and also reduce ISI
Design and Test Challenges in the 100G-400G transition

- High data rate for Pattern generator
- Low instrument intrinsic jitter <350fs for Pattern generator
- Jitter injection support for stress testing
- High sensitivity error detector
- Low instrument intrinsic jitter <150fs for Scope
- High bandwidth electrical/optical measurement
- CDR support
Tektronix 100/400G Test Solutions

Industry’s only complete solution for comprehensive Tx and Rx testing

**Signal Generation**
- PAM4 PPG with pre-emphasized remote head
- Device Under Test
  - ASIC/FPGA SERDES, transceivers, physical layer ICs

**Analysis Software**
- PAM4 PED with decoder remote head
- PAM4 BERT control and analysis
- DPOJET RT Jitter & Timing Analysis
- 80SJNB ET Jitter & Timing Analysis

**Signal Acquisition**
- DPO70000SX ATI
  - Real Time Oscilloscope
- DSA8300 Sampling Oscilloscope
- NEW!
PPG and PED instruments

Options and configurations

PPG Base Instruments

- **PPG1251** 12.5Gb/s PPG
  - Jitter insertion (LF+HF)

- **PPG1600x/300X** 16&30Gb/s PPG
  - 1/2/4 Channel
  - LF jitter insertion
  - HF jitter insertion

- **PPG320X** 32Gb/s PPG
  - 1/2/4 Channel
  - Adjustable output
  - LF jitter insertion
  - HF jitter insertion

- **PPG4001** 40Gb/s PPG
  - LF jitter insertion
  - HF jitter insertion

PED Base Instruments

- **PED320X** 32Gb/s PED
  - 1/2 Channel
  - Full or half rate clock input
  - AC or DC coupled input

- **PPG400X** 40Gb/s PED
  - 1/2 Channel
  - Full or half rate clock input
  - AC or DC coupled input

- **PED3202** 32Gb/s
  - 2 channel PED

- **PPG3204** 32Gb/s
  - 4 channel PPG

Industry’s only 40G PPG with Jitter Insertion

PatternPro competitive advantage

Industry’s best PED sensitivity

6mV auto-align and auto-sync
32Gb/s Multi-channel BERT electrical performance

Fast Risetime and Low Jitter

PPG320X 32Gb/s
OPT-ADJ

- **Data rate range** = 1.5 to 32 Gb/s
- **Voltage adjustability** = 300mV - 1Vpp single-ended (600mV - 2Vpp diff)
- **Rise/fall time** < 11ps (20-80%)
- **Intrinsic Jitter** < 7ps TJ@1E-12

Industry Best 32Gb/s Jitter Performance! 211fs
# DSA8300 Digital Serial Analyzer

## DSA8300 Optical Module Portfolio

<table>
<thead>
<tr>
<th>Single and Multi-mode, Broad Wavelength (750 - 1650 nm) Modules</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>80C07B</strong></td>
</tr>
<tr>
<td><strong>80C08D</strong></td>
</tr>
<tr>
<td><strong>80C12B</strong></td>
</tr>
<tr>
<td><strong>80C14</strong></td>
</tr>
<tr>
<td><strong>80C15</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Single-mode, Long Wavelength (1100 - 1650nm) Modules</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>80C11B</strong></td>
</tr>
<tr>
<td><strong>80C10C</strong></td>
</tr>
</tbody>
</table>
56Gbps Optical Reference Receiver on Highest optical Bandwidth oscilloscope

80C10C, 80C10C-CRTP

- High sensitivity with and without CR
- Support for Optical Bessel-Thompson Filter in HW (no DSP, no special pattern needed)
- Electrical Data Out (optional) for:
  - Clock Recovery,
  - Real-time oscilloscope for troubleshooting
  - BER analysis
- Best noise performance at 40G, 56G → best system for PAM4 @ 56 GBd
- Nearly 100 GHz optical Bandwidth
80C10C
Outstanding Performance and Value

Flexibility:
- Solution to 100GbE (4x25), OC768, G.709 FEC, OTU3+, and 40GbE test in one module
- Solution for 1550 nm and 1310 nm in one module
- Solution to 100G clock recovery, with Option CRTP (clock recovery trigger pickoff), and Tektronix CR286A Clock Recovery Instrument
- Solution to 40G clock recovery, with Option CRTP and 3rd party clock recovery Instrument.

Performance:
- Up to 80 GHz Optical Bandwidth
- Excellent Noise Performance
- Low Optical Return Loss
- Patented Technology For:
  - Low Aberrations
  - Extremely Flat Group Delay
  - ITU-Compliant OC-768 and G.709 FEC Filters

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Unfiltered bandwidth</td>
<td>70 GHz</td>
<td>55 GHz</td>
<td>80 GHz</td>
</tr>
<tr>
<td>Opt. CRTP available</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Clock Recovery Trigger Pickoff</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>40Gbs G.709 FEC Telecom 43.02 Gb/s &amp; 44.5 Gb/s</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>40GbE Datacom 41.25 Gb/s</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>OC768 40 GHz Telecom 39.8 Gb/s</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>OTU4 27.9 Gb/s</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>100GbE-4X Datacom 25.7 Gb/s</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>
Single-mode optical standards (100Gb/s stable since 802.3ba ratified in 2011)

- Current technology satisfies 56 Gb/s as well as current 25 Gb/s

Tek 80C10C optical module:

Just 5 dB down at 100 GHz

80 Gb/s RZ
Tektronix 100G/400G Signal Acquisition Systems

Equivalent Time Signal Acquisition • Real Time Signal Acquisition Software Control and Analysis

- Two world class acquisition systems cover the breadth of any 400G Verification and design needs, with the lowest noise, highest bandwidth in the industry
  - Real Time (70GHz ATI) single shot acquisition and triggering capabilities are key tools for advanced analysis and debug.
  - Equivalent Time low noise, high sensitivity tools enable the best margin in product and device characterization.

- Real Time
  - 70GHz Analog Bandwidth, 4.3ps rise time (20%-80%)
  - 200GS/s Sample Rate
  - <125fs jitter noise floor
  - ≥25GHz Edge trigger bandwidth
  - Compact 5 ¼” Oscilloscope package

- Equivalent Time
  - 85GHz Optical Bandwidth
  - 70GHz Electrical Bandwidth
  - <100fs jitter noise floor
  - 20nW to .6uW Optical Resolution.
  - Automated test of 80 Industrial Stds.
ATI Performance Oscilloscope

- 70GHz Analog Bandwidth, 4.3ps rise time (20%-80%)
- 200GS/s Sample Rate
- <125fs jitter noise floor
- ≥25GHz Edge trigger bandwidth
- Compact 5 ¼” Oscilloscope package

[ OR ]

- 1 channel x 70GHz bandwidth
  - Single-ended, 100mV_{fsr} to 300mV_{fsr}
  - 200GS/s sample rate
  - Up to 1 Gsamples record length
- 2 channels x 33GHz bandwidth
  - Single-ended, 62.5mV_{fsr} to 6V_{fsr}
  - 100GS/s sample rate per channel
  - Up to 1 Gsamples record per channel

- Low-noise ATI architecture
- Best-in-class signal capture
- Compact package with precise multi-unit sync
Comparing Methods: Tek Advantage

**Tektronix Architectural Innovation**

- **Improved SNR**
  - Each ADC sees full spectrum
  - Signal reconstruction involves **averaging** → improves SNR
- **Signal-path symmetry**
- **Patented architecture**

**Legacy Frequency Interleaving**

- Each ADC sees **half** spectrum
- Signal reconstruction involves **summation** → no improvement in SNR
70GHz ATI frequency response Flatness

- Current data shows very good frequency response flatness
- Expect ±0.5dB to 50% and ±1.5dB to 80% of BW (typical)
100Gbase-KP4  What is PAM?

- **Pulse Amplitude Modulation**
  - PAM4 combines two bit streams and uses 4 levels to encode 2 bits into 1 UI
  - For Example, 56 Gbit/s PAM4 runs at a symbol rate of 28 GBaud

<table>
<thead>
<tr>
<th>MSB</th>
<th>LSB</th>
<th>PAM4 LEVEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
</tbody>
</table>
What are the differences between PAM4 and NRZ?

- **PAM4**
  - 4 Levels -> 3 Eyes
  - Sensitive to SNR (eyes smaller)
  - 2 bits into 1 UI
  - ½ Baud Rate for same data throughput (28 GBaud = 56Gbps)
  - Adds complexity/cost to Tx/Rx

- **NRZ**
  - 2 Levels -> 1 Eye
  - Less Sensitive to SNR
  - 1 bit in 1 UI
  - 2X Baud Rate for same data throughput (28GBaud = 28Gbps)
  - Less expensive Tx/Rx
Tektronix PAM4 Signal Generation Performance

25Gbaud

28Gbaud

32Gbaud

LSB: Ch1 data signal (1V)
MSB: Ch2 data signal (2V)
PAM4: Sum of the two signals

PPG3202 Pattern Generator

Combiner

PSPL5380 PAM4 Kit

DSA8300 Scope
Tektronix 100G/400G BERT Signal Generation System

Signal generation • Signal Acquisition • Software Control and Analysis

PAM4 signal generation
- Programmable Tx pre-emphasis for device and channel loss compensation
- Independent programming of LSB and MSB data
- PRBS31 and user data patterns

PAM4 signal acquisition
- Auto-alignment of PAM4 signal at decoder
- Integrated clock recovery
- True hardware BER measurement of all LSB and MSB data
- PRBS31 and user data patterns

PAM4 control software
- Full GUI with PAM4 eye display at decoder input
- Signal generation and analysis control from a single software console
  - Full pattern and pre-emphasis control
  - Measurement point alignment and control
  - BER measurement and analysis
Tektronix 100G/400G BERT System

*Signal generation • Signal Acquisition • Software Control and Analysis*

- **Only dedicated PAM4 BERT system in the industry**
  - True PAM4 signal generation, acquisition, measurement, and system control
  - Equipment and software designed specifically for PAM4 testing

- **Signal Generation**
  - Remote head with programmable pre-emphasis
    - Independent control of LSB and MSB amplitude and pre-emphasis levels
    - Re-timing of signal at remote head to minimize PAM4 signal DDJ from long cables
  - Independent control of LSB and MSB data
    - Built-in PRBS and programmable user data
    - Independent patterns on LSB/MSB or split between LSB/MSB

- **Signal Acquisition**
  - Remote head with true PAM4 eye measurement and decoding
    - PAM4 diagnostic eye measured directly at decoder input
    - Separate, full adjustment of PAM4 sample points (threshold, time)
    - Re-timing of signal at remote head to minimize PAM4 signal DDJ from long cables
  - Integrated clock recovery
  - Hardware decoding of LSB and MSB data

- **Software Control and Analysis: Single console for full control of PAM4 BERT system**
  - Signal generation and acquisition (patterns, pre-emphasis, sample points)
  - Signal analysis (diagnostic eye, LSB/MSB BER, bathtub curves, etc.)
Example data with PPG3202 2 channel 32Gb/s generator and external combiner:

28G PAM4 PRBS23/31 Eye Diagram and Contour Plot

Eye diagram measured with 60GHz sampler and precision timebase.
PRBS23 pattern on LSB and PRBS31 pattern on MSB.

Contour plot measured with error detector and PatternPro software.

Eye opening is reduced from NRZ eye by PAM4 added deterministic jitter.
Contour slope is steep due to low RJ. Small changes in cables/etc have large impact on BER floor due to slim DJ margins at 28G.
PAM4 Transmitter Solution on Real time scope

- PAM4 Clock Recovery
- CTLE/DFE Equalization
- Channel Embedding/De-Embedding

- Comprehensive Measurements
  - Level separation mismatch - $R_{LM}$
  - Time and Level Deviation
  - Level Thickness
  - Jitter (RJdd, DJdd, TJ, J2, J9)
  - Eye Height
  - Eye Width
  - Noise Analysis (Phase 2)

- DPO70000SX/DX/C
  - PAM4 Analysis with Jitter and Noise
    - Opt. PAM4, DJA, DJAN
  - Channel Embedding/De-Embedding and Equalization
    - Opt. SDLA64
Clock Recovery

- New Clock Recovery for PAM
  - PLL - Type 1 and 2
  - Explicit Clock
CTLE / DFE Equalization

Enabled with opt. SDLA64
TX Measurements
PAM4 Levels and Thresholds

Levels are used for determining the thresholds, calculating noise, linearity, time deviation
Thresholds are used to calculate jitter, eye centers and other eye parameters

Levels and Thresholds are automatically detected or can be manually configured
TX Measurements
Level Thickness and Deviation

- **Thickness** - Measures thickness of each symbol level
- **Deviation**
  - Characterize timing properties of the signal and non-linear artifacts in the driver
  - Look at the skew between the narrowest point on each level
- **Done on QPRBS13 pattern**
DPOJET PAM4 (Real Time)

<table>
<thead>
<tr>
<th>Meas</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit Interval</td>
<td>38.786ps</td>
</tr>
<tr>
<td>Symbol Rate</td>
<td>25.781Gbd</td>
</tr>
<tr>
<td>Equiv Bitrate (2xBd)</td>
<td>51.562Gbps</td>
</tr>
<tr>
<td>Symbol Population</td>
<td>59843</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Meas</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>RLM (linearity)</td>
<td>0.97948</td>
</tr>
<tr>
<td>Level Deviation</td>
<td>1.8592%</td>
</tr>
<tr>
<td>Level Thickness</td>
<td>2.059%</td>
</tr>
<tr>
<td>TimeDeviationOrig</td>
<td>7.25% UI</td>
</tr>
<tr>
<td>TimeDeviationMean</td>
<td>2.65% UI</td>
</tr>
<tr>
<td>EyeCenterDevOrig</td>
<td>1.9687% UI</td>
</tr>
<tr>
<td>EyeCenterDevMean</td>
<td>2.00% UI</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Level</th>
<th>Mean</th>
<th>StdDev</th>
<th>Pk-Pk</th>
<th>TimeDev</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_A(0)</td>
<td>224mV</td>
<td>15.6mV</td>
<td>87.0mV</td>
<td>-5.0%</td>
</tr>
<tr>
<td>V_B(1)</td>
<td>77.4mV</td>
<td>15.1mV</td>
<td>77.8mV</td>
<td>-4.2%</td>
</tr>
<tr>
<td>V_C(2)</td>
<td>-67.7mV</td>
<td>21.1mV</td>
<td>96.1mV</td>
<td>-10%</td>
</tr>
<tr>
<td>V_D(3)</td>
<td>-220mV</td>
<td>-21.4mV</td>
<td>102mV</td>
<td>-9.8%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Eye</th>
<th>Thresh</th>
<th>J2</th>
<th>J9</th>
<th>TJ@BER</th>
<th>RJ(d-d)</th>
<th>DJ(d-d)</th>
<th>Width</th>
<th>EcDev</th>
<th>Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>Upper</td>
<td>151mV</td>
<td>26.7ps</td>
<td>32.7ps</td>
<td>34.0ps</td>
<td>0.833ps</td>
<td>22.3ps</td>
<td>11.4ps</td>
<td>3.1%</td>
<td>101mV</td>
</tr>
<tr>
<td>Middle</td>
<td>4.37mV</td>
<td>26.9ps</td>
<td>33.2ps</td>
<td>34.7ps</td>
<td>0.895ps</td>
<td>22.1ps</td>
<td>13.8ps</td>
<td>-1.2%</td>
<td>77.8mV</td>
</tr>
<tr>
<td>Lower</td>
<td>-144mV</td>
<td>29.3ps</td>
<td>35.6ps</td>
<td>37.0ps</td>
<td>0.893ps</td>
<td>24.5ps</td>
<td>9.68ps</td>
<td>-1.6%</td>
<td>51.9mV</td>
</tr>
</tbody>
</table>
Tektronix 400G PAM TX Analysis on Sampling scope

- Available Measurements (O/E)
  - Level separation mismatch - $R_{LM}$
  - Time and Level Deviation
  - Level Thickness
  - Eye Center Deviations
  - Composite Eye Width
  - Jitter
  - Eye Height and Width

DSA8300 Sampling Oscilloscope
- Software Opt. JNB02 and ADVTRIG
- 80E09B 60 GHz Electrical Sampling Module
- 82A04B Phase Reference Module
- Optical I/O - add one of the following:
  - 80C14 for Multi-mode PAM to 16 Gbps
  - 80C15 for Multi-mode PAM to 28 Gbps
  - 80C10C for Single mode PAM
DSA8300 Sampling Oscilloscope, Optical 56GBaud PAM4 Analysis with full Clock Recovery
PAM4 signal path compensation and CTLE
56 GBaud *Yes that is* PAM-4 at 112 Gbit!
Tektronix 100GBASE-SR4 Test Solutions
What is 100GBASE-SR4?

- IEEE 802.3bm 100G standard, defining 4 x 25Gb/s interconnects over multi-mode fiber (MMF), with a range of up to 100m
- RS-FEC is mandatory for 100GBASE-SR4
- Supports CFP2, CFP4, and QSFP-28 transceivers
# Tx Test

## SR4 Tx Measurements

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signaling rate, each lane (range)</td>
<td>25.78125 ± 100 ppm</td>
<td>GBd</td>
</tr>
<tr>
<td>Center wavelength (range)</td>
<td>840 to 860</td>
<td>nm</td>
</tr>
<tr>
<td>RMS spectral width(^a) (max)</td>
<td>0.6</td>
<td>nm</td>
</tr>
<tr>
<td>Average launch power, each lane (max)</td>
<td>2.4</td>
<td>dBm</td>
</tr>
<tr>
<td>Average launch power, each lane (min)</td>
<td>-8.4</td>
<td>dBm</td>
</tr>
<tr>
<td>Optical Modulation Amplitude (OMA), each lane (max)</td>
<td>3</td>
<td>dBm</td>
</tr>
<tr>
<td>Optical Modulation Amplitude (OMA), each lane (min)(^b)</td>
<td>-6.4</td>
<td>dBm</td>
</tr>
<tr>
<td>Launch power in OMA minus TDEC (min)</td>
<td>-7.3</td>
<td>dBm</td>
</tr>
<tr>
<td>Transmitter and dispersion eye closure (TDEC), each lane (max)</td>
<td>4.3</td>
<td>dB</td>
</tr>
<tr>
<td>Average launch power of OFF transmitter, each lane (max)</td>
<td>-30</td>
<td>dBm</td>
</tr>
<tr>
<td>Extinction ratio (min)</td>
<td>2</td>
<td>dB</td>
</tr>
<tr>
<td>Optical return loss tolerance (max)</td>
<td>12</td>
<td>dB</td>
</tr>
<tr>
<td>Encircled flux(^c)</td>
<td>≥ 86% at 19 μm, ≤ 30% at 4.5 μm</td>
<td></td>
</tr>
<tr>
<td>Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}</td>
<td>{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}</td>
<td></td>
</tr>
</tbody>
</table>

### Notes
- Full TDEC Tek test solution currently in process, using Tek Tx instruments in currently in place
- Center wavelength, RMS spectral width, Optical Return Loss, and Encircled Flux supported by alternate instruments
## Tx Test
### SR4 Transmitter Test Configuration

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSA8300/ADVTRIG/JNB02</td>
<td>Sampling scope mainframe</td>
<td>1</td>
</tr>
<tr>
<td>82A04B</td>
<td>Phase reference module</td>
<td>1</td>
</tr>
<tr>
<td>CR286A/HS/XLBW</td>
<td>Clock Recovery module</td>
<td>1</td>
</tr>
<tr>
<td>80C15 with option CRTP</td>
<td>Optical plugin for DSA8300 with CRTP option</td>
<td>1</td>
</tr>
<tr>
<td>80A08</td>
<td>Accessory kit</td>
<td>1</td>
</tr>
</tbody>
</table>
Sampling Scope System
Optical CDR, MM or SM Fiber, 28.6Gb/s

- CDR for optical MM & SM 25-28.5Gb/s standards
  - Optical head with dedicated Trigger O/E
  - Un-filtered Optical Bandwidth >35GHz
  - 62.5/125 μm Multi-Mode Fiber Input
  - Short and Long Wavelength Support (800-1600 nm)
  - Trigger O/E -15dBm sensitivity
- 100Gbase-LR4/ER4/SR4 optical receiver filters
- Best optical MM sensitivity to -9dBm
- Highest acquisition throughput @ 180kSamples/sec
- Jitter and noise analysis and decomposition
- CTLE filter application
- Embedding and de-embedding
- TDR, insertion, and return loss up to 50GHz
- RIN & RINxOMA support
Tektronix 80C15 Optical Sampling Module Highlights

NEW 80C15

- Single-Channel Optical Plug-in Module for DSA8300
- Unfiltered Optical Bandwidth >32 GHz
- 62.5/125 µm Multi-Mode Fiber Input
- Short- and Long-Wavelength Support 780-1650 nm
- 200 kS/s Acquisition Rate
- Jitter Floor <150 fs_{RMS} (with 82A04B)
- Reference Receiver Filters:
  - 32G FibreChannel (28.05 Gb/s)
  - OTU4 (27.95 Gb/s)
  - 100Gbase-LR4/ER4/SR4 (25.78 Gb/s)
  - 26G EDR Infiniband (25.78 Gb/s)
80C15: Tektronix Optical portfolio with unmatched accuracy, noise performance, and flexibility

<table>
<thead>
<tr>
<th>Feature / Specification</th>
<th>80C15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Fiber Type</td>
<td>SMF + MMF 9, 50, 62.5 µm</td>
</tr>
<tr>
<td>Wavelength Range</td>
<td>780nm-1650nm</td>
</tr>
<tr>
<td>Unfiltered Optical Bandwidth</td>
<td>32+ GHz</td>
</tr>
<tr>
<td>Unfiltered Risetime, typ</td>
<td>14 ps</td>
</tr>
<tr>
<td>Filter Rates</td>
<td>25.78 – 28.05 Gb/s</td>
</tr>
<tr>
<td>26 Gb/s Mask Test Sensitivity</td>
<td>-9 dBm</td>
</tr>
<tr>
<td>AOP @ 1310nm</td>
<td></td>
</tr>
<tr>
<td>Usable Electrical Out</td>
<td>32 Gb/s</td>
</tr>
</tbody>
</table>
Tektronix 80C15 module, optional CRTP (Electrical Out)

**80C15 CRTP**

- Single-Channel Optical Plug-in Module for DSA8300 with optional **Electrical Clock Recovery Trigger Pickoff** (CRTP)
- Unfiltered Optical Bandwidth >32GHz
- 62.5/125 µm **Multi-Mode** Fiber Input
- **Short-** and Long-Wavelength Support (800 - 1600 nm)
- 200 kS/s Acquisition Rate
- **Jitter Floor** <150 fs RMS (with 82A04B)
- Optical Receiver Filters:
  - 32G Fibre Channel (28.05 Gb/s)
  - OTU-4 (4 x 27.95 Gb/s)
  - 100Gbase-LR4/ER4/SR4 (25.78 Gb/s)
  - 26G EDR Infiniband (25.78 Gb/s)
Connection for 80C15

Tektronix 80C15 Connection Diagram
## Rx Test

### SR4 Receiver Test Specifications and Algorithm

#### Table 95–7—100BASE-SR4 receive characteristics

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signaling rate, each lane (range)</td>
<td>25.78125 ± 100 ppm</td>
<td>GBd</td>
</tr>
<tr>
<td>Center wavelength (range)</td>
<td>840 to 860</td>
<td>nm</td>
</tr>
<tr>
<td>Damage threshold(^a) (min)</td>
<td>3.4</td>
<td>dBm</td>
</tr>
<tr>
<td>Average receive power, each lane (max)</td>
<td>2.4</td>
<td>dBm</td>
</tr>
<tr>
<td>Average receive power, each lane(^b) (min)</td>
<td>−10.3</td>
<td>dBm</td>
</tr>
<tr>
<td>Receive power, each lane (OMA) (max)</td>
<td>3</td>
<td>dBm</td>
</tr>
<tr>
<td>Receiver reflectance (max)</td>
<td>−12</td>
<td>dB</td>
</tr>
<tr>
<td>Stressed receiver sensitivity (OMA), each lane(^c) (max)</td>
<td>−5.2</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>Conditions of stressed receiver sensitivity test(^d)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stressed eye closure (SEC), lane under test</td>
<td>4.3</td>
<td>dB</td>
</tr>
<tr>
<td>Stressed eye J2 Jitter, lane under test</td>
<td>0.39</td>
<td>UI</td>
</tr>
<tr>
<td>Stressed eye J4 Jitter, lane under test (max)</td>
<td>0.53</td>
<td>UI</td>
</tr>
<tr>
<td>OMA of each aggressor lane</td>
<td>3</td>
<td>dBm</td>
</tr>
<tr>
<td>Stressed receiver eye mask definition ({X_1, X_2, X_3, Y_1, Y_2, Y_3})</td>
<td>(0.28, 0.5, 0.5, 0.33, 0.33, 0.4)</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**
- Center wavelength and receiver reflectance supported by alternate instruments

---

**Supported by Tek Rx measurement tools**
100 GBASE-SR4 and TDEC

- 100GBASE-LR4, ER4 and PSM4 and CLR4 are all supported by 80C15 and 80C10C
- 100GBASE-SR4 bring MM; 80C15 can handle all of that
- What are the new measurement in SR4?

**Figure 95-3—TDEC conformance test block diagram**

A block diagram for the TDEC conformance test is shown in Figure 95–3. Other measurement implementations may be used with suitable calibration.
TDEC measurement process

- Relatively complicated processing of several histograms
- Transmitter and dispersion eye closure (<4.3dB)
100GBASE-SR4 and TDEC measurement automated with TekExpress
TDEC (Transmitter and dispersion eye closure) a penalty of an optical Transmitter

- TDEC is at best 0 dB (i.e. no penalty – the TX is IDEAL)
- Standards set the highest TDEC (highest penalty) allowable
- TDEC for Multi Mode fiber uses special BW limiting in the module:
- Discussion on SR4 and TDEC
Rx Test
SR4 Receiver Test Algorithm

**Recommended SR4 RX test algorithm:**
- Configure setup per slide 11
- Measure SEC, J2, and J4 using DSA8300
- Iteratively adjust SI insertion from AFG and RJ insertion from PPG until Table 95-7 specs for SEC, J2, and J4 are simultaneously met

**Notes:**
- Tektronix SR4 Solution requires E/O and O/E test components
  - 80C15 can be used with DSA300 for O/E
  - Recommended external E/O options available upon request
SR4 Stressed Receiver Block Diagram

Figure 95–5—Stressed receiver conformance test block diagram
## SR4 Receiver Test Configuration

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPG3204/HFJ/ADJ</td>
<td>4-ch 32Gb/s PPG w/ jitter insertion</td>
<td>1</td>
</tr>
<tr>
<td>PED3202</td>
<td>2-ch 32Gb/s error detector</td>
<td>2</td>
</tr>
<tr>
<td>DSA8300/ADVTRIG/JNB02</td>
<td>Sampling scope mainframe</td>
<td>1</td>
</tr>
<tr>
<td>80C15</td>
<td>Optical plugin for DSA8300</td>
<td>1</td>
</tr>
<tr>
<td>PPG3002, crosstalk generator</td>
<td>2CH 30G PPG</td>
<td>1</td>
</tr>
<tr>
<td>PSPL5333, crosstalk generation</td>
<td>1:2 power splitter</td>
<td>2</td>
</tr>
<tr>
<td>AFG325C</td>
<td>240 MHz function generator</td>
<td>1</td>
</tr>
<tr>
<td>CR268A</td>
<td>Clock recovery module</td>
<td>1</td>
</tr>
<tr>
<td>PSPL5361</td>
<td>40GHz pick off T</td>
<td>2</td>
</tr>
<tr>
<td>80A08</td>
<td>Accessory kit</td>
<td>1</td>
</tr>
</tbody>
</table>
Rx Test
SR4 Pattern Requirements

- SR4 test requires both user pattern and PRBS generation
- PatternPro PPG and PED can generate full suite of PRBS patterns, as well as any user patterns up to 2Mb memory depth
  - Solution for square wave and RS-FEC encoded scrambled idle patterns
- Each channel of PPG3204 can be programmed with an individual user pattern with channel-specific skew
  - Solution for emulating FEC-striping across four lanes

Table 95–9—Test patterns

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Pattern description</th>
<th>Defined in</th>
</tr>
</thead>
<tbody>
<tr>
<td>Square wave</td>
<td>Square wave (8 ones, 8 zeros)</td>
<td>83.5.10</td>
</tr>
<tr>
<td>3</td>
<td>PRBS31</td>
<td>83.5.10</td>
</tr>
<tr>
<td>4</td>
<td>PRBS9</td>
<td>83.5.10</td>
</tr>
<tr>
<td>5</td>
<td>RS-FEC encoded scrambled idle</td>
<td>82.2.10a</td>
</tr>
</tbody>
</table>

The pattern defined in 82.2.10 as encoded by Clause 91 RS-FEC for 100GBASE-SR4
# Rx Test

## Sinusoidal Interference Receiver Configuration and Calibration

The target values from Table 97-5 of **IEEE802.3bm Spec.**

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stressed eye closure (SEC), lane under test</td>
<td>4.3dB</td>
</tr>
<tr>
<td>Stressed eye J2 Jitter, lane under test</td>
<td>0.39UI</td>
</tr>
<tr>
<td>Stressed eye J4 Jitter, lane under test (max)</td>
<td>0.53UI</td>
</tr>
</tbody>
</table>

BERT running at 25.78Gb/s, PRBS11 pattern. 40GHz pick-off T connected to BERT output (through path) and 100MHz function generator (pick-off path). Function generator provides sinusoidal CMI to both P and N, closing the eye.
Rx Test
BERT System

Stressed Receiver Sensitivity

- Multi channel 32Gb/s pattern generator
  - Low inherent jitter <250fsec RMS
  - ~10psec rise/fall time (20-80%)
  - RJ, SJ, and BUJ jitter stress
  - Full rate or half rate clock output
  - DC coupled outputs
  - PRBS or custom patterns
  - Adjustable channel phase delay

- 1/2-ch 32Gb/s error detector
  - Best in class sensitivity @ 6mV
  - Auto or manual voltage adjust
  - Auto-sync to input pattern
  - PC GUI SW that provides:
    - Remote instrument control
    - Bathtub and Contour Analysis
    - JTOL measurements
    - J2/J9 measurements
Low instrument intrinsic jitter is critical for SR4

- **Tektronix PPG3204:**
  - Support for rates through 32G
  - Low intrinsic jitter across data rates

### Measured Results @ 25G

<table>
<thead>
<tr>
<th>Data Source: Ch7</th>
<th>Data Rate: 25 Gbps</th>
<th>Filter: False</th>
<th>Noise (Sampling Phase: 0 UI)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source: Ch7</td>
<td>Rate: 25 Gbps</td>
<td>Phase Reference: 25 MHz</td>
<td>Random Jitter:</td>
</tr>
<tr>
<td>SSK: Off</td>
<td>Pattern: 2047 bits</td>
<td>Sample Count: 304.70 k</td>
<td>RX (RMS) = 289.55 fs</td>
</tr>
<tr>
<td>Clock Reference: 32 GHz</td>
<td></td>
<td></td>
<td>Rn(v) (RMS) = 283.15 fs</td>
</tr>
<tr>
<td>Jitter (Decision Threshold: -1.28 ns)</td>
<td></td>
<td></td>
<td>R(n) (RMS) = 280.5 fs</td>
</tr>
</tbody>
</table>

### Measured Results @ 32G

<table>
<thead>
<tr>
<th>Data Source: Ch7</th>
<th>Data Rate: 32 Gbps</th>
<th>Filter: False</th>
<th>Noise (Sampling Phase: 0 UI)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source: Ch7</td>
<td>Rate: 32 Gbps</td>
<td>Phase Reference: 32 GHz</td>
<td>Random Jitter:</td>
</tr>
<tr>
<td>SSK: Off</td>
<td>Pattern: 2047 bits</td>
<td>Sample Count: 304.70 k</td>
<td>RX (RMS) = 229.47 fs</td>
</tr>
<tr>
<td>Clock Reference: 32 GHz</td>
<td></td>
<td></td>
<td>Rn(v) (RMS) = 223.21 fs</td>
</tr>
<tr>
<td>Jitter (Decision Threshold: -2.48 ns)</td>
<td></td>
<td></td>
<td>R(n) (RMS) = 220.3 fs</td>
</tr>
</tbody>
</table>

### Key 100G Electrical Specs

<table>
<thead>
<tr>
<th>100GBase-*R4</th>
<th>100GBase-*R4 (FEC)</th>
<th>CEI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rate</td>
<td>25.7813</td>
<td>27.7390</td>
</tr>
<tr>
<td>I UI (period)</td>
<td>38.7879</td>
<td>36.0500</td>
</tr>
<tr>
<td>Allocated Rj (UI)</td>
<td>0.13</td>
<td>0.13</td>
</tr>
<tr>
<td>Rj in fs RMS</td>
<td>360.2</td>
<td>334.8</td>
</tr>
</tbody>
</table>
Rx Test
32Gb/s Multi-channel BERT electrical performance

PPG320X 32Gb/s OPT-ADJ

- **Data rate** range = 1.5 to 32 Gb/s
- **Voltage adjustability** = 300mV - 1Vpp single-ended (600mV - 2Vpp diff)
- **Rise/fall time** <11ps (20-80%)
- **Intrinsic Jitter** < 7ps TJ@1E-12

**Industry Best 32Gb/s Jitter Performance!**

**Data Source:** MATH1
**SSC:** Off
**Phase Reference:** 32 GHz

**Noise:**
- Random Noise (RMS) = 581.45 UV
- Deterministic Noise (RMS) = 582.11 UV
- Deterministic Noise (V) = 128.35 UV

**Total Jitter @ BER**
- TJ (1E-12) = 6.76 ps
- Eye Opening (1E-12) = 50.89 ps

**Dual Dirac**
- RJ(d-e) = 243.96 fs
- DJ(d-e) = 3.32 fs

**Industry Best 32Gb/s Jitter Performance!**
Rx Test

DSA8300 SJNB SJ Measurements

28G Jitter Baseline
0ps added SJ
1ps measured PJ

28G Jitter with
20ps added SJ at 10MHz
20ps measured PJ
Rx Test
Best in class PED Sensitivity

- PED can measure input data signals of 6-750mVpp
- With 6mVpp, PED properly center voltage & phase sampling point and synchronizes to input pattern
- Contour plot below measured at 28Gb/s with 6mVpp input signal
- **Highly sensitive PED allows for very precise BER measurements at low input power levels**
Transceiver Test
Tektronix 100GBASE-SR4 Test Solutions

PPG3204 32G PPG

4x25G electrical
E/O
E/O
E/O
E/O

MUX
DUT, eg CFP4 SR4 XCVR

4x25G electrical
O/E
O/E
O/E
O/E

CR286A Clock Recovery

SR4 Optical Test Solutions

PED3202 32G PED

DSA8300 with 80E10B and 80C15 plug-ins

PPG3204 32G PPG

4x25G electrical
E/O
E/O
E/O
E/O

DUT, eg CFP4 SR4 XCVR

4x25G electrical
O/E
O/E
O/E
O/E

CR286A Clock Recovery

PED3202 32G PED

DSA8300 with 80E10B plug-ins

DUT, eg chip-to-module

PPG3204 32G PPG

4x25G electrical
E/O
E/O
E/O
E/O

4x25G electrical loopback

CR286A Clock Recovery

PED3202 32G PED

DSA8300 with 80E10B plug-ins

SR4 Electrical Test Solutions

Tektronix 100G -> 400G
What is Coherent Optical Modulation?

Traditional 10G transmissions modulate the amplitude of the light, a.k.a. or on-off keying (OOK). Direct detection is used in the receiver.

**OOK**
On-Off Keying
1 bit/Baud (symbol)

Coherent transmissions modulate the phase of the light, the simplest case is phase shift keying.

**PSK**
Phase Shift Keying
1 bit/Baud (symbol)

By doubling the number of phase states, the bit/Baud rate is also doubled.

**QPSK**
Quadrature Phase Shift Keying
2 bits/Baud (symbol)
What is Coherent Optical Modulation?

Rotating the polarization of one QPSK signal, and combining it with a second QPSK signal, doubles the bits/Baud rate again.

**DP-QPSK**
Dual-Polarization QPSK
4 bits/Baud (symbol)
# Common Modulation Formats

<table>
<thead>
<tr>
<th>Modulation Format</th>
<th>28 Gb/s</th>
<th>32 Gb/s</th>
<th>40 Gb/s</th>
<th>46 Gb/s</th>
<th>56 Gb/s</th>
<th>64 Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>NRZ/PAM2 1 bit per Baud (symbol)</td>
<td>28 Gb/s</td>
<td>32 Gb/s</td>
<td>40 Gb/s</td>
<td>46 Gb/s</td>
<td>56 Gb/s</td>
<td>64 Gb/s</td>
</tr>
<tr>
<td>BPSK 1 bit per Baud (symbol) per polarization</td>
<td>28 Gb/s</td>
<td>32 Gb/s</td>
<td>40 Gb/s</td>
<td>46 Gb/s</td>
<td>56 Gb/s</td>
<td>64 Gb/s</td>
</tr>
<tr>
<td>PAM4 2 bits per Baud (symbol)</td>
<td>56 Gb/s</td>
<td>64 Gb/s</td>
<td>80 Gb/s</td>
<td>92 Gb/s</td>
<td>112 Gb/s</td>
<td>128 Gb/s</td>
</tr>
<tr>
<td>QPSK 2 bits per Baud (symbol) per polarization</td>
<td>56 Gb/s</td>
<td>64 Gb/s</td>
<td>80 Gb/s</td>
<td>92 Gb/s</td>
<td>112 Gb/s</td>
<td>128 Gb/s</td>
</tr>
<tr>
<td>8PSK 3 bits per Baud (symbol) per polarization</td>
<td>84 Gb/s</td>
<td>96 Gb/s</td>
<td>120 Gb/s</td>
<td>138 Gb/s</td>
<td>168 Gb/s</td>
<td>192 Gb/s</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Modulation Format</th>
<th>28 Gb/s</th>
<th>32 Gb/s</th>
<th>40 Gb/s</th>
<th>46 Gb/s</th>
<th>56 Gb/s</th>
<th>64 Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>8QAM 3 bits per Baud (symbol) per polarization</td>
<td>84 Gb/s</td>
<td>96 Gb/s</td>
<td>120 Gb/s</td>
<td>138 Gb/s</td>
<td>168 Gb/s</td>
<td>192 Gb/s</td>
</tr>
<tr>
<td>16QAM 4 bits per Baud (symbol) per polarization</td>
<td>112 Gb/s</td>
<td>128 Gb/s</td>
<td>160 Gb/s</td>
<td>184 Gb/s</td>
<td>224 Gb/s</td>
<td>256 Gb/s</td>
</tr>
<tr>
<td>32QAM 5 bits per Baud (symbol) per polarization</td>
<td>140 Gb/s</td>
<td>160 Gb/s</td>
<td>200 Gb/s</td>
<td>230 Gb/s</td>
<td>280 Gb/s</td>
<td>320 Gb/s</td>
</tr>
<tr>
<td>64QAM 6 bits per Baud (symbol) per polarization</td>
<td>168 Gb/s</td>
<td>192 Gb/s</td>
<td>240 Gb/s</td>
<td>276 Gb/s</td>
<td>336 Gb/s</td>
<td>384 Gb/s</td>
</tr>
</tbody>
</table>
Coherent System Building Blocks

Data Source → Coherent Optical Modulator → Coherent Receiver → A/D → lots of math

Electrical:
- 4 data streams, "tributaries", 1 each for X-I, X-Q, Y-I, and Y-Q
- 4 sampled waveforms representing electric field on fiber cable
  Not data!

Optical:
- All 4 tributaries into 2 polarizations of light on fiber cable

Electrical:
- Original 4 tributaries finally recovered

Because polarization of light is not fixed as it travels down the fiber optic cable, the signal that was originally the X-I tributary, may still be partially on X-I, but is likely also on X-Q, Y-I, and Y-Q!
These 4 waveforms are not just the sampled original tributaries!
Coherent System Building Blocks

Data Source

Coherent Optical Transceiver

A/D

lots of math

TX

RX

Fiber optic cable

Fiber optic cable
Coherent Test System Building Blocks

Data Source → Coherent Optical Modulator (Tx) → Coherent Receiver (Rx) → A/D → lots of math

Coherent Signal Generation
- PPG3204 32Gb/s Pattern Generator
- AWG70001A Arbitrary Waveform Generator

Coherent Modulation/Transmitter
- OM5110 Multi-format Optical Transmitter

Signal Acquisition (scope)
- OM1106 Optical Modulation Analysis Software (Included with OM4106D)

Analysis Software
- DPO77004SX Digital Phosphor Oscilloscope

Coherent Receiver
- OM4245 Optical Modulation Analyzer

Either the Transmitter or Receiver is typically replaced by the customer’s DUT.

Fiber optic cable

Fiber optic cable
Example Industry Approaches to 400G and Beyond

- No industry consensus on how to build super-channels – no one architecture fits all requirements.
- Vendors differ on characteristics as basic as carrier count and carrier spacing to what modulation format should be used.

<table>
<thead>
<tr>
<th>system rate</th>
<th># of carriers</th>
<th>modulation format</th>
</tr>
</thead>
<tbody>
<tr>
<td>400 Gb/s¹</td>
<td>2</td>
<td>DP-16QAM</td>
</tr>
<tr>
<td>500 Gb/s²</td>
<td>5</td>
<td>DP-QPSK</td>
</tr>
<tr>
<td>500 Gb/s³</td>
<td>10</td>
<td>DP-QPSK</td>
</tr>
<tr>
<td>1.0 Tb/s⁴</td>
<td>10</td>
<td>DP-QPSK</td>
</tr>
<tr>
<td>1.5 Tb/s⁵</td>
<td>8</td>
<td>DP-16QAM</td>
</tr>
</tbody>
</table>

Sources:
1. Beyond 100G, copyright 2012, Fujitsu Network Communications, Inc.
2. Dawn of the Terabit Age, copyright 2011, Infinera Corporation
3. Coherent Super-Channel Technologies, OSA Webinar, copyright 2011, Infinera Corporation
4. Super-Channels: DWDM Transmission at100Gb/s and Beyond, copyright 2012, Infinera Corporation
5. 1.5-Tb/s, 8-carrier Band-Banded Superchannel Transmission over 56 x 100-km (5600-km) ULAF Using 30-Gbaud Pilot-Free OFDM-16QAM Signals with 5.75-b/s/Hz Net Spectral Efficiency, Alcatel-Lucent, Bell Labs
Thank you !!!