高速串行通道的仿真与验证

ANSYS中国
李宝龙

当今电子设计的挑战

Simulation Driven Product Development:™

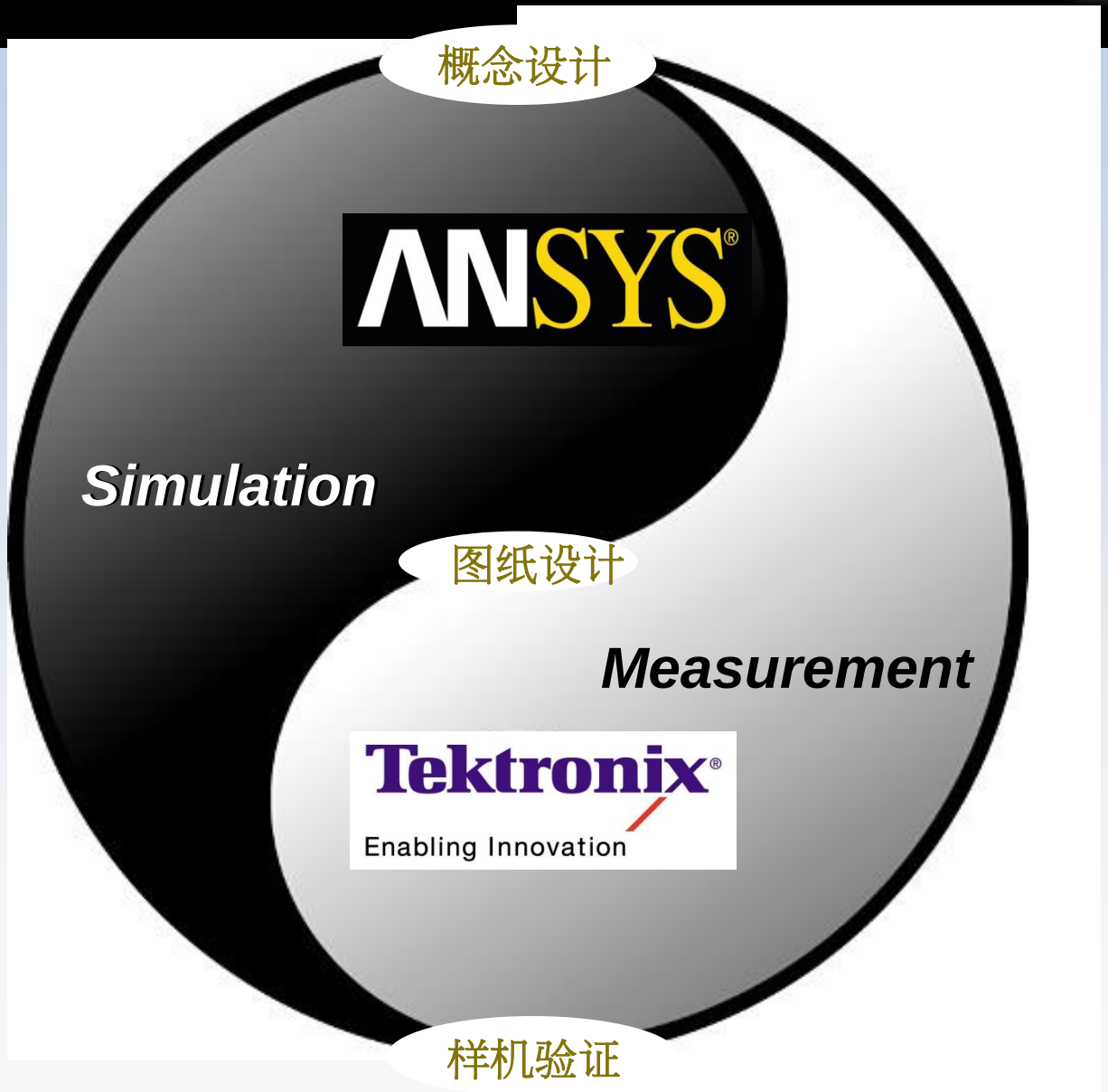
Digitally simulate performance across all physics of complete systems, in their real-world environments

- **BETTER** • *Innovative and higher-quality products*
- **FASTER** • *Dramatic time-to-market improvement*
- **CHEAPER** • *Minimize development, warranty and liability costs*

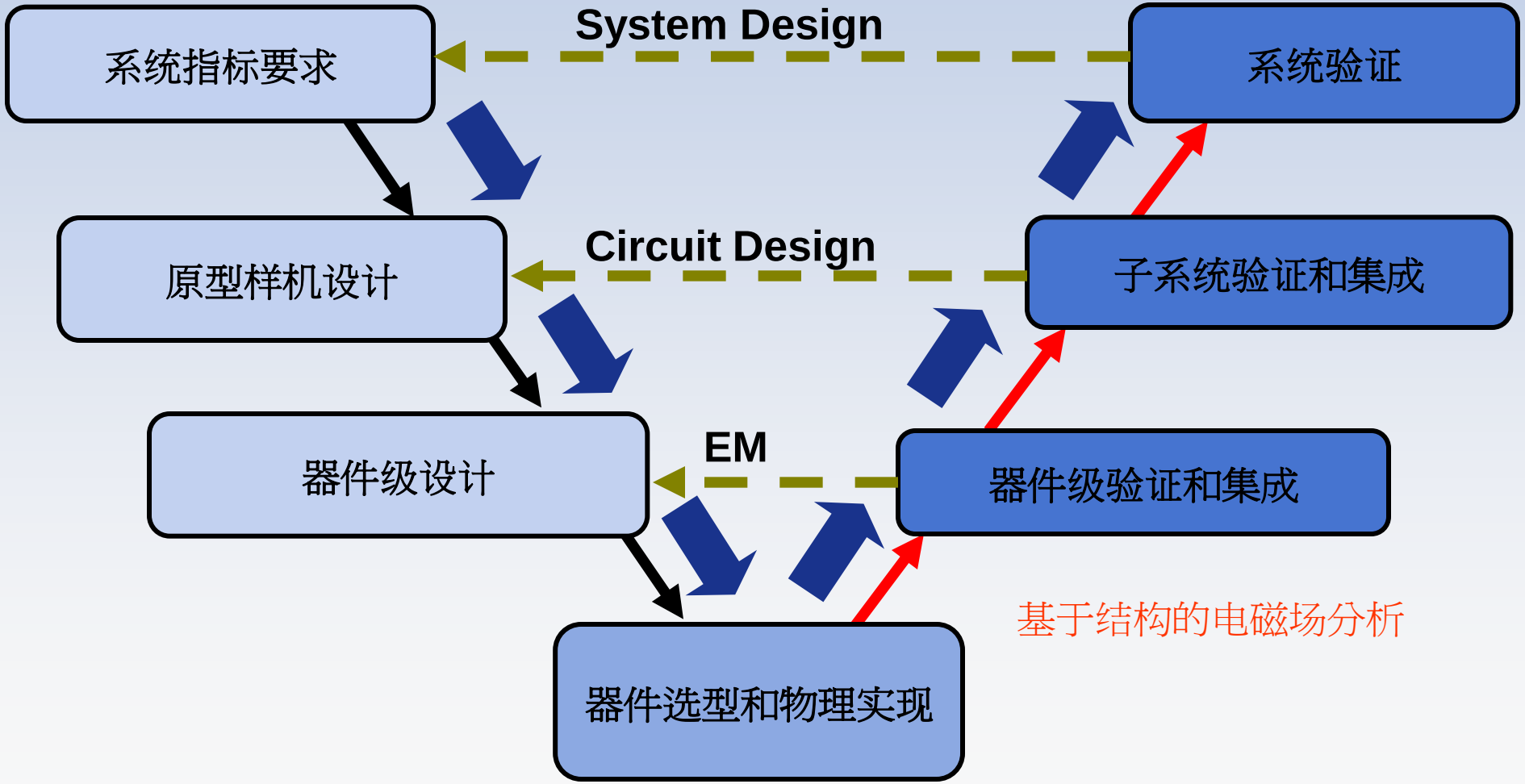
目录

- 现代电子设计流程
- 仿真与测试协同验证方法
  - 部件级
  - 通道级
  - 系统级
- 仿真与测试协同设计方法
  - 测试模型引入仿真软件
  - 仿真数据引入测试仪表
- 系统可靠性验证与设计空间探索
  - Apply the hybrid methodology
  - Validate against measured results
- 小结

现代电子设计流程



典型的高速通道设计流程



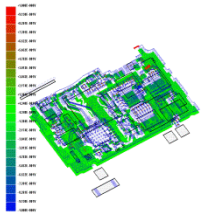
ANSYS高速PCB仿真的解决方案

Data Import

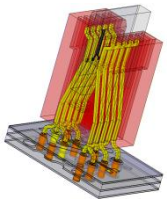
- Cadence
- Mentor
- Zuken
- Pro-E
- IGES/Step

- IBIS Model
- HSPICE
- Spectre

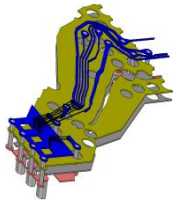
Extraction –提取 PCB / Connector / Cable / Package 的电气参数



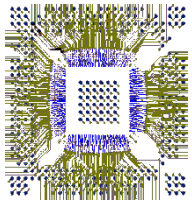
2.5D PCB 分析
SIwave



3D 电磁场分析
HFSS

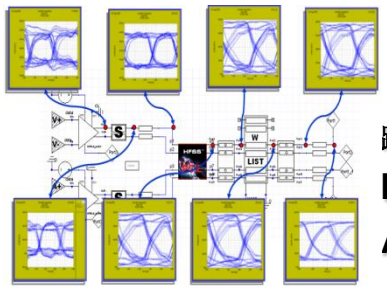


3D RLC输出
Q3D



高级封装分析
TPA

Simulation & Analysis – 整个系统的仿真以及各个模块的协同优化设计



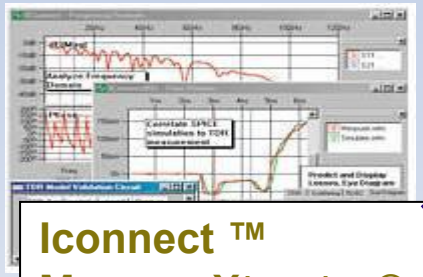
Ansoft Designer/Nexxim

跨时域、频域的 新一代的电路和系统仿真引擎

Harmonic Balance + Transient + Noise Analysis

仿真与测试协同验证方法

Tektronix®
Enabling Innovation



Iconnect ™
MeasureXtractor®

DSA8200

BERT Scope

Hybrid approach

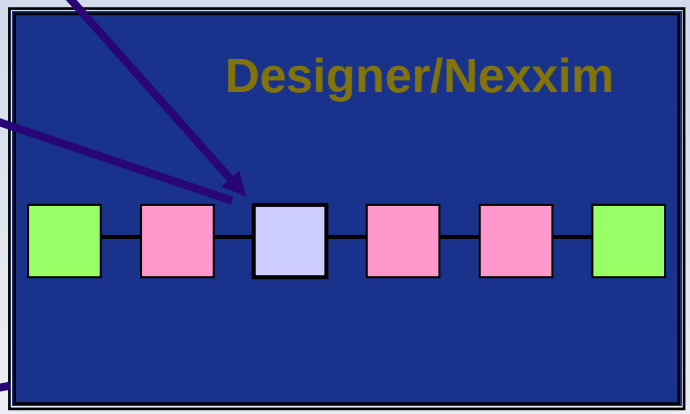
TDR-based model

frequency-domain

time-domain

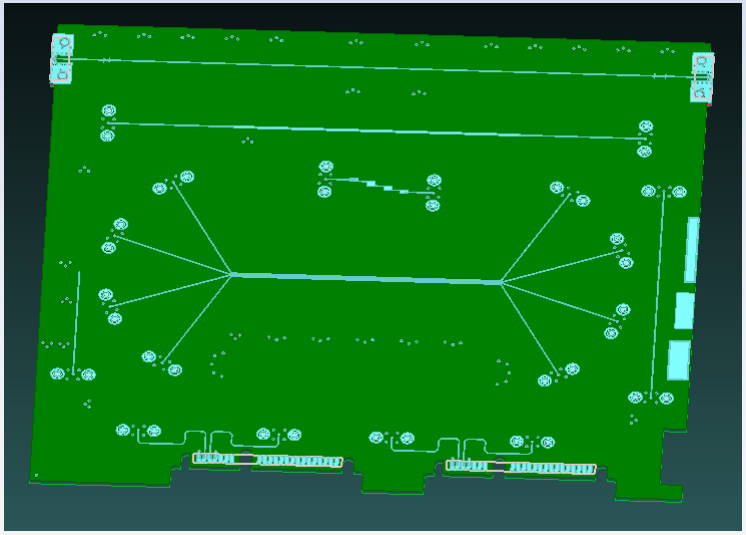
System Level

Designer/Nexxim



仿真与测试的验证对比是设计重要的里程碑.

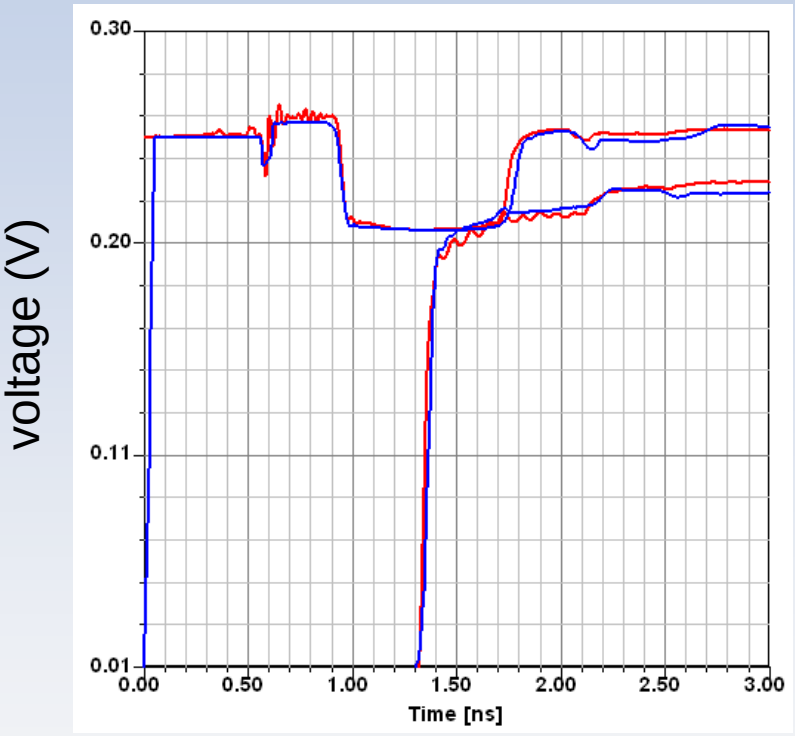
部件级验证



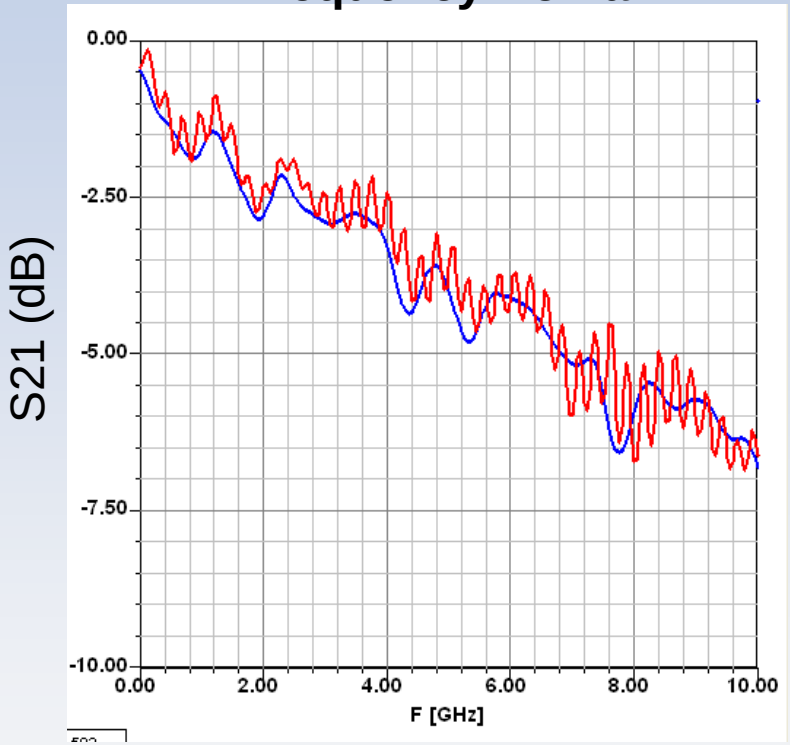
部件级仿真与测试验证

ANSYS®

Time Domain



Frequency Domain



Built-in Tline Simulation
TDR-based Measurement

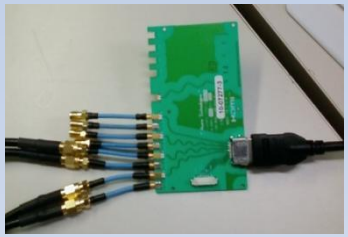
通道级验证

HDMI Full Channel

Tektronix®
Enabling Innovation

Instrumentation

DSA8200
w/ Iconnect

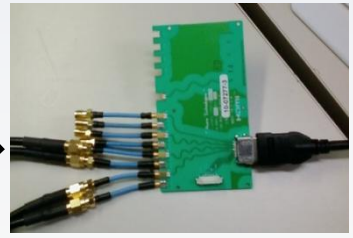


test adapter

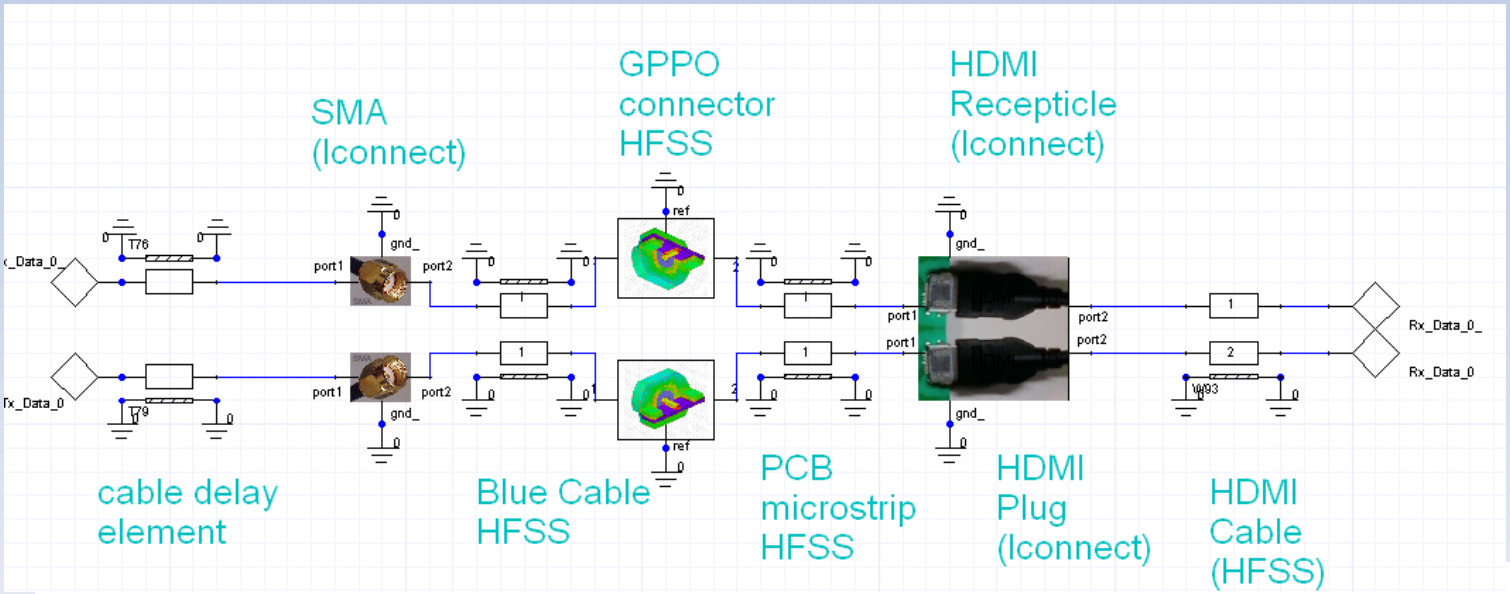
HDMI Assembly
(connectors + cable)

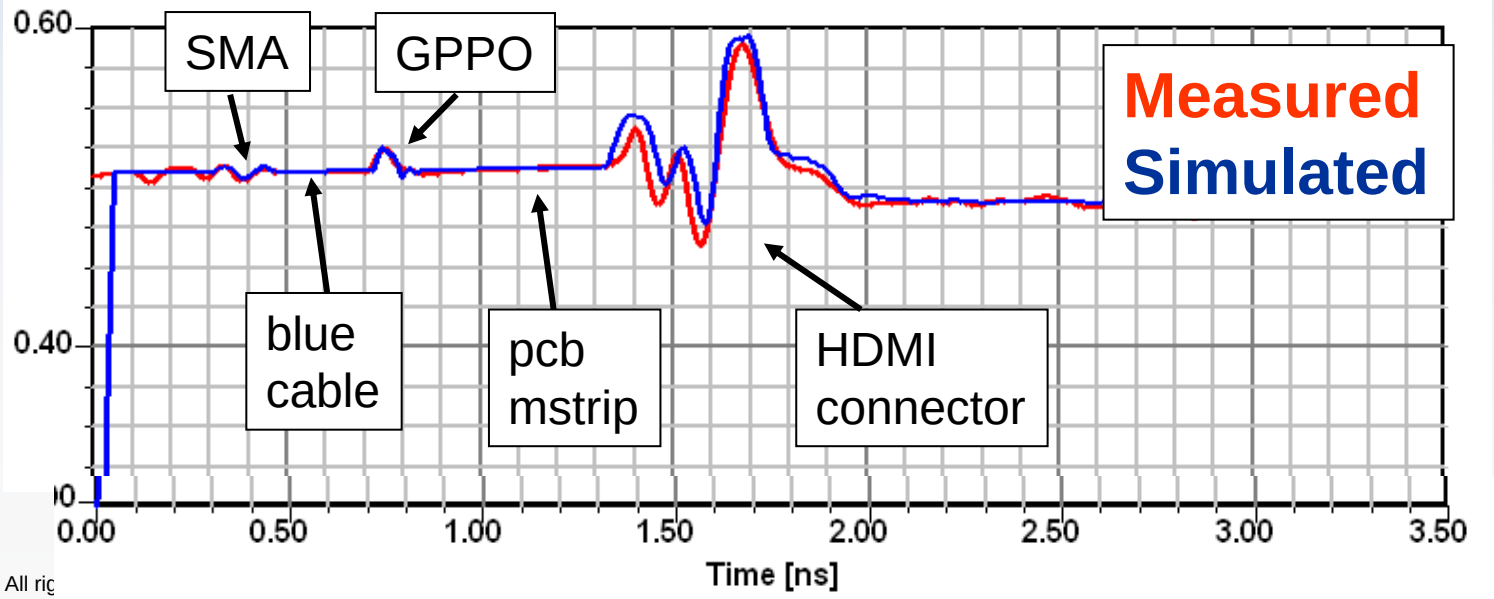
2.5m and 10m

test adapter

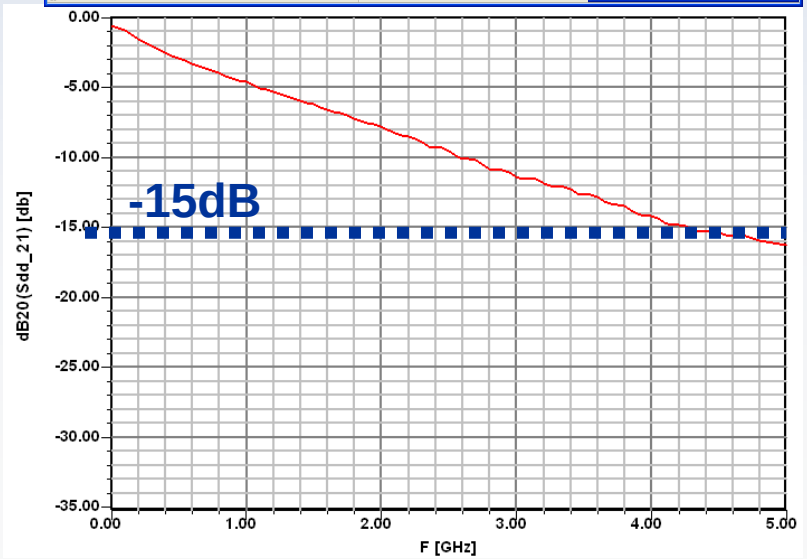


通道级仿真与测试验证——时域



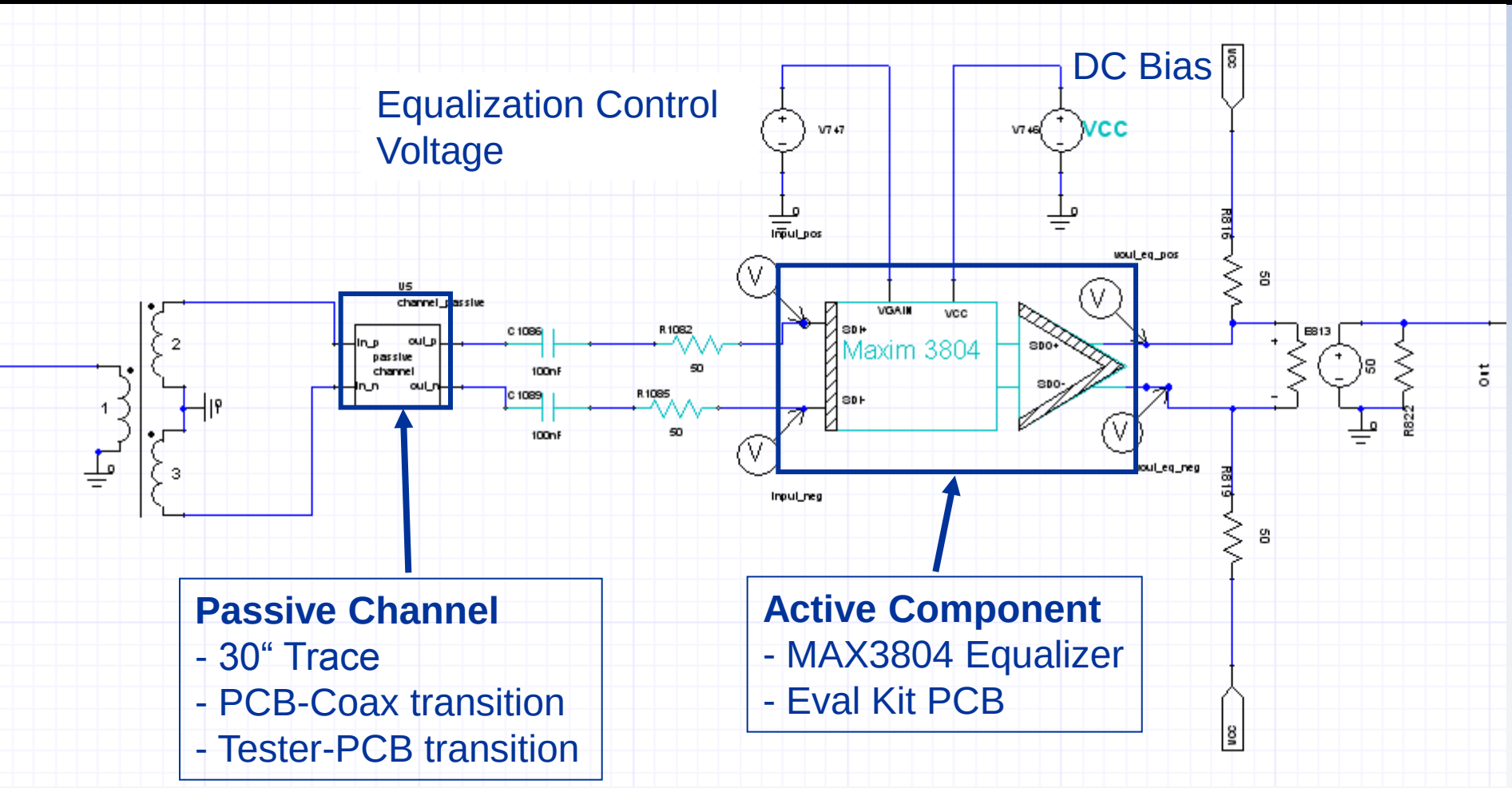


通道级仿真与测试验证——频域



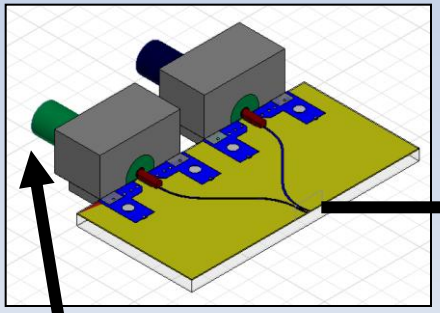
系统级验证：

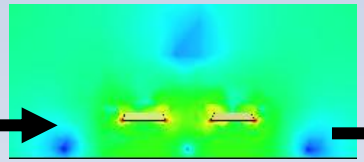
包括30“ traces, connectors 以及均衡器评估板



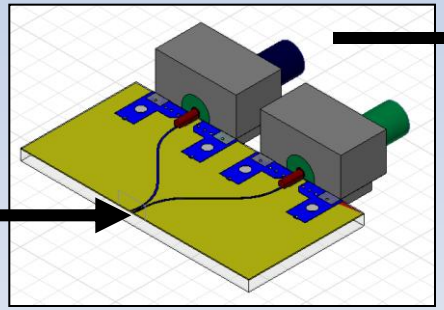
系统级验证框图

SMA launch onto PCB

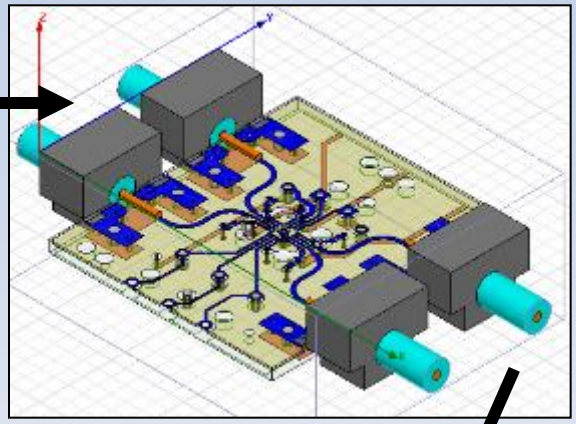




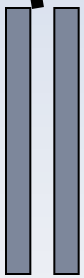
differential microstrip W-element model from HFSS



SMA launch off PCB



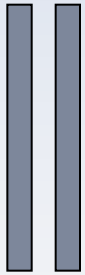
MAX3804 EV KIT



matched 3’ Hubner Suhner coax cables

pattern generator

HFSS DESIGNER NEXXIM

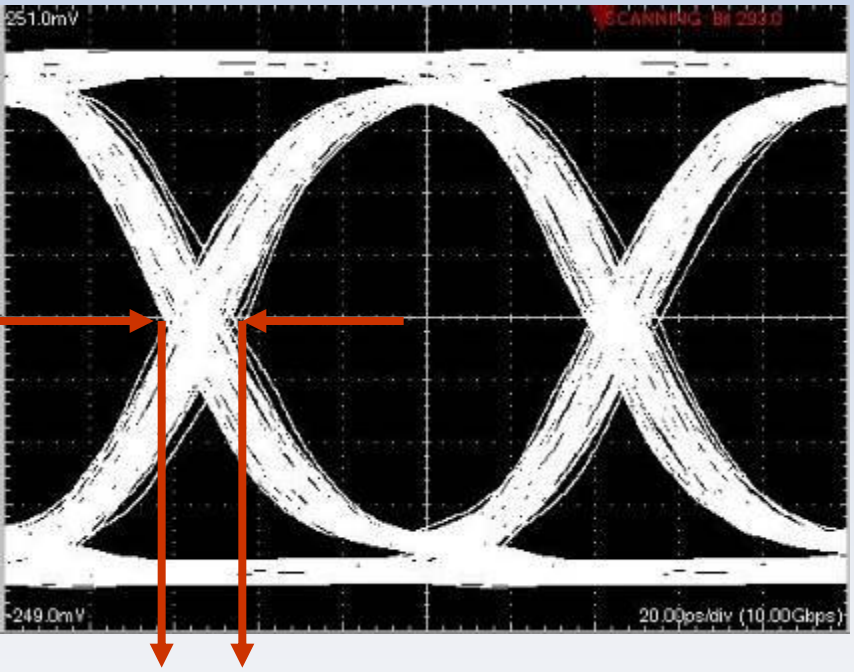


matched 3’ Hubner Suhner coax cables

Tektronix CSA8000 with FrameScan

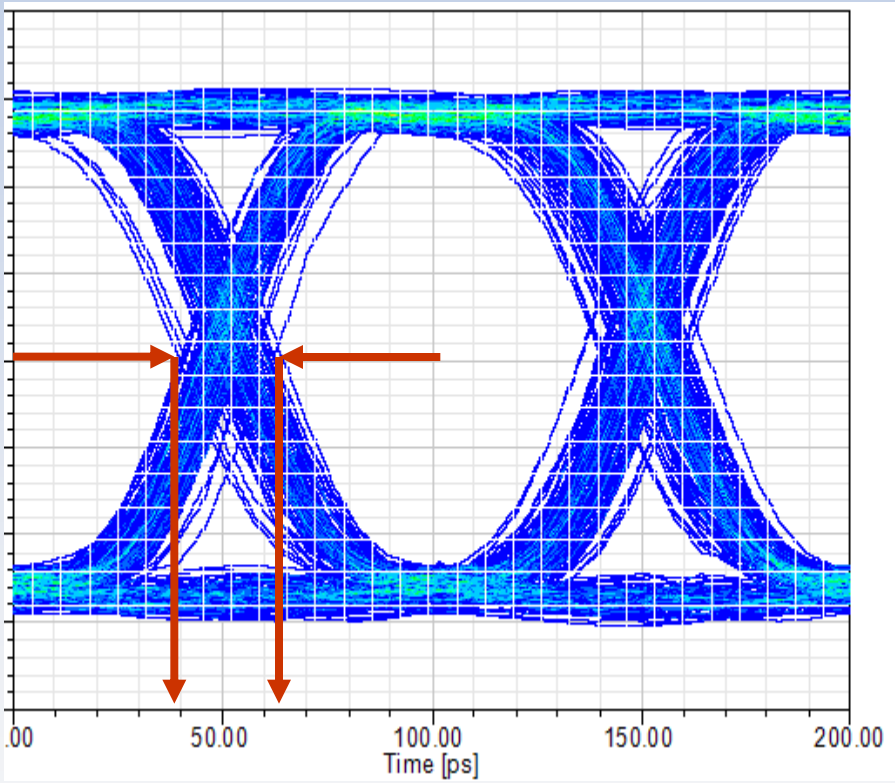
系统级验证对比

Measurement



jitter = 20ps

Simulation



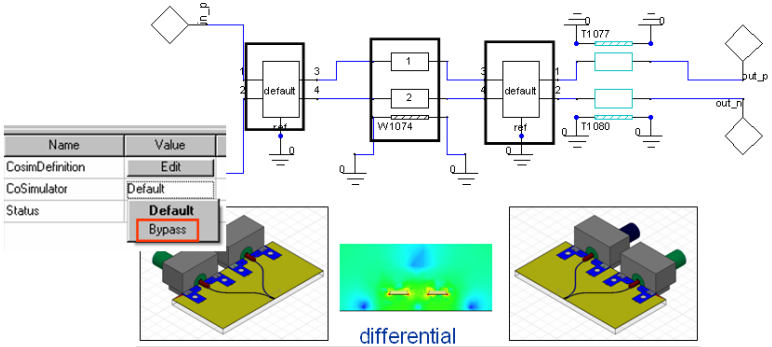
jitter = 23ps

仿真与测试协同设计方法1：
测试模型引入仿真软件

测试仪器
DSA8200+Iconnect

测试得到S参数或者波形文件S-par, Spice, CSV波形文件

实物元器件



Ansoft 软件仿真（时域、频域）

仿真与测试协同设计方法2:
仿真数据引入测试仪表

DSA8200+80SJNB

实物元器件

BERT Scope

仿真器件模型导入仪表

仿真自定义编码激励导入仪表

Ansoft 软件仿真建立信号模型

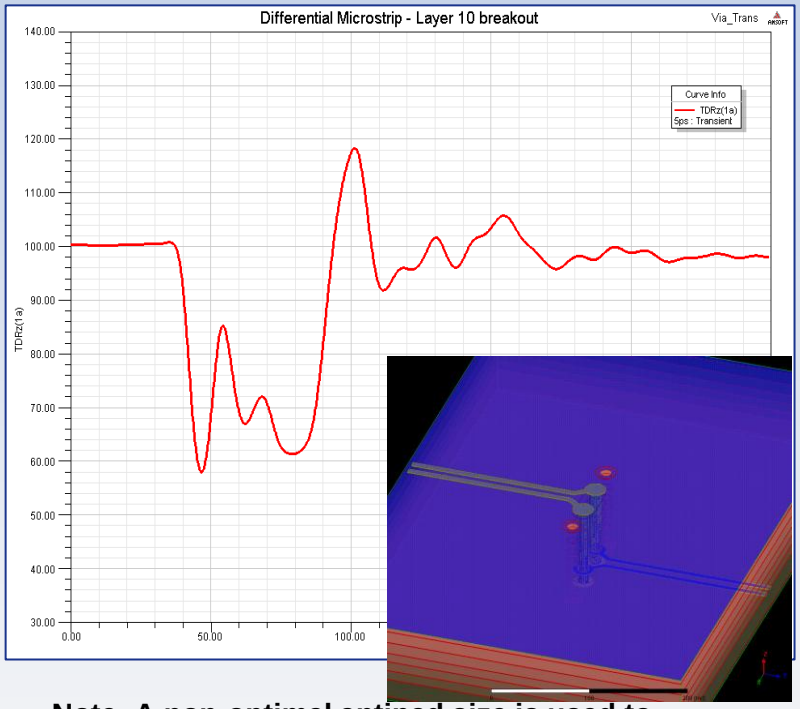
SIWAVE™
HFSS
Q3D Extractor

ANSOFT

DESIGNER

串行链路仿真优化

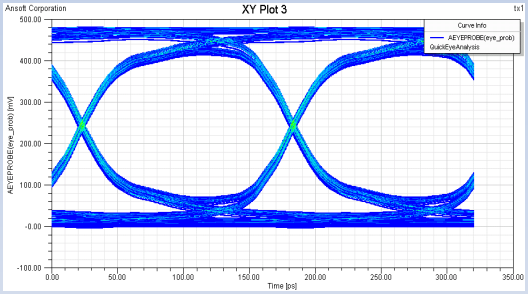
- 为什么要进行无源链路仿真？
  - 高速信号能否正确传输与无源链路性能关系密切；
  - 影响链路性能的因素有多种，每种因素的影响大小不同；
  - 优化每种因素所付出的代价不同，包括时间成本和和物料成本。

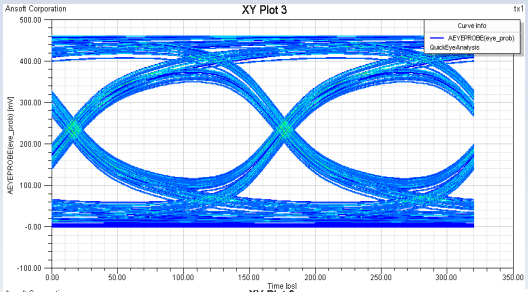


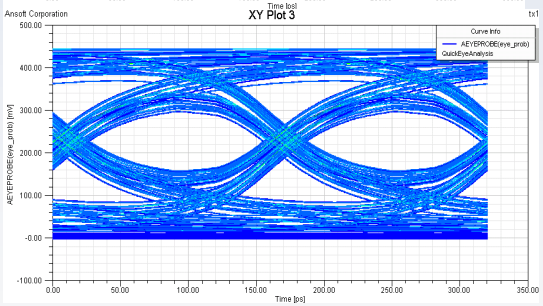
Note: A non-optimal antipad size is used to dramatize the reflection from the via transition in the animation

传输线长度对衰减影响

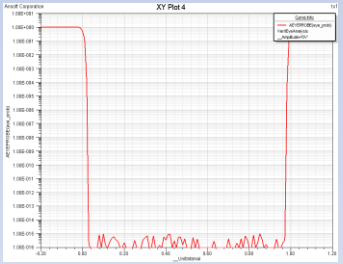
传输线长度增加

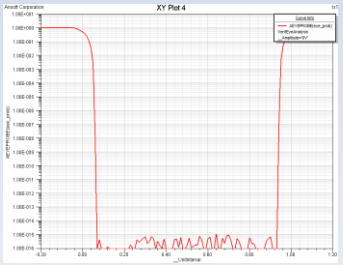


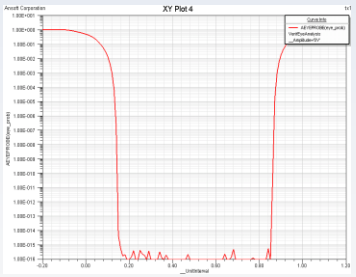




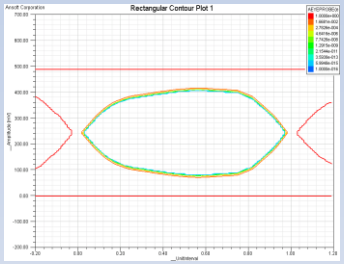
眼图

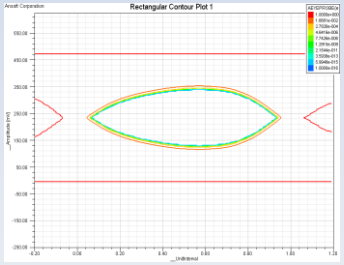


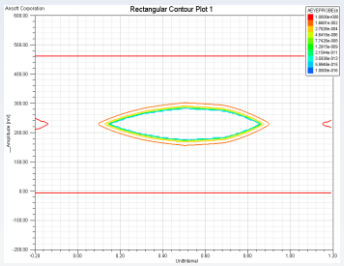




误码率







等高线眼图

瞬态仿真和统计仿真工具速度比较

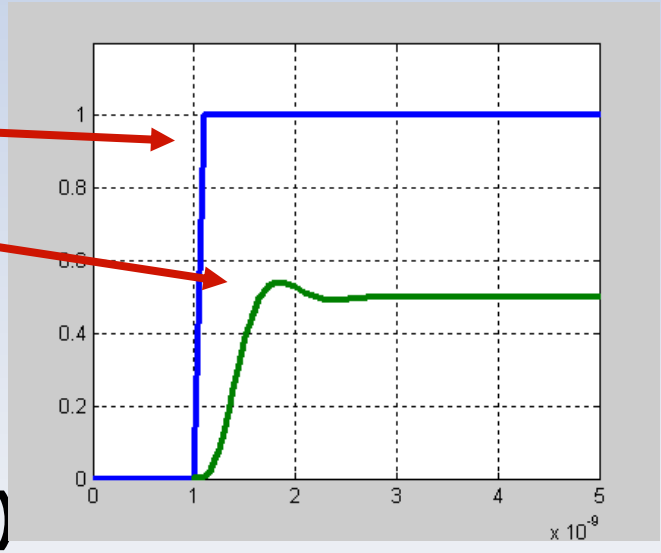
- 使用瞬态仿真器，能够得到非常准确的结果，当然必须输入准确的模型，仿真结果要在几个小时甚至1天以后才能得到。
  - 仿真时间 = UI*1/BER
- 统计仿真工具QuickEye可以迅速给出眼图；而 VerifiEye 能够快速提供误码率结果，这对前期的系统设计分析非常关键。
  - 基于快速卷积方法
  - 默认系统为线性时不变系统（LTI）

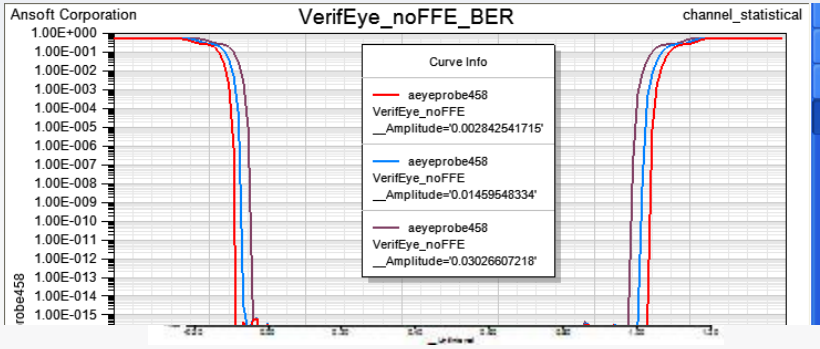
Statistical analysis1–
FastEye

"statisticalal Eye" Analysis
(lower accuracy, highest speed)

Algorithm:

- **Run transient**
  - Generates step response
- **Detect the delay**
- **Impose the step response**
  - On UI grid
- **Calculate probability of error (BER)**
  - For a single cell in the grid
  - Based on statistical assumptions
- **Generate Eye contour**
- **Visualizes worst eye**



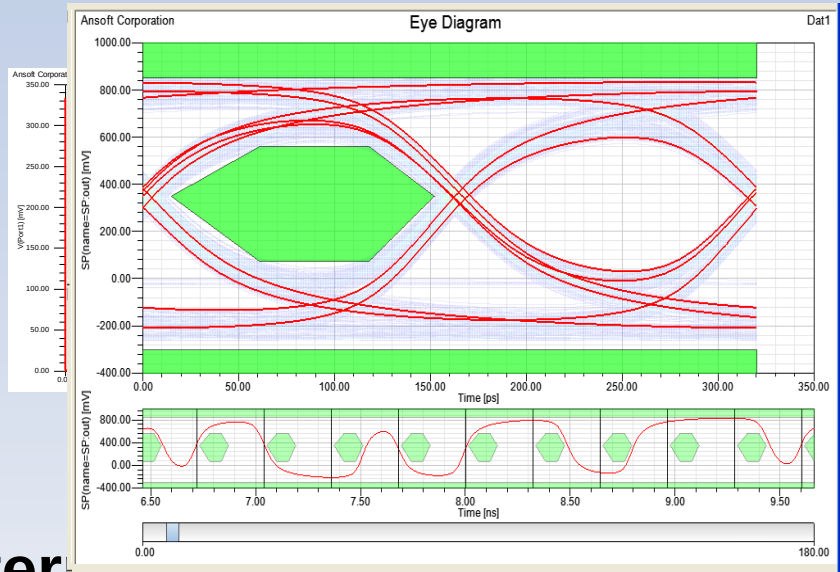


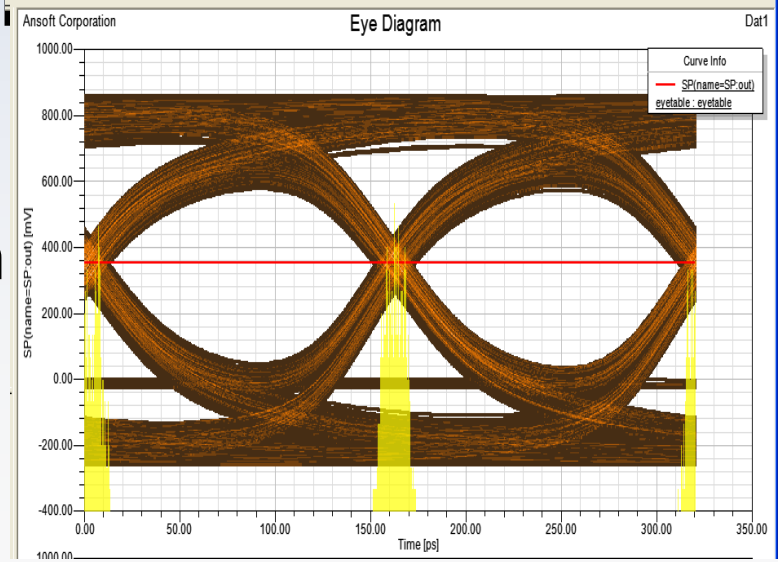
Statistical analysis2–
QuickEye

Bridge between statisticalal Eye & transient
(medium accuracy, medium speed)

Algorithm:

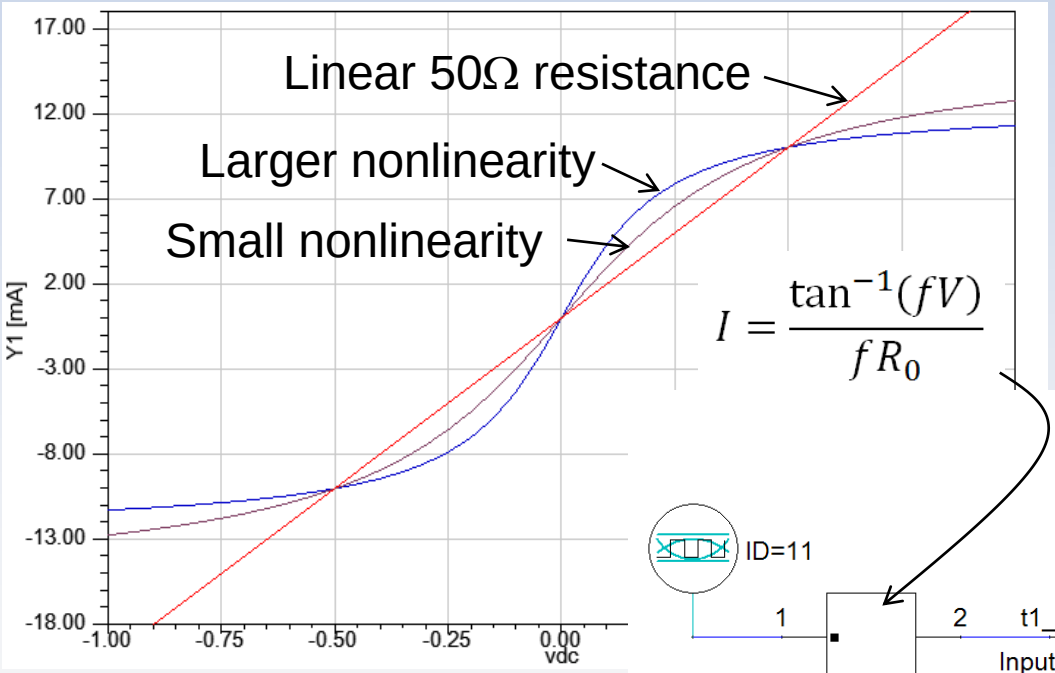
- **Run transient**
  - Generates step response
- **Convolve**
  - Input bit-stream with step response
- **Allows for very long input bit patter**
- **Provides fast time and eye plots**
- **Visualize eye mask violations**
- **Determine Jitter through Histogram threshold crossings**



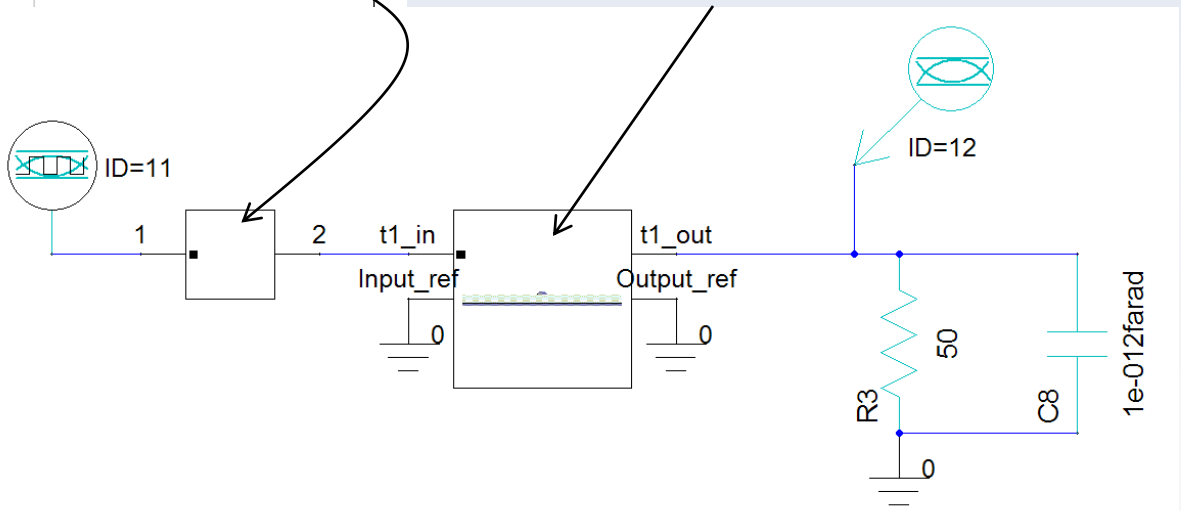


统计分析对于Non-LTI系统效果如何?

- **QuickEye and Verifeye assume linear channels**
- **If drivers are nonlinear, are QE and VE still useful?**
- **Simple channel with driver that has a nonlinear self impedance:**

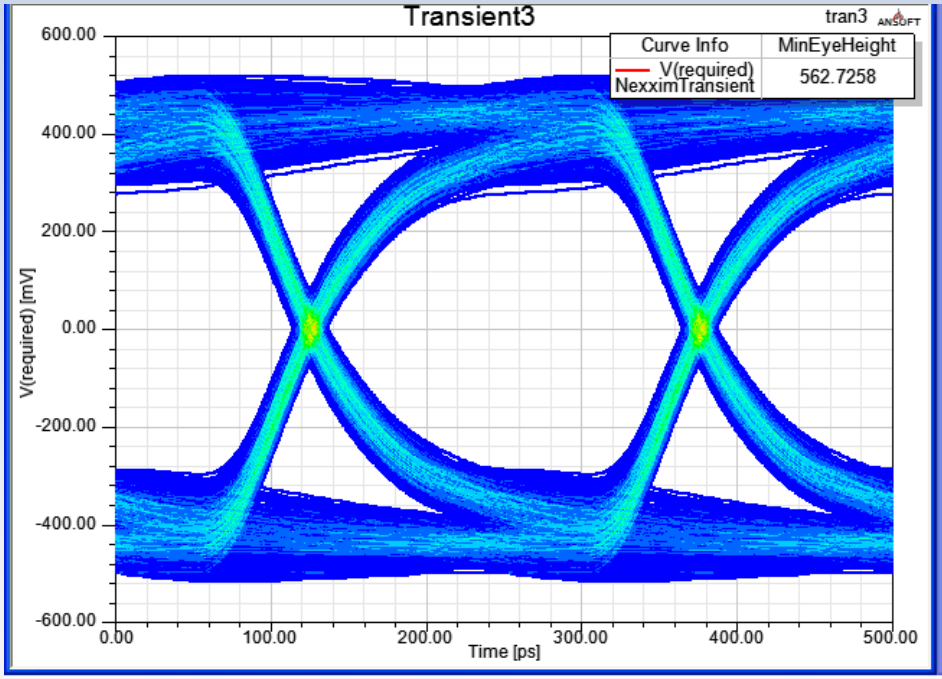


- **3 curves tested for driver impedance**

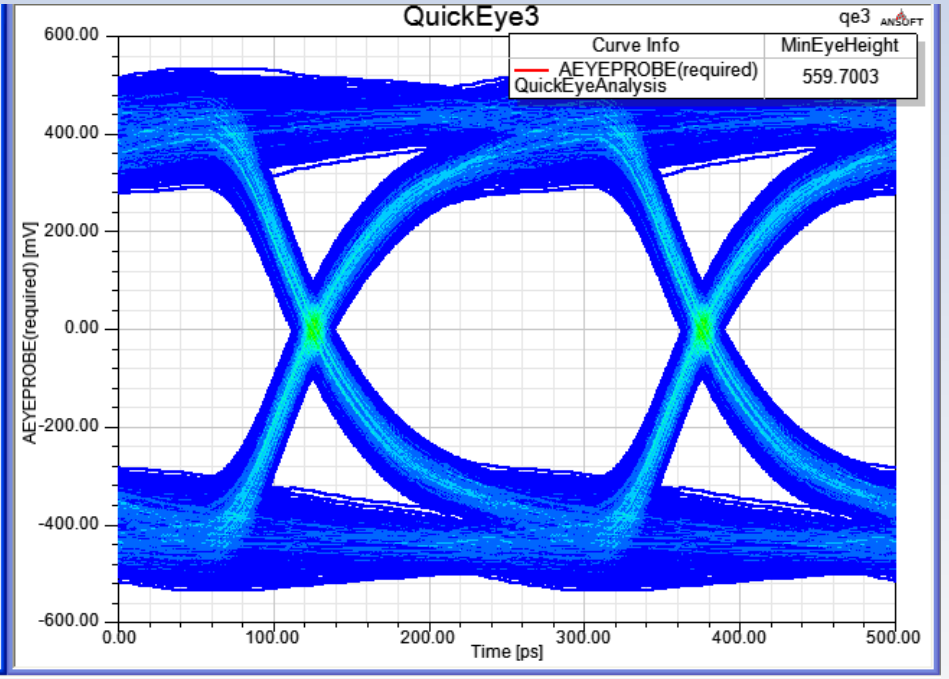


Transient vs. QuickEye: Larger Nonlinearity

Transient Eye Height = 563 mV



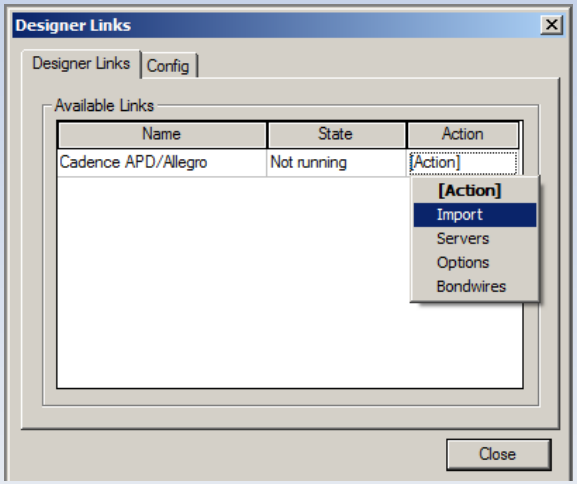
QuickEye Height = 560 mV



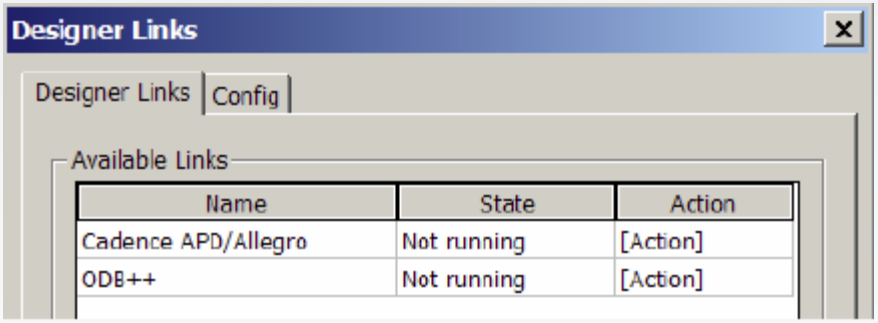
- **Test cases show that even though QuickEye and VerifEye make an assumption of linearity, accuracy is often excellent for moderately nonlinear drivers**

Ansoft Designer支持PCB数据直接导入

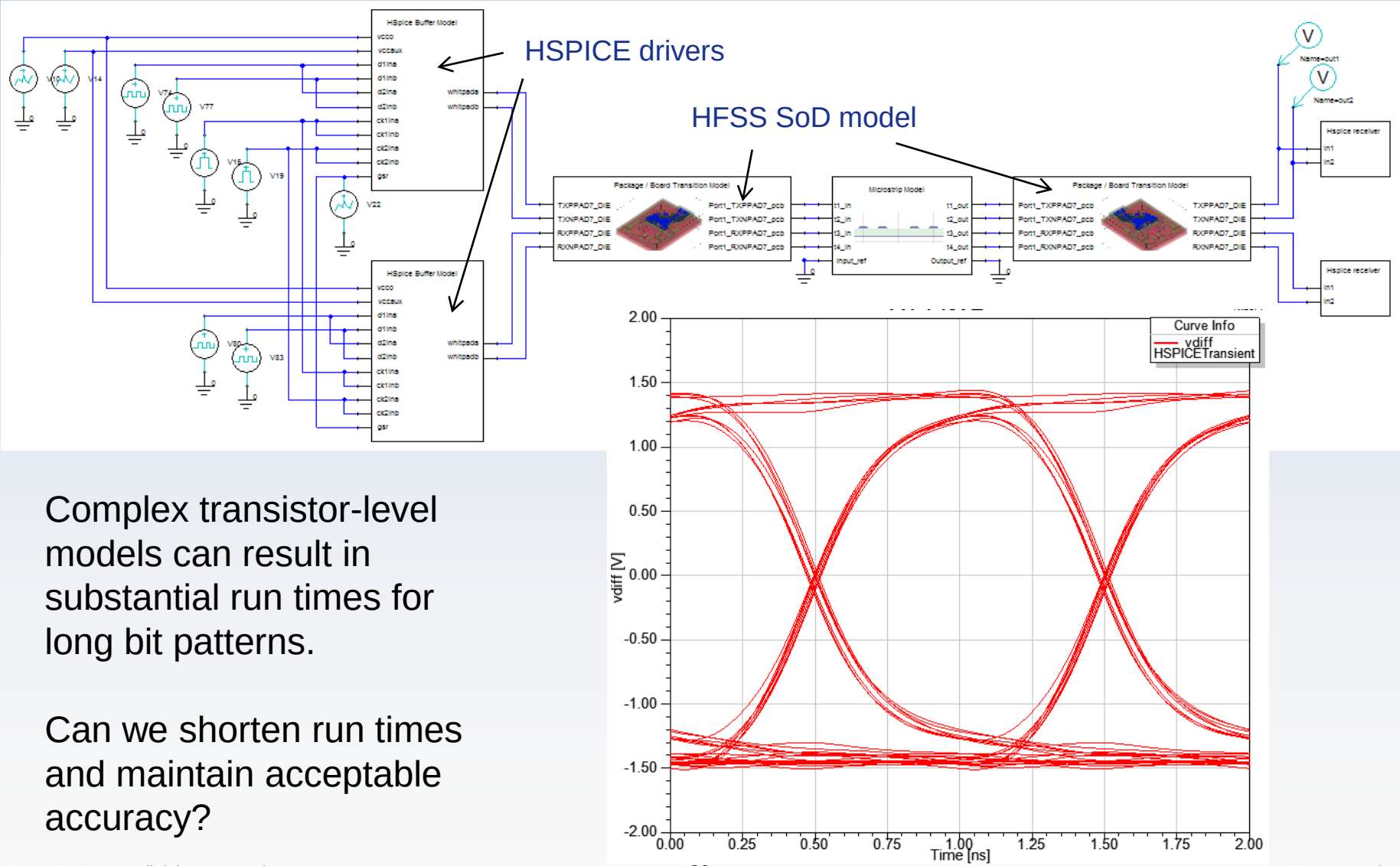
- **AnsoftLinks for Cadence APD, Allegro, SiP**
  - Direct MCM, BRD, SiP import
  - Run from either Cadence or Designer
    - Must have Cadence installed
  - Licensed thru AnsoftLinks option



- **AnsoftLinks for ODB++**
  - Common PCB Manufacturing format
    - Supported by Mentor, Zuken, Cadence, Altium



Ansoft Designer支持HSPICE加密模型



Complex transistor-level models can result in substantial run times for long bit patterns.

Can we shorten run times and maintain acceptable accuracy?

小结

- 虚拟样机仿真验证是现代电子设计的必然趋势
- 仿真与测试的验证是设计中的重要一环
- 现代的仿真与测试仪表可以协同辅助设计
- 充分的扫描和统计分析非常必要