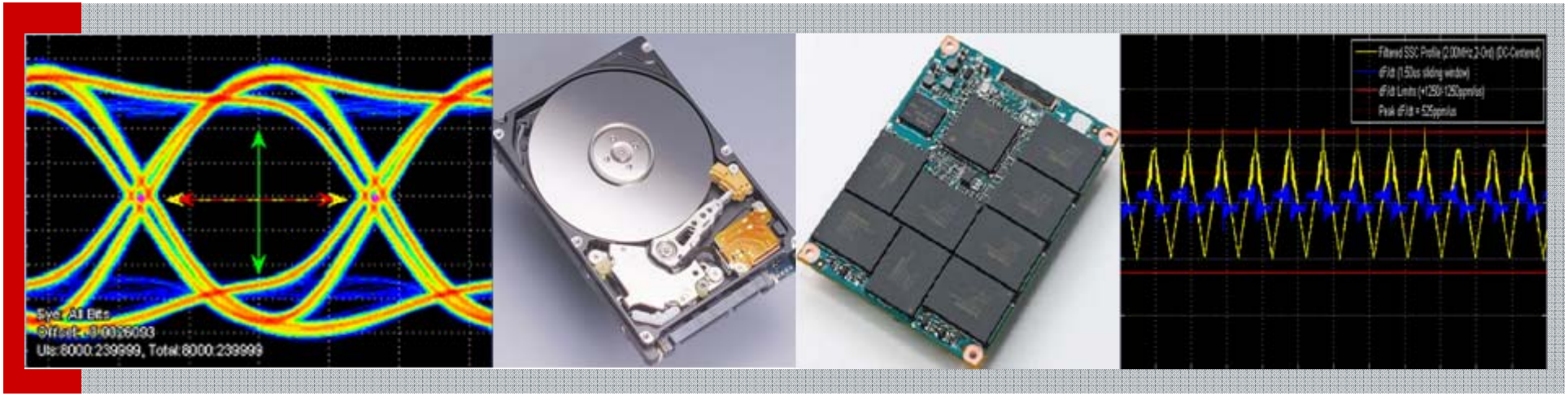
Physical Layer Validation of Storage Systems

- Advanced Tools for Validation, Debug and Characterization of SAS and SATA Designs

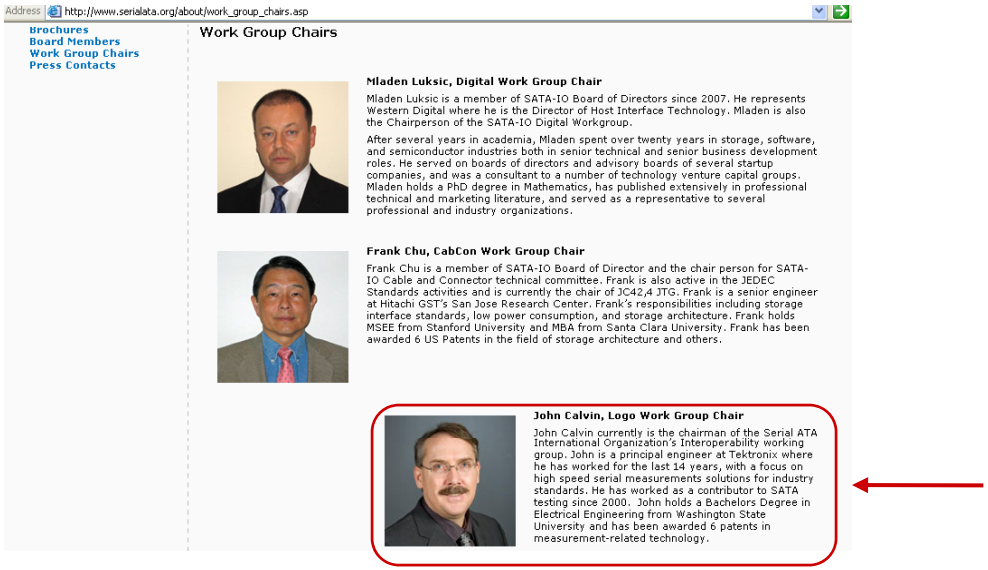


John Calvin
Tektronix Storage Portfolio Product Manager
Chairman of SATA-IO Logo and Interoperability Working group

Tektronix®

Presenter Biography

- **John Calvin, Logo Work Group Chair**
  - John Calvin currently is the chairman of the Serial ATA International Organization's Interoperability working group. John is a Product Manager at Tektronix where he has worked for the last 15 years, with a focus on high speed serial measurements solutions for industry standards. He has worked as a contributor to SATA testing since 2000. John holds a Bachelors Degree in Electrical Engineering from Washington State University and has been awarded 6 patents in measurement-related technology.
  - http://www.serialata.org/about/work_group_chairs.asp



Tektronix Innovation Forum

SATA Logo/Interoperability mission

- The Storage industry and SATA in particularly has shipped over **One Billion disk drives**. The cost sensitivity of the consumer market has made storage systems a commodity item. The lowest cost item usually emerges as the most attractive from a OEM/Supplier arrangment.
- The interchangeability of SATA storage demands a high degree of assured interoperability between devices at the principal electrical interfaces.
- **The SATA Logo/Interoperability organization's charter is to develop test techniques and methods which ensure this industries interoperability objectives are being met, for all SATA Certified products.**

Agenda

- Introduction
- SAS
  - Physical Layer Testing Overview
  - Measurements
  - Challenges in SSC
  - Test Reporting
- SATA
  - UTD 1.4 (6 Gb/s) Measurements
  - New Measurements
  - Receiver Testing
- Summary

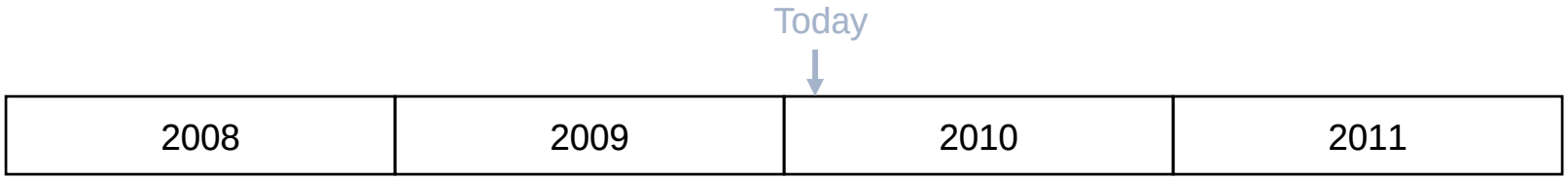
Technology Leader

Tektronix in Storage Standards

- Serial Advanced Technology Attachment (SATA)
  - Tektronix has the only comprehensive and fully automated SATA physical layer test automation package in the industry today, enabling the broad community of expert users, industrial automation and technical users since the beginning of SATA over a decade ago. .
  - Well established 20 Ghz scope performance has been utilized at industry interoperability events and test labs for 2 years and provides unparalleled trigger, capture and analysis capabilities.
  - In the field of Receiver testing, Tektronix has introduced the concept of full digital synthesis of waveform impairments as well as integrated methods of logical state control with high performance (24Gs/sec) Arbitrary Waveform Generators.

- Serial Attached SCSI (SAS)
  - Tektronix is currently recognized as one of the two valid tool providers for the UNH IOL SAS Consortium's Physical Layer test suite. These are the tests performed for SAS conformance at a recent Plugfest.
  - Best in class, proven real time instrumentation platform along with industry recognized 70GHz sampling scopes provides users flexibility and latitude with either advanced debug or higher bit rates.
  - The first and only tool provider to provide comprehensive Noise decomposition, as well as Jitter decomposition along BER contour calculations.

Storage Timelines and Solutions Development



- SATA Revision 3.0 (6Gb/s)

Draft Spec

Gen 3- Silicon Phase

Public Spec Release

Integration Phase

- Product Development
- SATA IO Unified Test Definition 1.4
- First official testing of Gen3 products in June 2009

Deployment Phase

- Commercial product deployment.

Gen ? (12Gb/Sec)

Possible Silicon Phase

- SAS Gen2 (6Gb/s)

Draft Spec

Gen 2- Silicon Phase

Public Spec Release

Integration Phase

- SCSI Trade Association Gen2 Plugfest (UNH IOL)
- STA test specification of SAS released.

Deployment Phase

- Commercial product deployment.

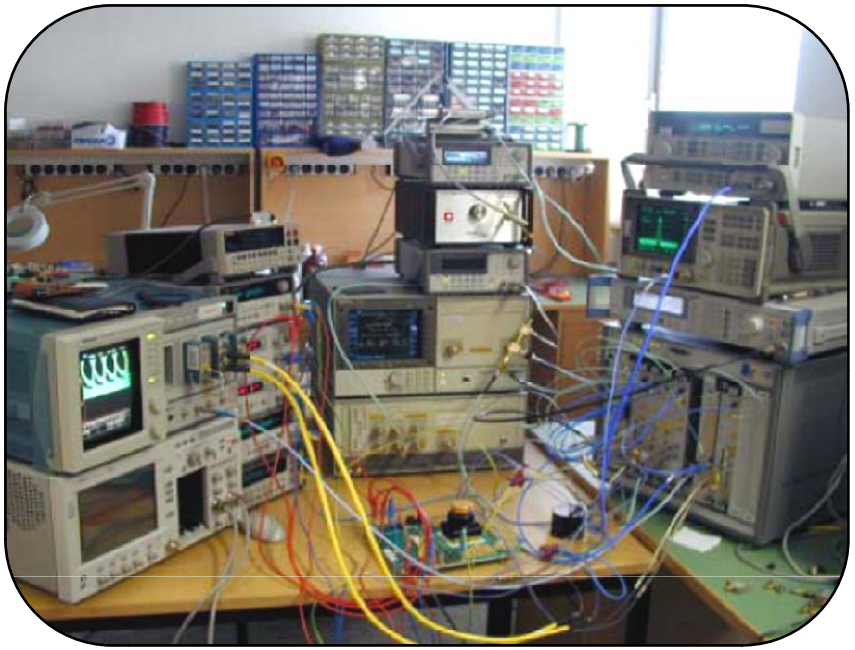
Gen 3 (12Gb/Sec)

- Silicon Phase

Compliance Testing – An ***Industry*** Productivity Issue

Greater speed means greater design challenges, with implications…

1. Greater test complexity
   - More instruments, configurations, and setup time
2. Breadth of tests demands highly experienced, ***senior equipment users*** to perform and interpret results.
3. Text complexity is high
   - Highly specialized – e.g., SSC modulation analysis, advanced receiver testing, Frequency domain S-Parameter measurements.
4. Days to perform effective, repeatable and reliable product validation tests



"Banner specs are no longer the gating issue. The latest equipment provides ample raw performance. What's needed is greater ease of use, setup and automation."

- Customer feedback

SAS Physical Layer Testing

Tektronix®

STA: PHY informative measurements

- SAS GROUP 1: COUPLING & OOB REQUIREMENTS
  - TEST 5.1.1 - AC COUPLING REQUIREMENTS
  - TEST 5.1.2 - TX MAXIMUM NOISE DURING OOB IDLE
  - TEST 5.1.3 - TX OOB BURST AMPLITUDE
  - TEST 5.1.4 - TX OOB OFFSET DELTA
  - TEST 5.1.5 - TX OOB COMMON MODE DELTA
- SAS GROUP 2: TX SPREAD SPECTRUM CLOCKING (SSC) REQUIREMENTS
  - TEST 5.2.1 - TX SSC MODULATION TYPE
  - TEST 5.2.2 - TX SSC MODULATION FREQUENCY
  - TEST 5.2.3 - TX SSC MODULATION DEVIATION AND BALANCE
  - TEST 5.2.4 - TX SSC DFDT (INFORMATIVE)
- GROUP 3: TX NRZ DATA SIGNALING REQUIREMENTS
  - TEST 5.3.1 - TX PHYSICAL LINK RATE LONG TERM STABILITY
  - TEST 5.3.2 - TX COMMON MODE RMS VOLTAGE LIMIT
  - TEST 5.3.3 - TX COMMON MODE SPECTRUM
  - TEST 5.3.4 - TX PEAK-TO-PEAK VOLTAGE
  - TEST 5.3.5 - TX VMA AND EQ (INFORMATIVE)
  - TEST 5.3.6 - TX RISE AND FALL TIMES
  - TEST 5.3.7 - TX RANDOM JITTER (RJ)
  - TEST 5.3.8 - TX TOTAL JITTER (TJ)
  - TEST 5.3.9 - TX WAVEFORM DISTORTION PENALTY (WDP)

The SAS consortium and the testing programs sponsored by the SCSI Trade Association (STA) perform these measurements on an informative basis.

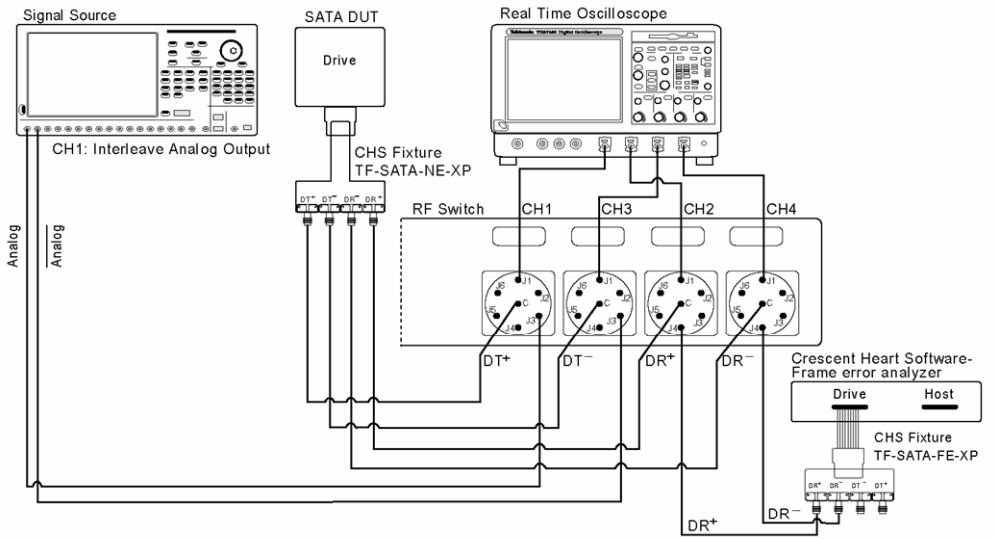
There are no sanctioned SAS compliance measurements.

GROUP 4: S-PARAMETER REQUIREMENTS

- TEST 5.4.1 - RX DIFFERENTIAL RETURN LOSS (SDD11)
- TEST 5.4.2 - RX COMMON-MODE RETURN LOSS (SCC11)
- TEST 5.4.3 - RX DIFFERENTIAL IMPEDANCE IMBALANCE (SCD11)
- TEST 5.4.4 - TX DIFFERENTIAL RETURN LOSS (SDD22)
- TEST 5.4.5 - TX COMMON-MODE RETURN LOSS (SCC22)
- TEST 5.4.6 - TX DIFFERENTIAL IMPEDANCE IMBALANCE (SCD22)

Integrated and Automated Test Control

TekExpress™ Test Automation Framework

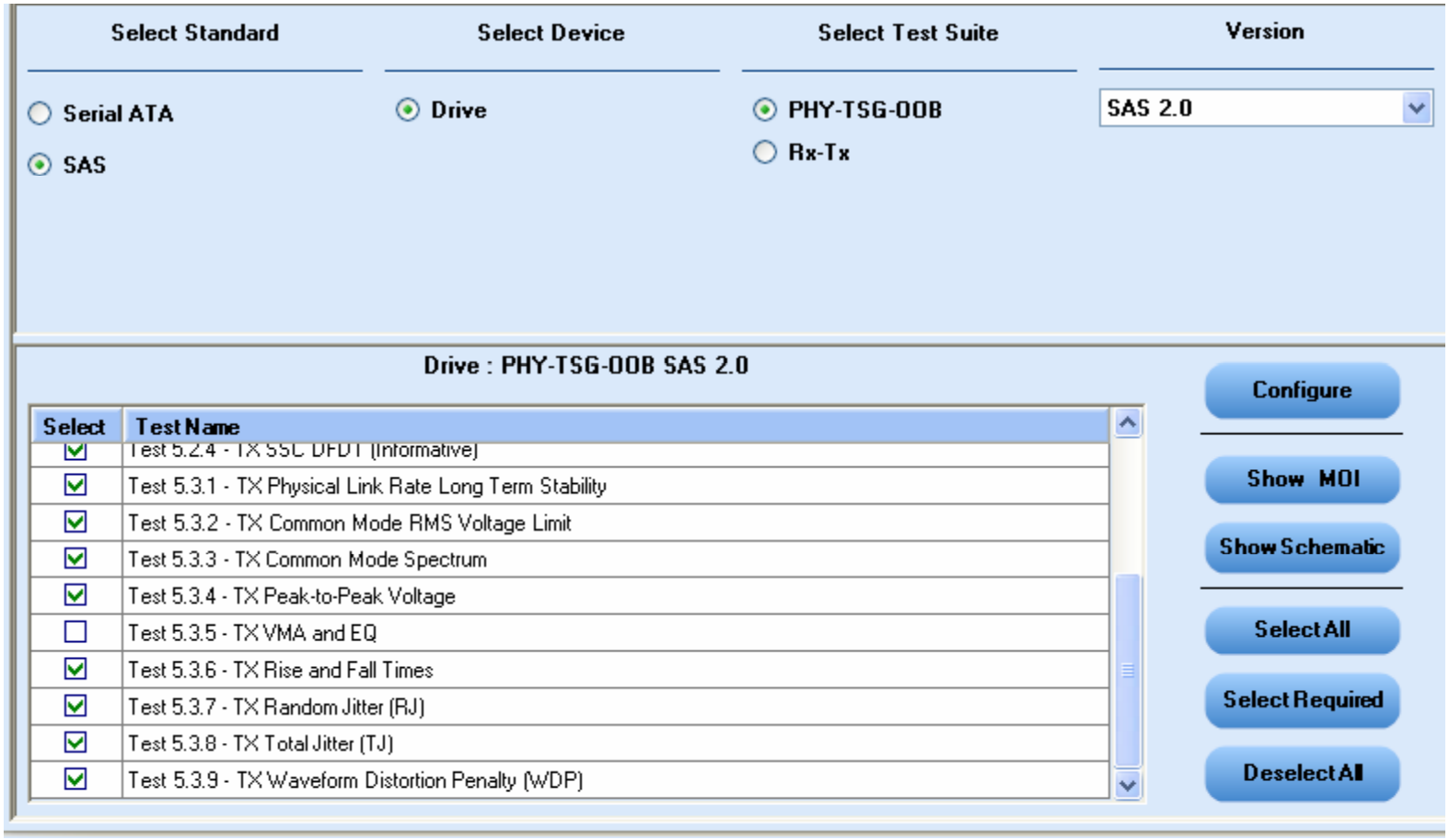


TekExpress Instrument Topology for TSG/PHY/OOB, RSG testing

- Arbitrary Waveform Generator (AWG)
  - DUT state control
  - Digitally synthesizes test signal impairments (Direct Synthesis)
- Complete offering includes:
  - Leading portfolio of Tektronix test instruments
    - Oscilloscopes
    - Signal generators
  - 3rd party integration with RF switch (Keithley), fixtures, API (NI), cabling, deskew, etc.
- Auto discovery of instruments using GPIB, USB, and LAN
  - 1GbE networking is used for data/waveform transport.
  - GPIB/488.2 is used for RF Switch and Power supply communications
- Test sequence automation
- One button control
- Reporting

- Simplifies Complex Measurements
- Improves Engineering Productivity
- Repeatable and Consistent results
- Automatic with no user intervention

TekExpress: SAS TSB/PHY/OOB



- Example SAS Report:
  - ftp://ftp.tektronix.com/outgoing/Sample_SAS_Report.mht

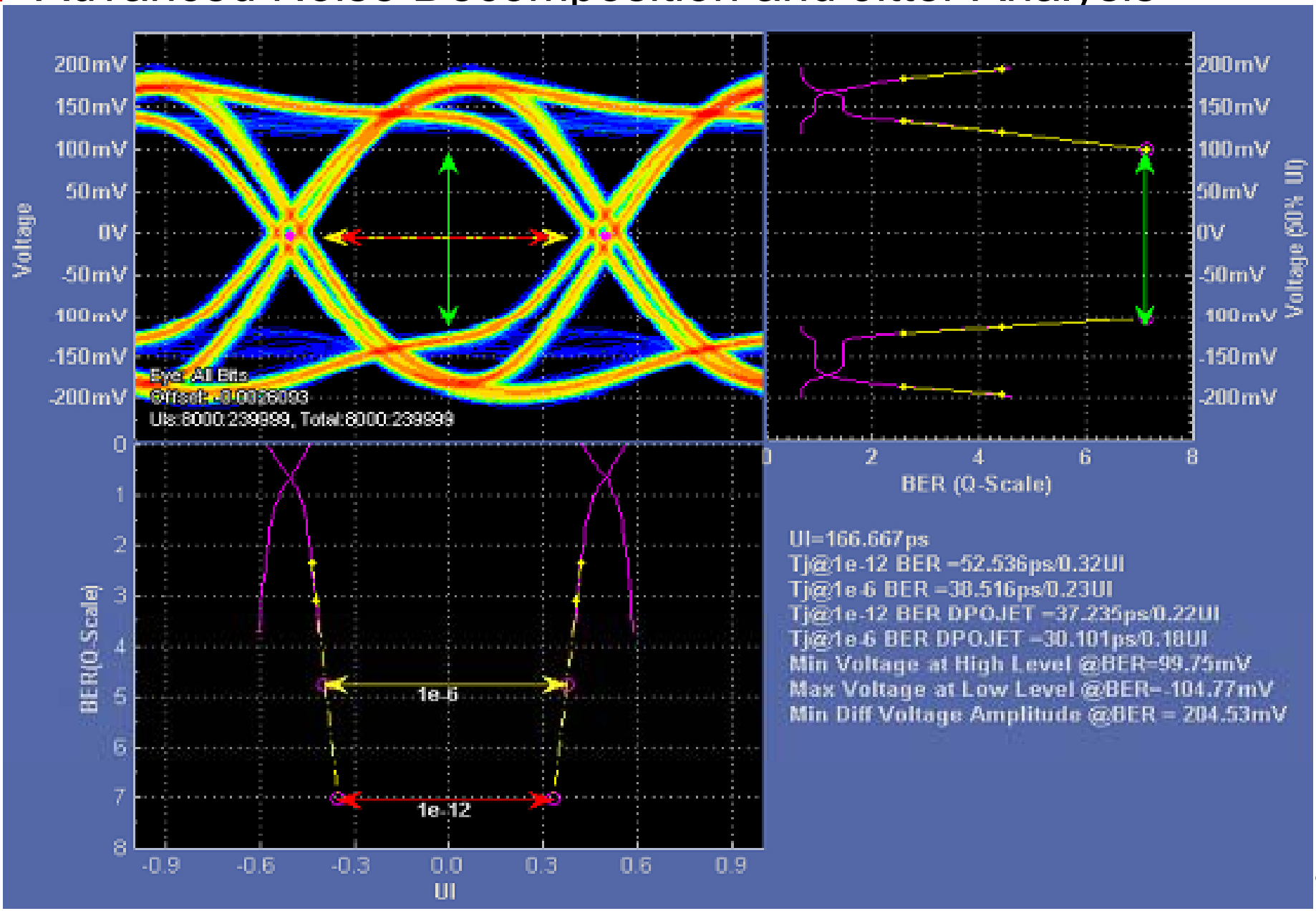
TekExpress: SAS TSB/PHY/OOB

Drive : PHY-TSG-OOB SAS 2.0 — Show Pass / Fail

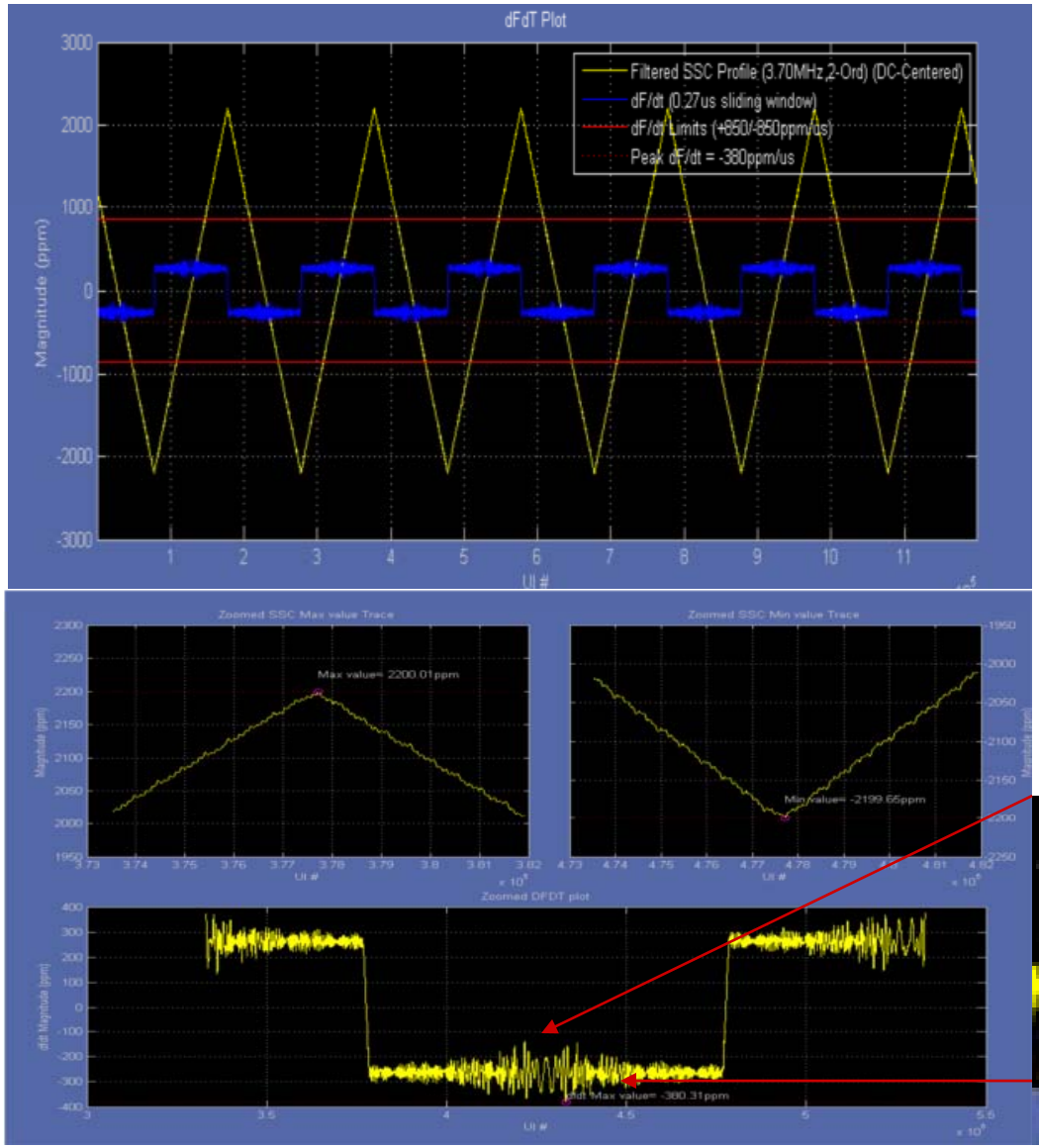
Test Name	Status	Low Limit	Measured Value	High Limit	Low limit margin, High limit margin	Pass/Fail Status
Test 5.1.2 - TX Maximum Noise Duri	Completed Test 5.1.2 - TX Maximum	120 mV	104	-NA-	16 - Passed	✓ Pass
Test 5.1.3 - TX OOB Burst Amplitude	Completed Test 5.1.3 - TX OOB Burs	2400 mV	Maximum peak-to-peak burst amplitu	-NA-	1796 - Passed	✓ Pass
		2400 mV	Minimum peak-to-peak burst amplitu	-NA-	2119.8 - Passed	
		240 mV	Minimum peak-to-peak burst amplitu	-NA-	364 - Passed	
		240 mV	Minimum peak-to-peak burst amplitu	-NA-	40.2 - Passed	
Test 5.1.4 - TX OOB Offset Delta	Completed Test 5.1.4 - TX OOB Offs	25 mV	-3.09832	-NA-	28.0983 - Passed	✓ Pass
Test 5.1.5 - TX OOB Common Mode	Completed Test 5.1.5 - TX OOB Com	50 mV	-3.47364	-NA-	53.4736 - Passed	✓ Pass
Test 5.2.1 - TX SSC Modulation Type	Completed Test 5.2.1 - TX SSC Mod	-	Down-spread SATA	-	-	✓ Pass
Test 5.2.2 - TX SSC Modulation Freq	Completed Test 5.2.2 - TX SSC Mod	30 KHz	Modulation frequency: 30	33 KHz	0 , 3 - Failed	✗ Fail
			Min Modulation frequency: 29.9976		Informative	
			Max Modulation frequency: 30.0017		Informative	
Test 5.2.3 - TX SSC Modulation Devi	Completed Test 5.2.3 - TX SSC Mod	-5000 ppm	Max deviation: -2200.53	0 ppm	Informative	✗ Fail
		-5000 ppm	Min deviation: -0.4482	0 ppm	Informative	
Test 5.2.4 - TX SSC DFDT (Informati	Completed Test 5.2.4 - TX SSC DFD	-5350 ppm/us	-327.7502	350 ppm/us	5022.2498, 677.7502 - Passed	✓ Pass

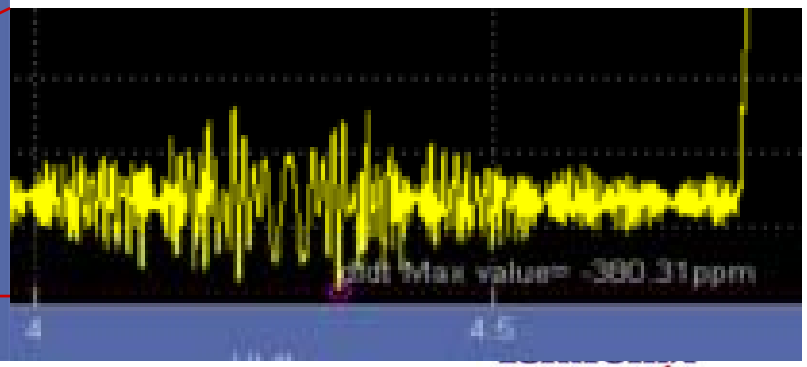
- Test Results are detailed in the analysis panel, showing measurement results, user or standard specified test limits and high and low margin values.
- The Pass/Fail criteria defaults to the SAS Standards limits, however users can relax or make them more stringent if needed.

Advanced Noise Decomposition and Jitter Analysis



SAS/SATA SSC Analysis





- Advanced tools required to provide detailed insights into SSC modulation problems and to automatically identify and zoom in on problem areas

- In this example, the regions of maximum and minimum modulation as well as the dF/dT absolute maximum are magnified and presented for scrutiny

SAS: Comprehensive Report: 29 fully automated tests

Test Name	Test Details			Low Limit	Measured Value	High Limit	Margin	Units	Test Result
	Pattern Name	Interface Speed	Measurement Details						
Test 5.2.1-TX SSC Modulation Type	HFTP	6.0Gb/s	Center-spread SAS	-NA-	SSC ON	-NA-	-NA-	-NA-	Pass
Test 5.2.2-TX SSC Modulation Frequency	HFTP	6.0Gb/s	SSC Modulation Frequency	>= 30	30.0000	<= 33	0 , 3	KHz	Pass
	HFTP	6.0Gb/s	Min SSC Modulation Frequency	>= 30	29.9992	<= 33	Informative		Informative
	HFTP	6.0Gb/s	Max SSC Modulation Frequency	>= 30	30.0011	<= 33	Informative		Informative
Test 5.2.3-TX SSC Modulation Deviation and Balance	HFTP	6.0Gb/s	Max Deviation	-NA-	-2199.6500	-NA-	-NA-	ppm	Informative
	HFTP	6.0Gb/s	Min Deviation	-NA-	2200.0074	-NA-	-NA-		Informative
	HFTP	6.0Gb/s	Avg Deviation	>= -350	0.1787	<= 350	350.1787, 349.8213		Pass
	HFTP	6.0Gb/s	Deviation asymmetry	-	0.3574	<= 288	287.6426		Pass
Test 5.2.4-TX SSC DFDT (Informative)	HFTP	6.0Gb/s	df/dt	>= -850	-380.3082	<= 850	Informative	ppm/us	Informative
Test 5.3.1-TX Physical Link Rate Long Term Stability	HFTP	6.0Gb/s	Mean Period	> -100	-2.1050	< 100	Informative	ppm	Informative
	HFTP	6.0Gb/s	Min Period	> -100	2200.0074	< 100	Informative		Informative
	HFTP	6.0Gb/s	Max Period	> -100	-2199.6501	< 100	Informative		Informative
Test 5.3.2-TX Common Mode RMS Voltage Limit	CJTPat-Gen 2	6.0Gb/s	Common-mode RMS voltage at IT (mV)-SAS 2.0	-	42.9927	< 30	12.9927	mV	Fail
Test 5.3.3-TX Common Mode Spectrum	CJTPat-Gen 2	6.0Gb/s	Common-mode spectrum (dBmV) at 100MHz-SAS 2.0	-	-33.5589	< 12.7	46.2589	mV	Pass
	CJTPat-Gen 2	6.0Gb/s	Common-mode spectrum (dBmV) at first harmonic-SAS 2.0	-	16.7701	< 26	9.2299		Pass
	CJTPat-Gen 2	6.0Gb/s	Common-mode spectrum (dBmV) at second harmonic-SAS 2.0	-	-9.8586	< 30	39.8586		Pass
Test 5.3.4-TX Peak-to-Peak Voltage	D30.3-Gen 2	6.0Gb/s	Peak to Peak voltage (mVppd)-SAS 2.0	> 850	1240.0000	< 1200	390 , 40	mV	Fail
Test 5.3.5-TX VMA and EQ	D30.3-Gen 2	6.0Gb/s	Transmitter equalization (dB)-SAS 2.0	> 2	2.0684	< 4	Informative	dB	Pass
Test 5.3.6-TX Rise and Fall Times	D10.2	6.0 Gb/s	Rise time in ps	>= 41.6	55.7616	-	14.1616	ps	Pass
	D10.2	6.0 Gb/s	Fall time in ps	>= 41.6	55.3999	-	13.7999		Pass
Test 5.3.7-TX Random Jitter (RJ)	D24.3-Gen 2	6.0Gb/s	Rj before CIC	-	0.7069	<= 25	24.2931	ps	Pass
	D24.3-Gen 2	6.0Gb/s	Rj after CIC	-	0.5321	<= 25	24.4679		Pass

SATA Physical Layer Testing

Tektronix®

It's the measurements ..

SATA UTD 1.4 Test Requirements

Phy Transmit Signal Requirements
TSG-01 : Differential Output Voltage
TSG-02 : Rise/Fall Time
TSG-03 : Differential Skew
TSG-04 : AC Common Mode Voltage
TSG-05 : Rise/Fall Imbalance
TSG-06 : Amplitude Imbalance
TSG-07 : Gen1 (1.5Gb/s) TJ at Connector, Clock to Data, fBAUD/10
TSG-08: Gen1 (1.5Gb/s) DJ at Connector, Clock to Data, fBAUD/10
TSG-09 : Gen1 (1.5Gb/s) TJ at Connector, Clock to Data, fBAUD/500
TSG-10 : Gen1 (1.5Gb/s) DJ at Connector, Clock to Data, fBAUD/500
TSG-11 : Gen2 (3Gb/s) TJ at Connector, Clock to Data, fBAUD/500
TSG-12 : Gen2 (3Gb/s) DJ at Connector, Clock to Data, fBAUD/500
TSG-13: Gen3 (6Gb/s) Transmit Jitter w/wo CIC
TSG-14 : Gen3 (6Gb/s)TX Maximum Differential Voltage Amplitude
TSG-15 : Gen3 (6Gb/s) TX Minimum Differential Voltage Amplitude
TSG-16 : Gen3 (6Gb/s) Tx AC Common Mode Voltage

Phy Receive Signal Requirement
RSG-01 : Gen1 (1.5Gb/s) Receiver Jitter Tolerance Test (Normative)
RSG-02 : Gen2 (3Gb/s) Receiver Jitter Tolerance Test (Normative)
RSG-03 : Gen3 (6Gb/s) Receiver Jitter Tolerance Test
RSG-05 : Gen1 Asynchronous Receiver Stress Test at +350ppm
RSG-06 : Gen1 Asynchronous Receiver Stress Test With SSC

SI General Requirements
SI-1:8 : Cable Characterization
SI-09 : Inter-Symbol Interference

Phy General Requirements
PHY-01 : Unit Interval
PHY-02 : Frequency Long Term Stability
PHY-03 : Spread-Spectrum Modulation Frequency
PHY-04 : Spread-Spectrum Modulation Deviation

Phy OOB Requirements
OOB-01 : OOB Signal Detection Threshold
OOB-02 : UI During OOB Signaling
OOB-03 : COMINIT/RESET and COMWAKE Transmit Burst Length
OOB-04 : COMINIT/RESET Transmit Gap Length
OOB-05 : COMWAKE Transmit Gap Length

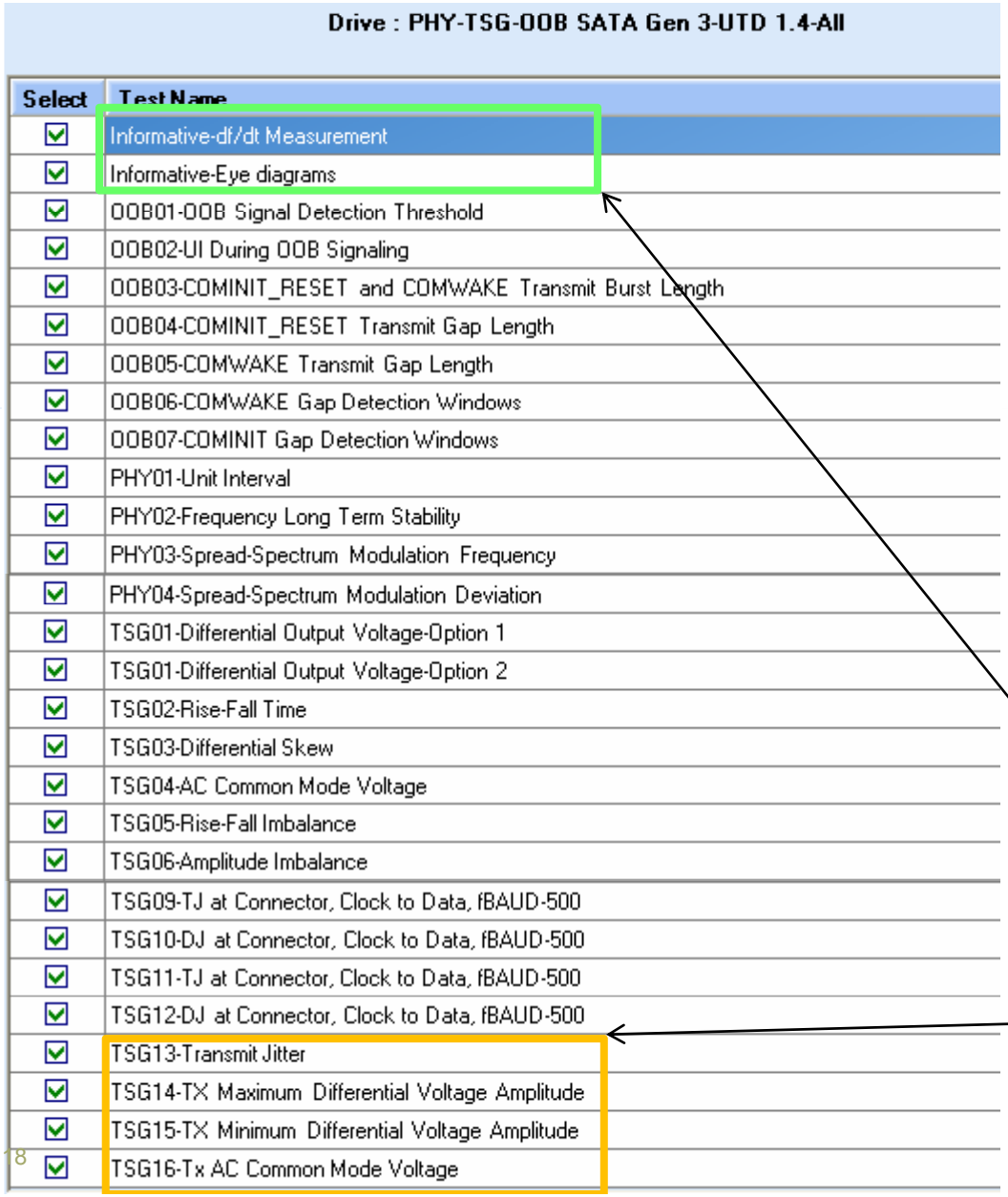
Phy Receiver/Transmitter Channel Reqs
RX/TX-01 : Pair Differential Impedance
RX/TX-02 : Single-Ended Impedance (Obsolete)
RX/TX-03 : Gen2 (3Gb/s) Differential Mode Return Loss
RX/TX-04 : Gen2 (3Gb/s) Common Mode Return Loss
RX/TX-05 : Gen2 (3Gb/s) Impedance Balance
RX/TX-06 : Gen1 (1.5Gb/s) Differential Mode Return Loss
RX/TX-07 : Gen3 (6Gb/s) Differential Mode Return Loss
RX/TX-08 : Gen3 (6Gb/s) Impedance Balance

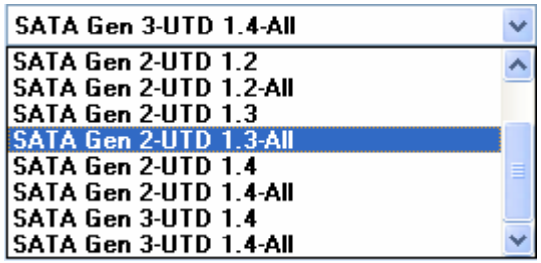
SATA Measurement Legends:

- No change from previous UTD 1.3 spec version
- Revised methodology from UTD1.3 to UTD 1.4
- New test definitions in UTD 1.4
- Obsolete

Full SATA Logo Test Specification available at..
http://www.serialata.org/documents/Interop_UnifiedTest_Rev1_4_v1_00_083109.pdf

SATA UTD 1.4 TSG/PHY/OOB Measurements

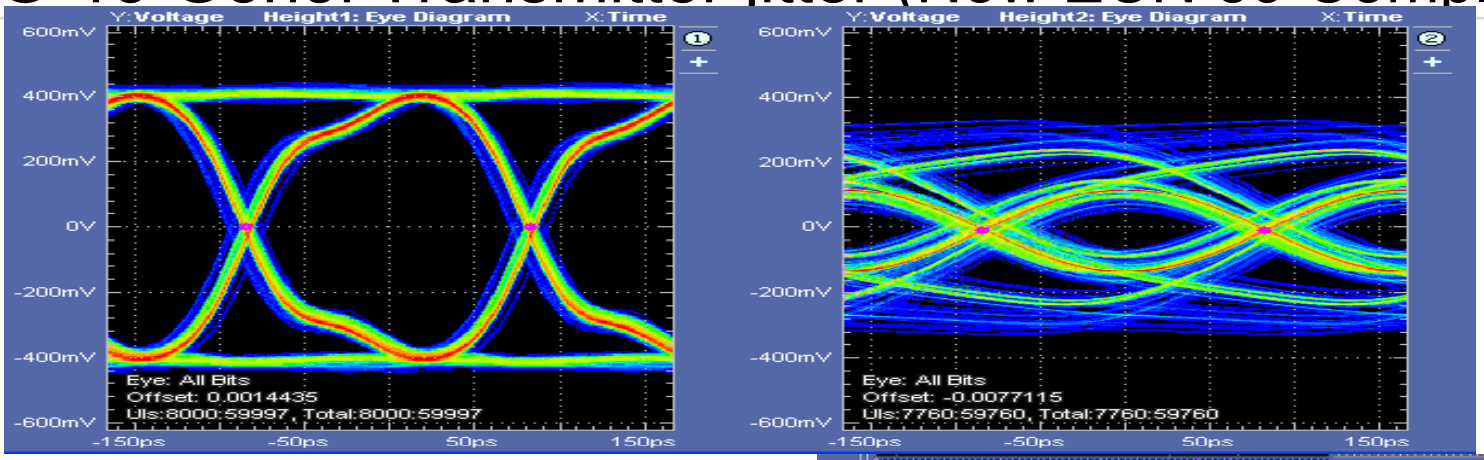


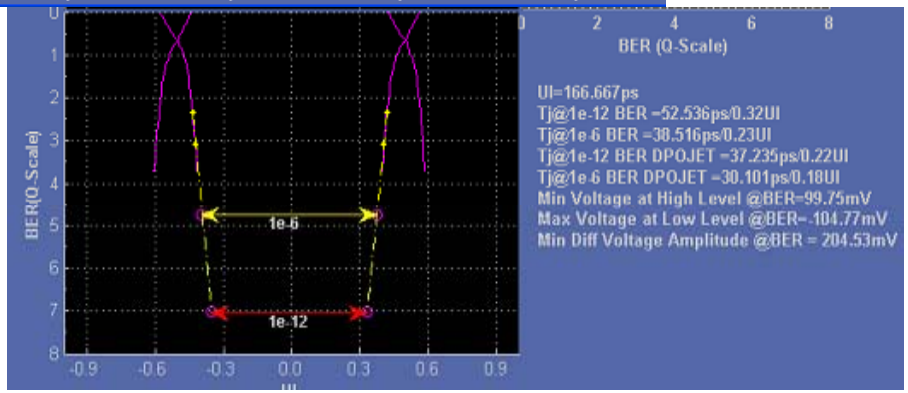


- Different Test program and degrees of regression testing now user selectable. UTD 1.2 and 1.3 tests use JIT3 and run on TDS and DPO class instruments. UTD 1.4 tests (Gen3) only operate on DPOJET.
- Debug and Diagnostic tools (Informative measurements)
- New SATA Gen3 measurements

New Measurements

TSG-13 Gen3i Transmitter jitter (Now ECN 39 Compliant)





The following scope set-ups are used in this test.

- RJ for 6Gb/s: SATA_TSG13_RJ_G3.set
- TJ for 6Gb/s: SATA_TSG13_TJ_G3.set
- TJ with CIC for 6Gb/s: SATA_TSG13_TJ_Flt_G3.set

Test pattern(s):	**SATA usage model:**
MFTP, LBP, HFTP, LFTP	6.0 Gbps

SATA 6Gbps: 10 us/div, 20 ps/pt (>100,000 UI).
Horizontal resolution will vary depending on the data rate and oscilloscope model

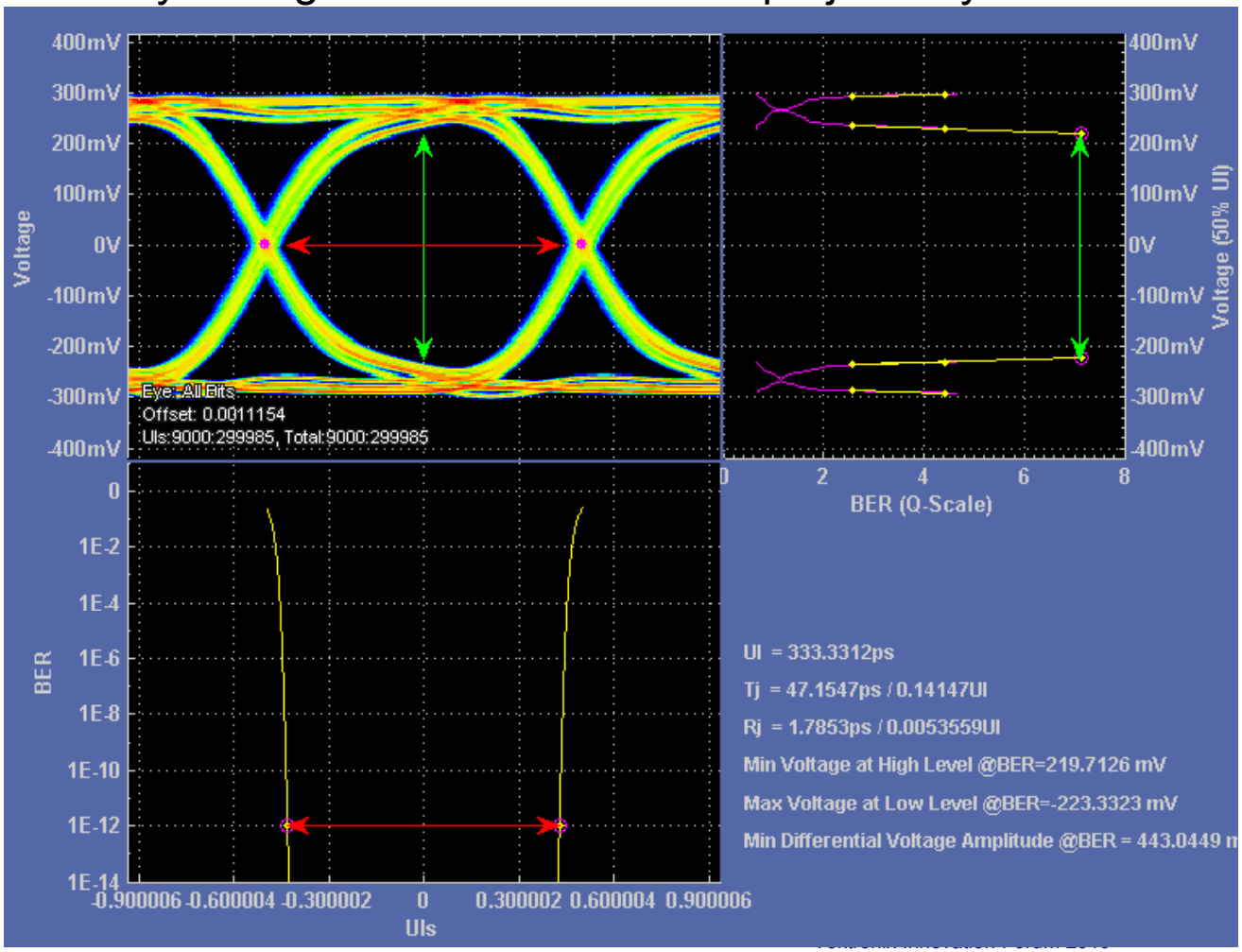
Observable Results:

- RJ measured (RJmeas) at a maximum of 0.18 UI into a Laboratory Load before the Compliance Interconnect Channel (CIC) when measured using the specified JTF for products running at 6.0 Gb/s
- TJ measured at a maximum of (RJmeas) + 0.34 UI into a Laboratory Load before the CIC when measured using the specified JTF (for products running at 6.0 Gb/s)

New Measurements

TSG-15 Tx Minimum Differential Amplitude @ BER.

- One of the most significant advancements in SATA PHY testing for Gen3 is the new minimum amplitude technique
- Analyzes signal noise content and projects eye closure down to 10E-12 BER.

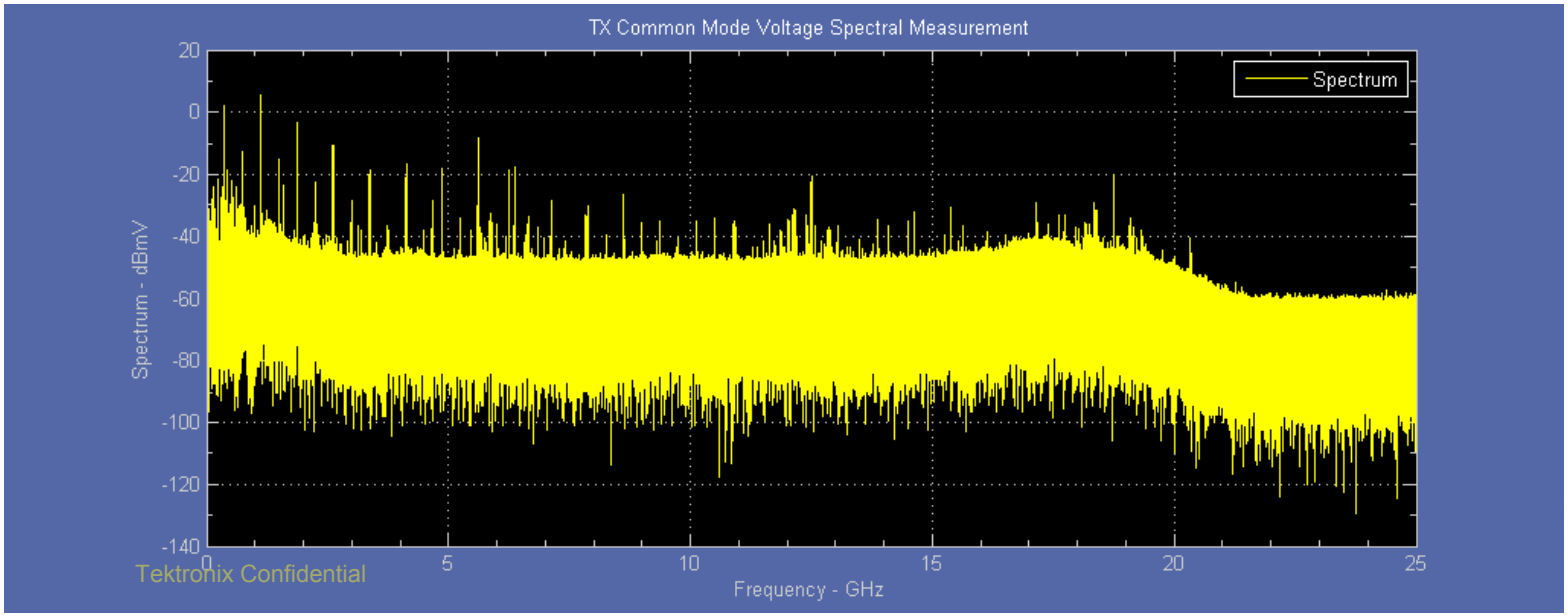


Goal of this measurement is the horizontal bathtub curve . This is similar to the WDP measurement in SAS

New Measurements

TSG-16 Tx AC Common Mode Signal Analysis

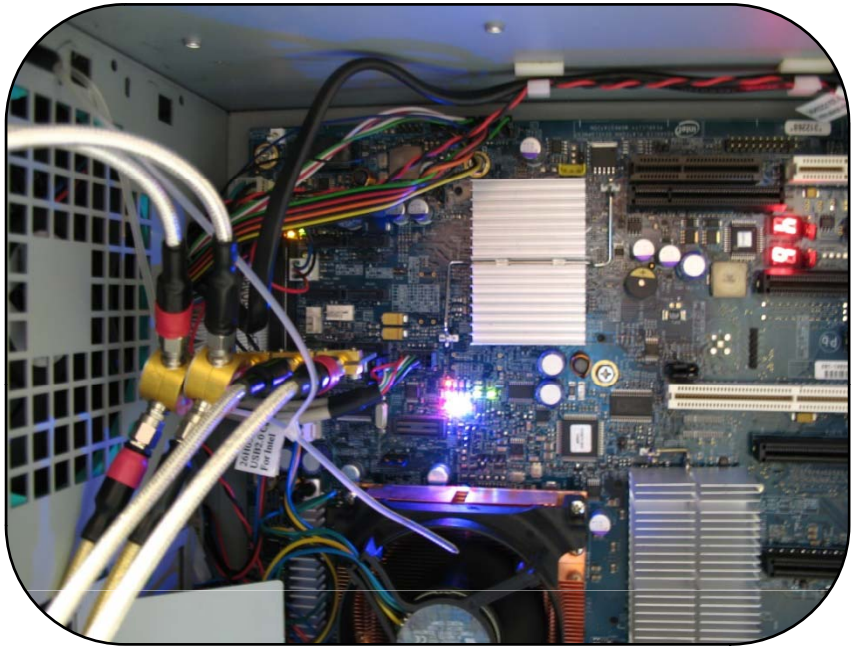
- 1st/2nd harmonics provide insight into common mode and time domain waveform asymmetry problems which results in EMI problems.
- Real-time waveform capture is absolutely vital if SSC is present. The constant movement of the spectral peaks and the determination of a nominal period cannot be performed on any other system.
- Spectral peaks are constantly moving
- Continuous multi-cycle analysis



Tektronix Innovation Forum

SATA: Receiver Signaling Tests

- The jitter composition for receiver testing is a precise mix of Random, Sinusoidal and Pattern Jitter.
- Additionally, the signal amplitude is lowered to the spec limit, and under these conditions a receiver is required to operate for 10, 5, and 2.5 minutes error free (for Gen1, 2, and 3 resp.)
- Sinusoidal (Sj) jitter frequencies
  - 5, 10, 33, 62 and recently piloted125MHz
- Why these frequencies?
  - High 62 and 33 MHz noise levels inside PC's known to create PLL peaking phenomenon at 5 and 10MHz, 125MHz is a high noise spectral location in PC architectures.
- SATA specifications require the error detection be made at a frame level



RSG/RMT testing with TekExpress

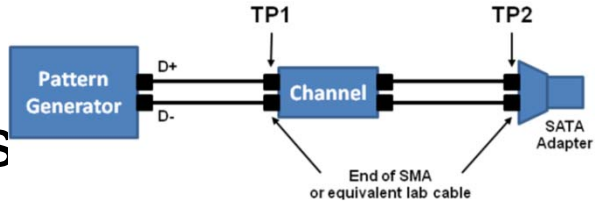
7.4.1.2 Frame Error Rate Measurements

The Frame Error Rate (FER) shall be measured and computed to be no greater than $8.200*10^{-8}$ at a 95% confidence level when tested with any given 8b/10b pattern, including the Frame Error Rate reference patterns cited in section 7.4.1.1. The Serial ATA CRC error detection mechanism is used to measure FER.

The Frame Error Rate is calculated based on the maximum size of a Data FIS, plus overhead for the FIS header and CRC Dwords. The Frame Error Rate assumes a target bit error rate of 10^{-12}.

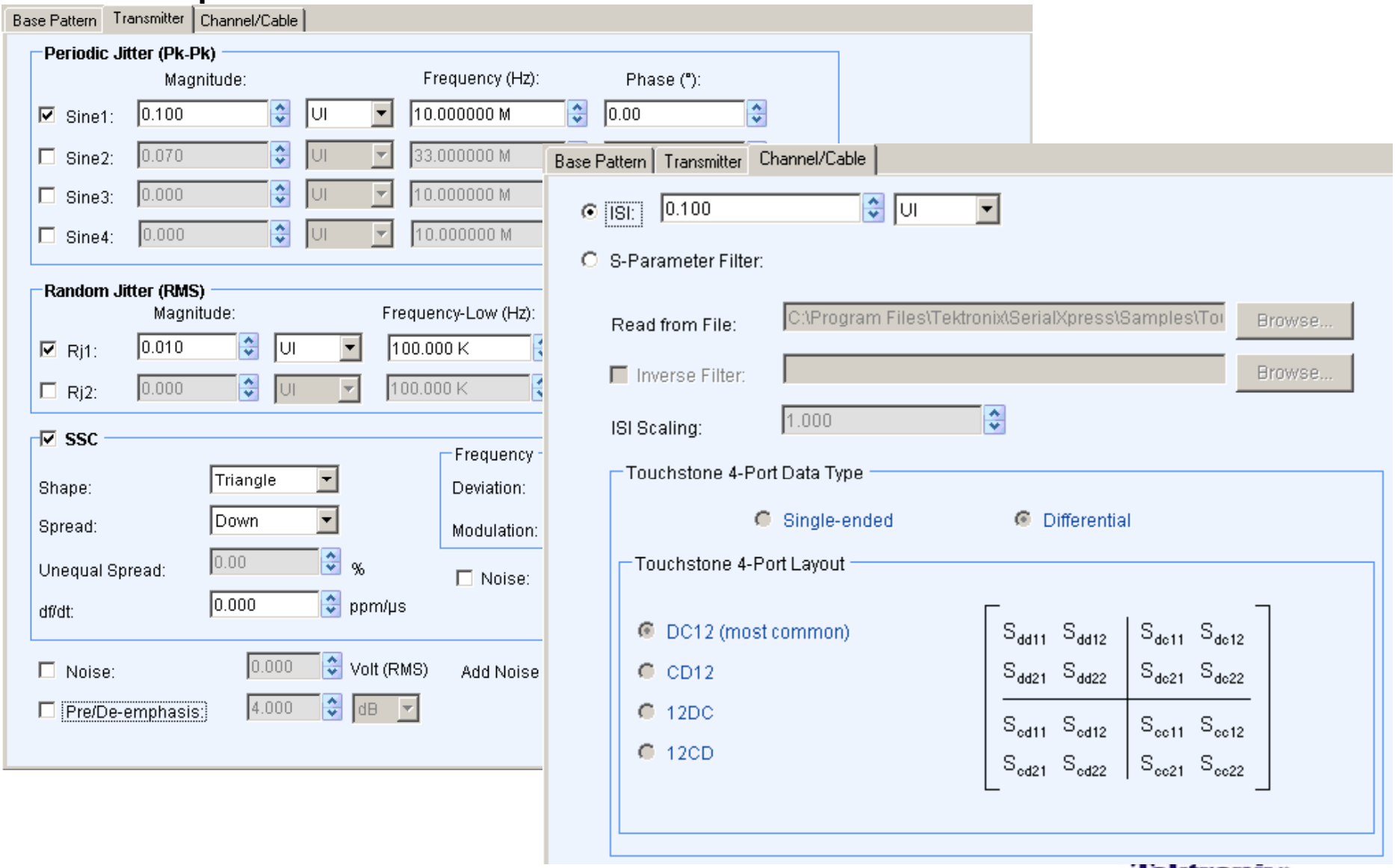
$$FER = (8192+8) \times 10 \times 10^{-12} = 8.200 \times 10^{-8}$$

SATA Receiver Test Jitter Specifications

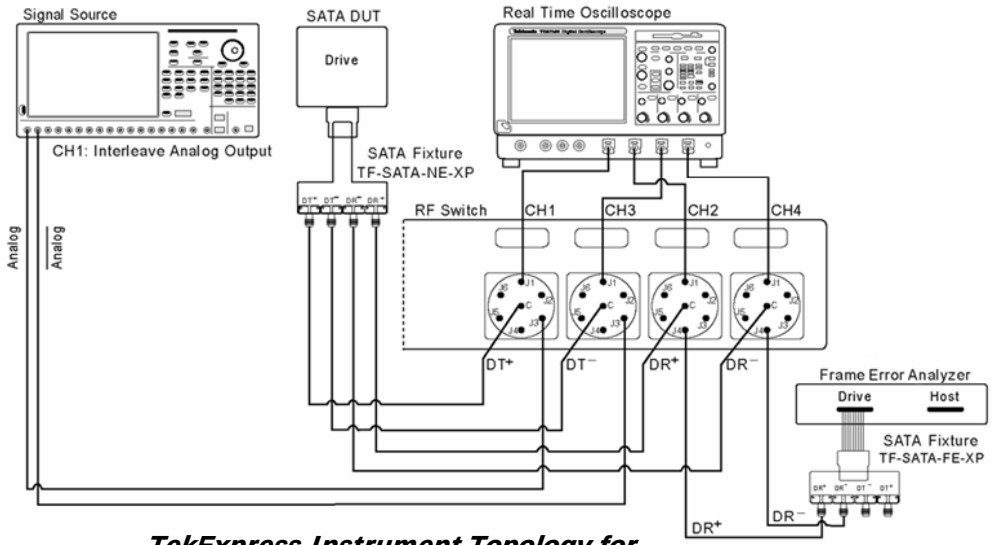


Step	Test Point	Calibration Pattern	Method	Gen1i	Gen1m	Gen2i	Gen2m	Gen3
Rise/ Fall Time	TP1	LFTP	Section 7.4.4 in SATA 3.0 Specification	100 ps (20/80%)		100 ps (20/80%)		62 ps to 75 ps (20/80%)
Rj	TP1	MFTP	Section 7.4.12 of SATA 3.0 Specification, Rj method also applied to Gen1i/m and Gen2i/m	8.57 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)		4.285 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)		2.14 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)
Sj	TP1	MFTP	Using Rj method defined in section 7.4.12 of SATA 3.0 Specification for all data rates	Sj=270mUI		Sj=270mUI		Sj=192mUI
Tj	TP2	Framed COMP with 2 Aligns and new LBP section	See UTD section 2.17.1.1	Tj(min)=501mUI Tj(max)=519mUI Using a channel that introduces 40 ps ± 6ps (i.e. min 34ps and max 46ps) of ISI in the given setup		Tj(min)=552mUI Tj(max)=588mUI Using a channel that introduces 40 ps ± 6ps (i.e. min 34ps and max 46ps) of ISI in the given setup		Tj(min)=498mUI Tj(max)=570 mUI Using a CIC that introduces a min 21ps and max 33ps of ISI in the given setup and that follows the definition in section 7.2.7 of SATA 3.0 Specification
Amplitude	TP2	Framed COMP with 2 Aligns and new LBP section	For this test the amplitude distribution will be either measured or projected to a 1E-12 BER contour at the 50% location of the bit interval using previously calibrated edge rates and jitter. It is required to ensure that the maximum allowed voltage is not exceeded. Sections 7.4.3 and 7.4.12 of SATA 3.0 Specification	325 mV	240 mV	275 mV	240 mV	240 mV

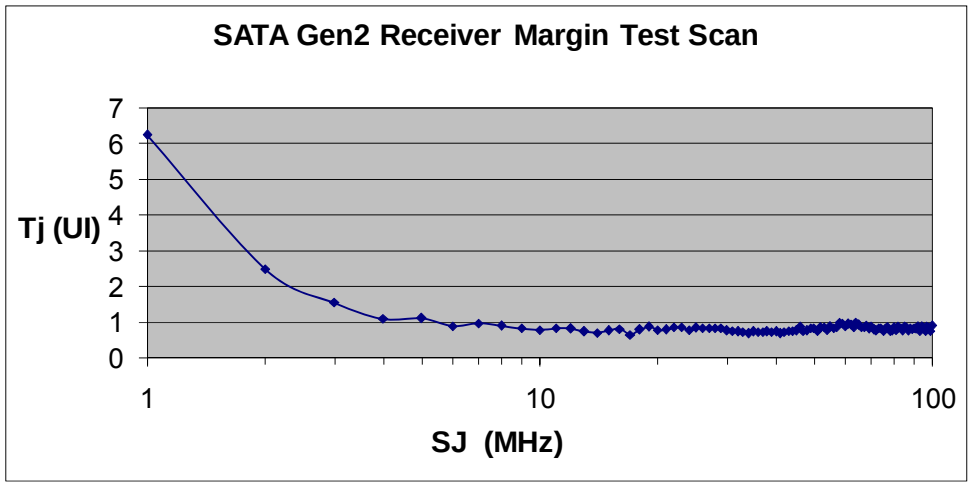
SerialXpress™ for Serial ATA Pattern Generation



Serial ATA Revision 3.0 Receiver Testing



TekExpress Instrument Topology for TSG/PHY/OOB, RSG testing

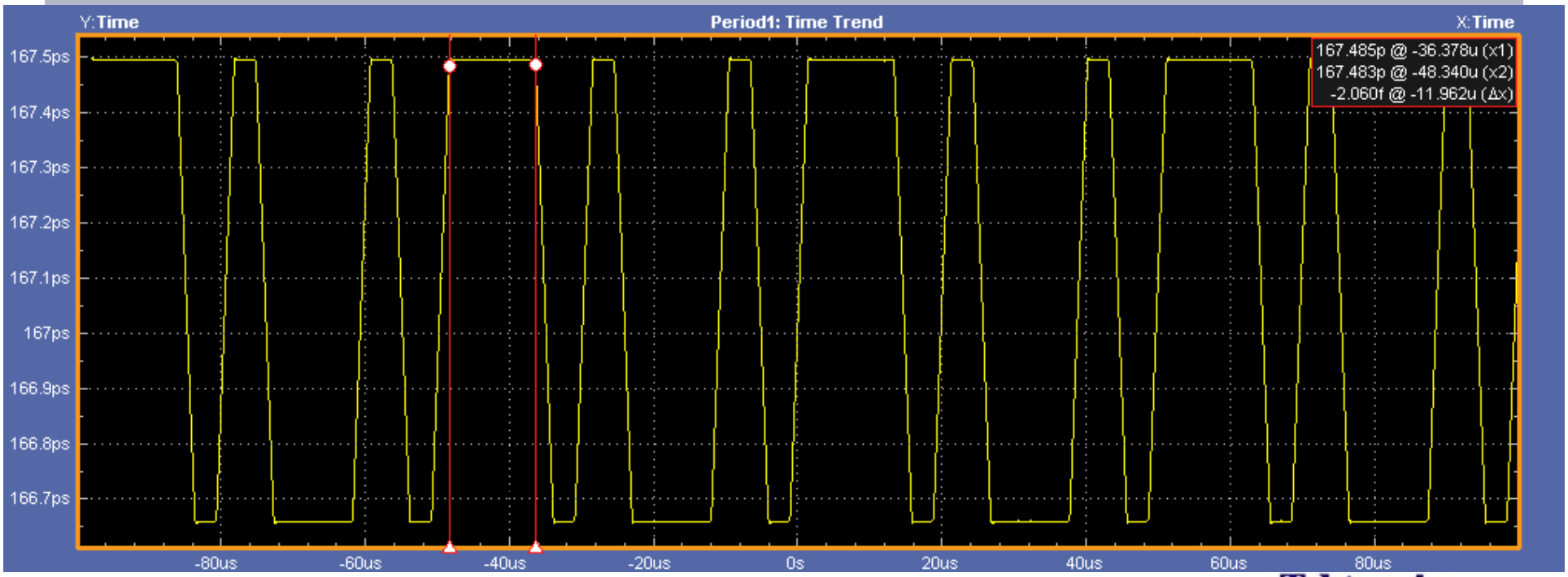


- Leading portfolio of Tektronix test instruments
  - Oscilloscopes with advanced jitter and link analysis software
  - Signal generators with stressed pattern generation software
- Tektronix Arbitrary Waveform Generator (6 Gb/s AWG)
  - Integrated DUT state control for disconnect-free solution
  - Digital Synthesis of CIC receiver ISI components with variable control.
  - Simplified SSC generation of complex dF/dT impairments or other modulation modeling needs
  - High Sinusoidal Jitter generation ability (0-100+UI, from ***DC to Nyquist***!)
- PHY Receive Signal Requirements
  - **RSG-01:** Gen1(1.5 Gb/s) Receiver Jitter Tolerance Test (Normative)
  - **RSG-02:** Gen2(3.0 Gb/s) Receiver Jitter Tolerance Test (Normative)
  - **RSG-03:** Gen3(6.0 Gb/s) Receiver Jitter Tolerance Test (Informative)
  - **RSG-05:** Asynchronous Receiver Stress Test at +350 ppm (Informative)

TekExpress Serial ATA Revision 3 Solution

Serial ATA Logo test futures

- dFdT (Phase modulation slew rate) has been approved in SATA through TP-03 for Tx testing. A reciprocal test for the Receiver is currently being piloted at the SATA IW#8 event in April 2010.
- The Tektronix AWG with it's digital waveform synthesis capability is leading the field of advanced modulation analysis. These tests expand the scope of conventional Receiver testing, while providing many insights into capabilities of the Phy's tracking architectures and how well it's is tuned for operating in a system environment where SSC noise and modulation issues can be significant.



TekExpress Serial ATA Revision 3 Solution

Complete Tektronix SATA/SAS Portfolio

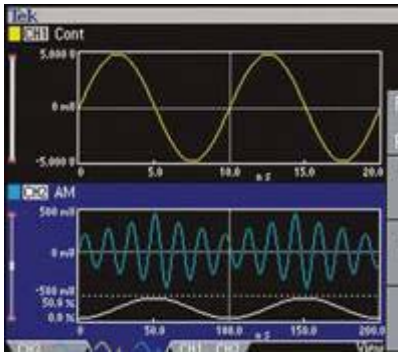
TekExpress Software	Comprehensive System level Gen1-3 Instrument Automation	
RSG/RMT Tests RSG/RMT- Receiver jitter and amplitude sensitivity compliance and margin test.	**AWG7122B with Opt.1, 6 and 8** SerialXpress Digital Signal Generation	
Rx/Tx Channel Tests ▪Rx/Tx - Device and Host electrical channel performance, Impedance and return loss	**DSA8200** 80E08 TDR Sampling Module for DSA8200 Sampling Scope S-Parameter Analysis Software 80SICON Software for DSA8200	
SI Cable Tests ▪SI - Cable crosstalk, skew and frequency domain measurements, sdd21, sdd11.	**DSA8200** 80E08 TDR Sampling Module for DSA8200 Sampling Scope	
PHY, TSG, and OOB Tests ▪PHY – Signal timing stability and SSC analysis. ▪TSG – Transmitter AC parametric, Jitter, Amplitude. ▪OOB- Out Of Band signal validation	**DSA72004B** DPOJET Jitter Analysis software SMA Adapters TCA-SMA 2 per scope Differential SMA Probe P7313SMA (optional)	

Resources

- What equipment do I need to test SATA and SAS?
  - ***SATA:***
    www.tek.com/applications/serial_data/sata/sata_tests.html
  - ***SAS:***
    www.tek.com/applications/serial_data/sas/recommended_equipment.html
- How can I learn more about SATA/SAS testing?
  - ***Tektronix SATA Knowledge Center:***
    www.tektronix.com/SATA
  - ***Tektronix SAS Knowledge Center:***
    www.tektronix.com/SAS
  - ***SATA International Organization:***
    www.serialata.org
  - ***SCSI Trade Association:***
    www.scsita.org
  - ***T10 Technical Committee:***
    www.t10.org
  - ***University of New Hampshire Interoperability Lab:***
    www.iol.unh.edu/services/testing/sas

Tektronix Innovation Forum

Enabling Innovation in the Digital Age



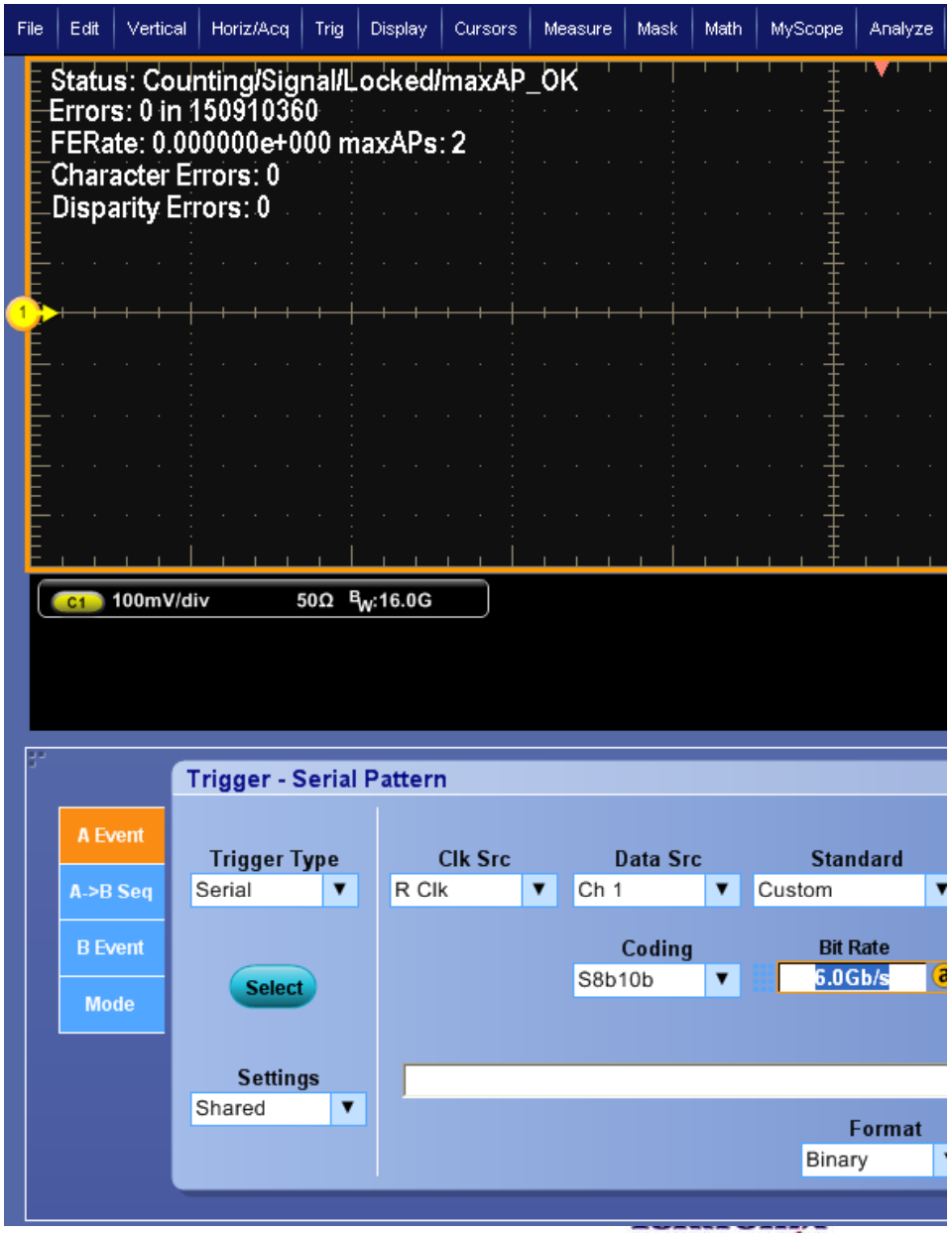
Accelerating Performance

Enabled by High-speed Serial Technologies

Tektronix

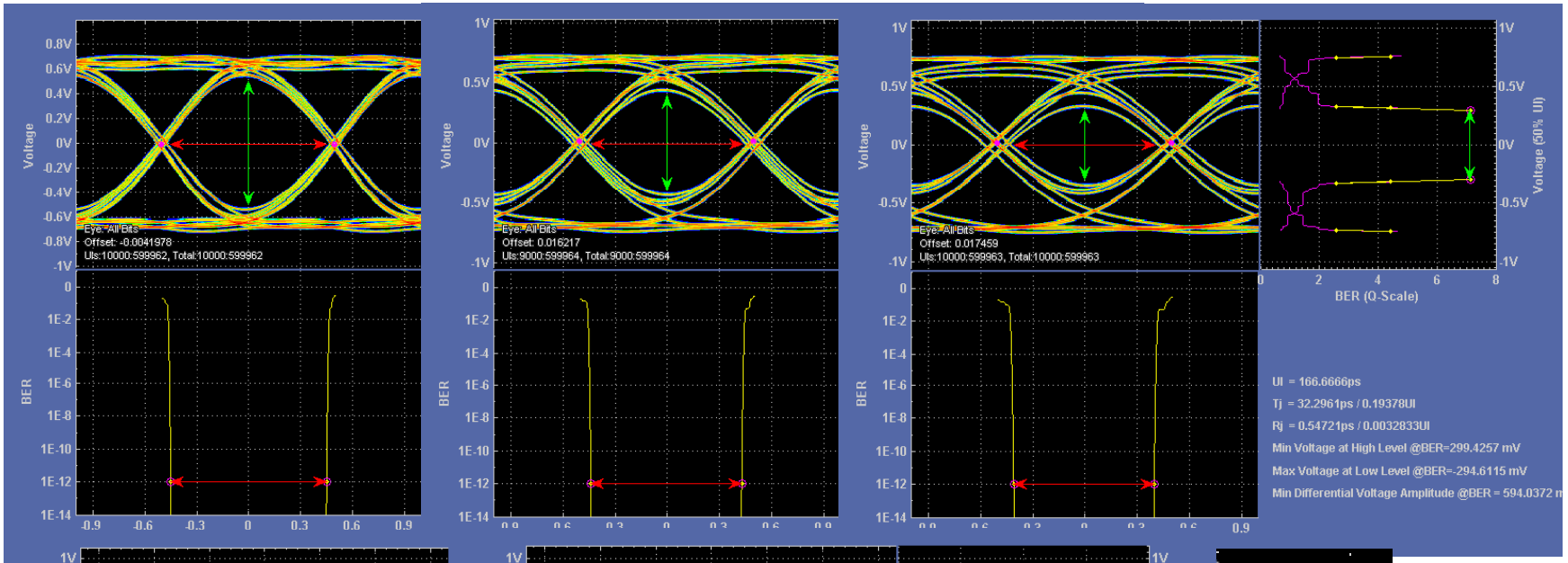
Integrated Instrument BERT

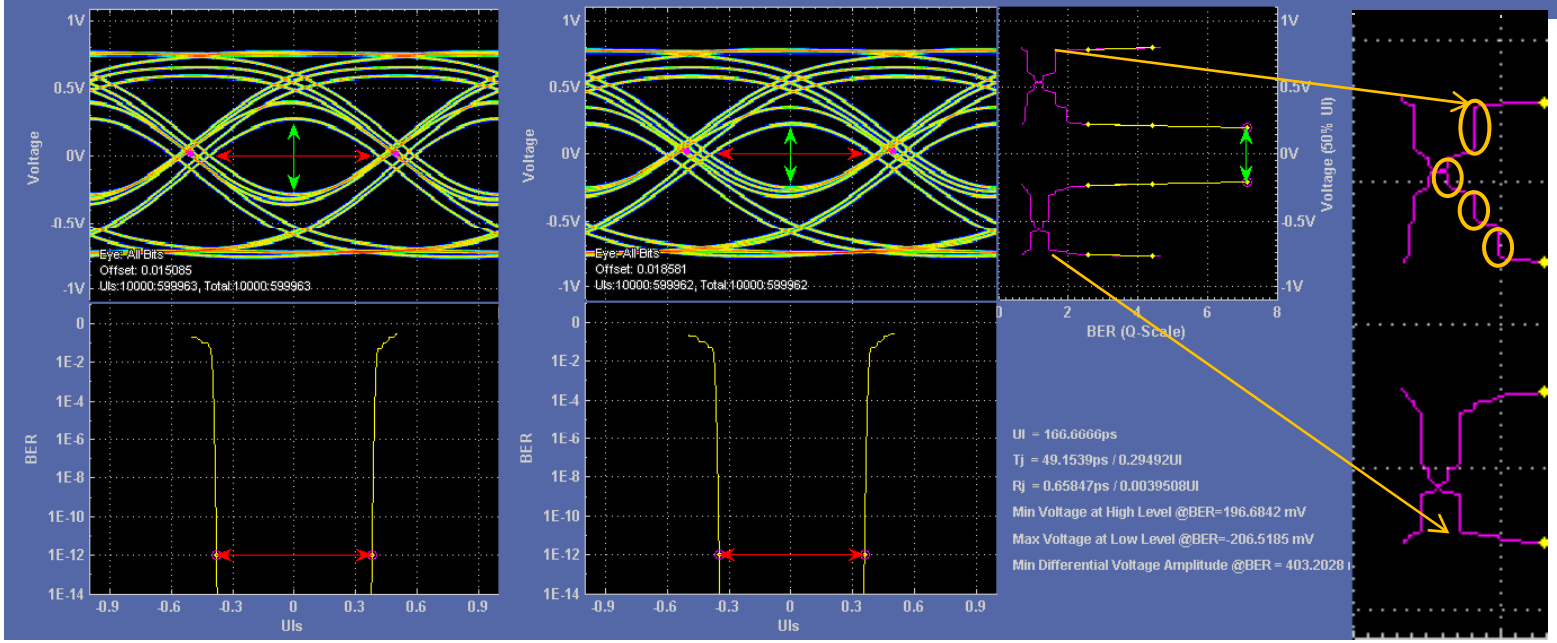
- Tektronix DPO/DSA/MSO 72004B/71604B/71254B Oscilloscopes offer a variable rate Frame Error and Bit Error Detector integated into the base instrument trigger system which can operate from 1.5G to 6.25G. This is an instrument setup used in conjunction with the High Speed Serial Trigger (STU) option.
- Released to SATA-IO in Tek RSG MOI on January 15, 2010. Certified by SATA-IO on April 8 2010.



Eye Waveform Synthesis Fidelity

Progressive Impairment of a SATA Gen3 (6Gb/s) Lone Bit Pattern





LBP Pattern:
1101000010
0011011011

- **4 Consecutive 1**
- **11011**
- **2 Consecutive 1**
- **Lone +1 bit**

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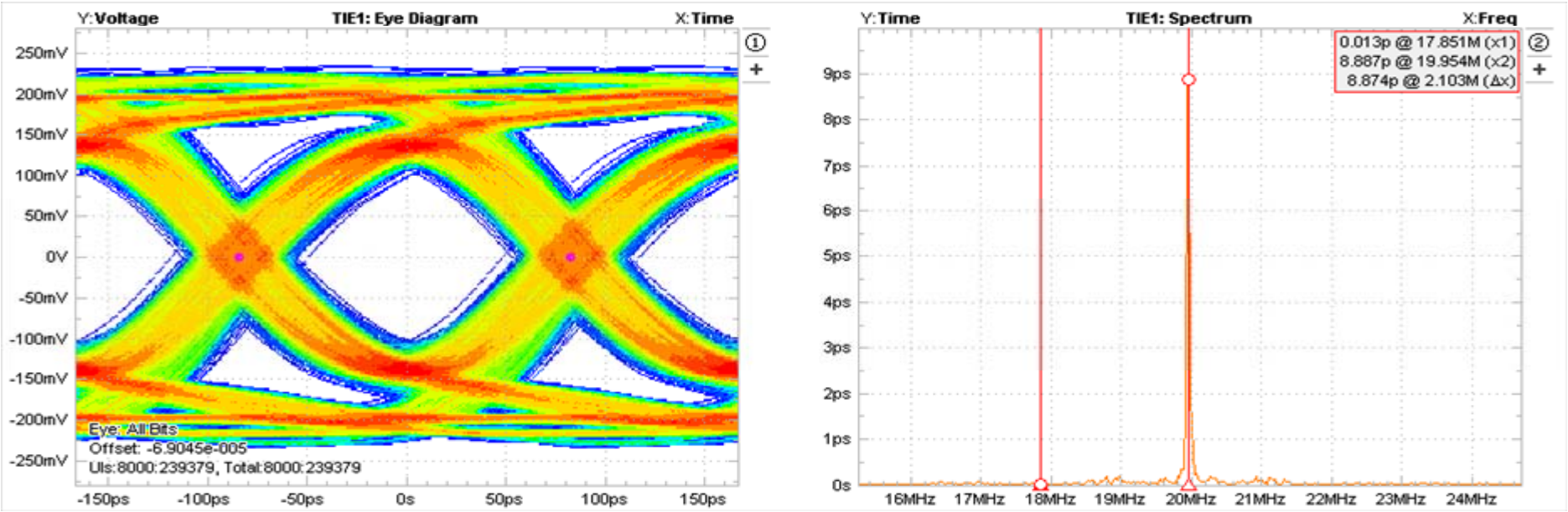
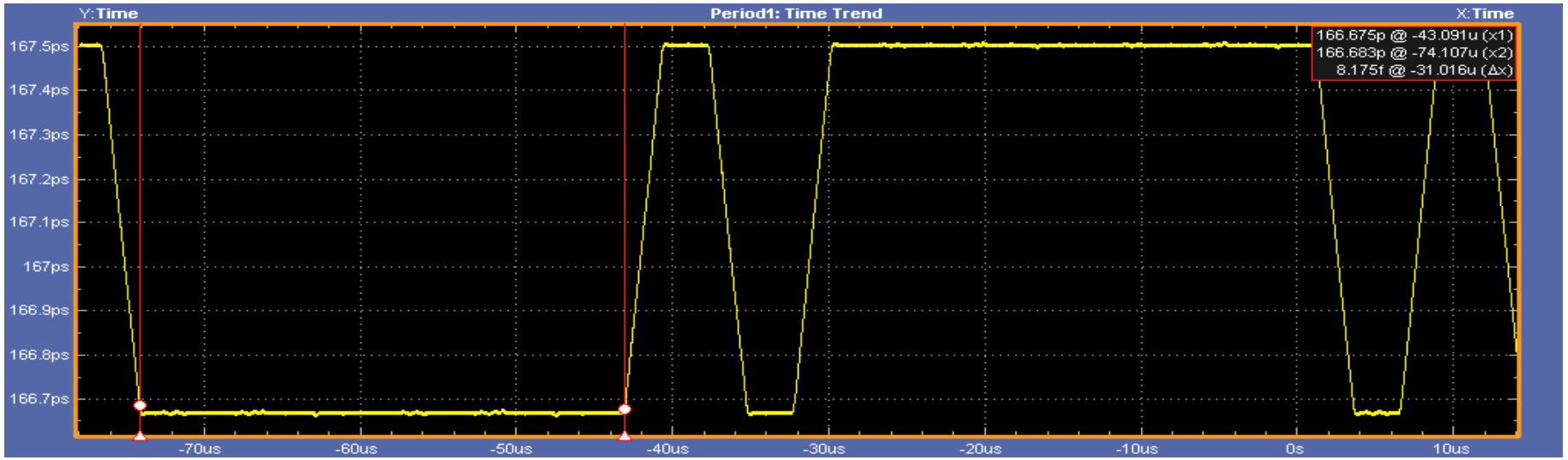
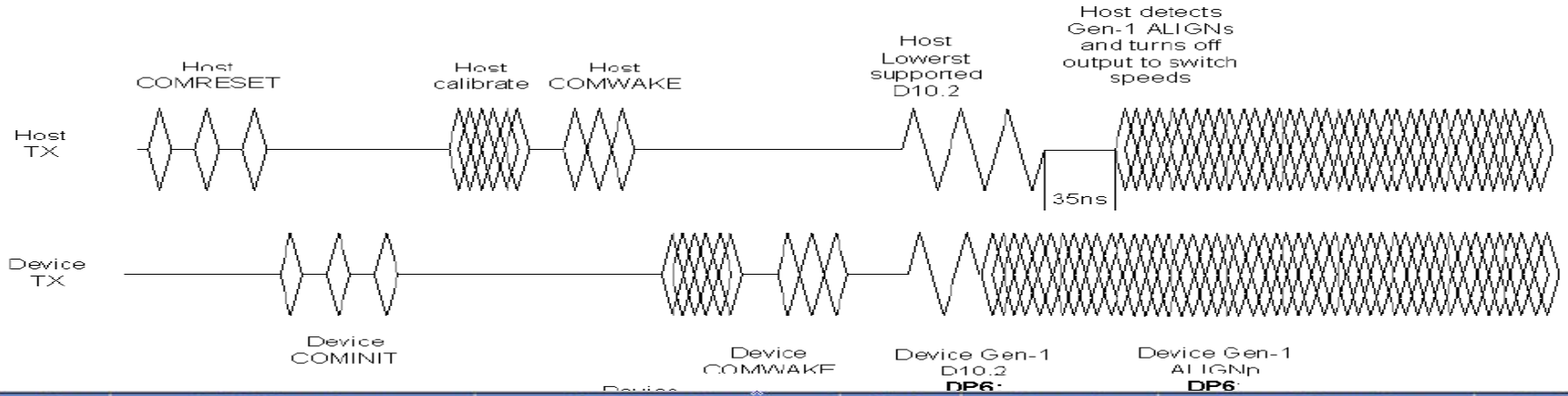
Additional Material





- AWG based sequences referred to as BIST-L initiators are used to negotiate the devices and hosts LSTM.



Index No	Ch 1 Waveform	Ch 2 Waveform	Wait	Repeat	Event Jump To	Go To
1	IDLE-12x	Empty		10		
2	crs01+_16x-24Gs	Empty				
3	IDLE-12x	Empty		10		
4	cwke01+_x16_24Gs	Empty				
5	IDLE-12x	Empty		5		
6	D10_2710_24Gs	Empty		20		
7	-align_32_24Gs	Empty		400		
8	-sync_256_al2_24Gs	Empty		65000		
9	-sync_256_al2_24Gs	Empty		65000	Comm-Reset	
10	-sync_256_al2_24Gs	Empty		65000	Speed Negotiation	
11	-r_rdy32_24Gs	Empty		100	BIST-FIS (Loopback) Activate	
12	-align_32_24Gs	Empty				
13	-r_rdy32_24Gs	Empty		10		
14	-r_ip32_24Gs	Empty		2		
15	-r_ok32_24Gs	Empty		2		
16	-align_32_24Gs	Empty		10		
17	-sync_256_al2_24Gs	Empty		10		
18	-x_rdy32-24Gs	Empty		20		
19	-SOF_24Gs	Empty				
24	-HF-32Dword_24Gs	Empty		Infinite	Next	
25	Gen3-FCP-2A-Clean	Empty		Infinite	Next	Test patterns
26	Gen3-FCP-2A-1Err	Empty				25

Serial ATA Compliance Test Solution

▶ Advanced Technical FAQ

Training: BIST-T –vs- BIST-L

BIST-T (Built In Self Test) –Transmit: Optional capability (not supported on all devices) which allows an 80 bit sequence to be broadcast from a phy's transmitter channel.

Advantages: Ultra low cost method of getting simple patterns out of a device (HFTP, MFTP, LBP etc).
No Align primitives inserted into data stream

Disadvantages: Not all silicon supports this mode of operation.
Pattern is very short.
No crosstalk
Can only test Phy/TSG/RxTx with this mode of operation.
Hosts typically require proprietary SW tools to enable this mode.

BIST-L (Built In Self Test) –Loopback: Required capability (devices are non SATA spec compliant without this) which accepts a signal on it's receiver, retimes it to the local device clock domain, and transmits the received signal out the transmitter.

Advantages: All devices are required to support this mode of operation.
Allows devices to broadcast complex patterns with easy external control. We send it the pattern we want the device to broadcast and it copies the received signal on it's transmitter.
This test mode is fundamental to testing receivers.

Disadvantages: Requires additional equipment cost for an external generator
Sometimes loopback modes include ALIGN primitives in the returned signal stream.

TekExpress Position:

By using the "Manual BIST" mode of operation and pausing the system on the DUT power-cycle Drive-Master or Intel's NAZBist can be used today, to issue a BIST-T command and have the DUT broadcast the required pattern. BIST-T mode of operation is supported today for the PHY/TSG and RxTx tests today provided that user intervention is acceptable to the user.

Serial ATA Compliance Test Solution

ASR

ASR (Asynchronous Recovery): This is a silicon based feature which detects a number of error conditions and resets the link based on these conditions.

1. Disconnect detected
    a. Loss of Data Sync condition
    b. ComReset (DC input signal for more than 20mSec).

This is an important architectural feature designed to allow devices to automatically reestablish a link condition should it be dropped for any reason.
The down side of this feature is that it makes testing nearly impossible (unless you use an AWG7102 or AWG7122B) it this capability is enabled.

30-40% of the silicon in industry today has this feature turned on.

Why does ASR interfere with testing?

ASR interferes with testing when one is required to use an external BIST initiation tool such as Drive Master or Intel's NAZ-Bist tools to set the test state. At which point you need to disconnect from the device and attach a test stimulus system (BERT, pattern generator etc). This disconnect triggers ASR and resets the device.

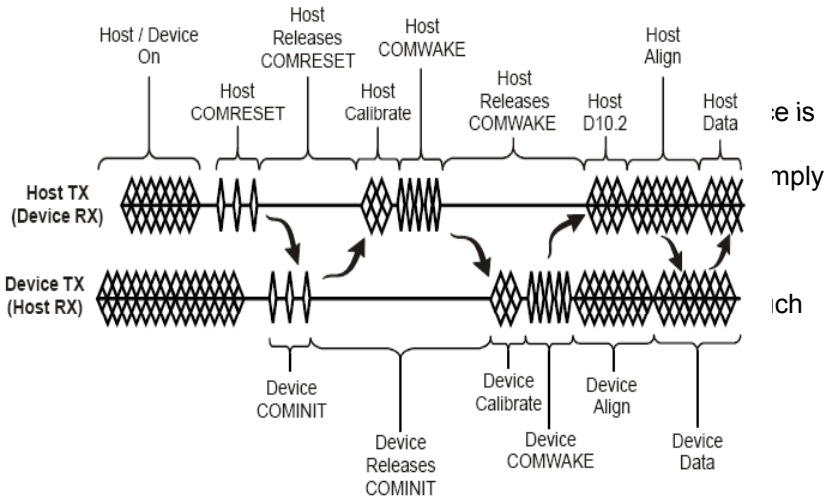
The AWG seamlessly initiates the BIST-L state and proceeds to testing with the required test pattern, without ever triggering the ASR circuitry. Competitors use power splitters, or solid state switches to get around this problem, but you now have additional hardware between the Tx source and the DUT.

Serial ATA Compliance Test Solution

OOB Channel Calibration

The OOB (Out of Band signaling) phase:
The OOB sequence is a multi stage sequence designed to put a SATA Phy into a suitable starting state. It negotiates line rate (Gen1-Gen3) between a host and a drive or port-multiplier. There is a critical step here called "Power-On Calibration" where the source impedance is adjusted once during startup to adapt to the line conditions presented by that host, cable and device pairing (adaptive equalization). Once OOB competes, no further line conditioning is performed.
If ones uses a bus analyzer or PC to put the DUT into a test state, and then disconnects and attaches a BERT (what is commonly done) the line conditions change radically. The internal adapted source impedance settings are not meant for a BERT configuration yielding different results than if the AWG initiates the OOB and BIST-L test states and not detached through the course of the measurements..

SATA 2.6G Spec page 25
7.4.21 OOB Signaling Tes
OOB signaling is used to
in an active mode, a low i
This section specifies the
to the OOB signaling seq
7.4.21.1 Power-On Seque
7.4.21.1.1 Calibration
When the host controller
that the electrical requirer



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