ACS Integrated Test System for Multi-Site Parallel Test

Figure 1. This example ACS integrated test system is configured for parallel, multi-site testing, which is ideal for applications such as:
• Multi-site parametric die sort
• Multi-site wafer level reliability testing
• Multi-site small scale analog functional testing

Industry Challenge

Cost of test has been identified as the number one challenge in the future of advanced semiconductors. The biggest impact on the cost of test as well as the cost of test system ownership is test system throughput. Parallel testing, regardless of the specific application, provides the greatest improvement to the throughput equation for on-wafer test. This is because the majority of the overhead relates to moving or repositioning the probe pins to the next test site. The overhead includes the cost and maintenance of the prober and consumables such as probe cards. Getting the most out of this investment is paramount. Increasing tester throughput can result in significantly decreased cost of test and time to market.

Solution Concept

First, consider the device under test (DUT). A DUT often includes a number of elements that need to be tested. In a sequential test regime, the testing of each element, no matter how simple, adds to the overall test time. If two identical elements can be tested in parallel, or even better, two identical and physically adjacent chips (as shown in **Figure 2**) can be tested in parallel, the total test throughput can be doubled. Not only is the tester throughput doubled, the number of prober moves is cut in half, resulting in significant test system throughput improvement.

It is important to pay critical attention to the possible parasitic interactions between chips. For instance, the coupling through the wafer substrate may require that certain low current tests be executed sequentially. Fortunately, the majority of the testing does not involve low currents.

Another key to managing the cost of test is to consider the use of existing or conventional probing solutions. For example, a conventional probe card can be used to probe the 20 pins of the two chips in **Figure 2**. This concept could be scaled to a larger number of chips while continuing to use readily available probing technology.
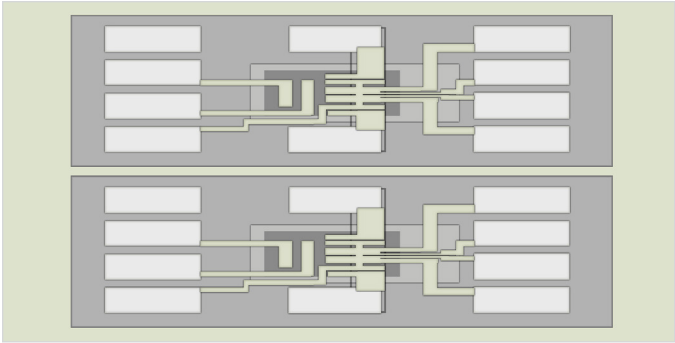
Figure 2. Two small chips site side by side within easy range of a conventional probe card. In this case, each chip consists of two FETs that can be tested in parallel for an overall throughput improvement of 400%.

System Architecture

It is easiest to think of a multi-site tester as a system of mini testers. Each mini tester consists of all the resources needed to execute a suite of tests on a single site. **Figure 3** shows a system of two mini testers. Each mini tester has several analog source-measure units (SMUs), a test sequencer/controller, and an optional switch matrix. The independent controllers allow each mini tester to operate autonomously from the other mini testers and the system controller. In this way, the system controller does not gate the execution of the testing, but rather initiates test sequences and organizes the resulting test data.

Keithley's ACS software integrated test systems support the mini tester architecture through the use of our Series 2600B System SourceMeter® instruments. By using the proprietary TSP-Link™ extensible virtual backplane technology and embedded script processing, groups of Series 2600B units can be formed into mini testers.

The distributed nature of the mini testers allows radical throughput improvements. Using true parallel testing, the four FET test sites in **Figure 2** can be fully tested in less time than a sequential tester could complete the first test on all four FETs (as depicted in **Figure 4**).
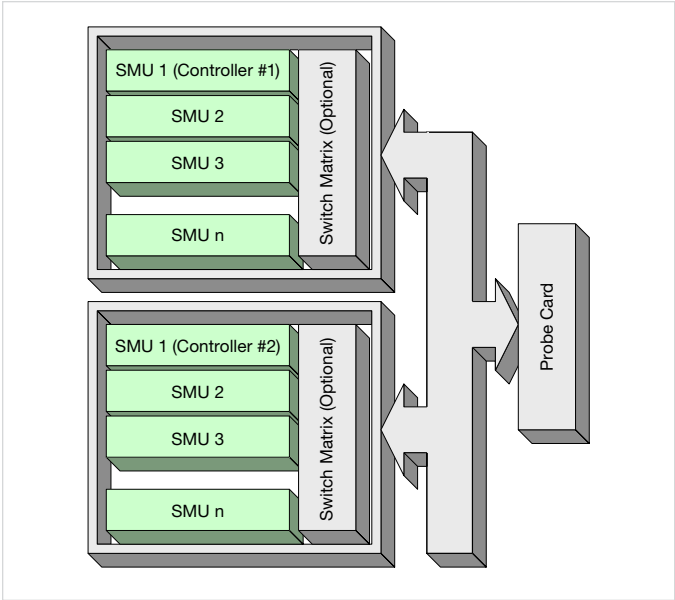

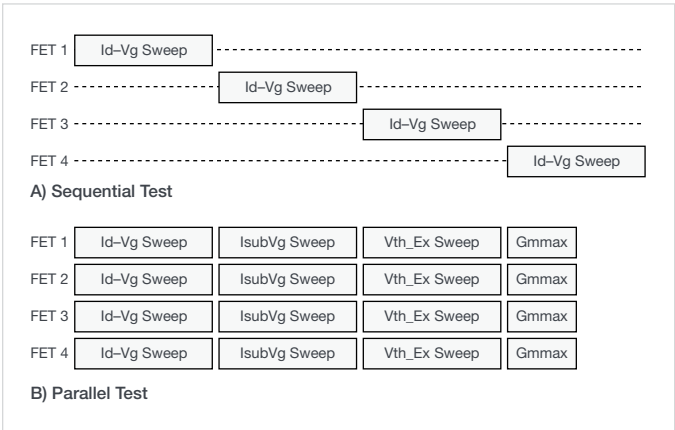Figure 3. Parallel test system architecture.

Figure 4. Comparison of sequential and parallel test.

Ease of Use

There are several potential challenges facing test engineers when implementing a parallel test project. Among these are setting up the test sequences and executing the test in a fully automatic prober environment. Keithley's Automatic Characterization Suite (ACS) software (**Figure 5**) addresses these challenges by providing intuitive user interfaces for:

- Wafer description

- Test setup

- Prober control

- Automation

- Summary report

ACS provides cassette and wafer level automation so that high-throughput parallel testing can be applied to full cassettes of wafers. ACS also includes real time binning graphics and plotting capability (**Figure 6**).
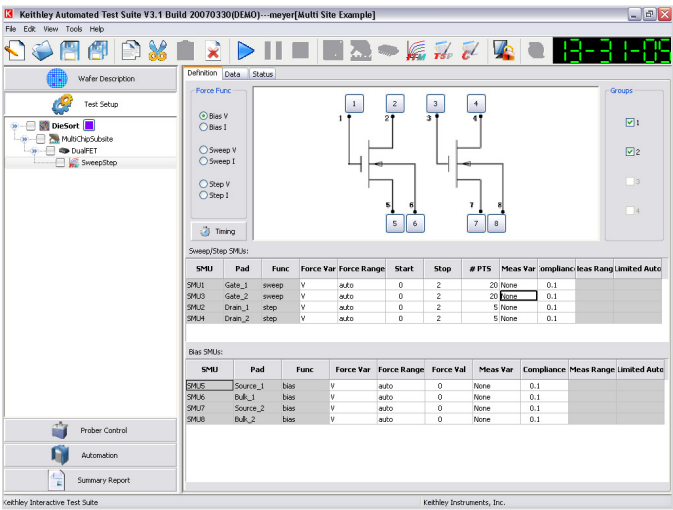

Figure 5. The ACS Test Setup user interface provides parallel testing features that make programming the Series 2600B as simple as pointing, clicking, and entering test parameters.
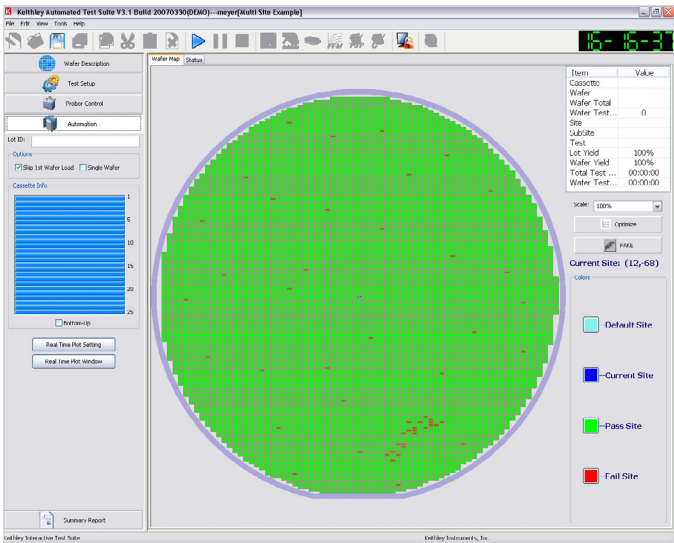

Figure 6. The ACS automation monitor screen displays color coded binning results in real time.

Conclusion

Increasing time to market and cost of test pressures means test engineers must do more with less. Leveraging Keithley's proven instrumentation and measurements, ACS integrated test systems fill an important gap between interactive laboratory based tools and high throughput production test tools.

The ACS software integrated test system depicted in **Figure 1** is uniquely well suited for multi site parallel testing for die sort, advanced reliability, and other high-throughput applications. The Series 2600B instruments' distributed test sequencing capability, provided by the embedded test script processing, supplies the high speed parallel test capability.

Contact Information:

Australia 1 800 709 465

Austria* 00800 2255 4835

Balkans, Israel, South Africa and other ISE Countries +41 52 675 3777

Belgium* 00800 2255 4835

Brazil +55 (11) 3759 7627

Canada 1 800 833 9200

Central East Europe / Baltics +41 52 675 3777

Central Europe / Greece +41 52 675 3777

Denmark +45 80 88 1401

Finland +41 52 675 3777

France* 00800 2255 4835

Germany* 00800 2255 4835

Hong Kong 400 820 5835

India 000 800 650 1835

Indonesia 007 803 601 5249

Italy 00800 2255 4835

Japan 81 (3) 6714 3086

Luxembourg +41 52 675 3777

Malaysia 1 800 22 55835

Mexico, Central/South America and Caribbean 52 (55) 56 04 50 90

Middle East, Asia, and North Africa +41 52 675 3777

The Netherlands* 00800 2255 4835

New Zealand 0800 800 238

Norway 800 16098

People's Republic of China 400 820 5835

Philippines 1 800 1601 0077

Poland +41 52 675 3777

Portugal 80 08 12370

Republic of Korea +82 2 565 1455

Russia / CIS +7 (495) 6647564

Singapore 800 6011 473

South Africa +41 52 675 3777

Spain* 00800 2255 4835

Sweden* 00800 2255 4835

Switzerland* 00800 2255 4835

Taiwan 886 (2) 2656 6688

Thailand 1 800 011 931

United Kingdom / Ireland* 00800 2255 4835

USA 1 800 833 9200

Vietnam 12060128

* European toll-free number. If not accessible, call: +41 52 675 3777

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