



Testing High Power Semiconductor Devices from Inception to Market

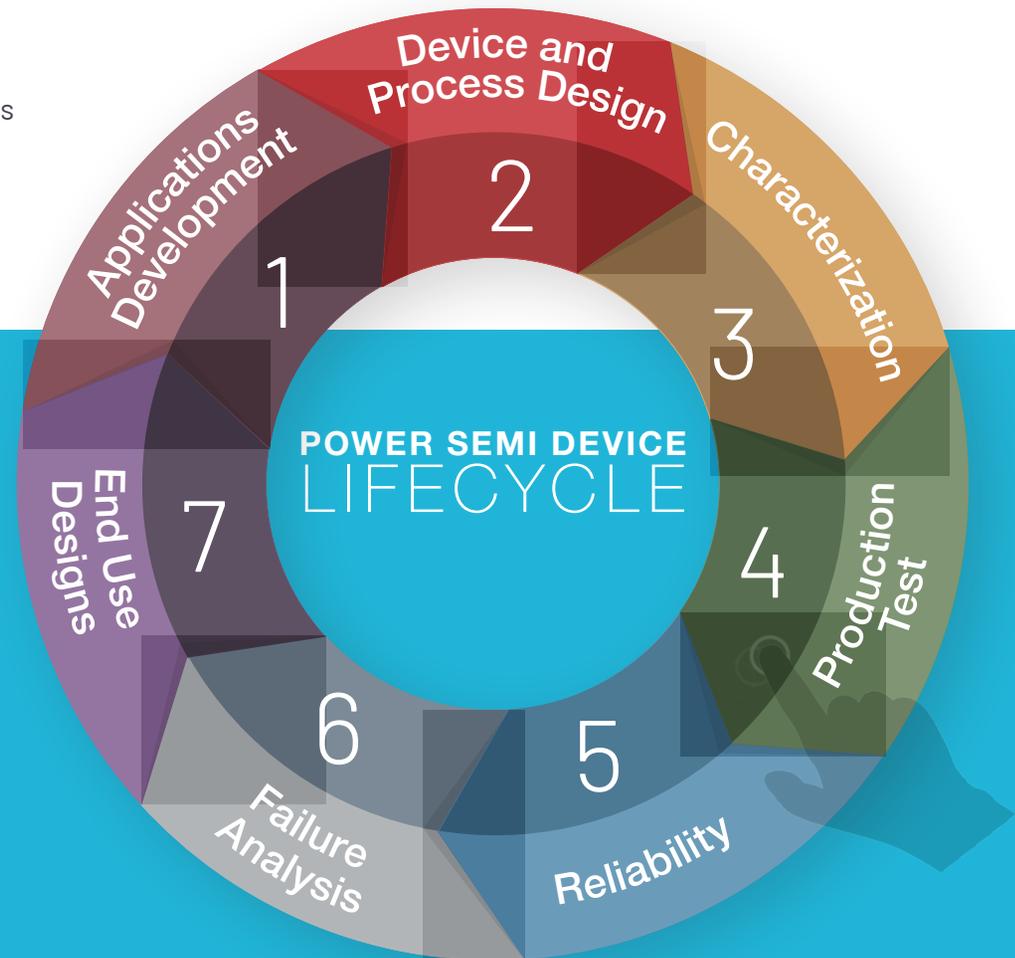
Methods for Efficient, Flexible Test and Characterization Throughout the Life Cycle of a Power Semi Device

PRIMER



Introduction

This primer examines the life cycle of a power semiconductor device and the tremendous variety of test and characterization activities and measurement challenges faced by the engineers involved in each stage throughout the cycle. From the early stages of designing a new power device to the point where it's ready for market, Tektronix's flexible set of high-power characterization tools are ideal for testing across the entire life cycle of a power device.



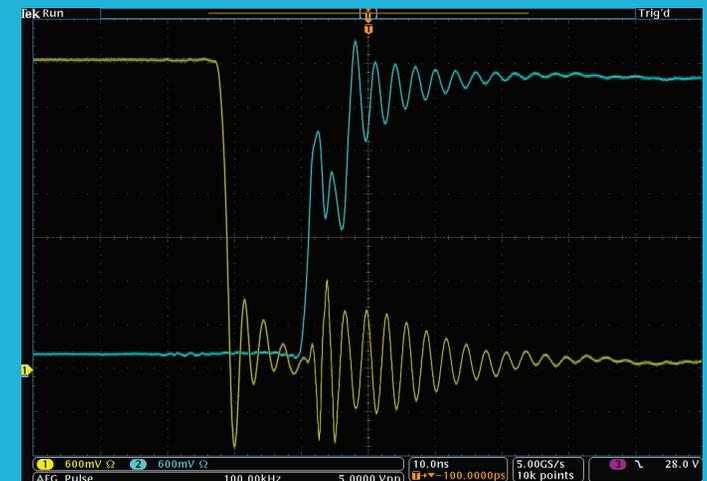
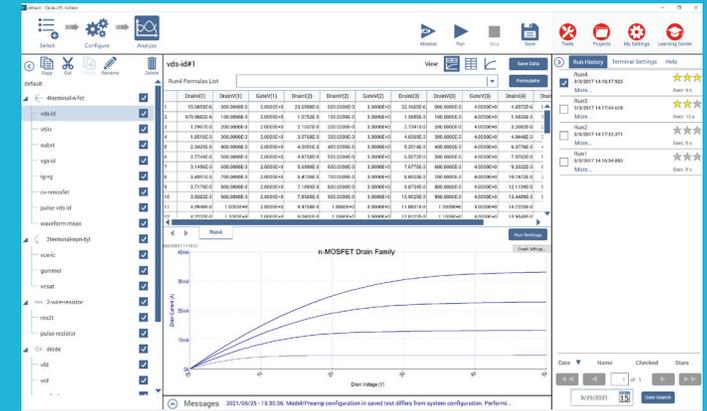
- I-V characterization is a fundamental method of understanding the current versus voltage relationship of power semiconductors. Instruments like source measure units (SMUs) or parameter analyzers show the relationship between the current flowing through a device or circuit and the applied voltage across its terminals.
- For detailed on-state, off-state, or capacitance-voltage characterization, a full parametric curve tracer (PCT) allows both easy data acquisition and detailed parameter extraction.
- For measuring energy loss during device turn-on and turn-off, as well as reverse recovery parameters of a power semiconductor device, a double pulse test system composed of an oscilloscope, power supply, and an AFG are used during device design, validation and for failure analysis.
- Process monitoring, production and reliability testing are critical to ensure commercial usage of a power semiconductor device in critical applications. Multi-channel parallel test systems with automated data evaluation are the tools used in semiconductor fabs.

Evaluating New Devices and Designs for New Application Requirements

Advances in wide bandgap semiconductor technology, particularly in the context of power semiconductor testing and high-power semiconductors, are enabling the development of a clean, renewable and reliable energy ecosystem while creating new challenges for engineers. Requirements are changing continuously along with the types of measurements. How can measurements be made quickly and easily without time being wasted to relearn software and instrumentation?



The Keithley [4200A-SCS Parameter Analyzer](#) and the Tektronix [5 and 6 Series MSO oscilloscopes](#) enable the engineer to perform I-V characterization and device analysis. Pinch and zoom enables deeper insights into device performance.



Methods for Efficient, Flexible Test and Characterization Throughout the Entire Life Cycle of a Power Semi Device

Tektronix offers a wide range of test capabilities, including pulse, DC, and C-V. Our [graphical SourceMeter® source measure unit \(SMU\) instruments](#) simplify the user experience so the engineer can focus on the device and the performance rather than the instrumentation. The Keithley [2461 Graphical High Current Digitizing SMU](#) and the [2470 Graphical High Voltage SourceMeter SMU](#) combined with [KickStart I-V Characterization Software](#) simplify the interaction between multiple SMUs to perform current versus voltage (I-V) testing on high power devices, speeding up the time to insight. For more advanced measurement requirements, the Keithley 4200A-SCS Parameter Analyzer reduces the time from setup to running characterization tests by up to 50%, allowing uncompromised measurement and analysis capability. Plus, embedded measurement expertise provides unparalleled test guidance and gives supreme confidence in the resulting measurements.

Breakdown and Leakage Current Measurements on High Voltage Semiconductor Devices Using the Keithley 2470 SourceMeter® Source Measure Unit (SMU) Instrument and KickStart Software

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Top 7 Characterization Tests for MOSFETs

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Breakdown and Leakage Current Measurements on High Voltage Semiconductor Devices Using the Keithley 2470 SourceMeter® Source Measure Unit (SMU) Instrument and KickStart Software

APPLICATION NOTE



Top 7 Characterization Tests for MOSFETs

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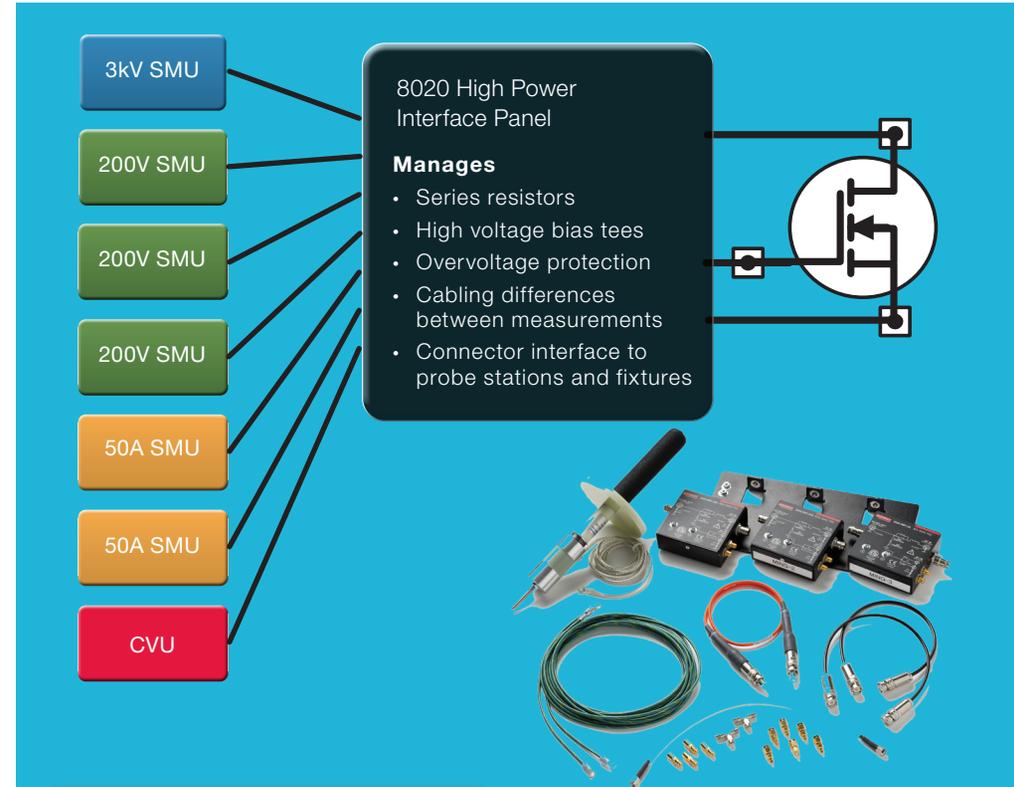
Characterizing Full Performance of New Device Design

To effectively design devices to meet the latest requirements, power device design engineers and process engineers must understand how to tweak the process to produce the desired device performance. There must be confidence that the device models are fairly accurate, and changing a particular process step must produce the necessary change in the device measurement parameter. Therefore, the device engineer must perform preliminary verification of key device parameters.

The combination of a Keithley [Parametric Curve Tracer system](#), the 8020 Probe Station Interface, and [ACS-BASIC Edition Software](#) enables the design engineer to run a wide range of tests that must be performed on wafer or a packaged part for DC, CV, and pulsed test. The ACS-BASIC software is designed from the device perspective and includes scores of device libraries and a built-in formulator to quickly relate measurement to device parameters.

Testing Modern Power Semiconductor Devices Requires a Modern Curve Tracer

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KEITHLEY SourceMeasures Number 3276

Application Note Series

Solving Connection Challenges in On-Wafer Power Semiconductor Device Test

Introduction
Measuring DC and capacitance parameters for high power semiconductor devices requires sufficient expertise to optimize the accuracy of various measurements. Even for those with this level of expertise, managing setup changes between ON-state, OFF-state and capacitance-voltage (CV) measurements can be time consuming and prone to errors. This is especially true in the on-wafer environment.

This application note provides an overview of how the Keithley Model 8020 High Power Interface Panel greatly simplifies the user's experience by:

- Integrating key measurement-enabling accessories for ON-state, OFF-state and CV measurements
- Enabling all CV measurement parameters, at both the component-level and circuit-level, with minimal connection changes at the device under test (DUT)
- Building in flexibility with a variety of connector options
- Expanding easily to support future measurement requirements and new device terminals

Configuring Common Semiconductor Device Measurements using Traditional Accessories and Standalone Instrumentation
A review of the requirements for the DC and capacitance measurements to be made on the DUT is an important first step.

ON-State Measurements
Characteristic curves for a power transistor, I_{CE} or diode, include a plot of its typical output characteristics. Output characteristics for power power devices can involve tens to hundreds of amps. Therefore, creating these curves requires a high current instrument, such as the Keithley Model 2655A High-Power System SourceMeter[®] instrument, when two Model 2655A are configured in parallel, they can generate up to 500A in pulsed current. This SME instrument is coupled with a lower power SME instrument, such as Keithley's Model 2602A, to drive the control terminal (e.g., gate) of a three-terminal device.

To produce optimal high current measurements, managing the resistance and inductance in the cabling is imperative. This can be achieved using low inductance coaxial Kelvin connectors and minimizing the inductive loop area at the DUTs. (Probe station geometries often dictate this inductive loop area.) The gate SME instrument also requires Kelvin connections so that high current pulses at the FET's source terminal don't affect the gate voltage and change the operating point of the device.

High power devices often exhibit high gain and must be prone to oscillation during testing. Adding series resistors helps eliminate such oscillation. In typical test systems, the resistor is inserted between the lower power SME instrument and the gate terminal. This resistor must be housed in a shielded enclosure so that electrostatic interference is not coupled in when characterizing other parameters, such as gate leakage. Otherwise, the series resistor would have to be removed for those other tests. Series resistor values can vary between devices and it may be necessary to try several values in order to select the appropriate value. It can be a design challenge to house and connect to these resistors precisely when performing on-wafer measurements. Figure 1 illustrates the typical setup for high current ON-state measurements.

OFF-State Measurements
OFF-state characterization includes measurement of the breakdown voltage and leakage current of the device. These parameters are typically tested at the

Figure 1. Typical On-state measurement setup.

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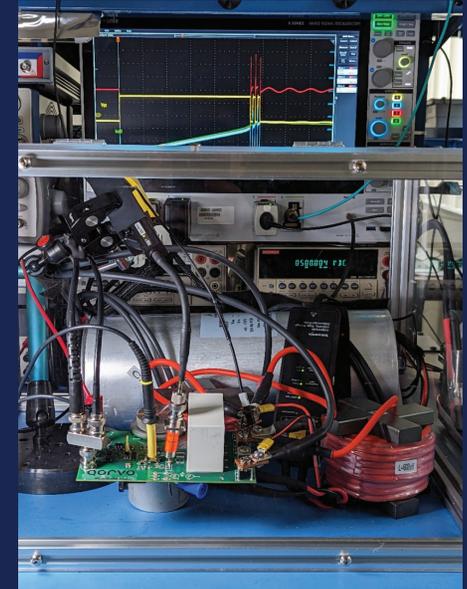
Solving Connection Challenges in On-Wafer Power Semiconductor Device Test

Methods for Efficient, Flexible Test and Characterization Throughout the Entire Life Cycle of a Power Semi Device

A characterization engineer provides the necessary measurement expertise and understanding of how measurement anomalies can impact non-targeted areas of device performance. It's imperative to get results fast to enable multiple iterations with device or process engineers and quickly convert measurements to device parameters.

Minimizing switching losses continues to be a major challenge for power device engineers working on SiC and GaN devices. The standard test method for measuring switching parameters and evaluating the dynamic behavior of Si, SiC and GaN MOSFETs and IGBTs is the [double pulse test \(DPT\)](#). Double pulse testing can be used to measure energy loss during device turn-on and turn-off, as well as reverse recovery parameters.

Double Pulse Testing Power Semiconductor Devices with a 5 or 6 Series MSO with Built-in Arbitrary Function Generator



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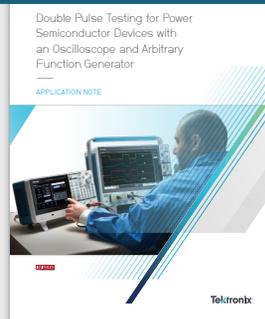
Double Pulse Testing Power Semiconductor Devices with a 5/6 Series MSO with Built-in Arbitrary Function Generator

APPLICATION NOTE



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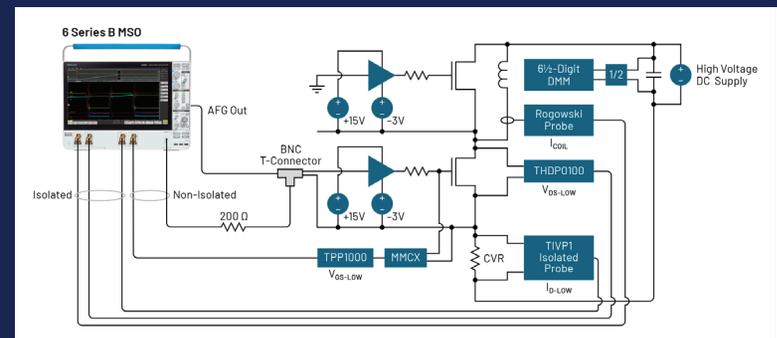
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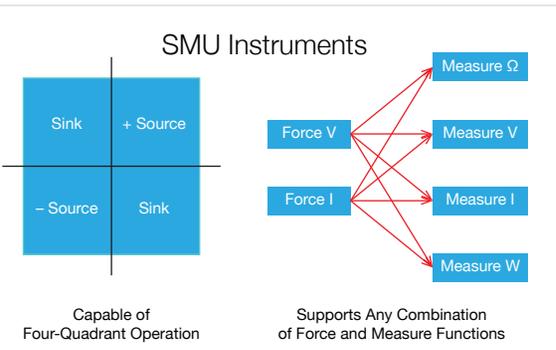


JOSH BROWN
Applications Engineer



Preparing the Device for Production

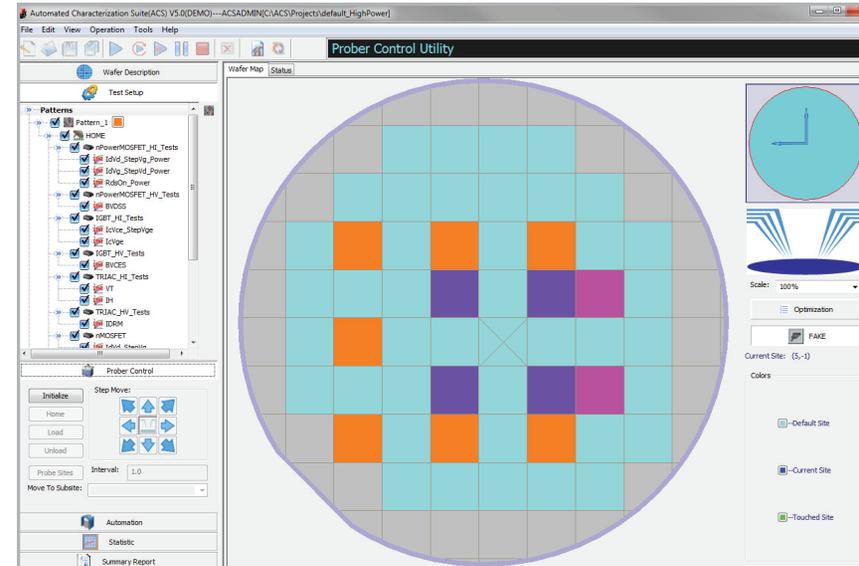
To properly prepare a device for production, the production test engineers must prove if the device can be produced reliably. Measurements must be gathered for statistical setting of device specifications, and test times must be optimized to meet required production throughput.



Multi-functional instruments offer the best way to obtain measurements quickly with minimal connection changes and switching.

SMU instruments are multi-functional instruments that are proven for use in semiconductor applications. SMU instruments with Test Script Processor (TSP®) technology are primed for throughput because of their tight synchronization, built-in processors for complex operations

and decision-making performed within the instrument, thus minimizing communication times. These SMU instruments are used in PCT configurations for interactive testing and also in [S500 Parametric Test Systems](#) for automated production testing. Automated Characterization Suite (ACS) Software combines advanced semiconductor test capabilities along with prober control, data reporting and statistics.



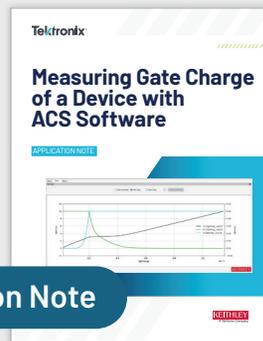
ACS maps devices and tests to sites and subsites, eliminating the need to duplicate each test for each subsite and reducing test development time.

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Keithley's ACS Software

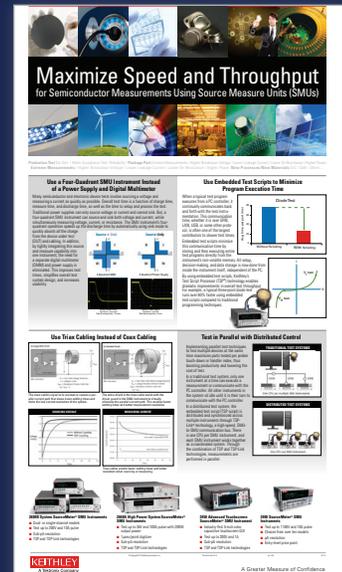


Read the Application Note



Maximize Speed and Throughput for Semiconductor Measurements Using Source Measure Unit (SMU) Instruments

Get the Poster



Meeting Reliability Standards for Commercial Use

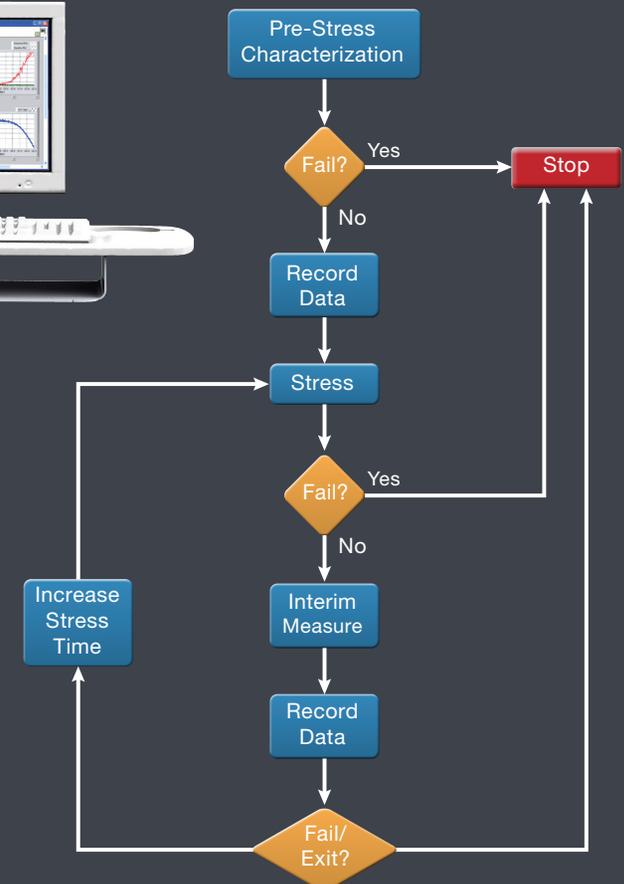
To conclude that a device meets reliability standards for commercial use, reliability test engineers have several responsibilities:

- Determining if a device will survive environmental stresses and continue to meet specifications
- Answering customer questions about device lifetime (MTBF, MTTF)
- Providing key insight into device fit for certain high reliability applications (mil/aero, automotive, etc.)

Creating statistically relevant results requires sufficient sample sizes of the test devices. The nature of stress-measure cycling over many devices necessitates multi-channel parallel test with automated data evaluation.



Process flow for HCI/NBTI/constant current EM tests.



Methods for Efficient, Flexible Test and Characterization Throughout the Entire Life Cycle of a Power Semi Device

S500 Integrated Test Systems are reliability test systems that can be custom built to accommodate from small to large number of devices. **ACS** features stress measure loop cycling with integrated decision making. Keithley also provides a wide range of power supply and SMU instrument solutions to permit simultaneous power and testing of any number of devices.

Learn more from these Application Resources

Optimizing Reliability Testing of Power Semiconductor Devices and Modules with Keithley SMU Instruments and Switch Systems

application brief



Optimizing Reliability Testing of Power Semiconductor Devices and Modules with Keithley SMU Instruments and Switch Systems

Introduction

To minimize early defect rates and to continuously improve the overall reliability and lifetime of power semiconductor, a variety of important tests are performed by both manufacturers and end-use designers. Many of these tests are outlined in JEDEC standards such as JESD22-A100 (Temperature, Bias, and Operating Life), JESD22-A110 (Highly Accelerated Temperature and Humidity Stress Test (HAST) or PHAST), Reliability Qualification of Power Amplifier Modules. This application brief discusses methods to optimize reliability testing of silicon and wide band gap (WBG) power semiconductor devices, modules, and materials by using Keithley SourceMeter® Source Measure Unit (SMU) Instruments and Switch Systems (Figures 1 and 2).

Typical Reliability Tests

Typical reliability tests involve stressing a batch or batches of sample devices by hundreds or thousands of hours with bias voltages that are greater than or equal to their normal operating voltages while subjecting them to temperatures that are well beyond normal operating conditions. During this stress, a variety of key operating parameters are measured at specific time intervals. Some of the more popular reliability tests for power semiconductors are HTDB (High Temperature Operating Life, HTRB (Rush Life Failure Rate), HTRF (High Temperature Forward Bias), HTRH (High Temperature Reverse Bias), and HAST (Highly Accelerated Temperature & Humidity Stress Test). These tests will often use a continuous bias (Figure 3) or cyclic bias (Figure 4). A continuous bias can be a fixed voltage or a staircase ramp. A cyclic bias will typically vary the duty cycle and/or frequency of the bias voltage. In both cases, key device parameters will be tested continuously or at specific time intervals.

Reliability Testing Challenges

Reliability testing of today's WBG power semiconductors presents several key challenges for engineers and test system designers. Most importantly, since most of these devices are being targeted for energy efficiency applications, they have much lower leakage and on-resistance specifications compared to traditional silicon. The test instrumentation must therefore be capable of providing the necessary accuracy, resolution, and stability to meet the electrical requirements of these devices. In addition, since WBG devices exhibit failure mechanisms that are different from silicon, effective reliability testing per JEDEC standards requires larger sample sizes and longer stress durations to adequately predict important reliability parameters. This requires test instrumentation that is capable of supplying enough power to test many devices in parallel while maintaining the accuracy and resolution mentioned above. Finally, the test instrumentation must be able to respond to the high-speed behavior associated with these devices and produce the masses of data associated with testing devices in parallel. Each instrument in the system must be fast, and all units must operate in a highly synchronized manner.



Figure 1. Keithley Series 2500A and 7070 Series Switch Systems.



Figure 2. Keithley Series 3500A and 7070 Series Switch Systems.

V_{DS} Ramp and HTRB Reliability Testing of High Power Semiconductor Devices with Automated Characterization Suite (ACS) Software

KEITHLEY
Application Note Series

Number 5220

V_{DS} Ramp and HTRB Reliability Testing of High Power Semiconductor Devices with Automated Characterization Suite (ACS) Software

Introduction

Wide bandgap semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) offer physical properties superior to those of silicon (Si) for power device applications, enabling devices based on these materials to withstand high voltages and temperatures, as well as providing higher frequency response, greater current density, and faster switching [1]. These emerging power devices have great potential; however, the technologies necessary to create and refine them are still under development and therefore less mature than silicon technology. This creates some key challenges associated with designing and characterizing these devices, as well as process monitoring and reliability issues [2].

Before they can gain commercial acceptance, the reliability of wide bandgap devices must be proven and there is a demand for higher reliability requirements. The continuous drive for greater power density at the device and package levels creates consequences in terms of higher temperatures and temperature gradients across the package. New application areas often mean more severe ambient conditions. For example, in automotive hybrid traction systems, the cooling liquid for the combustion engine may reach temperatures as high as 120°C. In order to provide sufficient margin, this means the maximum junction temperature (T_{Jmax}) must be increased from 150°C to 175°C [4]. In safety-critical applications such as aircraft, the zero-defect concept has been proposed to meet stricter reliability requirements.

V_{DS} Ramp and HTRB Reliability Tests

The V_{DS} ramp and the High Temperature Reverse Bias (HTRB) tests are among the most common reliability tests for power devices. In a V_{DS} ramp test, as the drain-source voltage is swept from a low voltage to a voltage that is higher than the rated maximum drain-source voltage, specified device parameters are evaluated. The test is useful for testing the design and process conditions, as well as verifying that devices deliver the performance specified on their data sheets. For example, Dynamic R_{DS(on)} monitored using a V_{DS} ramp test, provides a measurement of how much a device's R_{DS(on)} increases after being subjected to a drain bias [5]. Although a V_{DS} ramp test is generally used as a quick form of parameter verification, an HTRB test evaluates long-term stability under high drain-source bias. During an HTRB test, the device samples are stressed at or slightly less than the maximum rated reverse breakdown voltage (usually 90% or 80% of V_{BR0}) at an ambient temperature close to their maximum rated junction temperature (T_{Jmax}) over a

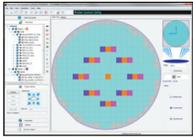


Figure 1. Automated Characterization Suite (ACS) graphical user interface period of time (usually 1,000 hours)[3][5][6][7]. The leakage current is continuously monitored throughout the test and a fairly constant leakage current is generally required to pass the test. Because it combines electrical and thermal stress, this test can be used to check the junction integrity, crystal defects and ionic-contamination level, which can reveal weaknesses or degradation effects in the field depletion sensor area at the device edges and in the passivation [8].

Test Instrumentation and Measurement Considerations

Power device characterization and reliability testing require test instrumentation with higher voltage as well as more sensitive current measurement capability than ever before [2]. During operation, the device undergoes both electrical and thermal stress when in the ON state; they have to pass tens or hundreds of amps with minimal low duty voltage high currents when they are OFF; they have to block thousands of volts with minimal leakage currents (high voltage low current). Additionally, during the switching transient, they are subjected to a brief period of both high voltage and high current. The high current experienced during the ON state generates a large amount of heat, which may degrade device reliability if it is not dissipated efficiently [1].

Reliability tests typically involve high voltages, long test times, and often multiple devices under test (multi-test testing). As a result, well-designed test systems and measurement plans are essential to avoid breaking devices, damaging equipment, and losing test data. Consider the following factors when executing V_{DS} ramp and HTRB reliability tests:

New High Power Semiconductor Devices are Pushing Instrumentation to Extremes

New High Power Semiconductor Devices Are Pushing Instrumentation to Extremes

TECHNICAL BRIEF

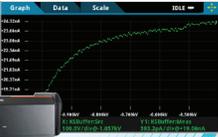


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Implementing the Device in Actual Designs

Once a device is validated, it's ready for commercial use. Those who purchase devices must verify that the device is within tolerance for a particular application to ensure that the expected power efficiency gains will be achieved in the end product. As the device matures and becomes available from multiple suppliers, power device consumers want to quickly inspect incoming devices in order to identify and eliminate counterfeit devices to avoid potential failures in the end product.

Tektronix and Keithley offer a wide variety of power supply and source measure unit solutions to power basic circuit boards. Keithley's [Parametric Curve Tracer \(PCT\) Configurations](#) and [ACS Basic Edition Software](#) include a large library of power device tests so incoming inspection test on individual device performance can be quickly verified. Additionally, [Tektronix's oscilloscopes](#) with optional power analysis modules enable quick and accurate analysis of switching loss, harmonics, and safe operating area. Choose from a wide variety of [high voltage, current, and differential probes](#) to partner with an oscilloscope.

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Testing Modern Power Semiconductor Devices Requires a Modern Curve Tracer

David Wyban
Applications Engineer



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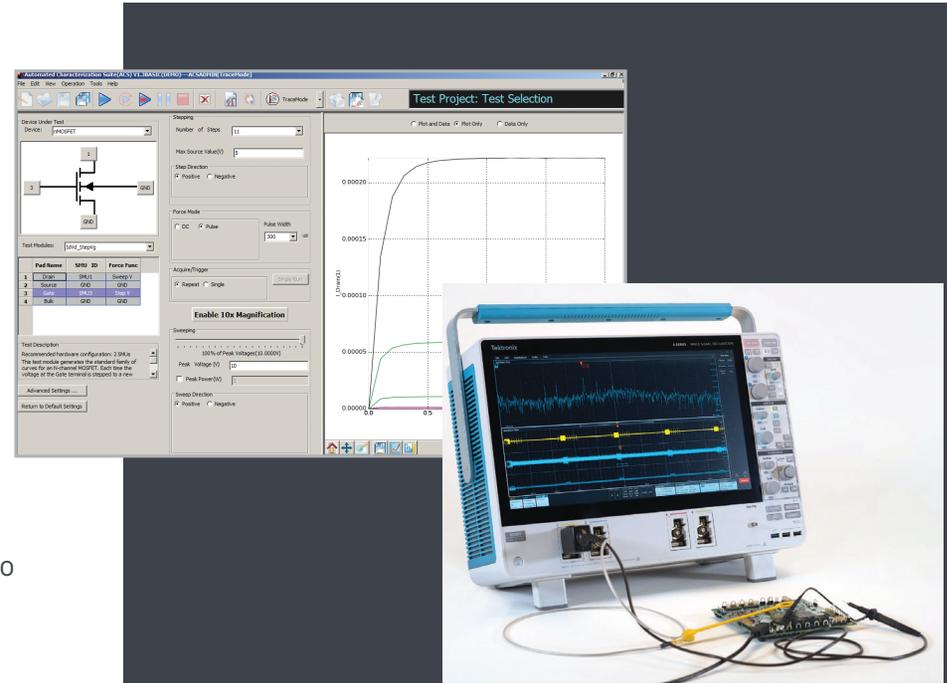


Today's power supply designers are faced with increasing pressure to achieve power conversion efficiencies of 90% and even higher.

Failure Analysis of Devices and Actual Designs

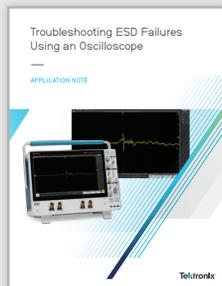
Failure analysis engineers must determine whether a failure has been caused by end-product use or by a design flaw that was previously overlooked. Once this determination has been made, design and process engineering must be made aware of the cause of the failure so that either process or design changes can be implemented to prevent future failures.

It's important that basic device specifications, both static and dynamic, can be measured quickly. The end use application is mimicked in an effort to reproduce the failure. Keithley [Parametric Curve Tracer Configurations](#) feature trace mode, which provides quick device analysis. [Tektronix oscilloscopes](#) enable the engineer to diagnose failures resulting from ground loops, ESD and component failure on circuit boards.



Learn more from our Experts | Download these Application Resources

Troubleshooting ESD Failures Using an Oscilloscope



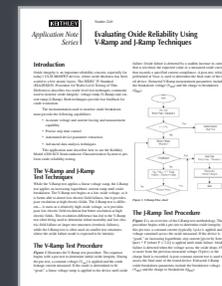
Measuring Low Resistance Devices with High Current Using the 2460 SourceMeter SMU Instrument



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Evaluating Oxide Reliability Using V-Ramp and J-Ramp Techniques



EMI Troubleshooting with the Latest-Generation Oscilloscopes



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Rev. 02.2022

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