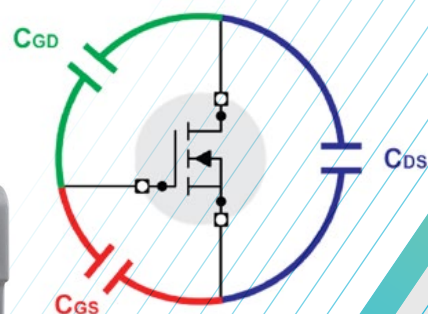
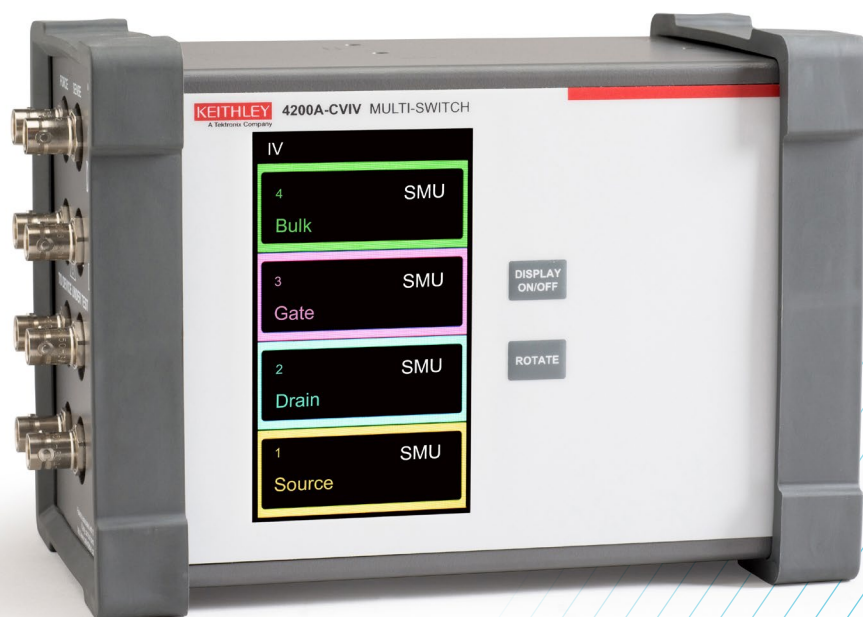


Making Three-Terminal Capacitance-Voltage Measurements Up to 400 V Using the 4200A-CVIV Multi-Switch Bias Tee Capability

APPLICATION NOTE



KEITHLEY
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Introduction

The switching speeds of semiconductor devices such as MOSFETs, IGBTs and BJTs are affected by the capacitance of the components themselves. In order to design their circuits for efficiency, designers need to know these parameters. For example, designing an efficient switch-mode power supply would require the designer to know the device capacitance because this would affect the switching speed and, therefore, the efficiency. This information is usually provided in a MOSFET's datasheet.

The capacitance of three-terminal power semiconductor devices can be looked at in two different ways: at the component level and at the circuit level. Looking at the capacitances at the component level involves characterizing capacitance between every device terminal. Looking at the capacitance at the circuit level involves characterizing the combination of component-level capacitances. For example, **Figure 1** illustrates the component-level capacitances of a power MOSFET.

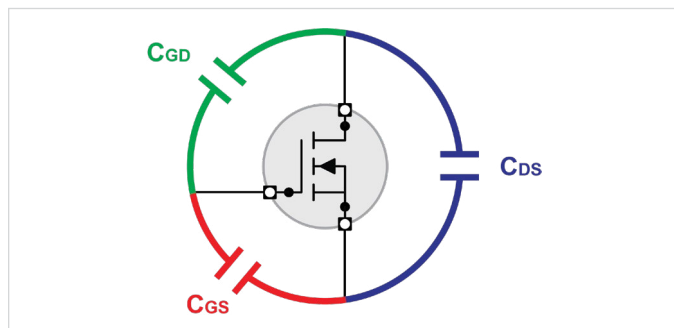


Figure 1. Component-level capacitances for a power MOSFET

Figures 2 through 4 illustrate the relationship between the component-level and circuit-level capacitance for a power MOSFET. Similar capacitance measurements can also be made for BJT and IGBT devices.

The relationships are derived as follows:

- $C_{ISS} = C_{GS} + C_{GD} = \text{input capacitance}$
- $C_{OSS} = C_{DS} + C_{GS} = \text{output capacitance}$
- $C_{RSS} = C_{GD} = \text{reverse transfer capacitance}$

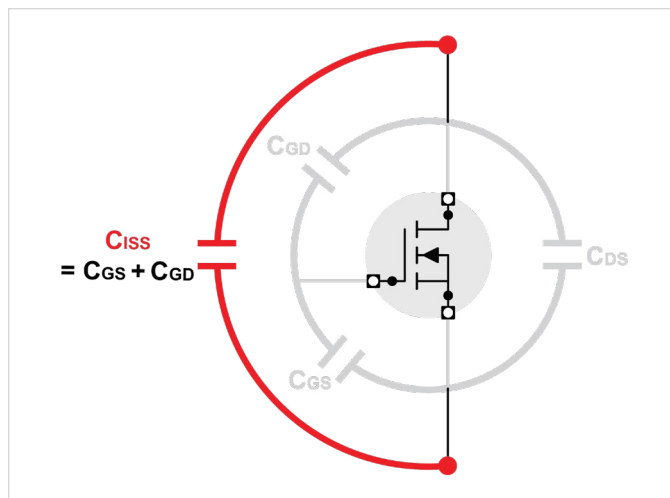


Figure 2. Input capacitance for a power MOSFET

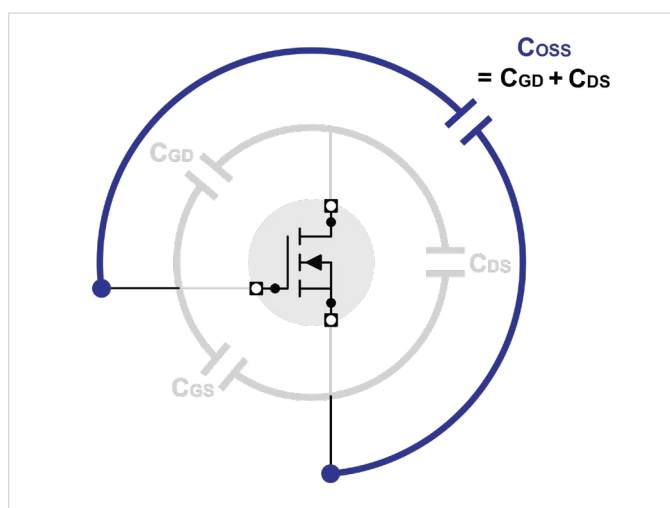


Figure 3. Output capacitance for a power MOSFET

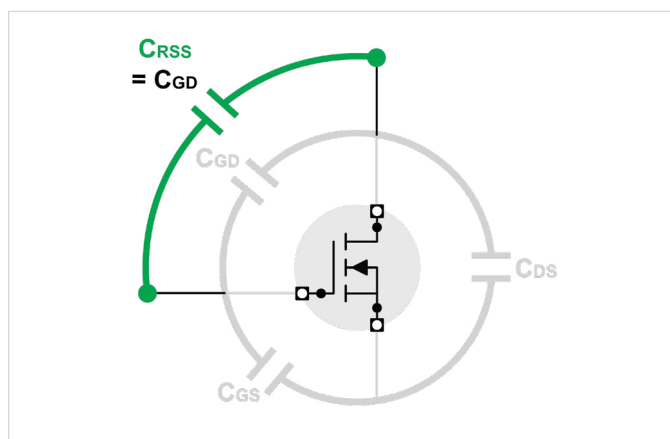


Figure 4. Reverse transfer capacitance for a power MOSFET

Device capacitance typically varies with the applied voltage. Therefore, complete characterization requires knowledge of the capacitance at the maximum rated voltage. This application note explains how the C_{ISS} , C_{OSS} and C_{RSS} measurements are made using the bias tee capabilities provided by the 4200A-CVIV Multi-Switch and that were added in Clarius V1.4. The CVIV can easily switch between I-V and C-V measurements without recabling. It can also move the C-V measurements to any device terminal without recabling or lifting probe needles.

This application note also shows how the instrument DC output voltage was doubled from 200 V to 400 V for higher voltage measurements on the drain, which is beneficial for testing higher power semiconductors, such as GaN devices. This capability was added in Clarius V1.6 and updated in Clarius V1.9. This application note assumes the reader is familiar with making C-V measurements with the Keithley 4200A-SCS using the 4200A-CVIV.

For more information on bias tee capabilities, refer to these Keithley application notes:

- Using the 4200A-CVIV Multi-Switch to Make High Voltage and High Current C-V Measurements
- Switching Between C-V and I-V Measurements Using the 4200A-CVIV Multi-Switch and 4200A-SCS Parameter Analyzer

Device Connections

All the SMU and CVU connections described in this application note are made through the 4200A-CVIV. The CVIV could have one 4210-CVU or 4215-CVU and up to four SMUs connected to a device. Refer to the 4200A-CVIV Multi-Switch User's Manual for more information.

Using the 4200A-CVIV offers these advantages:

- User-ready, built-in projects to measure C_{ISS} , C_{RSS} and C_{OSS} at up to 200 V and 400 V.
- Automated measurements enabled by the 4200A-CVIV Multi-Switch. There is no need to reconnect the device or cables.
- Open and short C-V compensation.

Figure 5 shows the connection of a MOSFET to the CVIV. For this specific application, at least three SMUs and one CVU are required to complete the test.

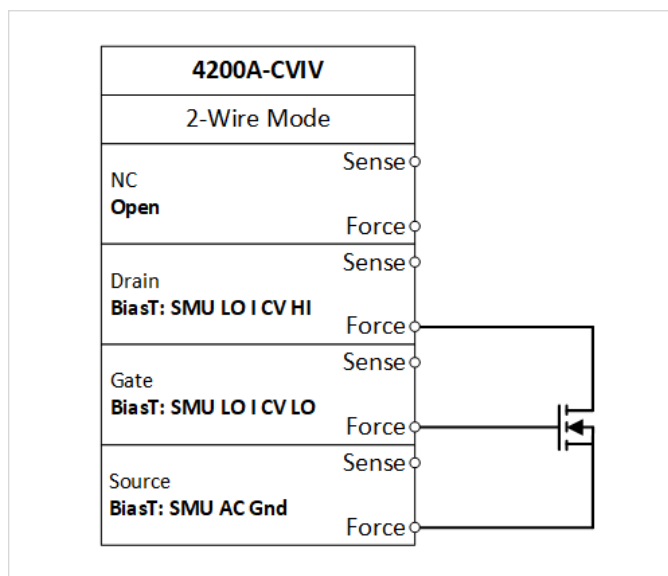


Figure 5. MOSFET connections to the output terminals of the 4200A-CVIV

Figure 6 shows the actual CVIV connections to a packaged MOSFET. Note that all the channels are open on the CVIV. The four channels of the 4200A-CVIV will be configured based on the configuration of each test, so no cable reconnections are required for each test.

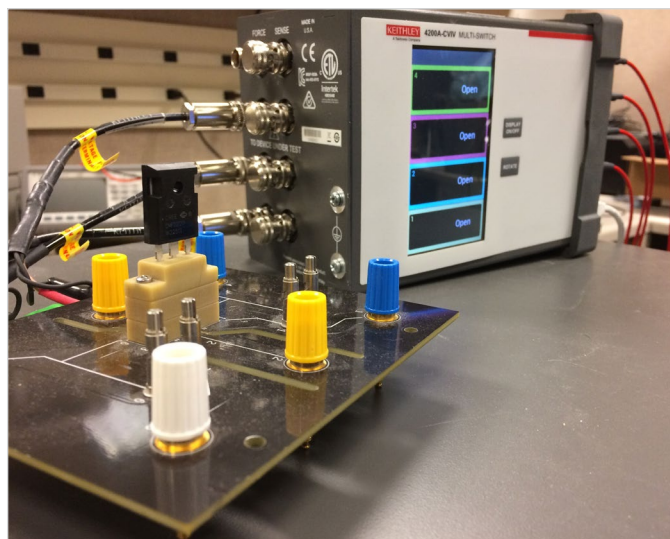


Figure 6. Packaged MOSFET connected to the 4200A-CVIV

Configuring the Measurement in Clarius

The library in Clarius has two projects that perform three-terminal capacitance measurements on MOSFETs. Both projects are similarly configured in Clarius; the difference is with the capability. One project, “MOSFET 3-terminal C-V Test Using 4200A-CVIV Bias Tees,” uses a single SMU on the drain, sweeping from 0 to 200 V. The other project, “MOSFET 3-terminal C-V tests up to 400 V using 4200A-CVIV Bias Tees,” uses a novel approach to double the voltage to go from 0 to 400 V. This approach uses three SMUs sweeping simultaneously, one on each terminal, to provide a 400 V DC differential across the drain.

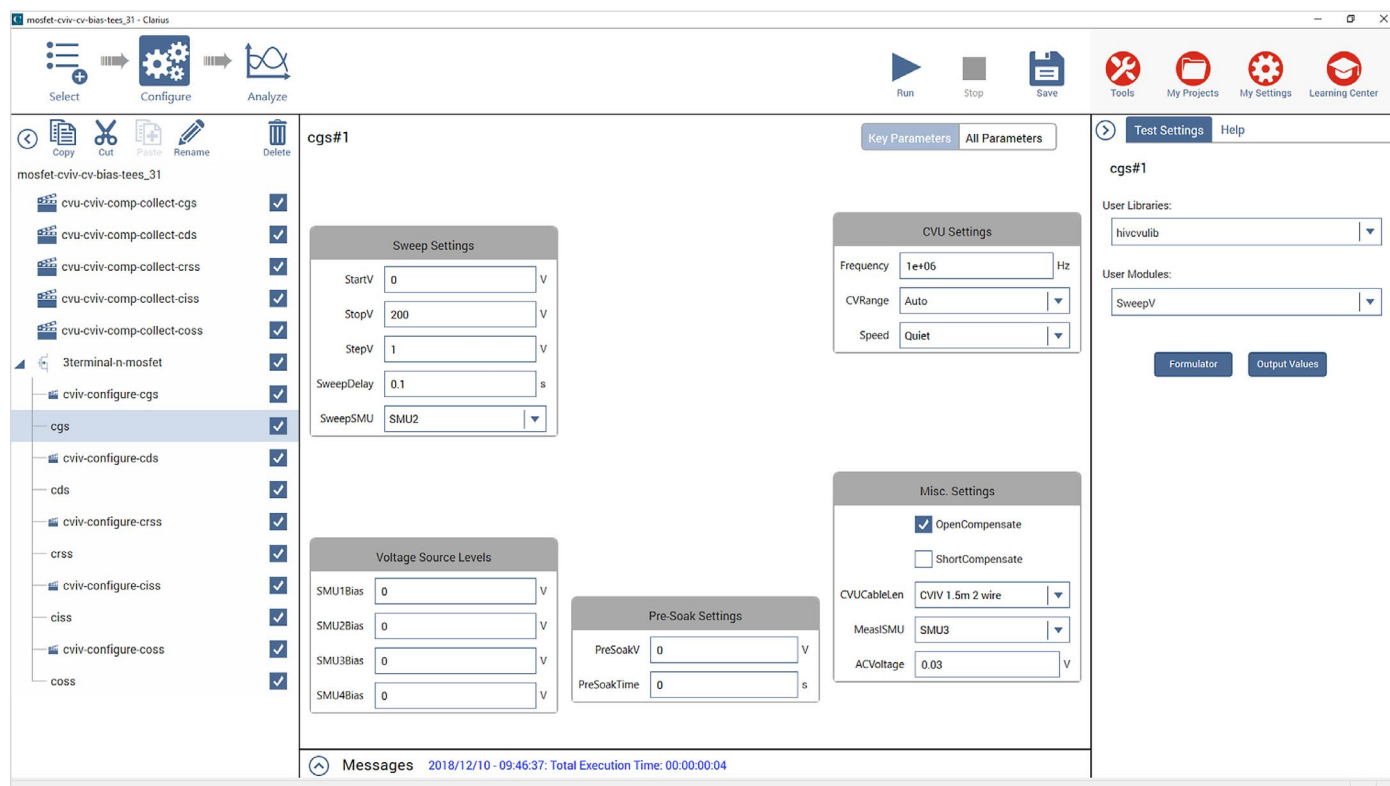


Figure 7. MOSFET-CVIV-CV-Bias-Tees project using the SweepV user module

Figure 7 shows the “MOSFET 3-terminal C-V Test Using 4200A-CVIV Bias Tees” project that uses the SweepV user module in the *hivcvulib*.

This user module enables one sweeping SMU at the drain and capacitance measurements taken at each terminal.

First, open and short compensations are performed to ensure accurate measurements. Specific configuration steps are necessary to perform these compensations. They are called

compensation collect actions and are provided in the project tree. Compensation is performed for each test configuration before any test is executed. The 4200A can store the compensation for each configuration so multiple tests can be performed.

This project has five different configurations: C_{GS} , C_{DS} , C_{RSS} , C_{ISS} and C_{OSS} .

CVIV Configuration

The CVIV must be configured accordingly for each test.

The CVIV has many output modes, which are described in the user manual. Table 1 lists the various output modes.

Table 1. 4200A-CVIV output modes

4200A-CVIV Output Mode	Application and Description
Open	Default setting. Also disconnects a channel from the device.
SMU	Used for I-V measurements. Connects Force HI and Sense HI to the device.
CV HI	Used for C-V measurements. Connects the CVU (HPOT and HCUR) to the device.
CV LO	Used for C-V measurements. Connects the CVU (LPOT and LCUR) to the device.
CV Guard	Used to guard unwanted impedance when making C-V measurements on multi-terminal devices. Apply CV Guard to the terminal to be excluded from the C-V measurement.
Ground Unit	Used for I-V measurements. Connects Force LO and Sense LO to the device.
AC coupled AC ground	Used for C-V measurements. Allows an AC path to ground without providing a DC path.
BiasT SMU CV HI and BiasT SMU CV LO	Used for C-V measurements up to 200 V DC bias. Allows a DC current of up to 1 A, ideal for on-state device measurements.
BiasT SMU LO I CV HI and BiasT SMU LO I CV LO	Recommended for C-V measurements up to 200 V DC bias. Allows a DC current of up to 100 μ A, ideal for off-state device measurements.
BiasT SMU AC Gnd	Used to guard unwanted impedance when making C-V measurements on multi-terminal devices. Allows DC bias up to 200 V. Apply BiasT SMU AC Gnd to the terminal to be excluded from the C-V measurement.

Figures 8 through 12 indicate states for each channel of the CVIV for each of the component- and circuit-level capacitance measurements.

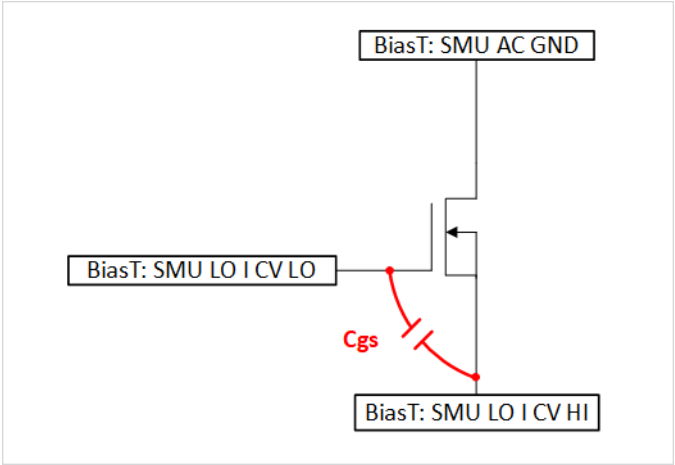


Figure 8. C_{GS} configuration

Figure 8 shows the C_{GS} configuration. This test measures capacitance between the gate and source of the MOSFET while an SMU sweeps DC voltage at the drain.

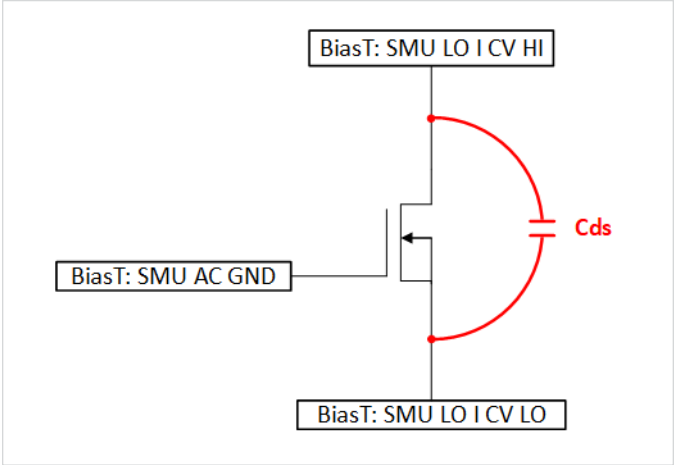


Figure 9. C_{DS} configuration

Figure 9 shows the C_{DS} configuration. This test measures capacitance between the drain and source of the MOSFET while an SMU sweeps DC voltage at the drain.

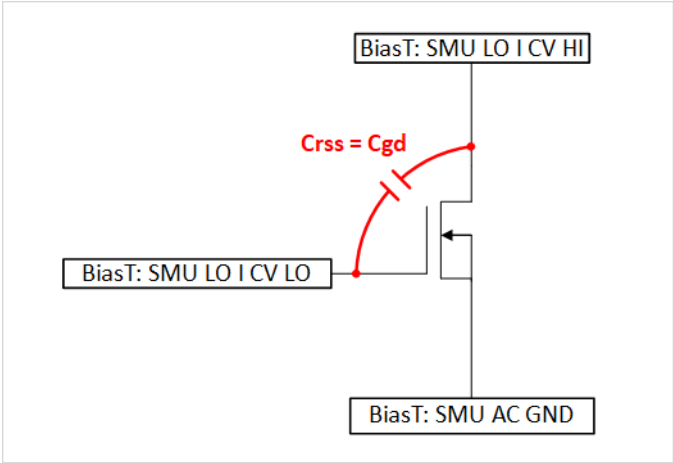


Figure 10. C_{RSS} and C_{GD} configuration

Figure 10 shows the C_{RSS} configuration. This test measures reverse transfer capacitance of the MOSFET while an SMU sweeps DC voltage at the drain.

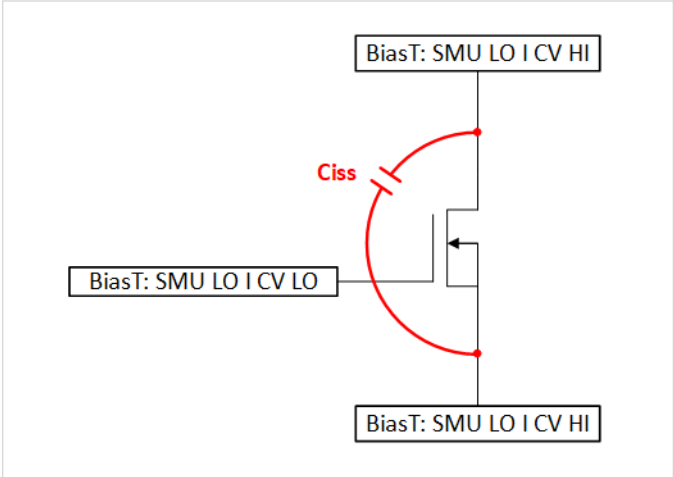


Figure 11. C_{ISS} configuration

Figure 11 shows the C_{ISS} configuration. This test measures the input capacitance of the MOSFET while an SMU sweeps DC voltage at the drain.

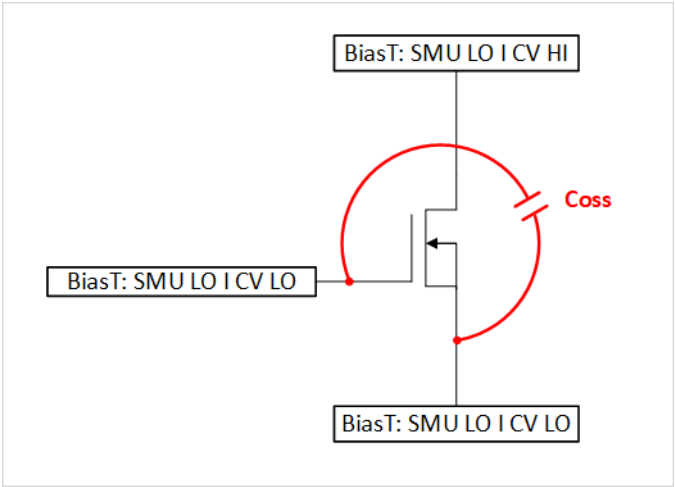


Figure 12. C_{OSS} configuration

Figure 12 shows the C_{OSS} configuration. This test measures the output capacitance of the MOSFET while an SMU sweeps DC voltage at the drain.

Once the tests are executed, the data is plotted. **Figure 13** shows the capacitance characteristics data of a MOSFET as generated with the 4200A.

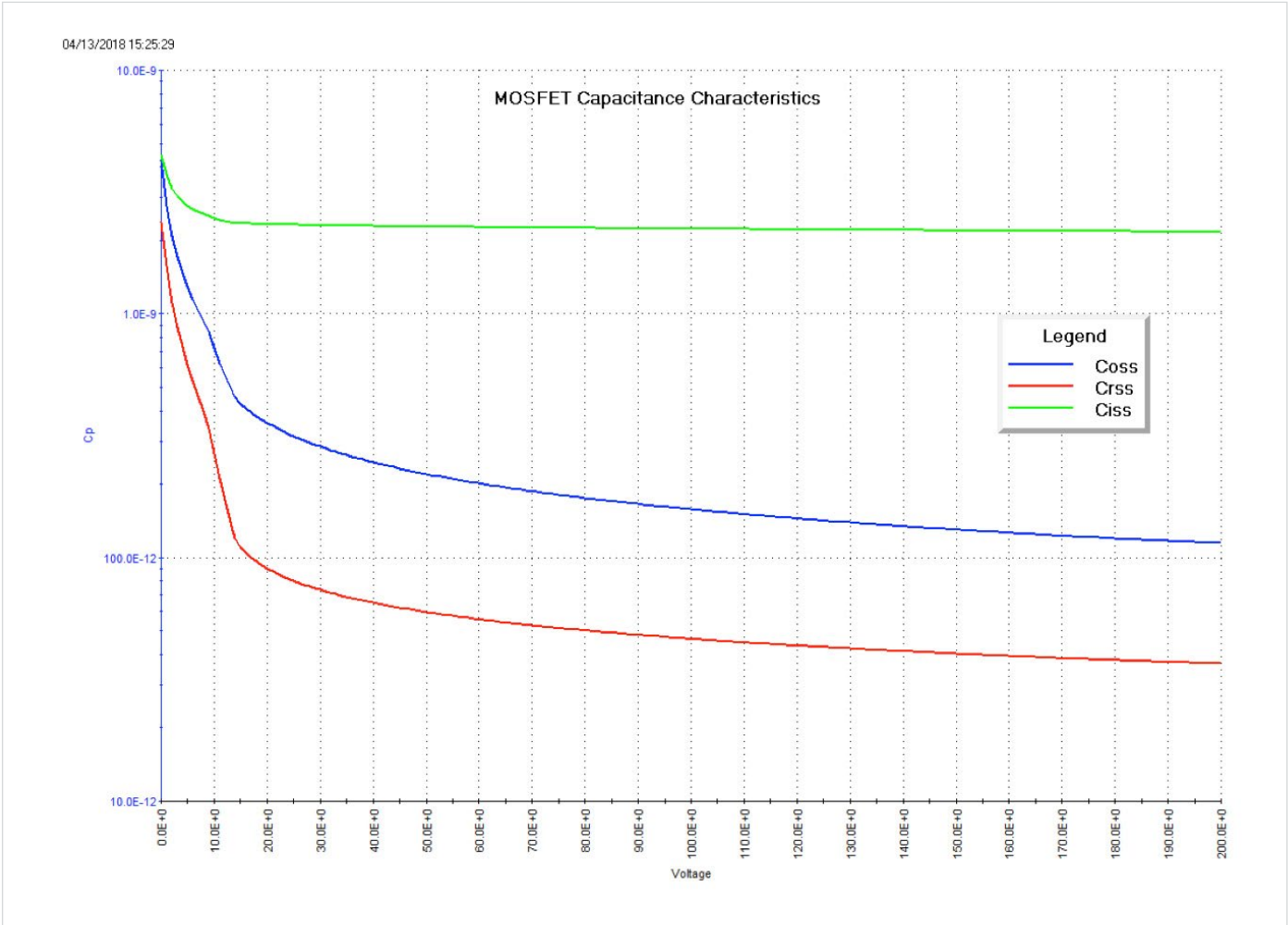


Figure 13. Capacitance characteristics of a MOSFET sweep to 200 V

400 V DC Voltage Sweep

A novel method has been developed to take advantage of the 4200A-CVIV Multi-Switch and sweeping multiple SMUs simultaneously to double the output voltage to 400 V at the MOSFET terminal. These tests are usually done in the OFF state ($V_{GS} = 0$ V). There's usually one sweeping SMU at the drain and, using the bias tee capabilities built into the 4200A-CVIV, the capacitance is then measured at each terminal.

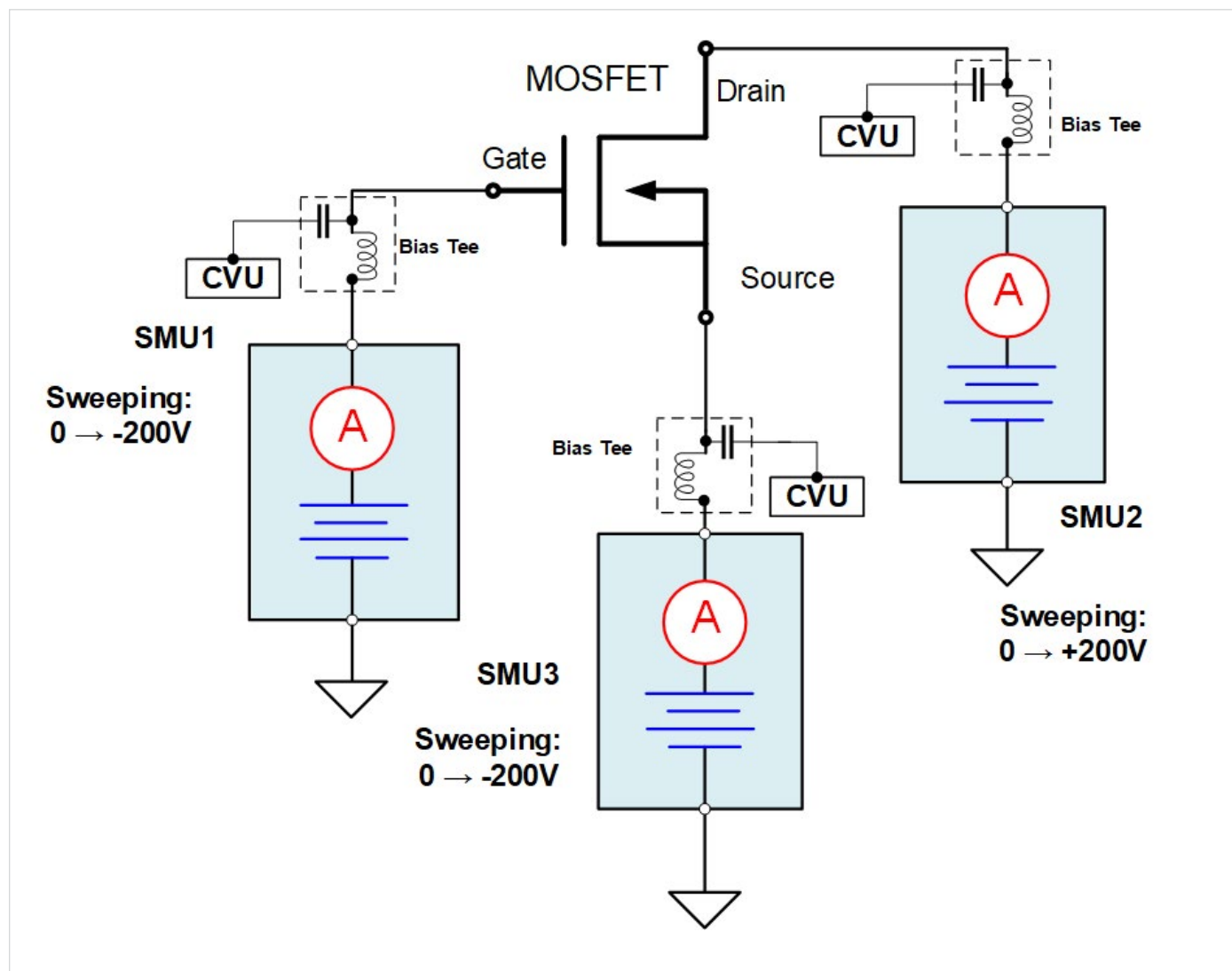


Figure 14. Three SMUs sweeping simultaneously

Figure 14 shows three sweeping SMUs connected to the three terminals of the MOSFET. SMU1 and SMU2 will enable a voltage sweep up to 400 V differential. SMU2 and SMU3 must sweep simultaneously at the same voltage, which enables a 0 V drop at the gate. Using this method, we can produce a 400 V sweep at the drain.

Note: This method is to be used on packaged devices only, and not for wafer-level devices.

These measurements are performed using the *multipleSMU_SweepV* user module, available in the *hivcvulib* user library.

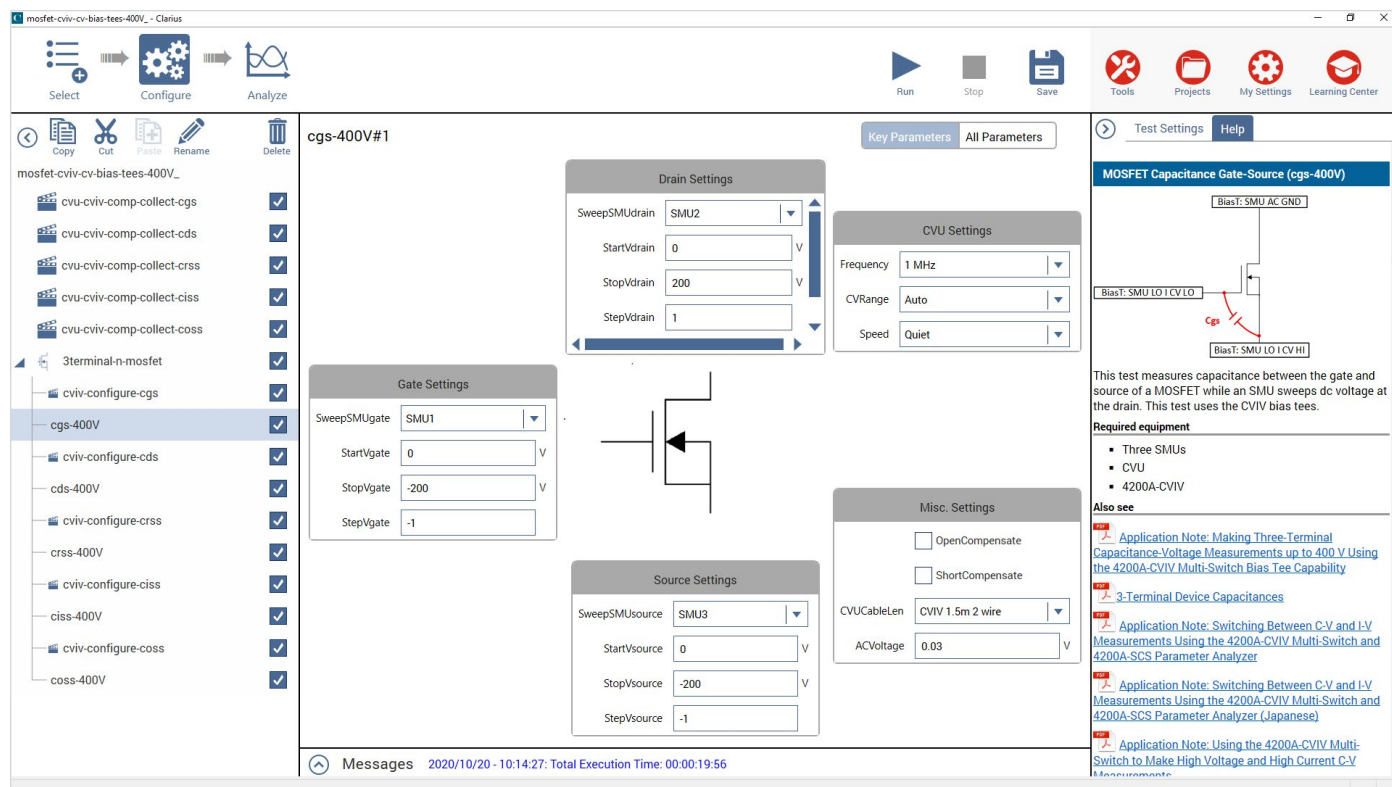


Figure 15. Project for outputting up to 400 V DC differential

Figure 15 shows the MOSFET 3-terminal C-V tests up to 400V using 4200A-CVIV Bias Tees project that uses the user module *multipleSMU_SweepV*.

The project tree is set up the same way as the previous project. All of the CVIV configuration actions, including the compensation, are done in exactly the same way. The only difference is that there are two more SMUs that must be configured. The device connections are still the same.

By default, the test should sweep from 0 to 400 V on the drain. Both the gate and source SMUs should sweep simultaneously and at the same voltage. The user is restricted when changes are made to start and stop voltages on the terminals.

The user also has the ability to change the CVU settings such as the frequency, range and speed based on the impedance of the device being tested.

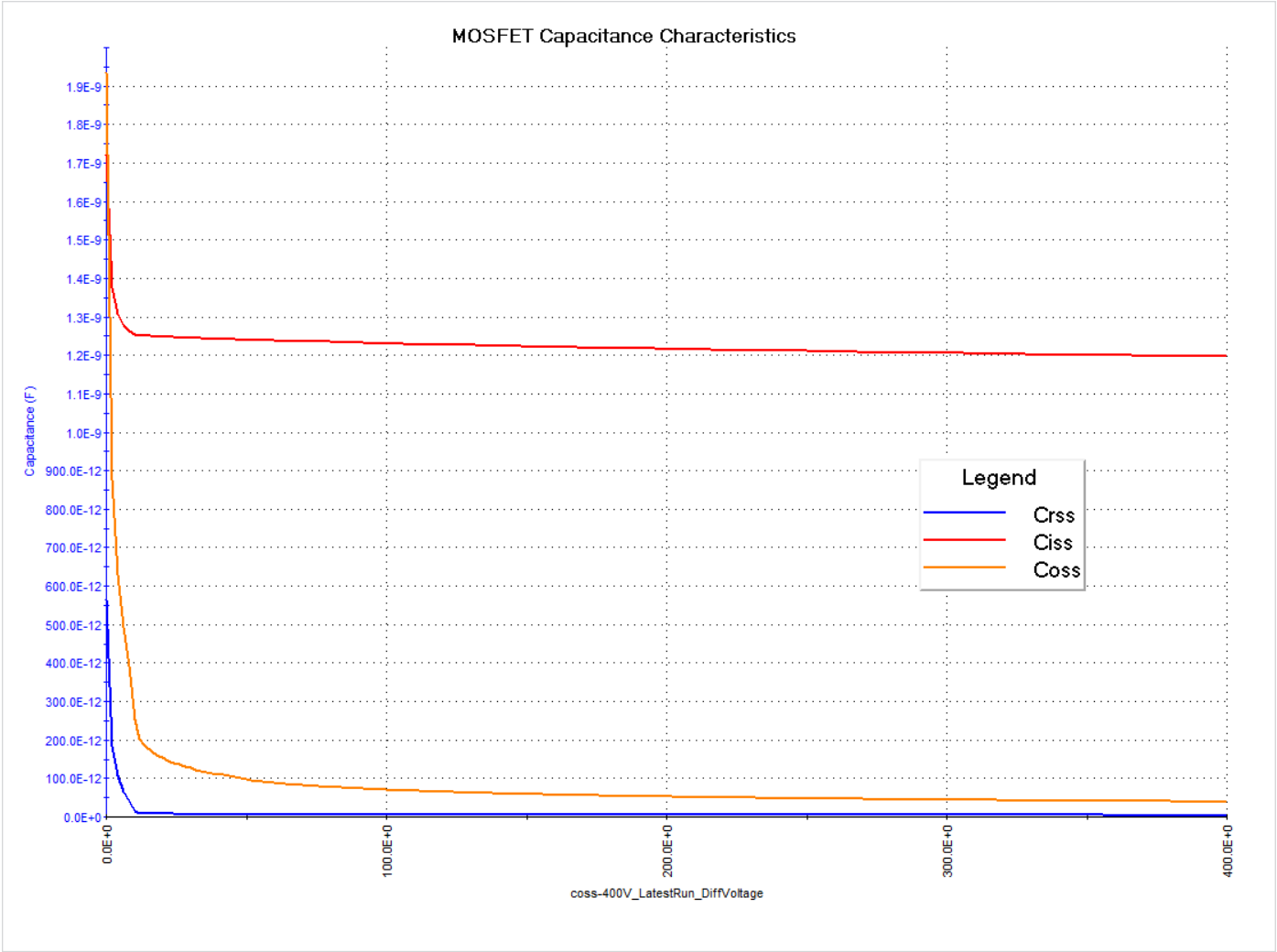


Figure 16. Capacitance characteristics of a MOSFET sweep to 400 V

Figure 16 shows the C-V sweep up to 400 V on a MOSFET generated by the 4200A-SCS. The differential voltage is a calculated value. It's the difference between the drain and the source voltages.

Run1 Formulas List									
	multipleSMU_S	Cp	Gp	Time	DrainVoltage	GateVoltage	SourceVoltage	DiffVoltage	FrequencyVal
1	0	1.7217E-9	1.0779E-3	000.0000E-3	000.0000E-3	000.0000E-3	000.0000E-3	000.0000E-3	1.0000E+6
2		1.3747E-9	682.4445E-6	1.1321E+0	1.0000E+0	-1.0000E+0	-1.0000E+0	2.0000E+0	1.0000E+6
3		1.3068E-9	618.0853E-6	2.2607E+0	2.0000E+0	-2.0000E+0	-2.0000E+0	4.0000E+0	1.0000E+6
4		1.2769E-9	591.6332E-6	3.3917E+0	3.0000E+0	-3.0000E+0	-3.0000E+0	6.0000E+0	1.0000E+6
5		1.2618E-9	579.0844E-6	4.5208E+0	4.0000E+0	-4.0000E+0	-4.0000E+0	8.0000E+0	1.0000E+6
6		1.2533E-9	572.9777E-6	5.6486E+0	5.0000E+0	-5.0000E+0	-5.0000E+0	10.0000E+0	1.0000E+6
7		1.2517E-9	571.9208E-6	6.7769E+0	6.0000E+0	-6.0000E+0	-6.0000E+0	12.0000E+0	1.0000E+6
8		1.2508E-9	571.0873E-6	7.9057E+0	7.0000E+0	-7.0000E+0	-7.0000E+0	14.0000E+0	1.0000E+6
9		1.2499E-9	570.1984E-6	9.0337E+0	8.0000E+0	-8.0000E+0	-8.0000E+0	16.0000E+0	1.0000E+6
10		1.2492E-9	569.5463E-6	10.1610E+0	9.0000E+0	-9.0000E+0	-9.0000E+0	18.0000E+0	1.0000E+6
11		1.2484E-9	568.8524E-6	11.2894E+0	10.0000E+0	-10.0000E+0	-10.0000E+0	20.0000E+0	1.0000E+6

Figure 17. Output data for the 400 V sweep

Figure 17 shows the output data, which lists the sweep voltages on the three terminals. The diffVoltage is the calculated differential voltage value.

Conclusion

Switching speeds of semiconductor devices like MOSFETs, IGBTs and BJTs are affected by the capacitance of the component itself. This application note demonstrates how using the 4200A-CVIV enables making these measurements at 200 V DC bias without the need to reconnect any cables, which reduces user error and permits automated testing. It also allows measuring circuit-level capacitances directly without going through component-level capacitances, which allows the circuit-level designer to get to the desired data faster.

Moreover, when measuring capacitance on three-terminal devices, one of the terminals is usually not included in the measurement and its capacitance could impact the overall measurement. Using a bias tee at every terminal eliminates the need for external capacitors or shorts.

We have also shown a new method to double the DC bias of the 4200A on three-terminal devices by using three SMUs sweeping simultaneously. The gate and the source SMUs sweep at the same polarity simultaneously to avoid an on-state of the device. The drain SMU will sweep the opposite polarity of the source and gate, so that the differential voltage is doubled. This supports a voltage sweep up to 400 V at the drain, which is beneficial to test higher power semiconductors such as GaN.

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