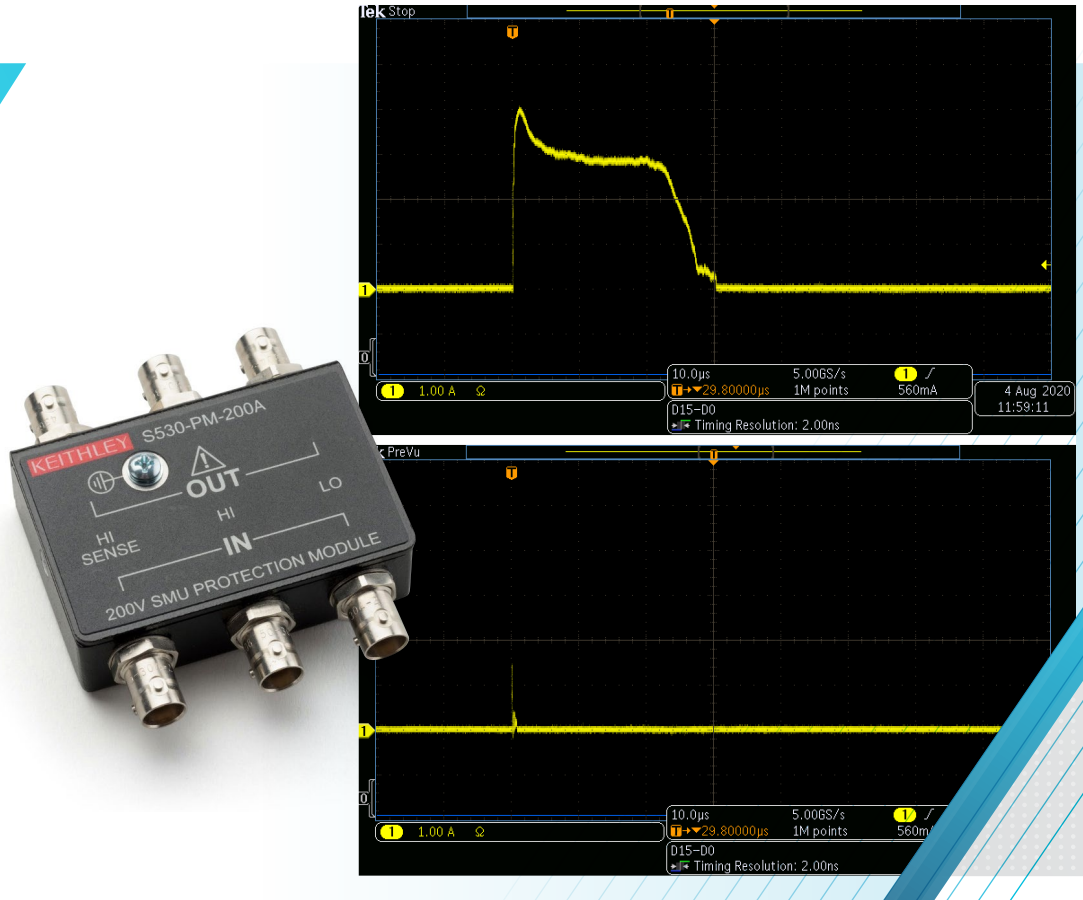
Protecting Parametric Test Systems and the Test Environment from Damaging Transient Overvoltages and Overcurrents

APPLICATION NOTE



KEITHLEY
A Tektronix Company

Tektronix®

Introduction

The demand for high quality, high reliability components based on high power semiconductor technologies such as gallium nitride (GaN) and silicon carbide (SiC) continues to grow. These components are critical to the advancement of an expanding array of applications in the automotive, 5G communications, and green energy industries, among others. To ensure the quality and reliability of these components, device manufacturers must perform a growing number of reliability tests on power semiconductor wafers in both the quality lab and the production/fabrication environment. Many of these reliability test sequences include breakdown condition tests. Measuring breakdown parameters is increasingly required to predict a device's safe region of operation. Sometimes, those breakdown conditions in reliability testing and breakdown test occur as a result of unexpected behaviors, such as a second breakdown. Physical damage to the test environment, such as a wafer burn mark, a melted probe-card needle, or other equipment damage, can also lead to breakdown problems. This application note outlines the various causes of these unexpected behaviors and how to prevent them.

Breakdown testing of power transistors

Measuring breakdown-related parameters is especially critical to characterizing the electrical parameters of power transistors. For example, in bipolar power transistors, breakdowns are controlled by three mechanisms: thermal instability, tunneling effects, and avalanche multiplication. In avalanche breakdown, a second breakdown follows the avalanche condition with increasing voltage. This second breakdown reduces the impedance of the device quickly, which then consumes a high level of current if the test system lacks a proper current-handling mechanism.

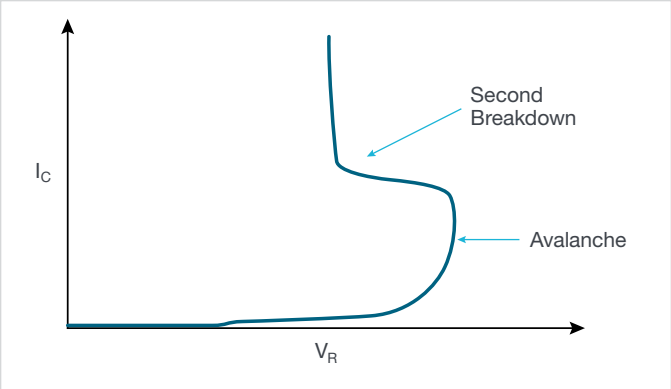


Figure 1. A second breakdown on a power transistor.

Current glitch from breakdown condition

When devices encounter hard breakdown conditions during testing, the test system can deliver unintended currents from multiple sources, many in the form of parasitic capacitances. These multiple sources can include the source measure unit (SMU) output stage, the system cables, and the switching matrix.

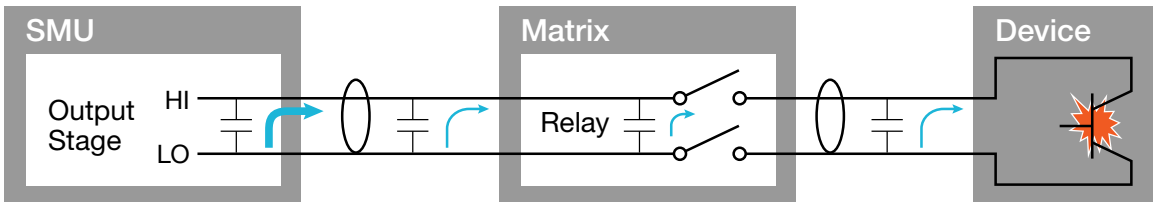


Figure 2. Sources of unintended currents that can cause glitches during breakdown testing.

As **Figure 2** illustrates, parasitic capacitances can come from multiple sources during breakdown testing. This is especially common when testing at high voltages; for example, at voltages higher than 40 V, this parasitic capacitance current can quickly exceed 10 A, which can lead to faulty matrix relay operation, melting of probe-card needles, and burned devices under test.

Figures 3 and 4 illustrate the results of current glitches from multiple parasitic capacitances. If this occurs frequently during device production test, it will lead to increased maintenance costs and decreased productivity, both of which are highly undesirable in a semiconductor production line.

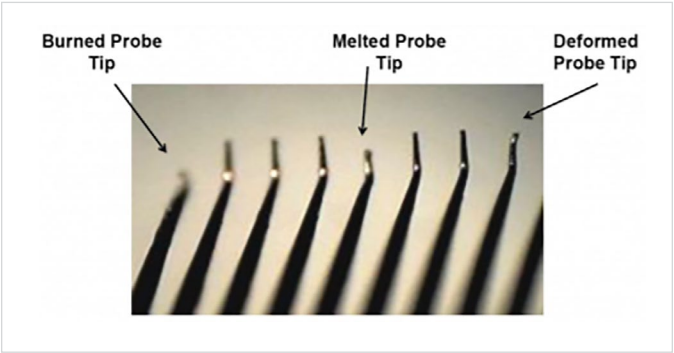


Figure 3. Probe-card needle damage.

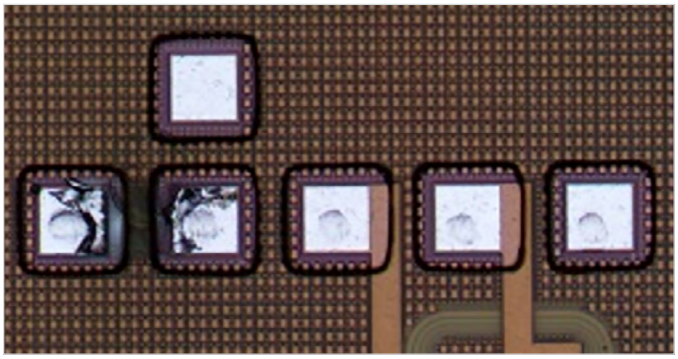


Figure 4. Wafer pad burn marks.

High voltages on standard voltage SMUs

Power devices often demand higher test output voltages than a standard SMU can supply; a normal SMU is typically limited to a maximum output voltage of 200 V. For these high voltage testing conditions, a 1000 V or 3000 V SMU can be used in conjunction with a normal 200 V SMU.

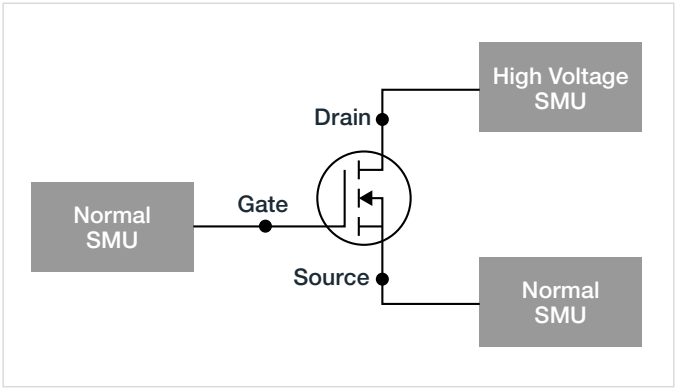


Figure 5. Mixed SMU testing configuration.

Figure 5 is a test configuration with a high voltage SMU placed only on the device's Drain. The Gate and Source are connected to normal SMUs with maximum outputs of 200 V or less. However, the design of 200 V SMUs doesn't take into account the potential for damage resulting from high voltages external to the SMU. During breakdown testing, the device under test can be destroyed and the high voltage on the Drain can seriously damage the normal SMUs connected to the Gate or Source.

An SMU's limit circuit

SMUs are widely used in semiconductor testing because they have the advantage of combining sourcing and measurement functions with a source limit function that the user can set to any desired value. Many users mistakenly believe this limit function allows an SMU to handle any unexpected overcurrents and overvoltages. In reality, in all SMU designs, the limit function cannot effectively limit a source with very fast source level changes, which can be generated when external conditions change.

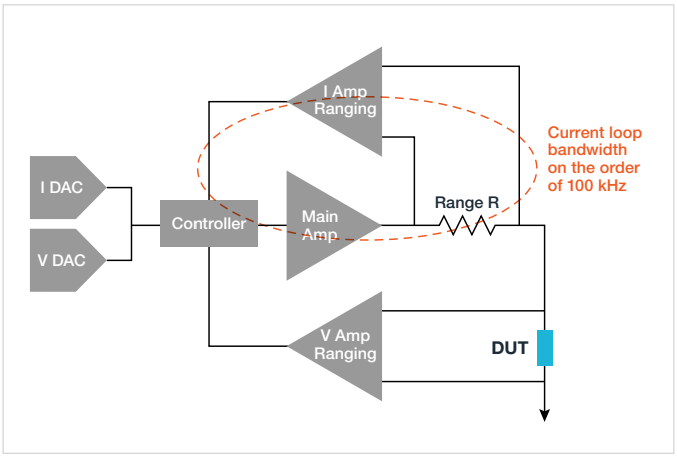


Figure 6. SMU limit circuit block diagram.

Figure 6 offers a simplified view of limit circuit in SMUs. An SMU's limit circuit can deliver an accurate limit level and adjustable limit level for multiple applications. As a result, the limit circuit function has a bandwidth that's typically >100 kHz. However, this bandwidth speed is not fast enough for transient signals in breakdown situations. The traditional approach to addressing this issue has been to add series resistors circuits to the probe card. However, given that this method can result in inaccurate parameter results when performing other types of tests, many test engineers avoid using this technique.

Transient overvoltage and overcurrent protection module

To prevent the test environment from destroying devices and damaging test equipment and to avoid the problems associated with designing and building series resistor circuits on a probe card, Keithley has developed a transient overvoltage and overcurrent protection module. This protection module offers a much faster response than an SMU's limit circuit function can. It eliminates current glitch peaks and prevents high voltages from external sources that exceed 200 V from reaching the device under test or the instrumentation. In addition, unlike a series resistor circuit on the probe card, the protection module has no impact on the accuracy of other parametric tests.

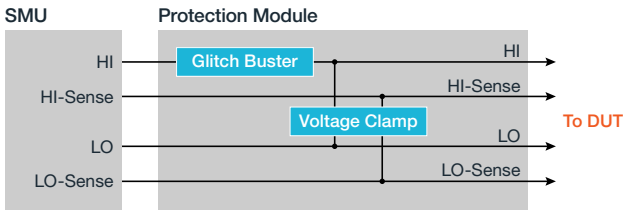


Figure 7. Protection module block diagram.

The protection module (**Figure 7**) has two major parts: the glitch buster, which is designed to prevent transient overcurrents, and the voltage clamp, which clamps external voltages in excess of 200 V. These circuits are designed to react to transient currents and voltages within a single micro-second, unlike an SMU's limit circuit, which has a bandwidth of several tens of microseconds.

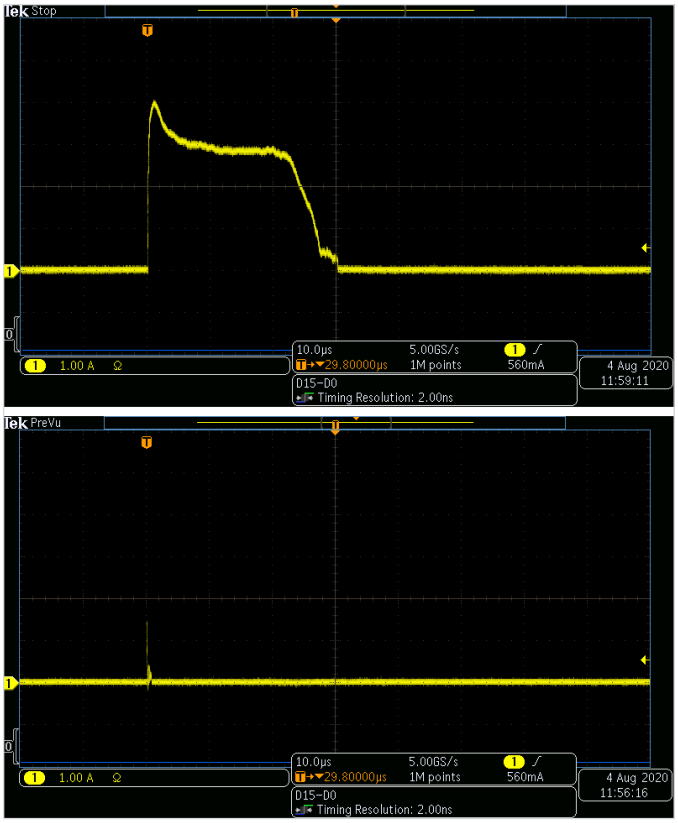


Figure 8. Transient current by shorted device without protection module (top) vs. with protection module (bottom).

Figure 8 shows a transient current when a DUT is shorted, which simulates breakdown. In the current waveform, a very high current peak (~4 A/30 µs) occurs before the limit circuit function begins working properly. This unintended peak current can be controlled by the glitch buster in the protection module. **Figure 8** shows the peak is about 4 A (30 µs) without the protection module and 1 A (<1 µs) with the protection module.

Figure 9. The S530-PM-200A is a component of Keithley's S530 Parametric Test System.

Figure 9 shows the protection module for 200 V SMUs built into the newest releases of the Keithley S530 Parametric Test Systems.

Conclusion

As the importance of reliability testing in semiconductor production rises and the demand for power semiconductors increases, parametric test systems engineers must learn how to address extreme test conditions that can lead to system and device failures, which can increase maintenance costs, system downtimes, and the cost of test. These problems can reduce profitability and delay time-to-market. With its built-in protection module for overvoltage and overcurrent, the S530 addresses these challenges.

For Further Reading

ON Semiconductor, "AN1628—Understanding Power Transistors Breakdown Parameters," https://www.onsemi.com/pub/Collateral/AN1628-D.PDF.

R. Studnicki, "What burns my probes?", IEEE SW Test Workshop, Semiconductor Wafer Test Workshop, June 9-12, 2013, San Diego, California, https://www.swtest.org/swtw_library/2013proc/PDF/SWTW13-3.pdf.

B. Zafer and B. Tunaboylu, "Experimental characterization of wafer probe burn," Turkish Journal of Electrical Engineering and Computer Science, 2016, https://pdfs.semanticscholar.org/1261/5326ea70553dd9a9e87cfc8d1b63580ed631.pdf?_ga=2.254269640.1312513917.1597713229-812659525.1597713229.

Contact Information:

Australia 1 800 709 465
Austria* 00800 2255 4835
Balkans, Israel, South Africa and other ISE Countries +41 52 675 3777
Belgium* 00800 2255 4835
Brazil +55 (11) 3759 7627
Canada 1 800 833 9200
Central East Europe / Baltics +41 52 675 3777
Central Europe / Greece +41 52 675 3777
Denmark +45 80 88 1401
Finland +41 52 675 3777
France* 00800 2255 4835
Germany* 00800 2255 4835
Hong Kong 400 820 5835
India 000 800 650 1835
Indonesia 007 803 601 5249
Italy 00800 2255 4835
Japan 81 (3) 6714 3086
Luxembourg +41 52 675 3777
Malaysia 1 800 22 55835
Mexico, Central/South America and Caribbean 52 (55) 56 04 50 90
Middle East, Asia, and North Africa +41 52 675 3777
The Netherlands* 00800 2255 4835
New Zealand 0800 800 238
Norway 800 16098
People's Republic of China 400 820 5835
Philippines 1 800 1601 0077
Poland +41 52 675 3777
Portugal 80 08 12370
Republic of Korea +82 2 565 1455
Russia / CIS +7 (495) 6647564
Singapore 800 6011 473
South Africa +41 52 675 3777
Spain* 00800 2255 4835
Sweden* 00800 2255 4835
Switzerland* 00800 2255 4835
Taiwan 886 (2) 2656 6688
Thailand 1 800 011 931
United Kingdom / Ireland* 00800 2255 4835
USA 1 800 833 9200
Vietnam 12060128

*** European toll-free number. If not accessible, call:** +41 52 675 3777

Rev. 02.2018

KEITHLEY
A Tektronix Company

Find more valuable resources at TEK.COM

092120 SBG 1KW-67745-0