100G Physical Layer Characterization and Test of 25+ Gb/s signaling in latest Ethernet and OIF CEI Standards

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1

Agenda

100G Physical Layer Characterization and Test of 25+ Gb/s signaling in latest Ethernet and OIF CEI Standards

50 Minutes:

100G Technology – An update on the standards
- Market Drivers, Common Topologies, Trends

Tx Testing Overview – Instrumentation/ Signal acquisition requirements
- Signal Decomposition
- Eye Diagram & Jitter Analysis

Rx Testing Overview – Instrumentation/ Signal generation requirements
- Pattern Generation
- Stressed Receiver Error Detection

2

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Market Drivers: (Bandwidth, Bandwidth, Bandwidth)

- The continuing drive to ever higher data rates for electrical devices is evidenced by the following emerging standards:

Standard	Description	Bit Rate
100GBASE-R4	100 Gb/s Ethernet, implemented as 4 x 25 Gb/s	• 25.78 Gb/s
SONET OTU4	100 Gb/s Telecom standard, implemented as 4 x 25 Gb/s	• 27.95 Gb/s
OIF CEI 3.0 IA	• CEI-25G-LR supports backplane interfaces up to 680 mm with two connectors • CEI-28G-SR supports chip-to-chip interfaces up to 300 mm with one connector at 28 GBaud/s	• 25 GBaud/s • 28 GBaud/s
INCITS T11.2	• 32GFC Fibre Channel	• 28.05 Gb/s

- **15 billion fixed and mobile networked devices** and machine-to-machine connections by 2015.
- By 2015, global IP Traffic will expand 4X from 20 exabytes/month to 81exabytes/month. (IEEE report). CAGR 32%
- Networked Storage Capacity will grow to 7910 exabytes by 2015 with 50% of this being accessed via Ethernet.

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System Configurations

- The 100G ecosystem is converging on a modulo 4 configuration for reasons related to scalability advances in silicon design which make 28Gb/sec SERDES a common building block.

Standard	Description	Geometry	Reach	Data Rate	BER
IEEE 802.3ba / 802.3bj	100GBASE-LR4 100GBASE-ER4	2 SM fibers	10 km 40 km	4x25.78125 Gb/s	≤ 10-12
	100GBASE-SR4*	8/12 MM fibers	≤ 10 m	4x25.78125 Gb/s	≤ 10-12
	100GBASE-CR4* 100GBASE-KR4*	4 cables, backplane	*	4x25.78125 Gb/s	≤ 10-12
OIF CEI	CEI-28G-LR/SR CEI-28G-VSR*	*N* traces on PCB	30 cm 15* cm	19.90-28.05 Gb/s	≤ 10-15
INCITS T11.2 Fibre Channel	32GFC	*8/12 MM* channels optical and 8 electrical	TBA* ~≤ 10 m	28.05* Gb/s	≤ 10-12*

- Established Electrical, SM Optical interconnects and emerging MM technology present unique opportunities test challenges.

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TX: Measurement Challenges – System Bandwidth

- For characterization purposes, one typically requires bandwidth sufficient to examine the 3rd (or ideally the 5th) harmonic of the signal acquired. Shown below are a number of the current and emerging standards, their bit rates and the required/desired bandwidth:

Standard	Bit Rate (Gb/s)	Required Bandwidth (3rd harmonic)	Desired Bandwidth (5th harmonic)
16G Fibre Channel	14.025	21 GHz	35 GHz
PCIe4.0	16.00	24 GHz	40 GHz
100GBASE-R4	25.781	39 GHz	64 GHz
CEI-28G-SR/VSR	27.975	42 GHz	70 GHz
40GBASE-FR	41.25	62 GHz	103 GHz

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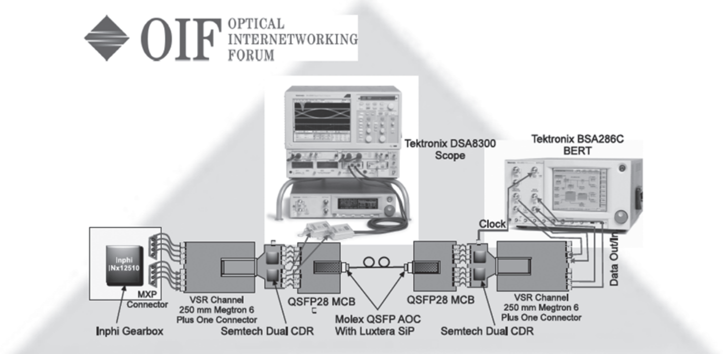
OIF CEI-28G-VSR Topology and test overview



An overview of OIF's typical 28G CFP2 Host, Channel and CFP2 Module Endpoint. The OIF 28G-VSR spec is the fundamental building block for 100GE, OTN, 32GFC and IB EDR.

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Transmitter Measurement Challenges and Instrumentation: DSA8300

- As bit rates continue to increase, the amplitudes of high bit-rate signals decreases.
- Depending on the slew-rate (i.e. rise time/signal amplitude), vertical noise can exhibit itself as additional jitter and eye closure.
- Electrical, Long and Short wavelength Optical signal acquisition.
  - 3rd harmonic of 28 Gb/s is 42 GHz; 50 GHz is desired
  - Dynamic range: VECP requires 50+ dB of dynamic range
- Jitter on Optical and Electrical signals
  - <100 to <200 fs component specifications
  - 300 fs electrical system specification
  - 400 fs optical system specification
- Concurrent Electrical and Optical Signal Capture

7

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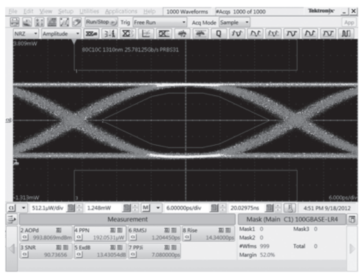
Ethernet: Measurements for 40GBASE-LR4, 100GBASE-LR4/ER4

- Similar to **10GBASE-*R** single-mode optical
- Newly defined aspects are:
  - Optical **Reference Receiver** at **19.34 GHz**; Clock Recovery at **10 MHz PLL LBW**
  - **Masks** – scaled version of 802.3ae. **New masks for 25 and 28 Gb/s** available as files from Tektronix
  - Masks – **hit ratio** of 5×10^{-5} hits per sample (0.005%); **calculation in oscilloscope math** (contact Tektronix for details)



100GBase-LR4 Mask Test DSA8300 & 80C10C-F1 Reference Receiver

8

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Document: OIF2012.290.00 **CEI Implementation Agreement Draft 7.1**

1.B.1.1 Host-to-Module transmitter output Electrical Specifications

It is recommended that each host-to-module lane meet the specifications of Table 1-9.

Table 1-9. Host-to-Module Electrical Specifications at TP0a

Parameter	Symbol	Min.	Max.	Units	Conditions
Differential Voltage, pk-pk	T_Vdiff	600	-	mV	PRBS31 pattern. Emphasis off. Note 1
Common Mode Voltage	T_Vcm	-100	1700	mV	Note 2
Differential resistance	T_Rd	80	120	ohms	
Differential resistance Mismatch	T+_Rdm	-	10	%	at 1 MHz
Differential Return Loss	T_SDD22	-	See 10.3.1.3 (CEI-28G-SR)	dB	
Transition Time: 20/80%	T_tr, T_tf	8	-	ps	Emphasis off.
Common Mode Noise, rms	T_Ncm	-	12	mV	See 12.3
Uncorrelated Unbounded Gaussian jitter	T_UUGJ	-	0.15	UI	
Uncorrelated Bounded high probability jitter	T_UBHPJ	-	0.15	UI	Note 4
Duty Cycle Distortion (component of UBHPJ)	T_DCD	-	0.035	UI	Note 5
Total Jitter	T_TJ	-	0.28	UI	Note 3

Note 1: Max voltage is limited by specifications at TP1a
Note 2: Load type 0 with min. T_Vdiff, AC-Coupling or floating load.
Note 3: T_TJ includes all of the jitter components measured without any transmit equalization
Note 4: Measured with all possible values of transmitter equalization, excluding DDJ.
Note 5: Included in T_UBHPJ

- OIF-CEI Tx specifications
  - **Complex Jitter decomposition and high dynamic range vertical noise analysis are key to current designs.**
  - **T_UBHPJ is the combination Bounded Uncorrelated Jitter (BUJ) and High Probability Bounded Jitter (PJ)**
  - **T_UUGJ is just Random Jitter (RJ) being very pedantic to eliminate BUJ from the mix which is a common problem today.**

9

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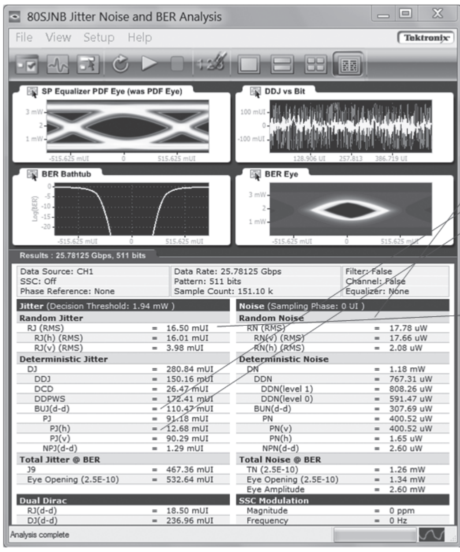

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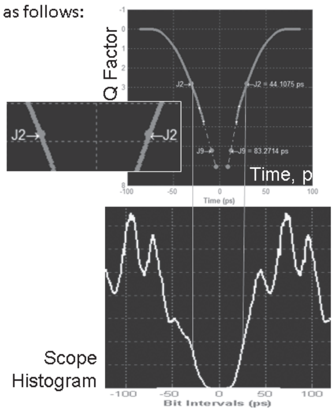
Jitter Methodology J2 and J9 Jitter

- **IEEE 802.3ba requires J2 and J9 jitter** measurements, and defines J2 and J9 as follows:
- **IEEE 802.3ba 86.8.3.3.1 J2 Jitter**

  J2 Jitter is defined as the time interval that includes all but 10^{-2} of the jitter distribution, which is the time interval from the 0.5th to the 99.5th percentile of the jitter histogram. This may be measured using an oscilloscope, or if measured by plotting BER vs. decision time, J2 is the time interval between the two points with a BER of 2.5×10^{-3}. Oscilloscope histograms should include at least 10,000 hits, and should be taken over about 1% of the signal amplitude. Test Patterns are PRBS31, Scrambled Idle, or live traffic.



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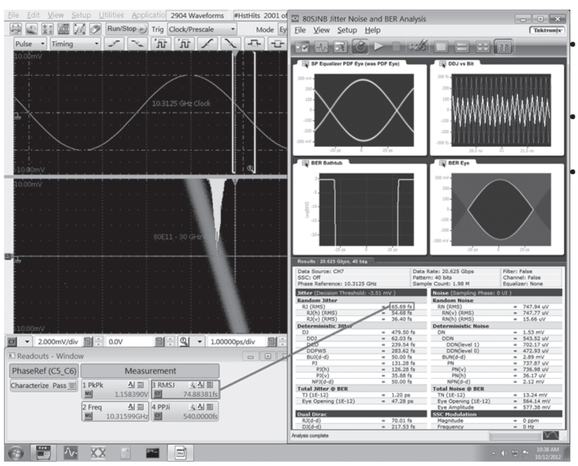
Example - Clock signal acquired with 82A04B / 80E11



- Phase Ref
  - 10.3125 GHz
  - 1.2 V
- Data Input:
  - 600 mV
- Jitter:
  - 75 fsec RMS
  - RJ = 66 fs

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Key 100G Transmitter Test Products Summary

- Enhanced phase reference module and electrical sampling modules
  - 82A04B – enhanced phase reference module that enables <100 fs instrument jitter
    - Highest performance, multi-channel, low jitter solution

  - 80E11, 80E11X1 – ultra-low jitter (85 fs RMS, typical), 70 GHz dual and single channel samplers
    - Highest bandwidth, ultra-low jitter, high fidelity signal acquisition

  - 80E07B, 80E08B, 80E09B, 80E10B – ultra-low jitter (95 fs RMS, typical) versions of the existing remote samplers
    - Remote samplers minimize aberrations due to cabling and test fixturing.
    - Select modules to meet bandwidth and noise requirements (20 GHz – 60 GHz)
    - 80E08B and 80E10B include highest performance integrated TDR capability

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Receiver Measurement Challenges and Instrumentation

- Generator jitter noise levels and specifically jitter constituent components (Rj, DDJ etc) are key to ensure the various minimum impairment levels can be achieved and full receiver margins reached.
- Error location and advanced error profiling tools to offer insights to where the signal failures occur.
- Electrical to Optical conversion process is needed at various short and long wavelengths, with a linear E/O transfer function.
- Optical to Electrical conversion systems which can operate at short and long wavelengths, with good SNR capabilities.
- Electrical and Optical BER *Measurements* to BER levels of 10e-15.

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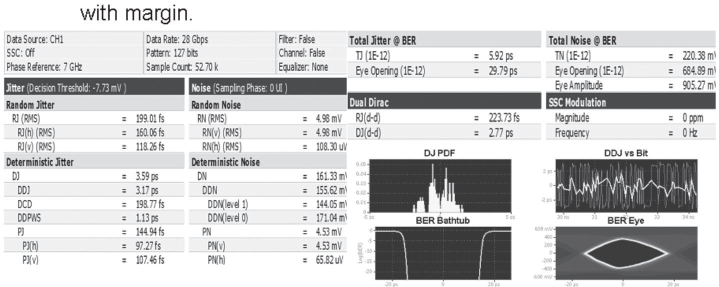
Receiver testing for High Speed DataCom at 100G Instrument Intrinsics.

- BSA286C:
  - Support for rates through 28.6G offer 3% margin over standard base spec's.
  - <350pSec RMS Rj allows following the J2 and J9 jitter intercepts with margin.

Key Comms Rates	100GBase-*R4	100GBase-*R4 (FEC)	32G Fibre-Channel	CEI
Rate	25.7813	27.7390	28.0500	28.0500
I UI (period)	38.7879	36.0500	35.6500	35.6500
Allocated Rj (UI)	0.13	0.13	0.14	0.13
Rj in Psec RMS	0.3602	0.3348	0.3565	0.3310



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Receiver testing for High Speed DataCom at 100G Receiver Configuration and Calibration

- Using 802.3ba Rx case study
- Physical Medium Dependent (PMD) sub-layer and medium, type 40GBASE–SR4 and 100GBASE–SR10
- Rx and Tx testing
- Section 86 of the 802.3ba base spec (Page 271) is our target area.

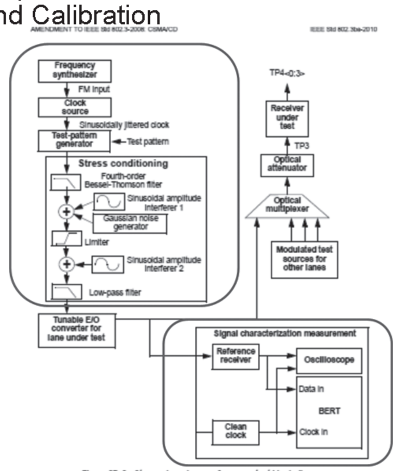

Figure 87–3—Stressed receiver conformance test block diagram

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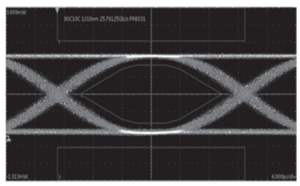
Optical Transmitter Classes (E/O systems)

- Long-Haul
- Telecom/SONET
- Line-side
- Optical Transport

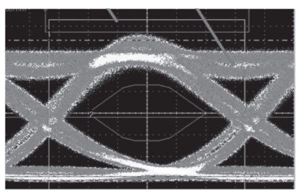
Mach-Zehnder Modulated CW driven



- High-power
- High-quality/precision alignment
- High cost
- Standards: ITU-T, OIF, 802.3 ER/LR

- Ethernet
- Storage Area Networks
- Short Range

VCSEL AM Modulated



- Low-power
- Low-quality/loose alignment
- Low cost
- Standards: T11, 802.3 SR

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Rx/Tx testing for Industrial HSSD at 28G (long λ) Receiver Configuration and Calibration

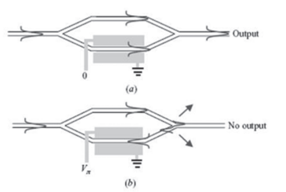


FIGURE 12.15 Mach–Zehnder interferometric modulator. If no electric field is applied on the electrodes, the input light exits from the output. When a specific voltage is applied, the output becomes zero.

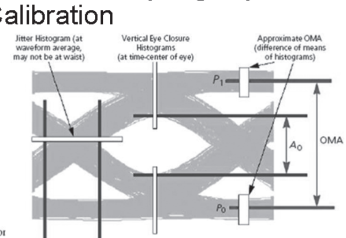
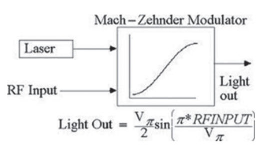


Figure 4. Stressed-Eye Measurement Points as Defined in IEEE 802.3ae



1310nm: optimal dispersion, sub-optimal loss.
1550nm: sub-optimal dispersion, optimal loss.

Instrument grade modulation uses MZ based systems for linearity and precision.

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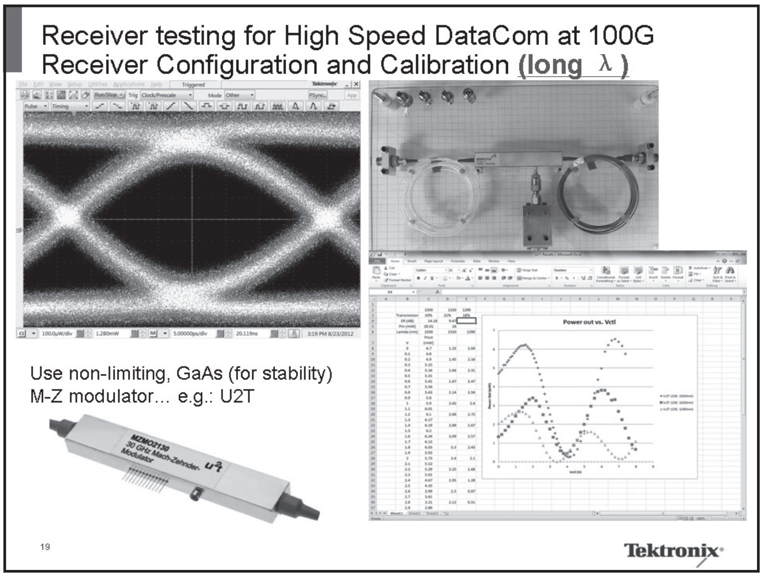
Receiver testing for High Speed DataCom at 100G
Receiver Configuration and Calibration (long λ)
Use non-limiting, GaAs (for stability)
M-Z modulator… e.g.: U2T
MZM02130
30 GHz Mach-Zehnder-Modulator
Power out vs. Vctl
19
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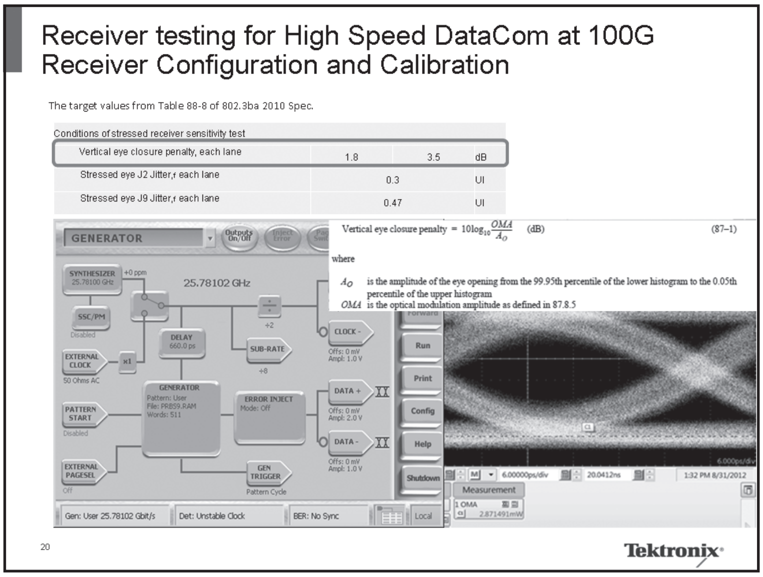
Receiver testing for High Speed DataCom at 100G
Receiver Configuration and Calibration
The target values from Table 88-8 of 802.3ba 2010 Spec.
Conditions of stressed receiver sensitivity test
Vertical eye closure penalty, each lane 1.8 3.5 dB
Stressed eye J2 Jitter, each lane 0.3 UI
Stressed eye J9 Jitter, each lane 0.47 UI
Vertical eye closure penalty = 10log10 OMA/AO (dB) (87–1)
where
AO is the amplitude of the eye opening from the 99.95th percentile of the lower histogram to the 0.05th percentile of the upper histogram
OMA is the optical modulation amplitude as defined in 87.8.5
GENERATOR
SYNTHESIZER 25.78100 GHz
25.78102 GHz
SSC/PM
DELAY 660.0 ps
SUB-RATE
EXTERNAL CLOCK
50 Ohms AC
CLOCK -
DATA +
DATA -
GENERATOR Pattern: User File: PRBS9.RAM Words: 511
ERROR INJECT Mode: Off
PATTERN START
EXTERNAL PAGESEL
GEN TRIGGER
Run
Print
Config
Help
Shutdown
Gen: User 25.78102 Gbit/s
Det: Unstable Clock
BER: No Sync
Local
Measurement
OMA
2.871491mW
20
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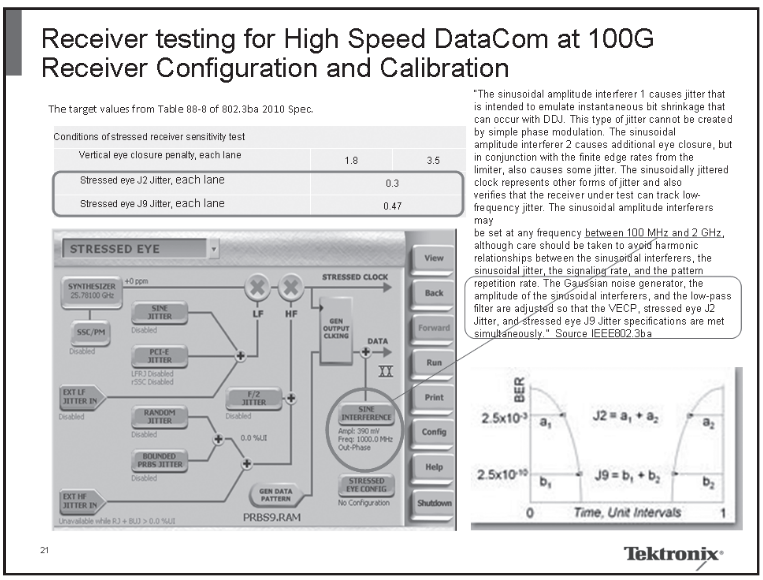
Receiver testing for High Speed DataCom at 100G
Receiver Configuration and Calibration
The target values from Table 88-8 of 802.3ba 2010 Spec.
Conditions of stressed receiver sensitivity test
Vertical eye closure penalty, each lane 1.8 3.5
Stressed eye J2 Jitter, each lane 0.3
Stressed eye J9 Jitter, each lane 0.47
"The sinusoidal amplitude interferer 1 causes jitter that is intended to emulate instantaneous bit shrinkage that can occur with DDJ. This type of jitter cannot be created by simple phase modulation. The sinusoidal amplitude interferer 2 causes additional eye closure, but in conjunction with the finite edge rates from the limiter, also causes some jitter. The sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferers may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferers, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The Gaussian noise generator, the amplitude of the sinusoidal interferers, and the low-pass filter are adjusted so that the VECP, stressed eye J2 Jitter, and stressed eye J9 Jitter specifications are met simultaneously." Source IEEE802.3ba
STRESSED EYE
SYNTHESIZER 25.78100 GHz
SSC/PM
SINE JITTER
PCI-E JITTER
EXT LF JITTER IN
RANDOM JITTER
BOUNDED PRBS JITTER
EXT HF JITTER IN
F/2 JITTER
STRESSED CLOCK
GEN OUTPUT CLKING
DATA
SINE INTERFERENCE
STRESSED EYE CONFIG
GEN DATA PATTERN
PRBS9.RAM
View
Back
Forward
Run
Print
Config
Help
Shutdown
BER
2.5x10-3
2.5x10-10
J2 = a1 + a2
J9 = b1 + b2
Time, Unit Intervals
21
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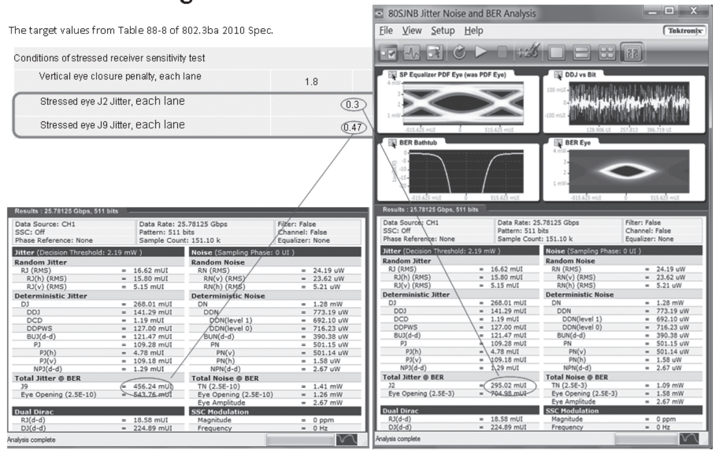
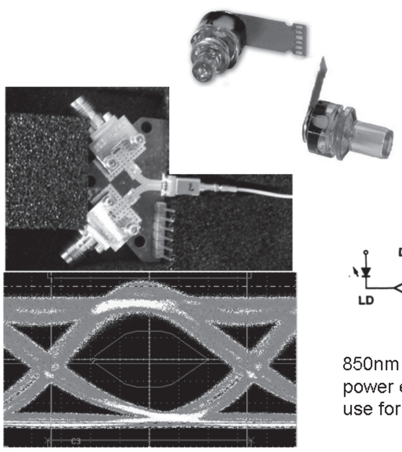
Receiver testing for High Speed DataCom at 100G
Receiver Configuration and Calibration

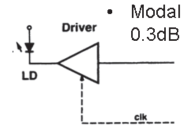


22

Receiver testing for High Speed DataCom (short λ)
Receiver Configuration and Calibration (650-1300nm)



FEC: Q=4.3, targeting BER < E-12 after FEC.
Data rate = 25781 MBd, Power budget = 8.0 dB
Transmitter
- Power OMA = -2dBm
- RIN (OMA) = -128dB/Hz
- DJ = 8.56ps;
- DCD_DJ = 2.14ps.
- MPN k(OMA) = 0.3;
- Modal Noise Penalty = 0.3dB

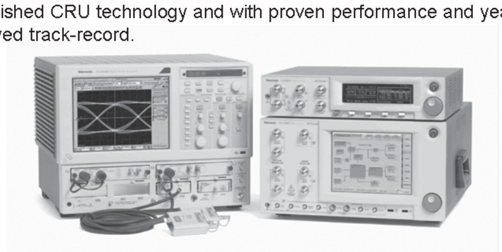


850nm VCSELs are cheap, small and power efficient so they are the best to use for short-reach data com.

23

Receiver testing for High Speed DataCom at 100G
Summary

- The BERTScope instrument has to have low ~350fSec intrinsic Rj to have a solution which can simultaneously intercept the J2/J9 spec points.
- VECP requires high fidelity signal integrity. High Vertical noise will never permit convergence on the require 1.8dB VECP values.
- One Sampling Instrument can perform simultaneous optical, single and multi-channel electrical with Bandwidth and Noise floor levels well in excess of most margin needs.
- Established CRU technology and with proven performance and years of a deployed track-record.



24

Backup

25

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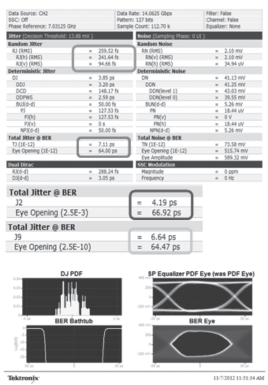
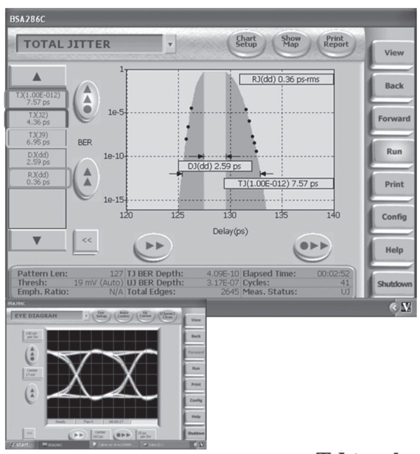
Jitter J2/J9 comparisons between BSA286C and DSA8300 with 80E10 remote sampler (60GHz) 14.06Gbps





26

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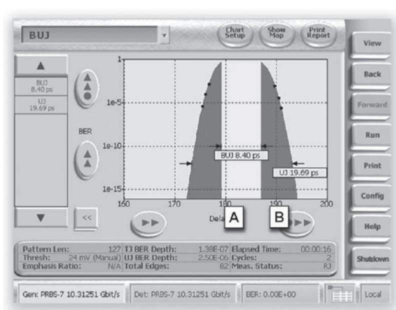
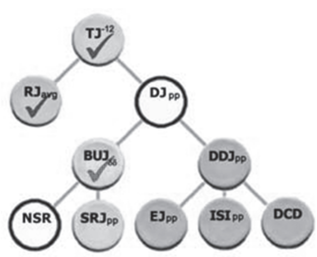
BERTScope Bounded Uncorrelated Jitter *Measurements*

- Classification of Rj and BUJ requires deep analysis into the lower probability regions of the cumulative PDF of isolated bits.
- At higher probabilities, the Truncated Gaussian nature of BUJ and Rj are in-distinguishable.





27

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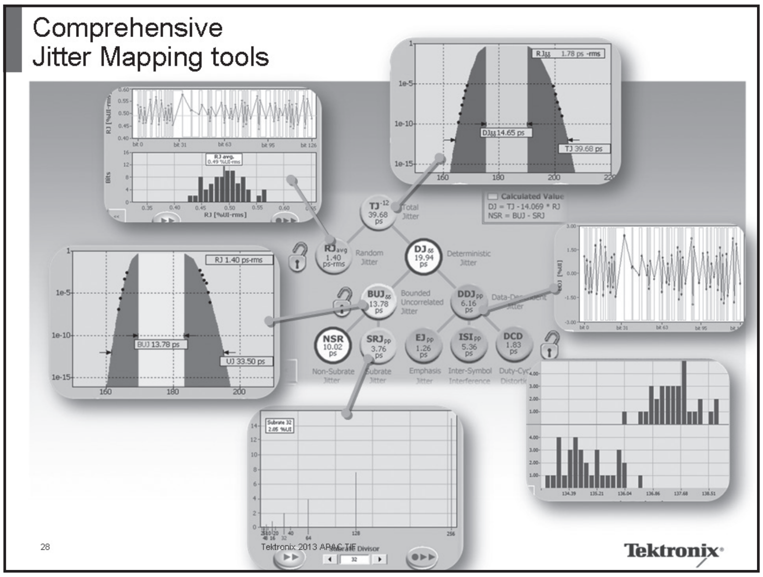
Comprehensive
Jitter Mapping tools
RJ 1.40 ps-rms
BUJ 13.78 ps
UJ 33.50 ps
DJ 14.65 ps
TJ 39.68 ps
RJ 1.78 ps-rms
Calculated Value
DJ = TJ - 14.069 * RJ
NSR = BUJ - SRJ
TJ 39.68 ps Total Jitter
RJ 1.40 ps-rms Random Jitter
DJ 19.94 ps Deterministic Jitter
BUJ 13.78 ps Bounded Uncorrelated Jitter
DDJ 6.16 ps
NSR 10.02 ps Non-Subrate Jitter
SRJ 3.76 ps
EJ 1.26 ps Emphasis Jitter
ISI 5.36 ps Inter-Symbol Interference
DCD 1.83 ps
28
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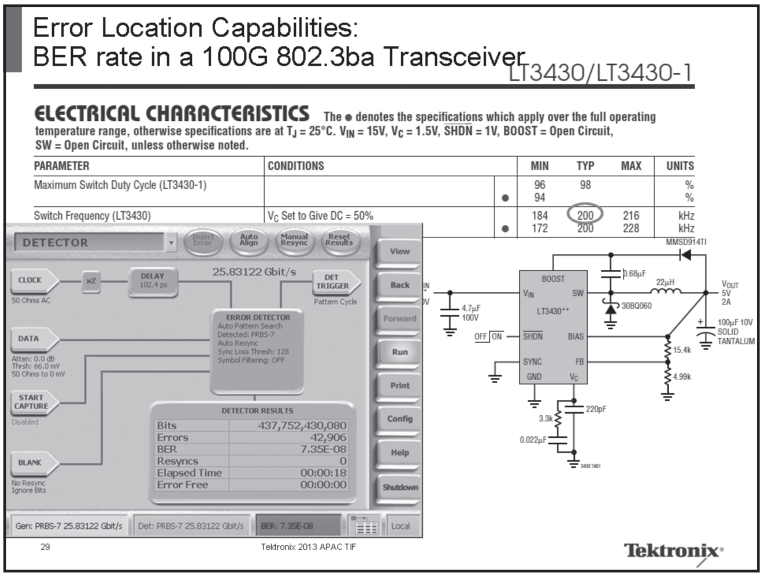
Error Location Capabilities:
BER rate in a 100G 802.3ba Transceiver
LT3430/LT3430-1
ELECTRICAL CHARACTERISTICS
PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS
Maximum Switch Duty Cycle (LT3430-1) | 96 | 98 | %
94 | %
Switch Frequency (LT3430) | VC Set to Give DC = 50% | 184 | 200 | 216 | kHz
172 | 200 | 228 | kHz
DETECTOR
25.83122 Gbit/s
ERROR DETECTOR
Auto Pattern Search
Detected: PRBS-7
DETECTOR RESULTS
Bits 437,752,430,080
Errors 42,906
BER 7.35E-08
Resyncs 0
Elapsed Time 00:00:18
Error Free 00:00:00
Gen: PRBS-7 25.83122 Gbit/s
Det: PRBS-7 25.83122 Gbit/s
BER: 7.35E-08
29
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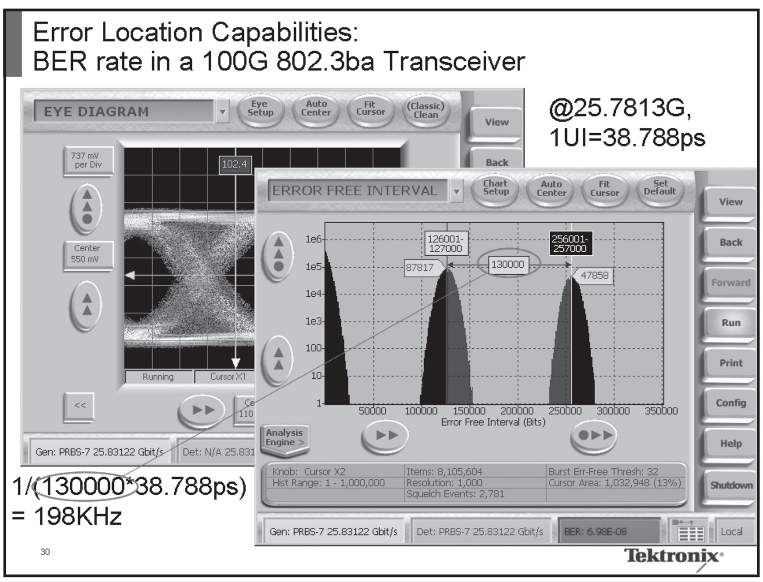
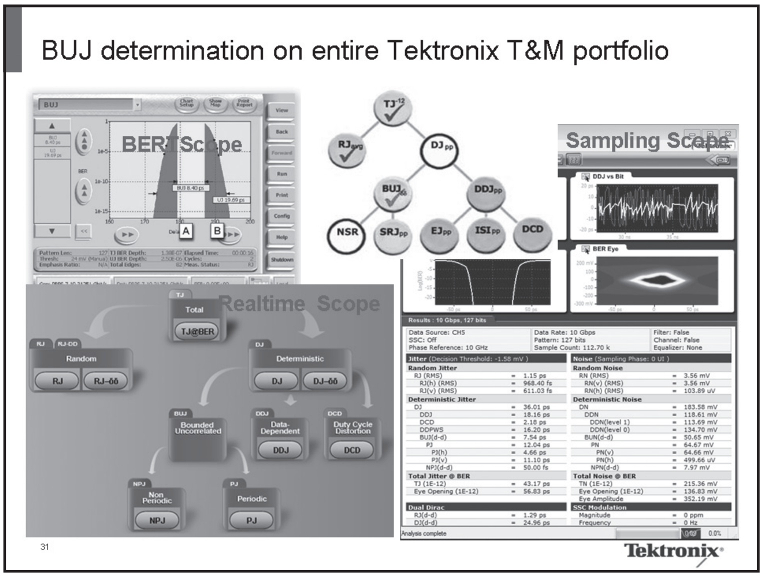

Error Location Capabilities:
BER rate in a 100G 802.3ba Transceiver
@25.7813G,
1UI=38.788ps
EYE DIAGRAM
ERROR FREE INTERVAL
126001-127000
256001-257000
87817
130000
47858
Error Free Interval (Bits)
Gen: PRBS-7 25.83122 Gbit/s
Det: PRBS-7 25.83122 Gbit/s
BER: 6.98E-08
1/(130000*38.788ps)
= 198KHz
30
Tektronix


BUJ determination on entire Tektronix T&M portfolio
BERTScope
Sampling Scope
Realtime Scope
TJ
RJ
DJ
BUJ
DDJ
NSR
SRJ
EJ
ISI
DCD
Total
TJ@BER
Random
Deterministic
Bounded Uncorrelated
Data-Dependent
Duty Cycle Distortion
Non Periodic
Periodic
NPJ
PJ
31
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