Explore BERTScope's Benefit In High Speed Serial Data

SYNTHESYS RESEARCH, INC.

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Agenda

- BERTScope In High Speed Serial Data
- USB 3.0 Compliance Testing
- SATA Compliance Testing
- PCIE Rx & PLL Loop bandwidth Testing
- One Stop Shopping for HSSD from Tektronix

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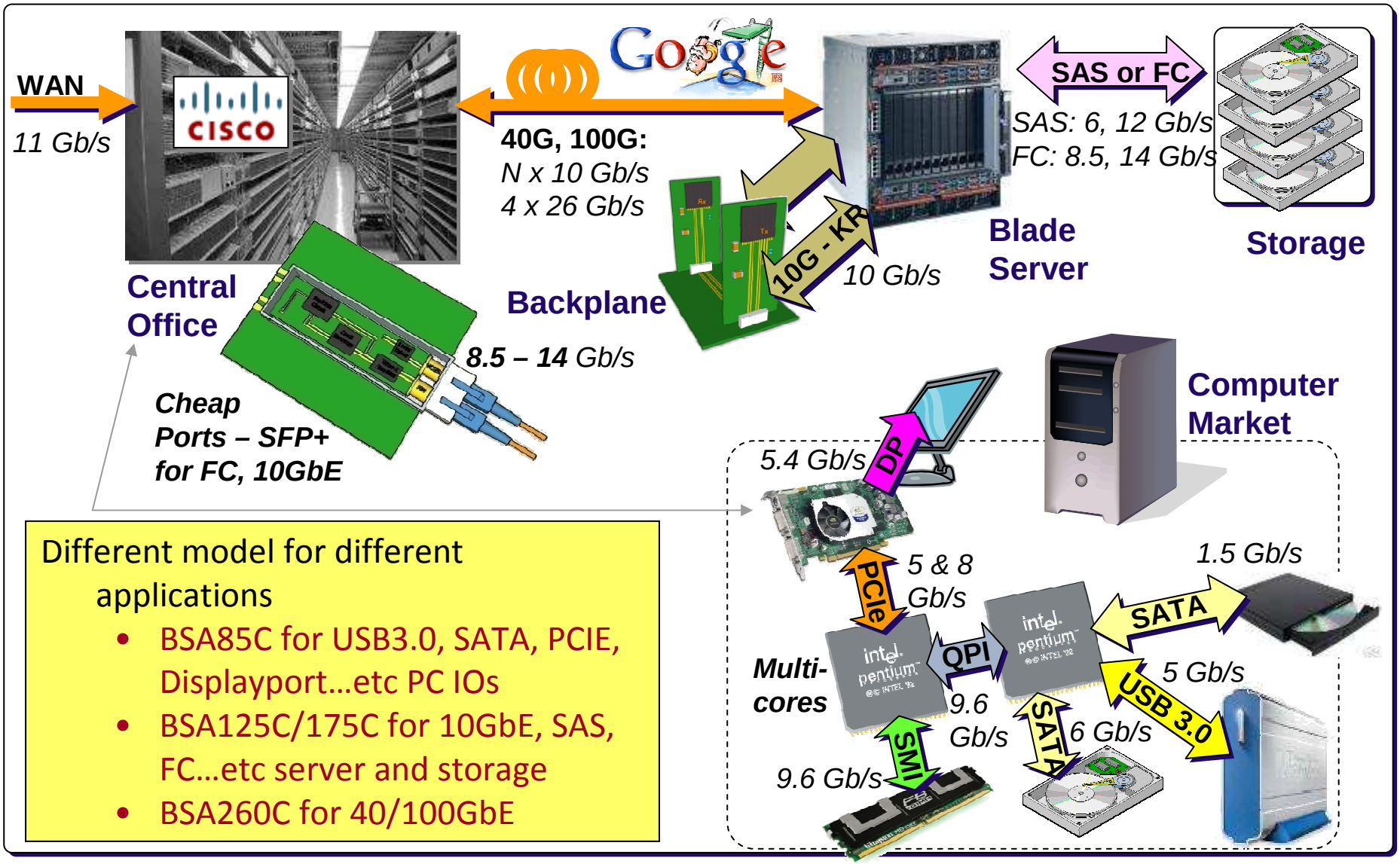
BERTScope's Applications In High Speed Serial Data



Different model for different applications

- BSA85C for USB3.0, SATA, PCIE, Displayport…etc PC IOs
- BSA125C/175C for 10GbE, SAS, FC…etc server and storage
- BSA260C for 40/100GbE

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USB 3.0 Rx Compliance Testing

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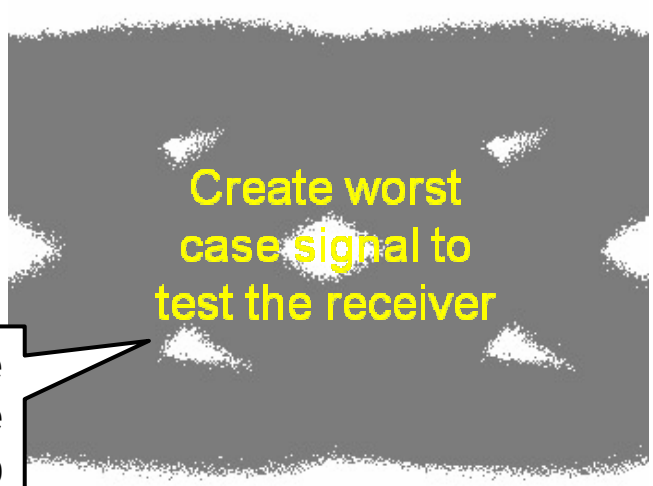
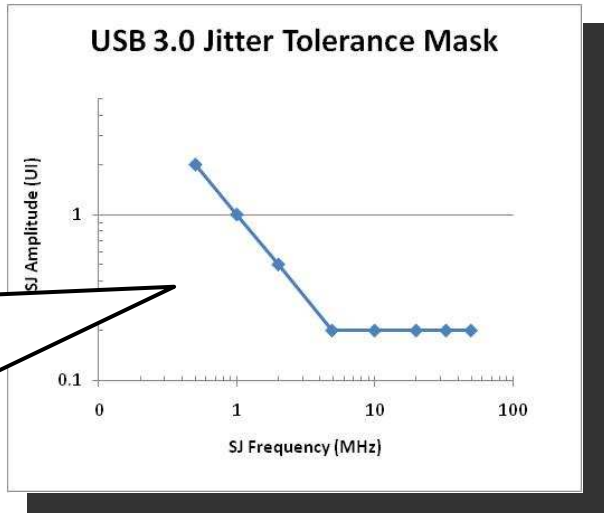
USB 3.0
Receiver Test Flowchart



Only needs to be performed once per setup

Test receiver with stressed eye and added sinusoidal jitter (SJ) in Jitter Tolerance template



Stressed Eye Calibration

1. Setup Equipment
2. Adjust RJ
3. Adjust SJ
4. Measure TJ
5. Adjust Eye Height

Jitter Tolerance

1. Setup Equipment
2. Loopback Initiation
3. Jitter Tolerance

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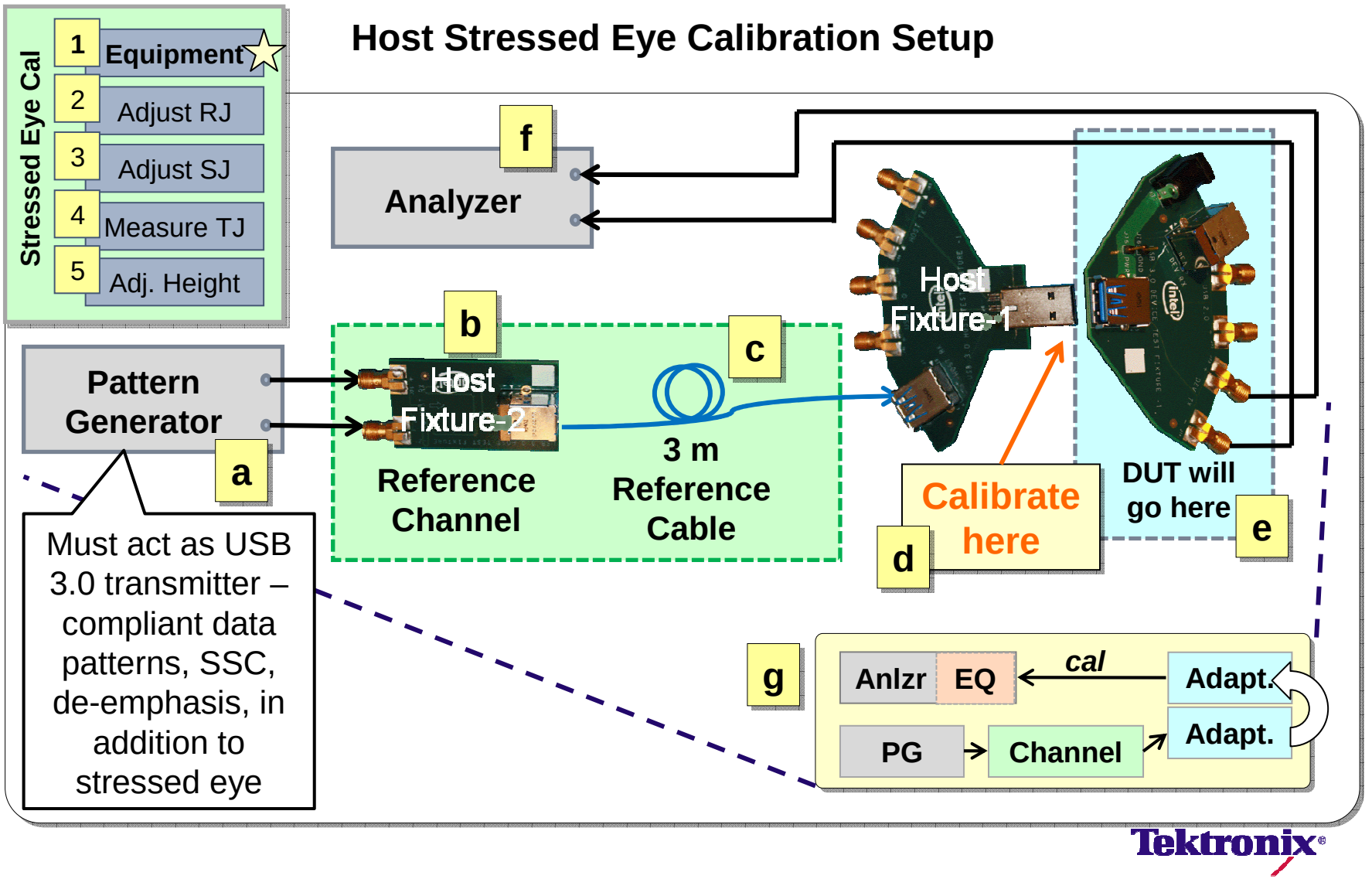
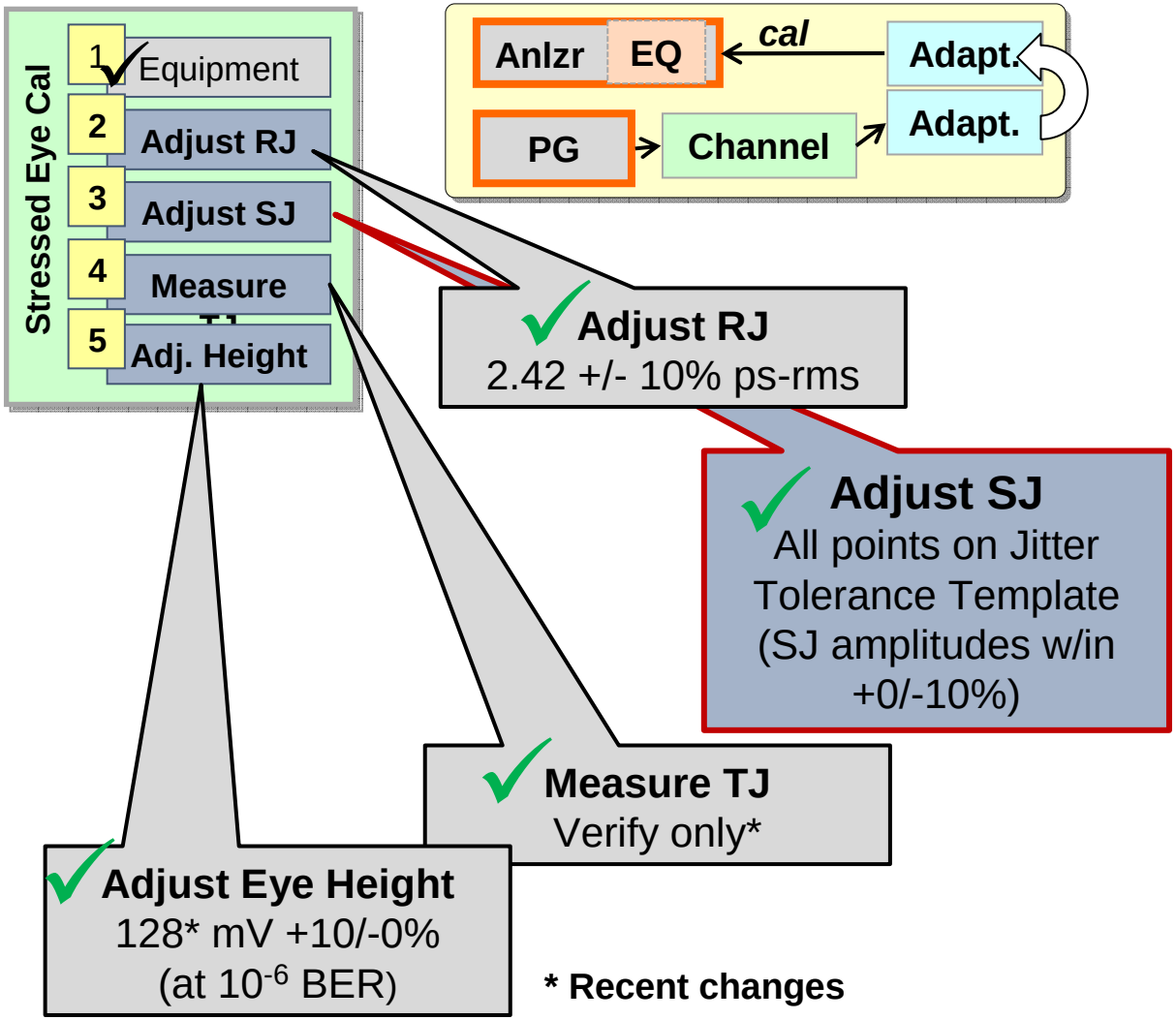
USB 3.0 Stressed Eye Calibration Equipment Setup



USB 3.0 Stressed Eye Calibration
Jitter and Eye Height



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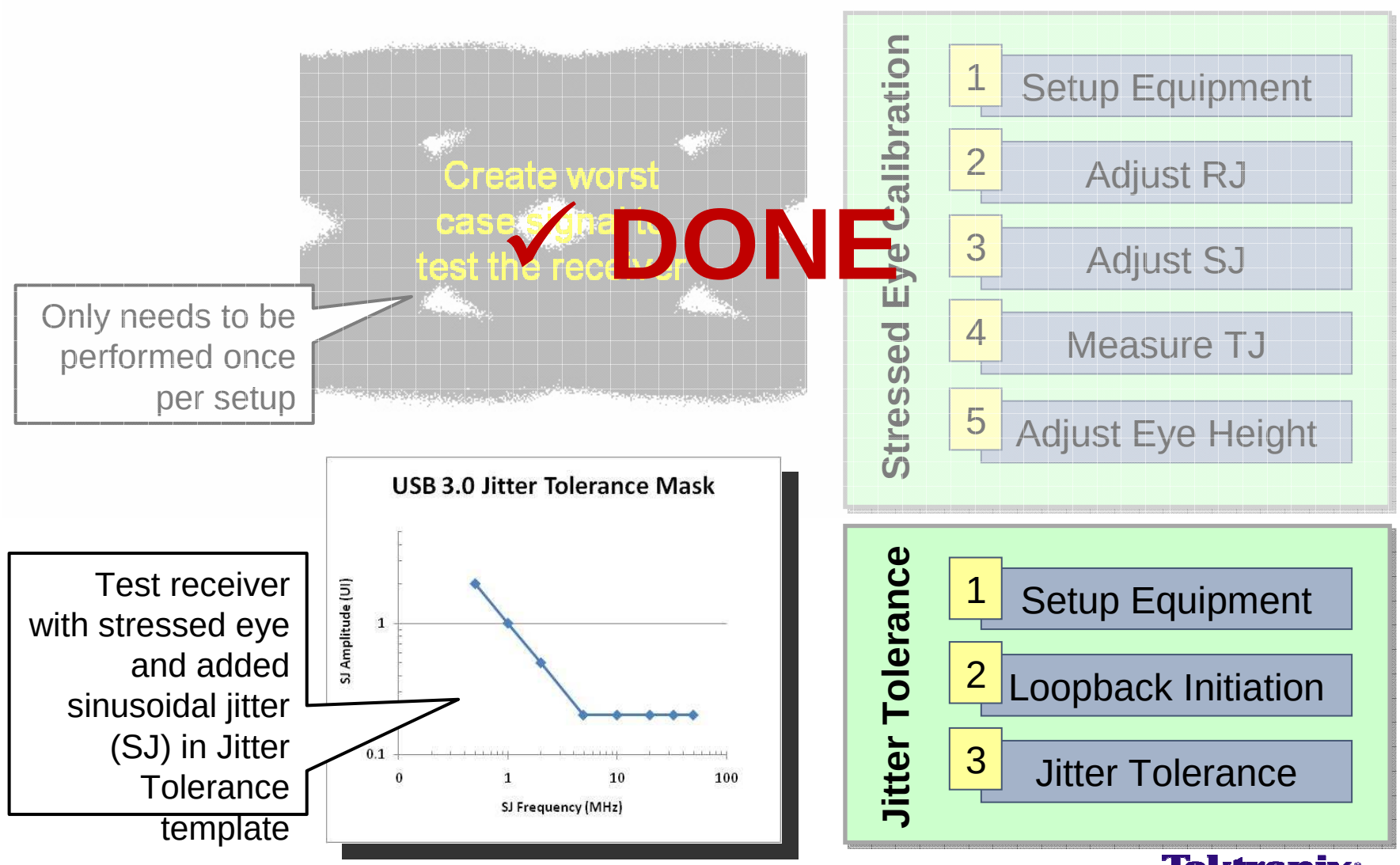
USB 3.0
Receiver Test Flowchart



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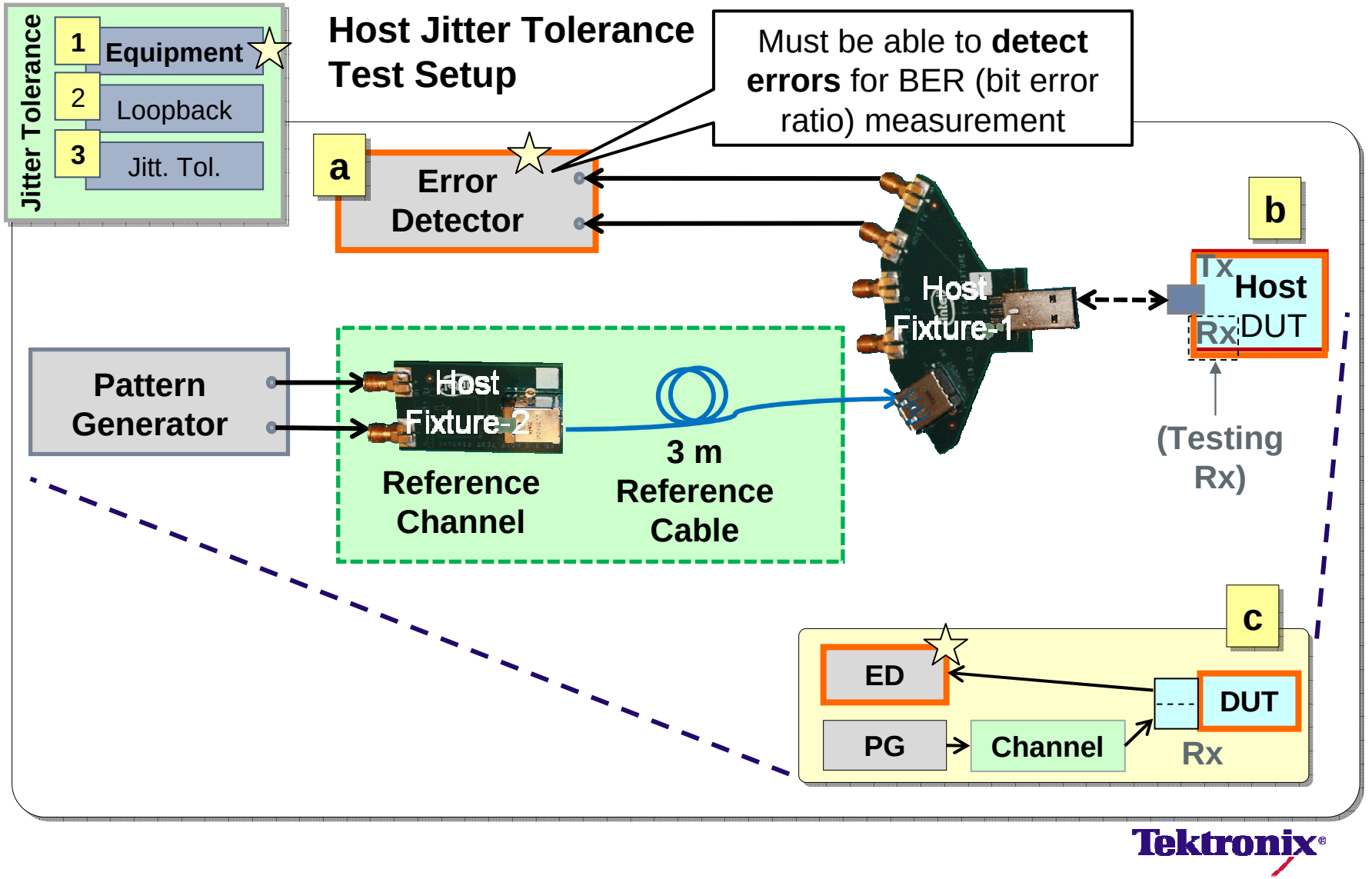
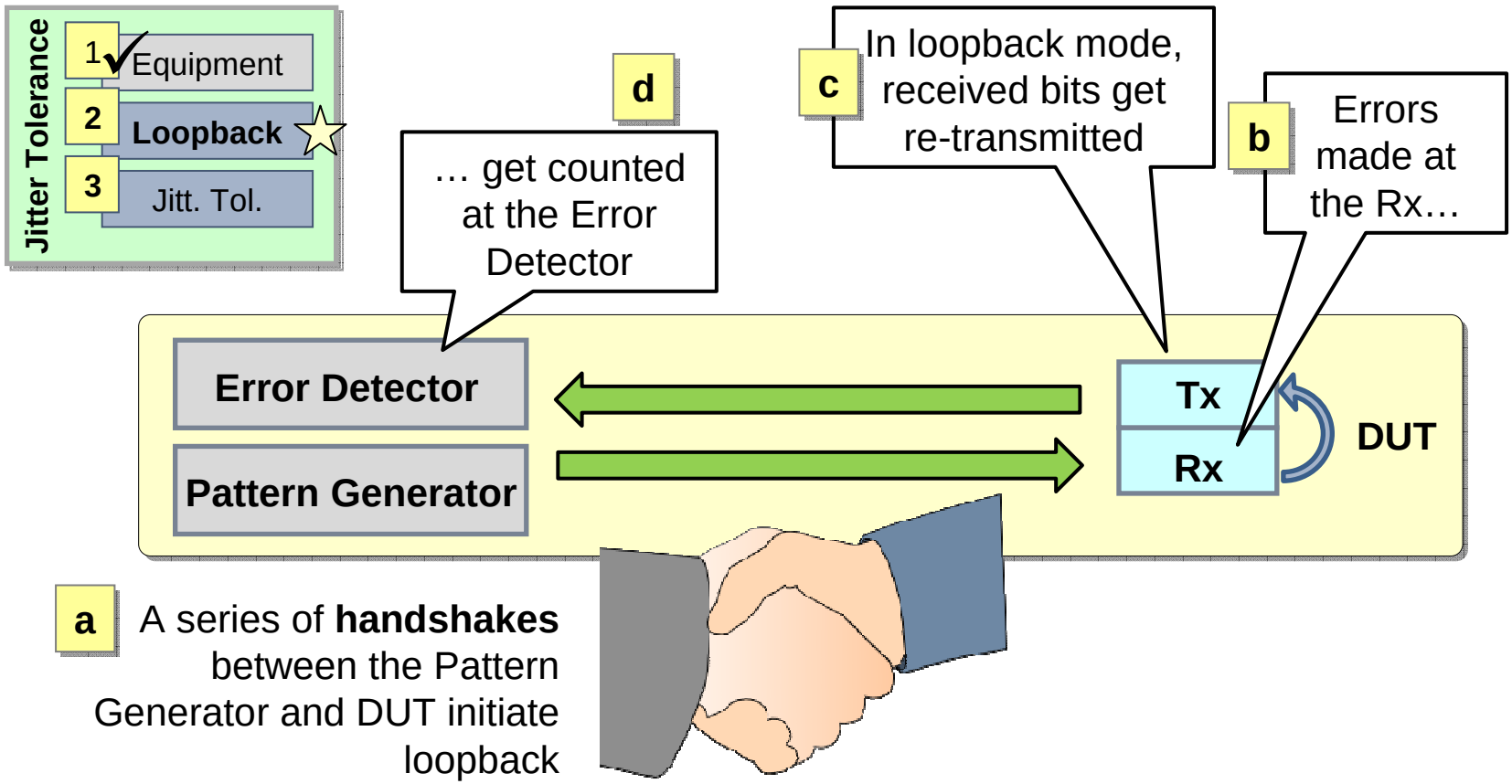
USB 3.0 Jitter Tolerance Testing
Equipment Setup



USB 3.0 Jitter Tolerance Testing
Loopback Initiation



e

Notes:

1.Once in loopback, the DUT should not exit loopback unless directed

2."Loopback BER", where the DUT keeps track of its own BER, is not required for compliance testing

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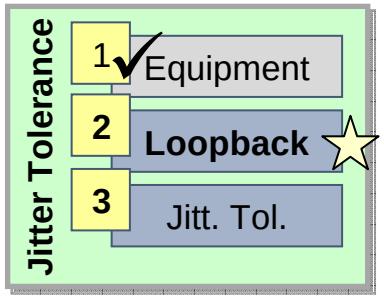
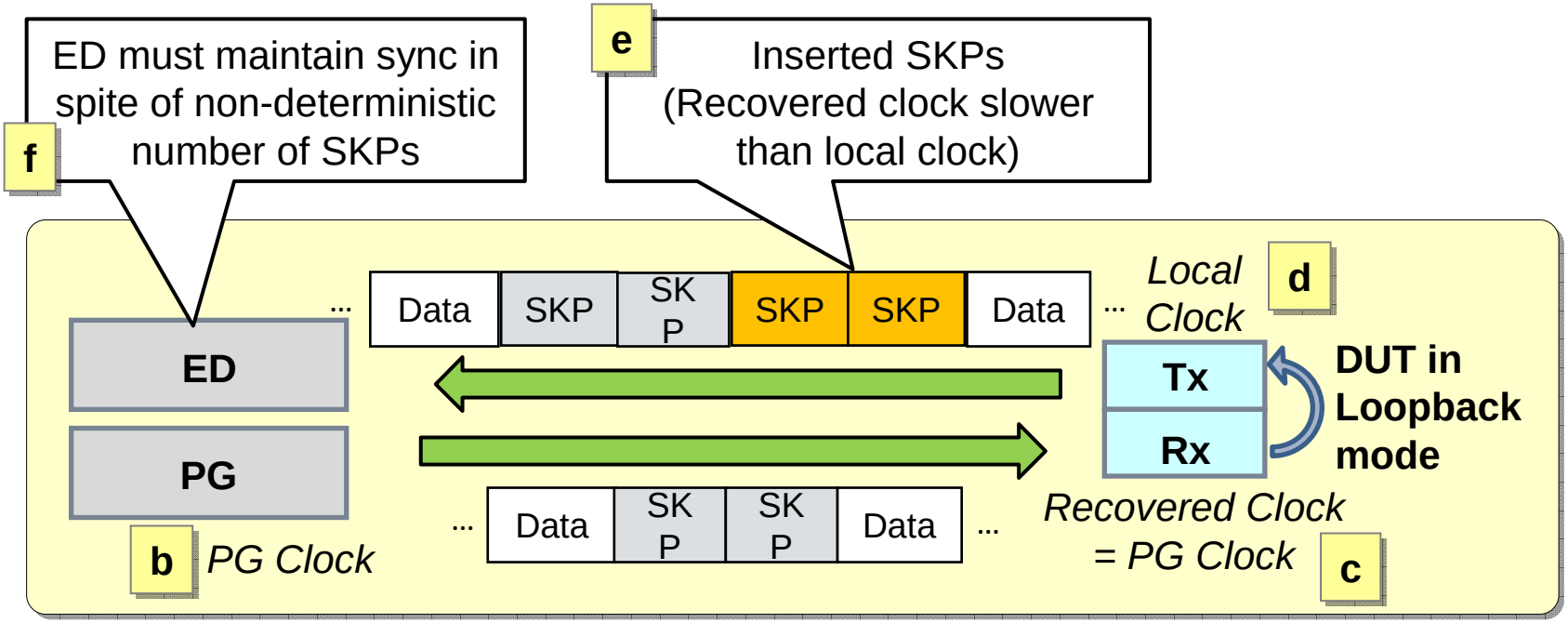
USB 3.0 Jitter Tolerance Testing
Asynchronous BER Testing



a

Clock compensation symbols (SKPs) are used to adjust for the differing clock frequencies in the received data vs. the transmitter (common in 8b/10b systems)



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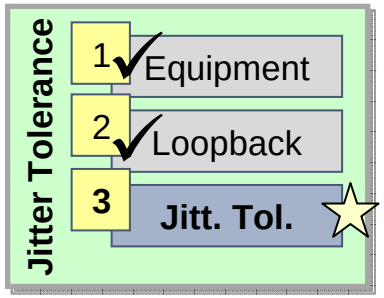
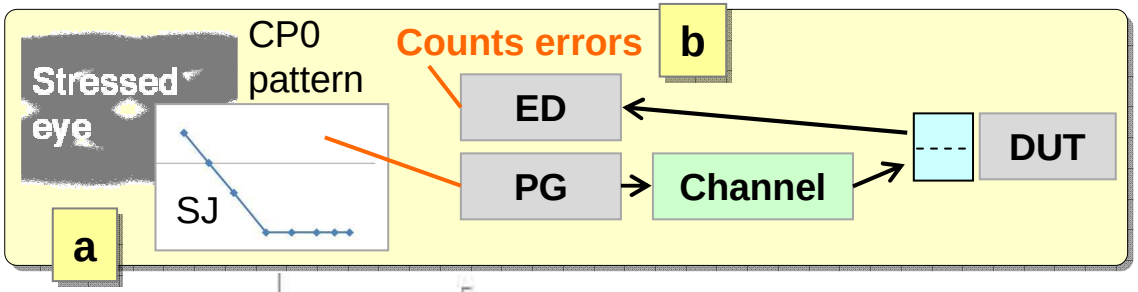
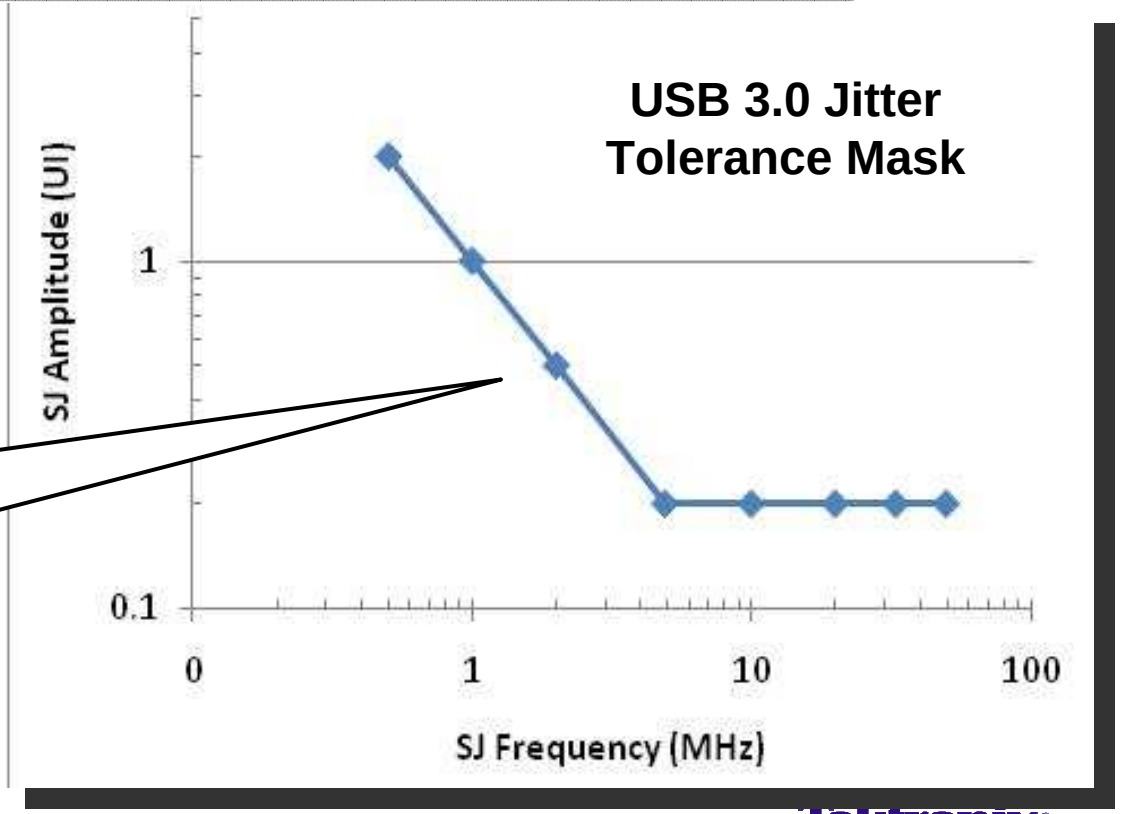
USB 3.0
Run Jitter Tolerance







Test each point with **$3x10^{10}$ bits.** The DUT fails if one or more errors is found or if it loses bit lock.

c

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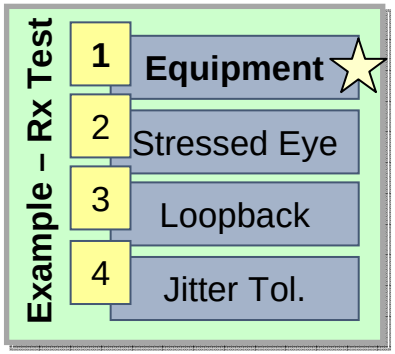
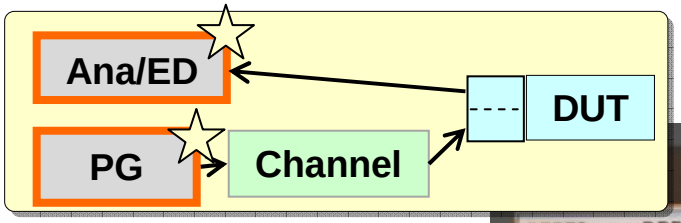
USB 3.0
BERTScope Instrumentation

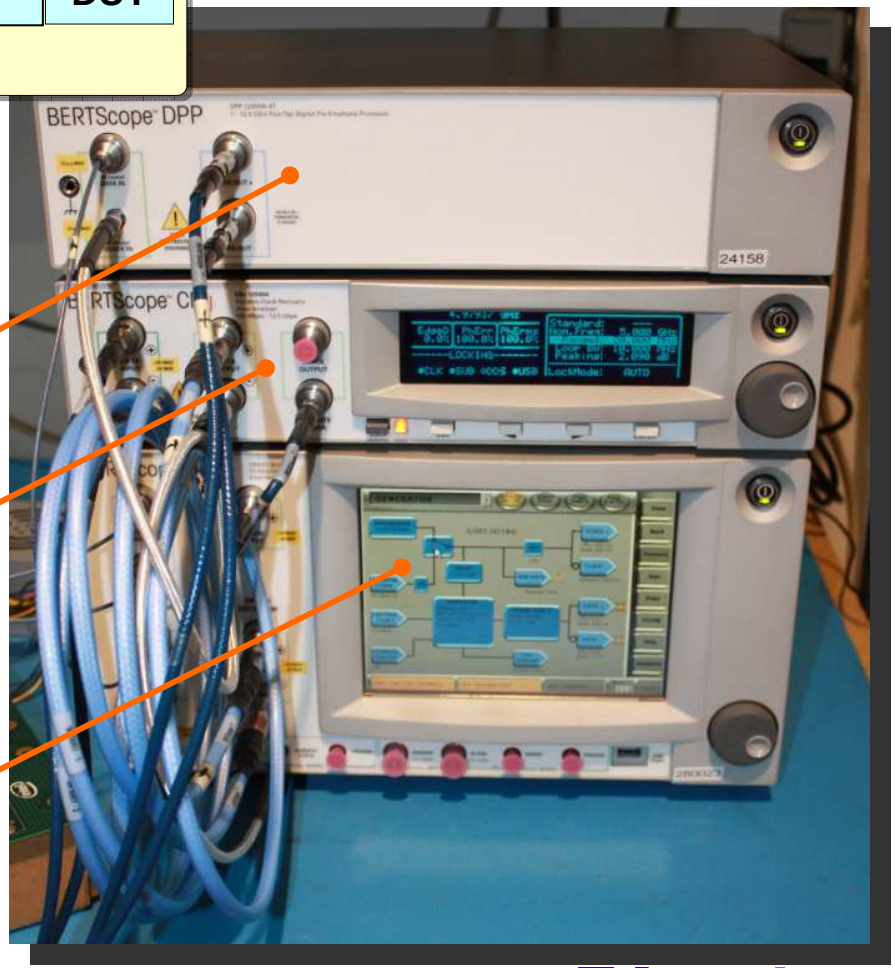




BERTScope DPP (3 and 4 tap) for **compliant 3 dB de-emphasis**

BERTScope CR 125A with Extended Loop Bandwidth Option for **compliant JTF**

BERTScope 85C for integrated **stressed pattern generation** (**RJ, SJ,** and **SSC**) and **BER analysis** including **jitter**, **eye height**, **CTLE** emulation, **asynchronous BER testing** and automated **Jitter Tolerance** testing.



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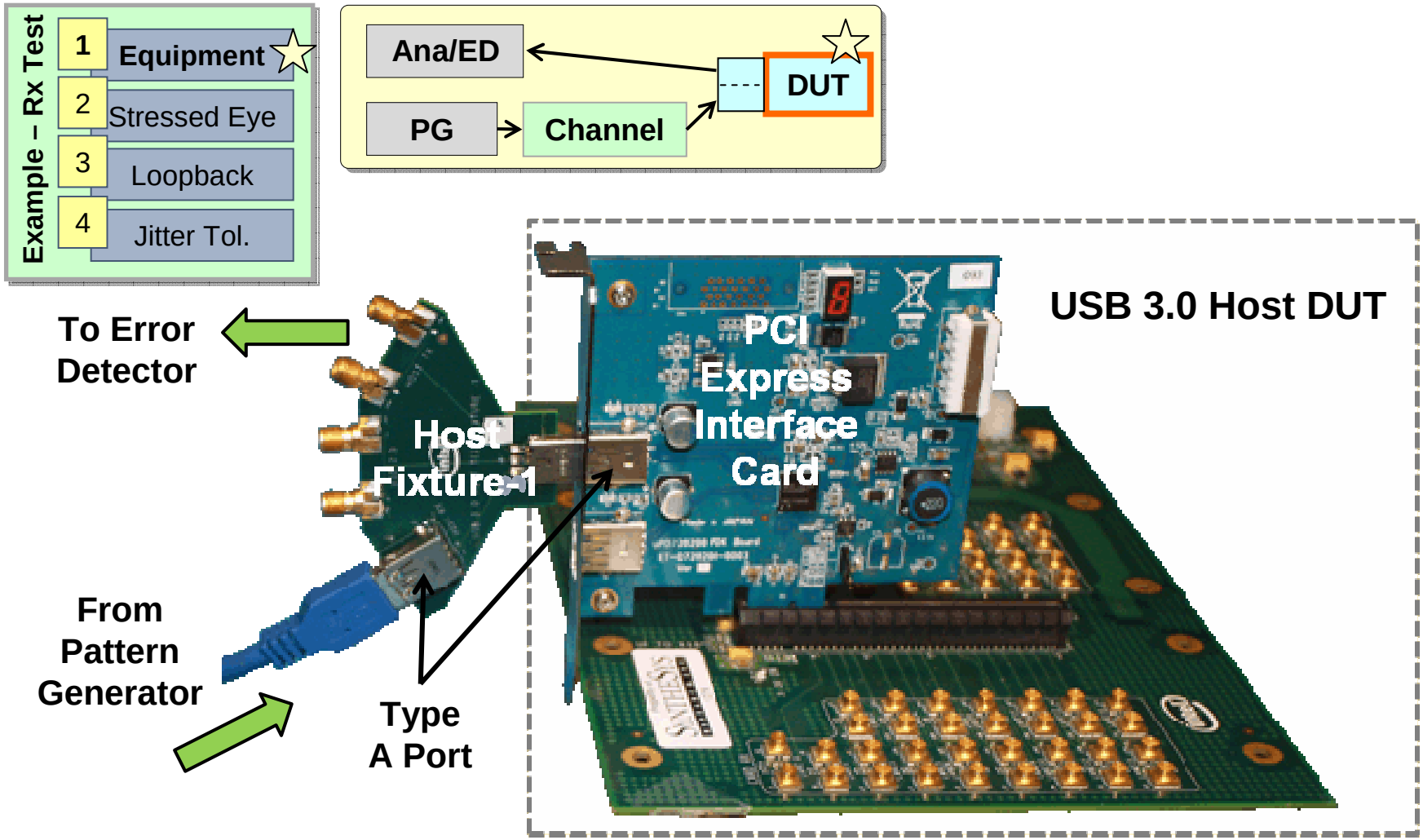
USB 3.0
Host DUT



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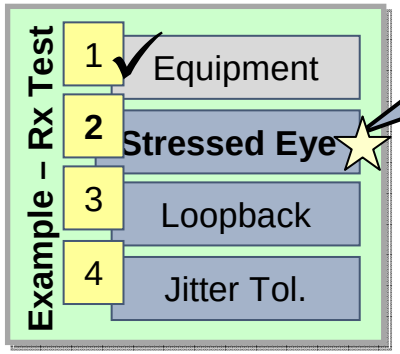
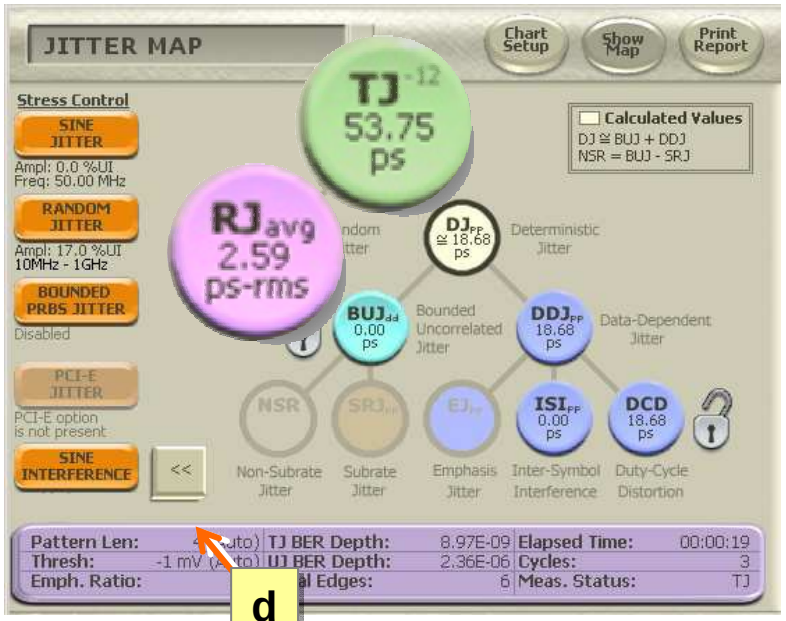
USB 3.0 Stressed Eye Calibration Jitter



For **Stressed Eye Calibration**, we need to **inject jitter from the PG** and **measure jitter in the Analyzer**

a

Jitter Map tool performs **BER-based Jitter Decomposition** and quickly measures to depths lower than 10^{-6}

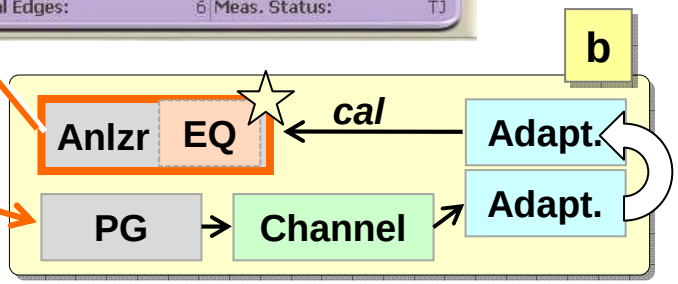


d

Stressed Pattern Generator control shows RJ and SJ injection

c

b



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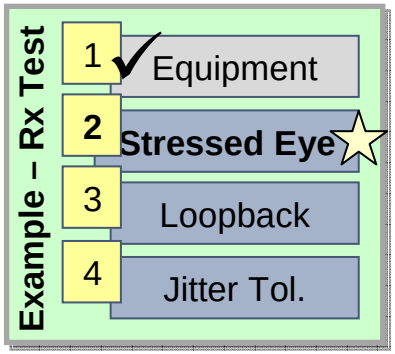
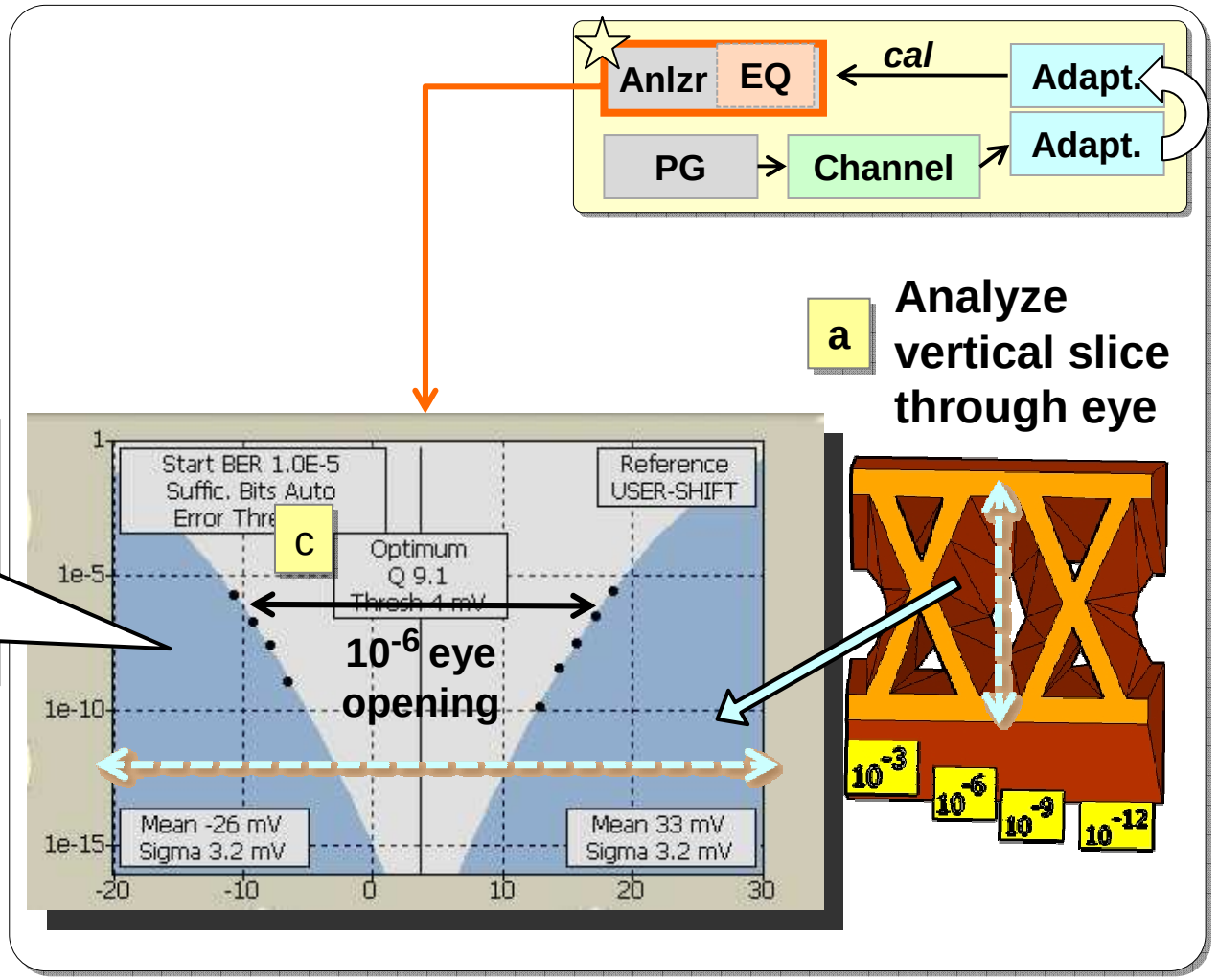
USB 3.0 Stressed Eye Calibration
Eye Height



b Eye height should be measured at 10^{-6} depth – the BERTScope quickly measures deeper than this



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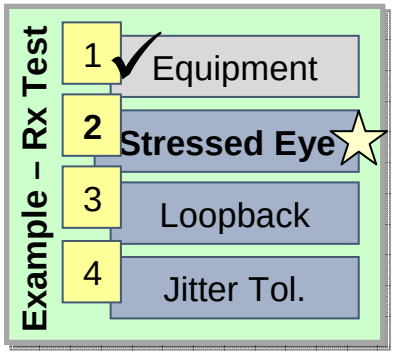
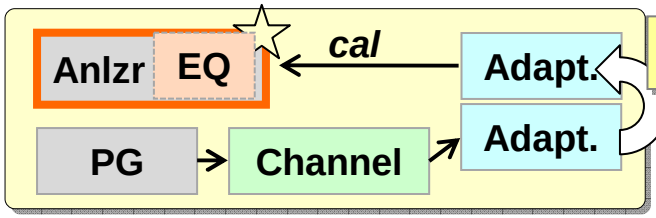
USB 3.0 Stressed Eye
CTLE Equalization Emulation

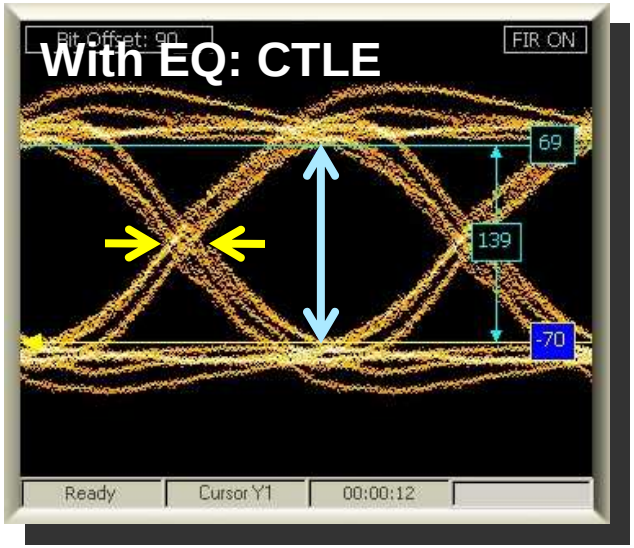


b Averaged waveforms show only data dependent effects, shown on CP3



c

d



e

1. Measure difference in eye height and jitter
2. Subtract from measured eye height and TJ from previous slides

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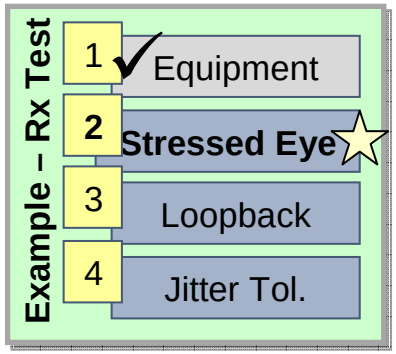
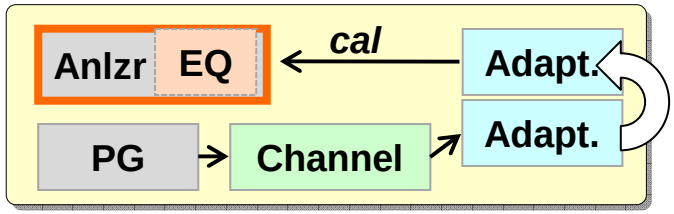
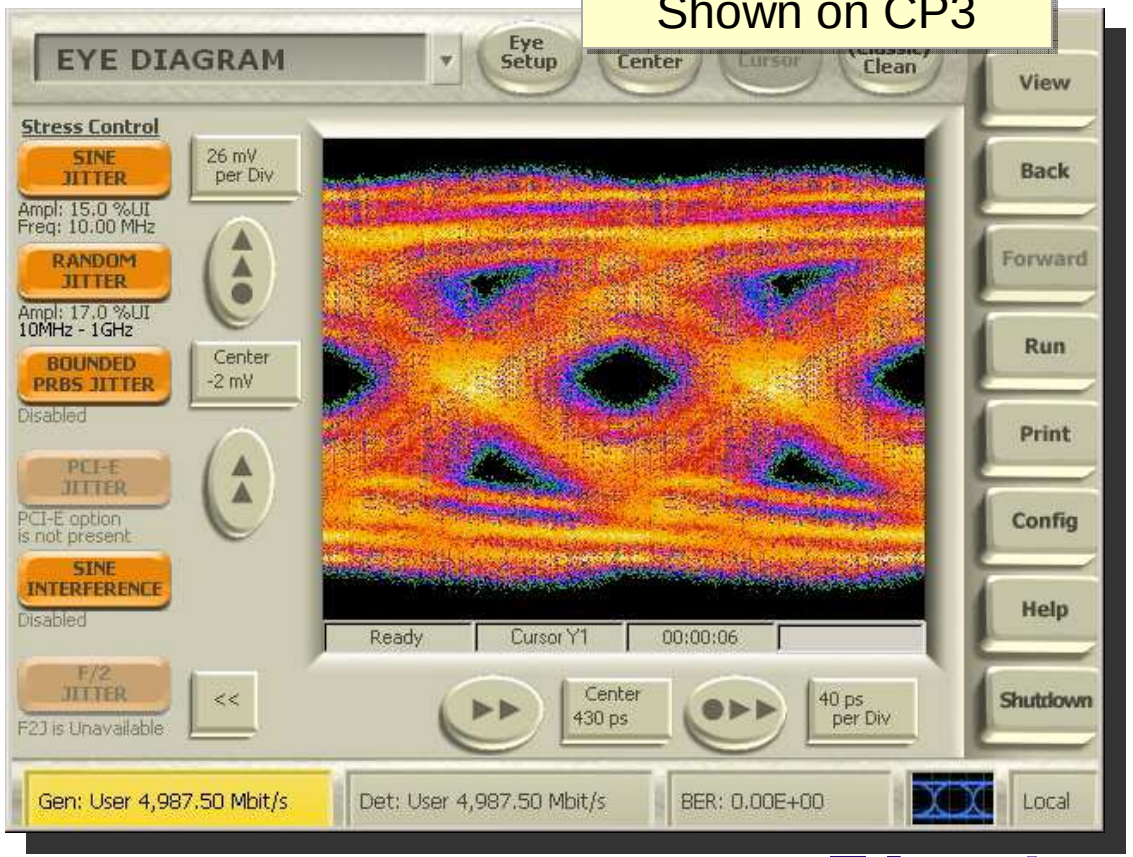
USB 3.0
Final Stressed Eye





Final Stressed Eye
Shown on CP3



Stressed Eye Calibration only needs to be performed once per setup

(Setup is different for Hosts and Devices)

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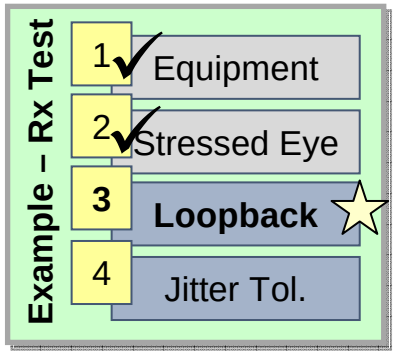
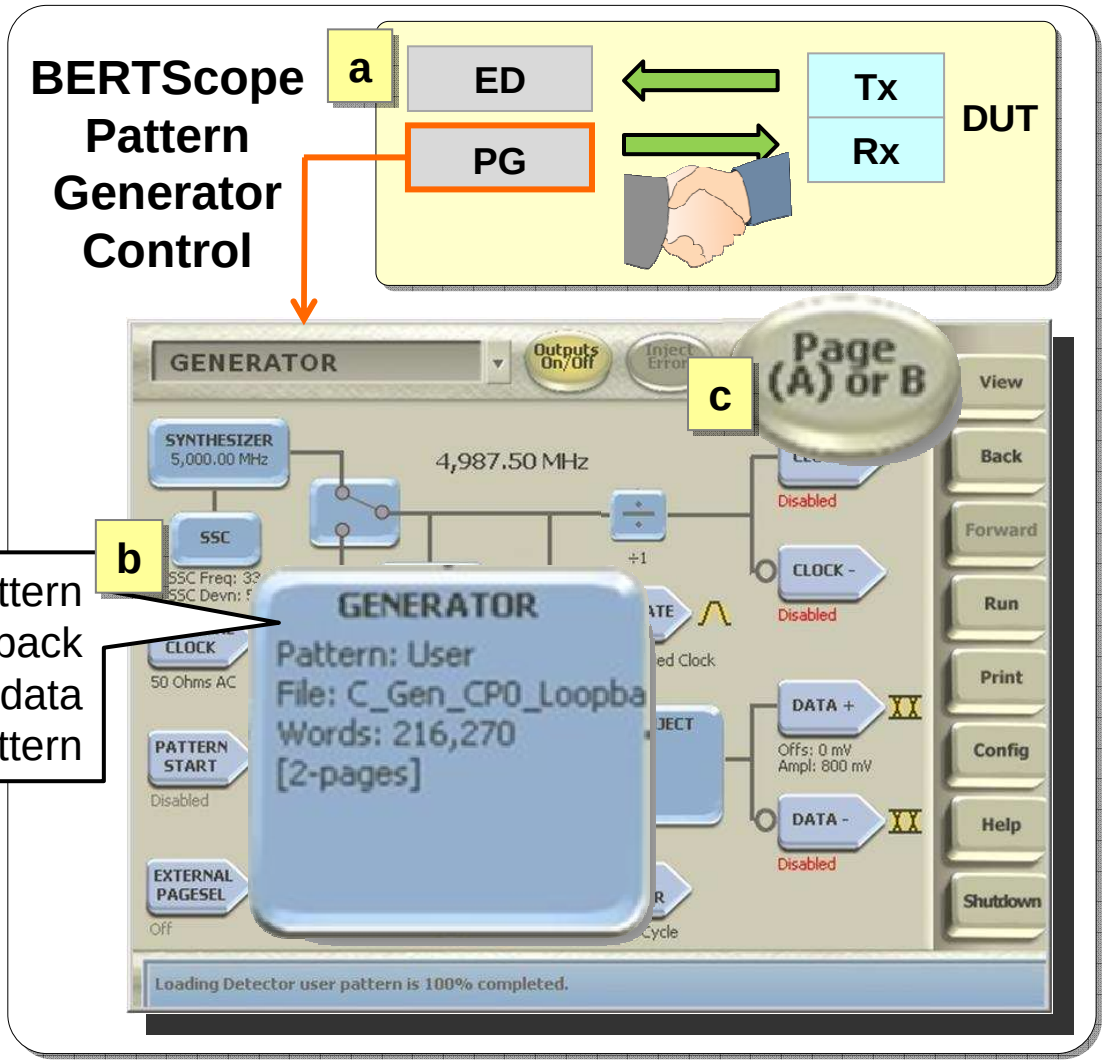
USB 3.0
Loopback Initiation





Use flexible two-page pattern memory to flip between loopback initiation sequence and test data pattern

d

Patterns available at www.bertscope.com

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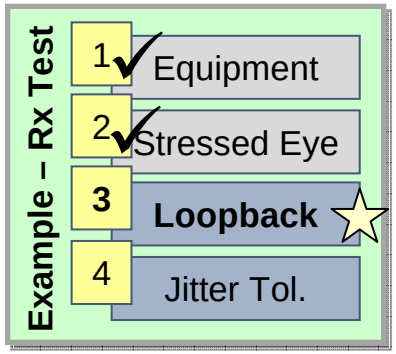
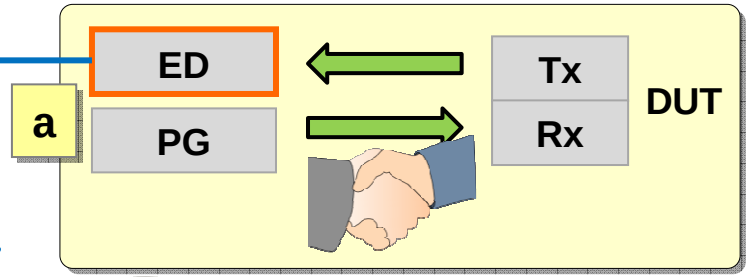
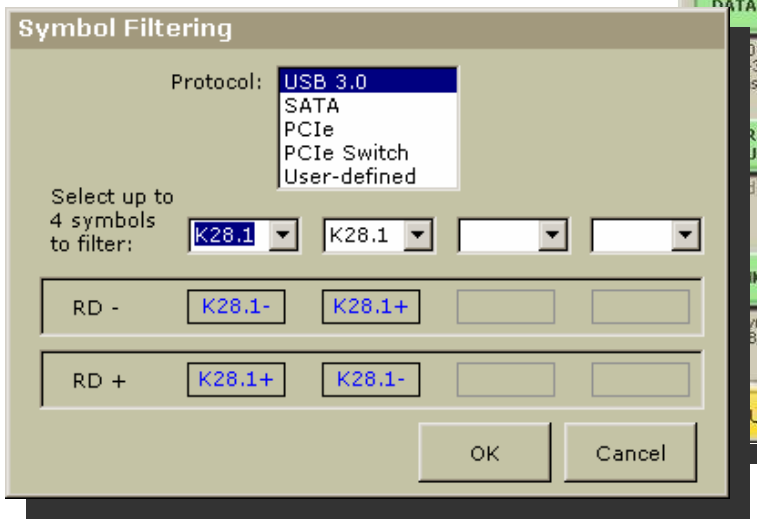
USB 3.0
Loopback Confirmation

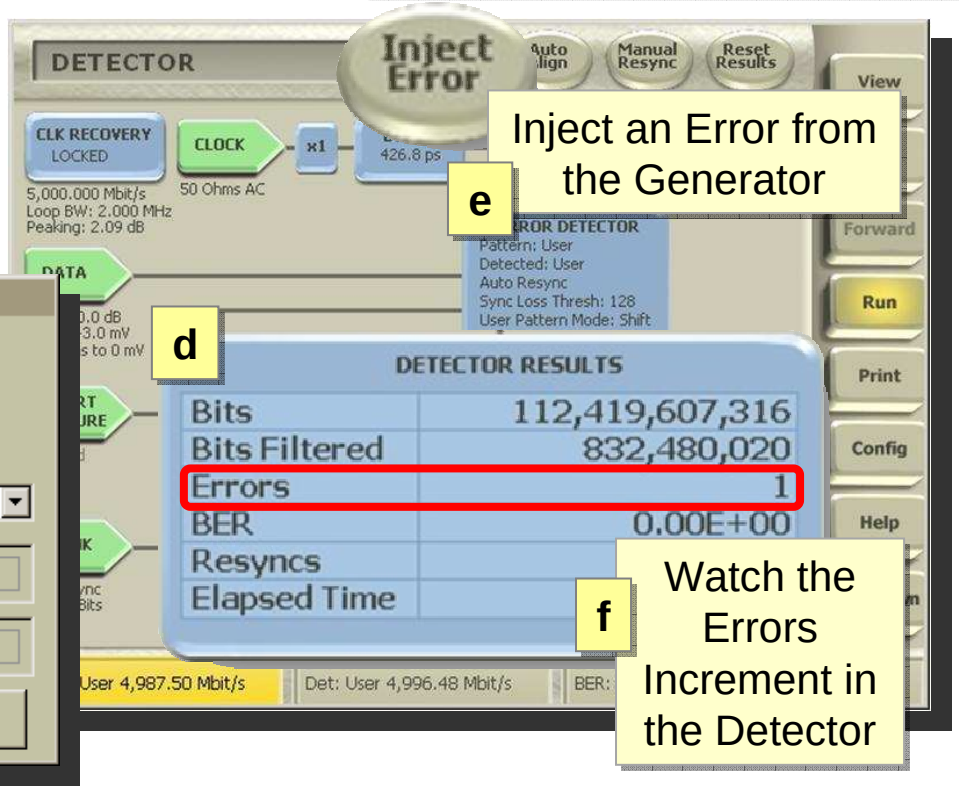


c Confirm that the DUT is in loopback



b Enable Symbol Filtering to get ED in sync





e Inject an Error from the Generator

f Watch the Errors Increment in the Detector

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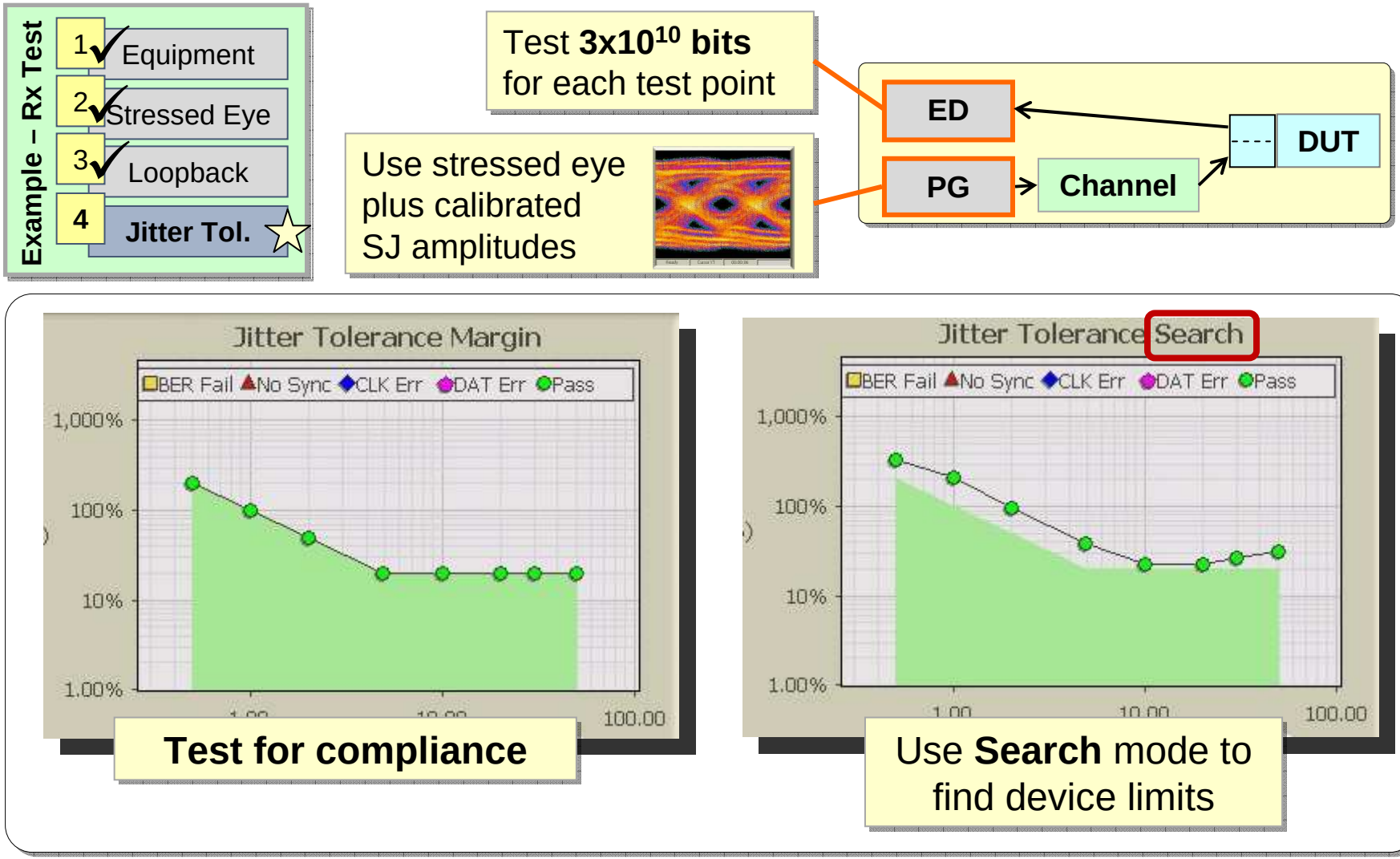
USB 3.0
Jitter Tolerance Test



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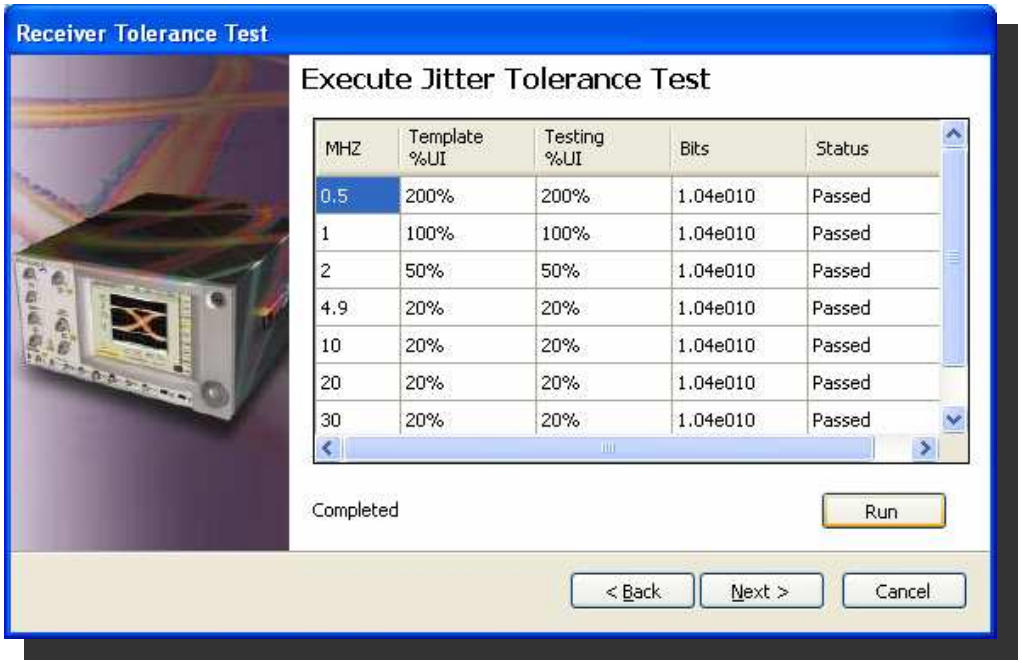
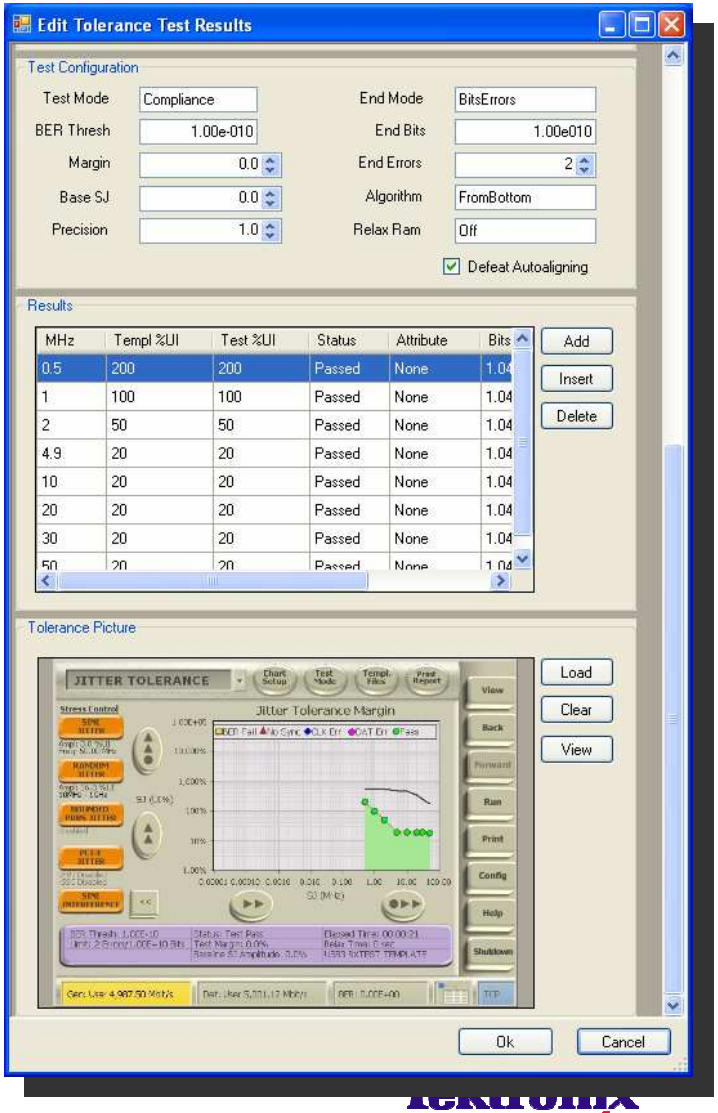
USB 3.0
Automation software (Coming Soon)

USB 3.0 Automation Software

- Automated stressed eye calibration
- Fast automated receiver testing
- Easy loopback initiation
- Database back-end for fast report generation





SATA Rx Compliance Testing

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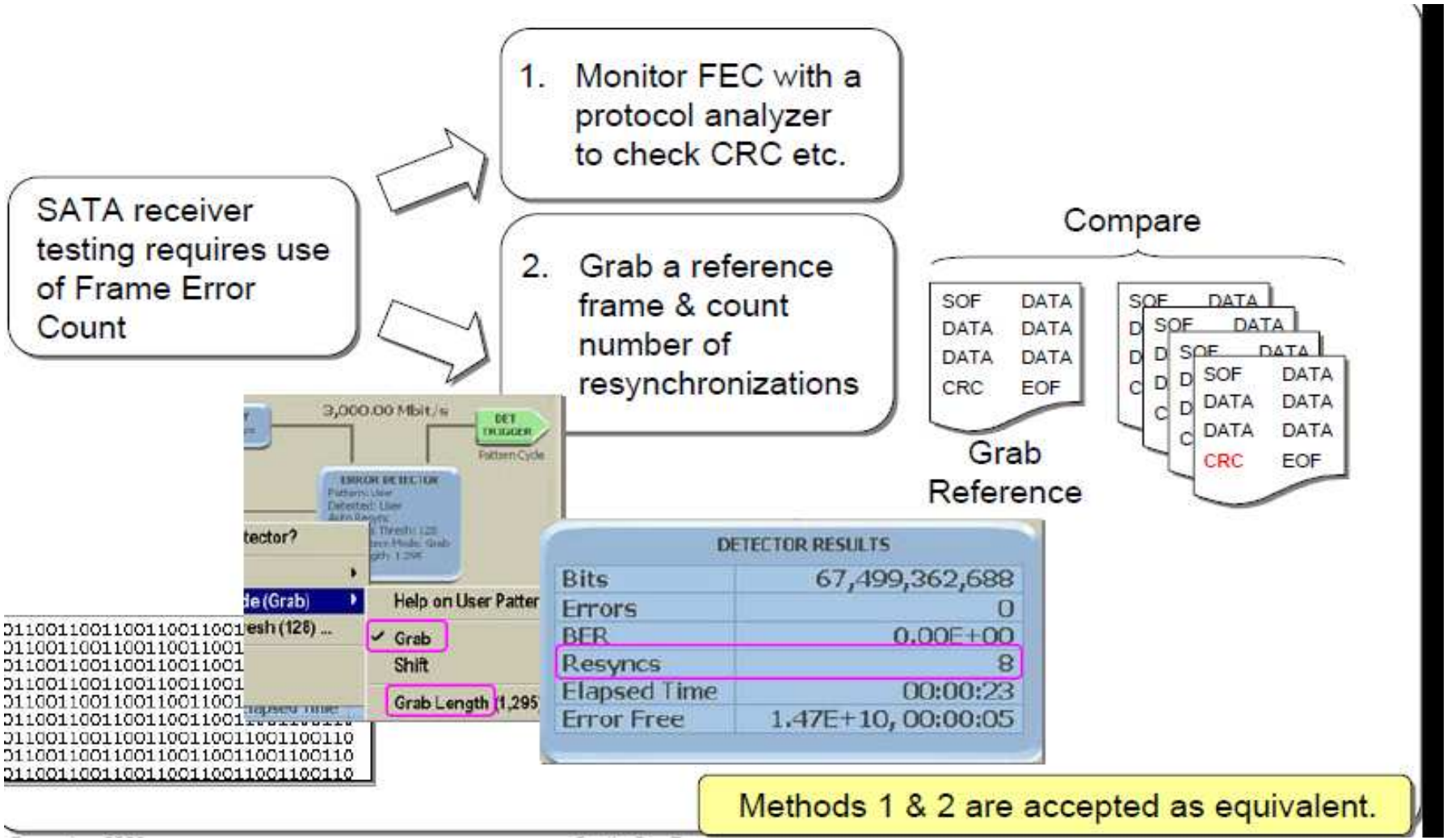
SATA
Frame Error Count

SATA receiver testing requires use of Frame Error Count

1. Monitor FEC with a protocol analyzer to check CRC etc.

2. Grab a reference frame & count number of resynchronizations



Methods 1 & 2 are accepted as equivalent.

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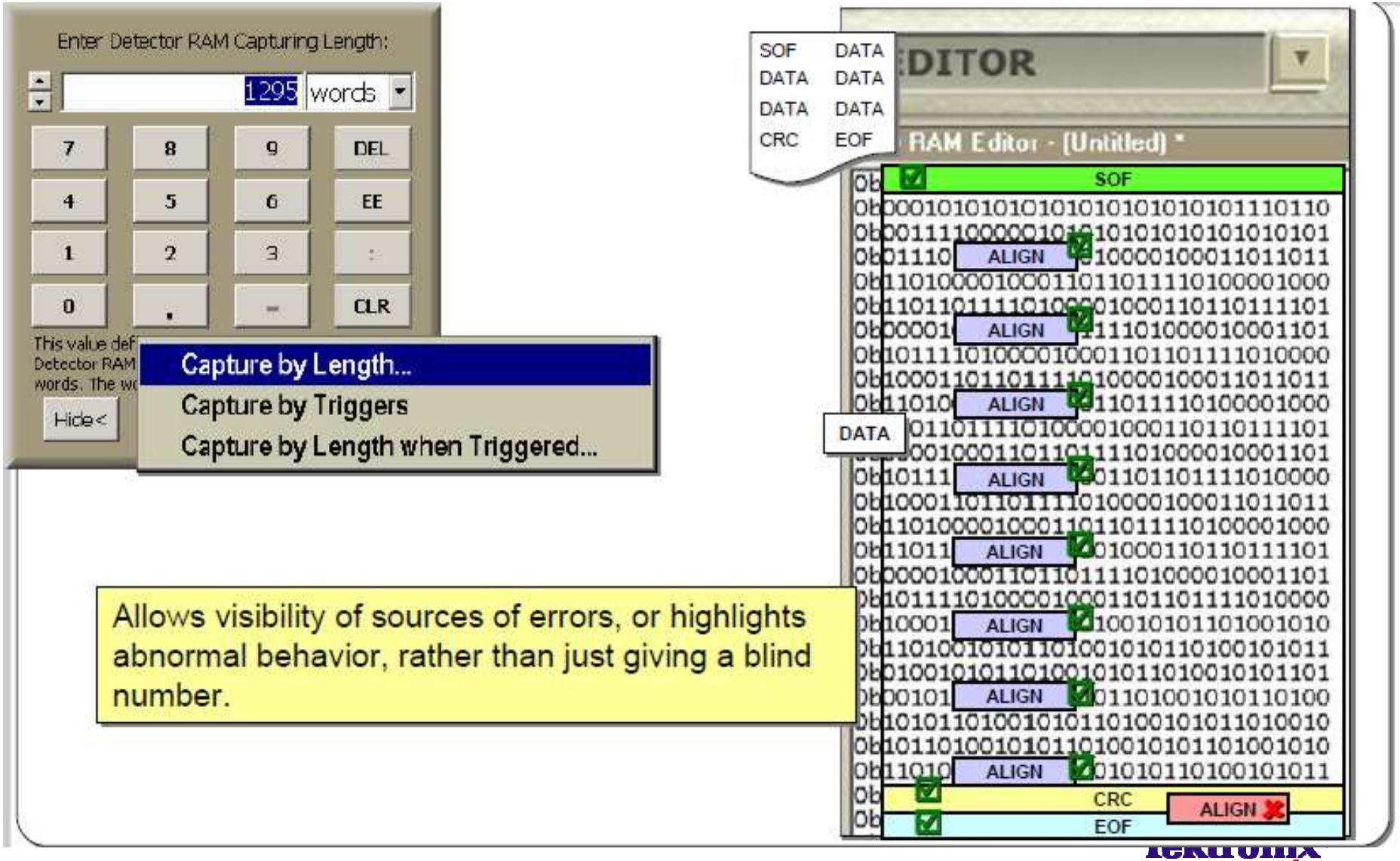
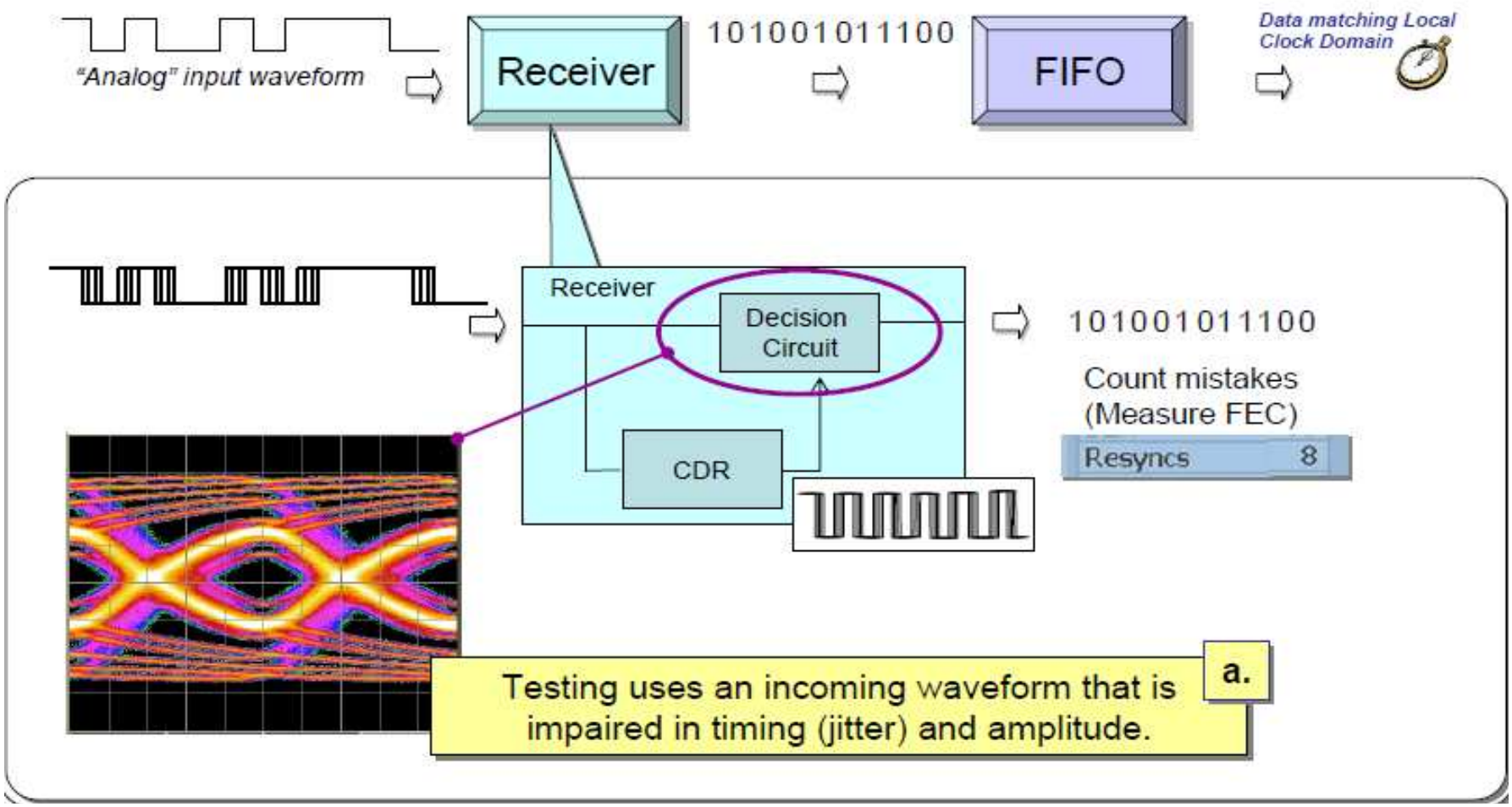
SATA
Grab Mode (Running Disparity)



SATA
Testing Decision Circuit



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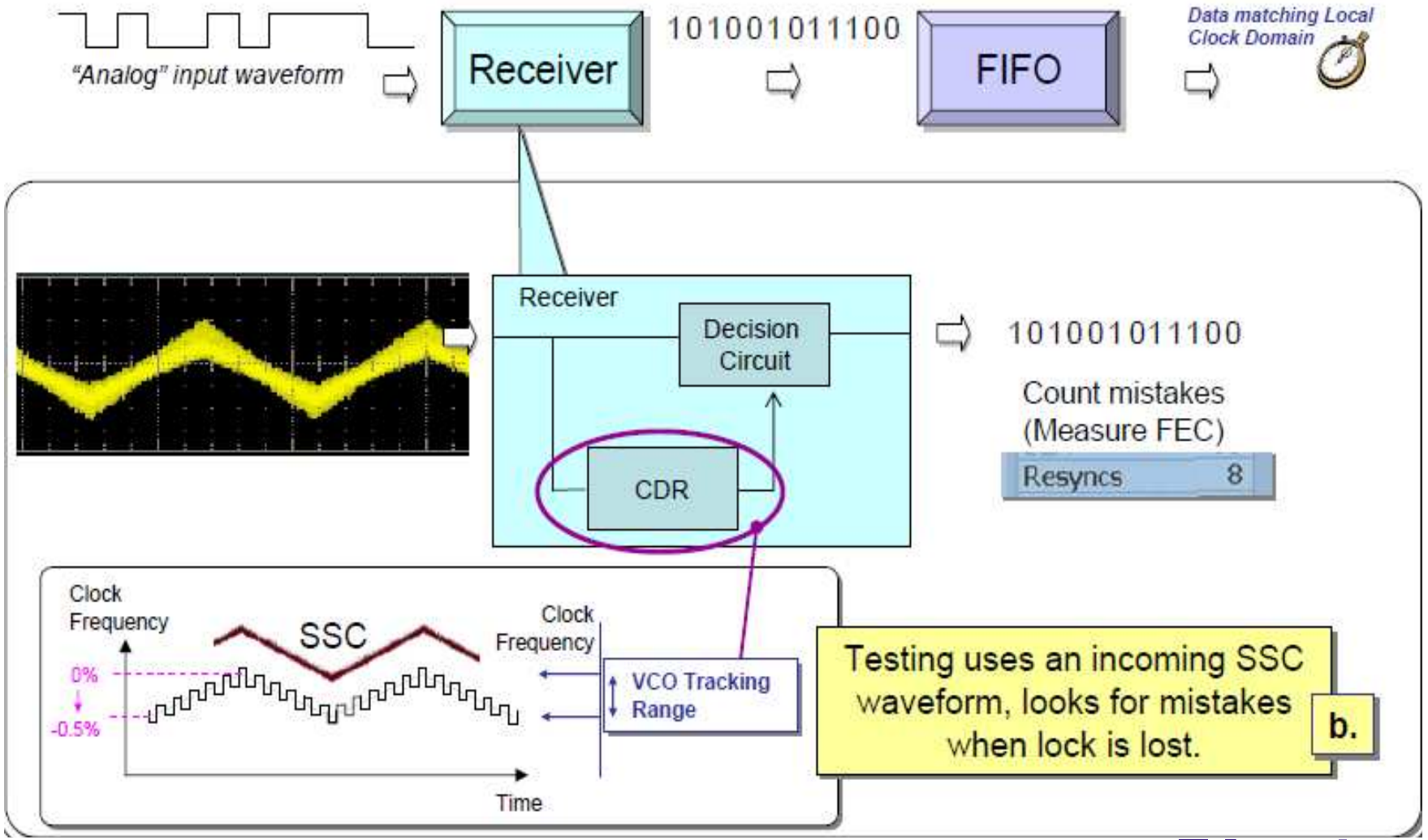
SATA
Testing CDR



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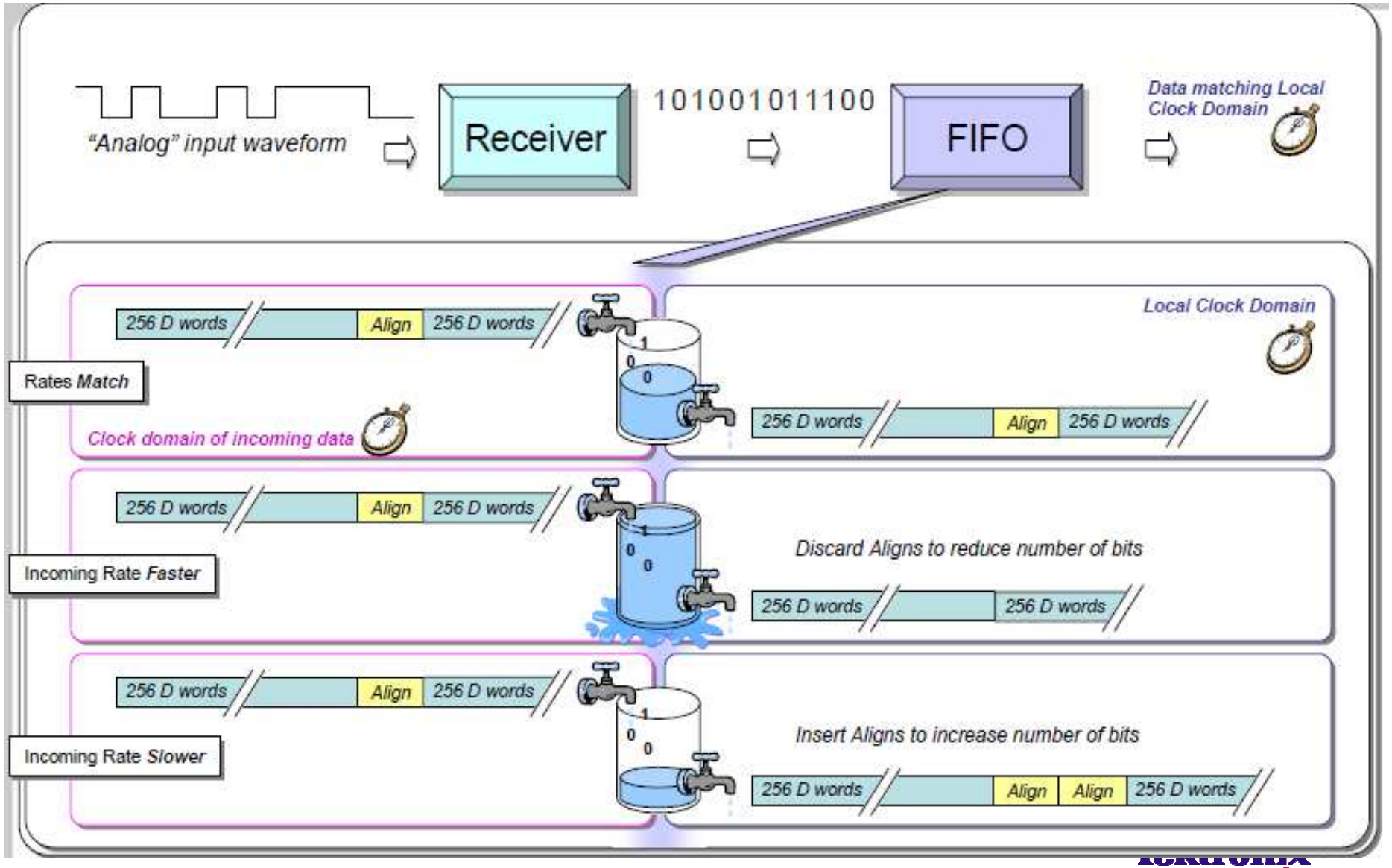
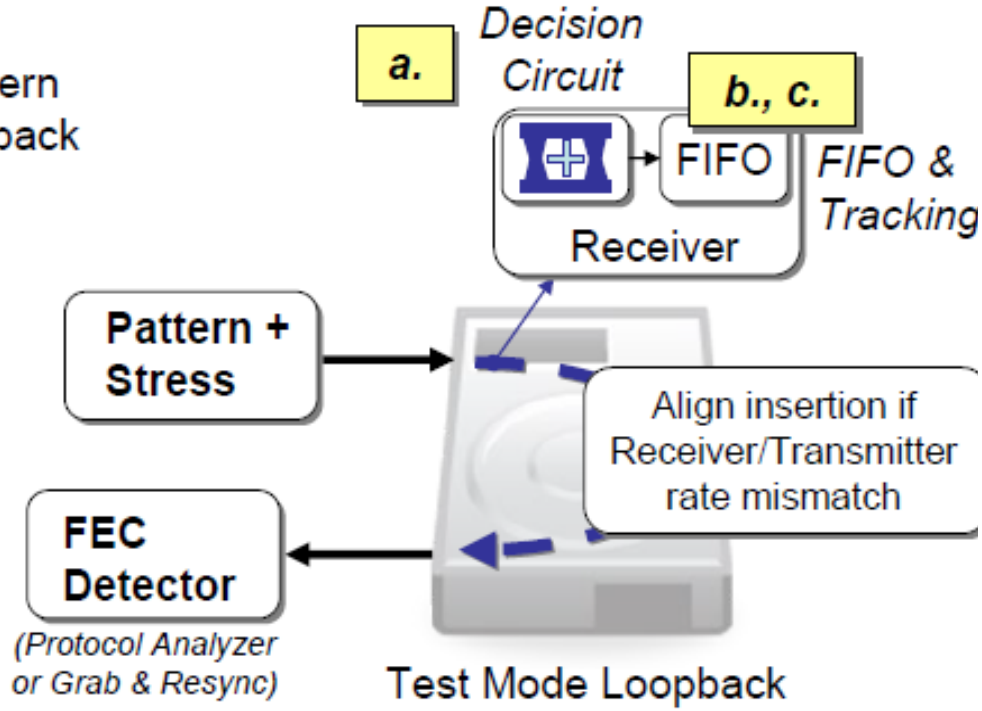
SATA
Testing FIFO (+-350ppm timing offset)



SATA
Compliance and beyond

Receiver Testing:

1. Generate stressed framed COMP pattern
2. Received pattern retimed and looped back to output of transmitter
3. If clock domains differ between received signal and system clock, aligns inserted.
4. Increase impairments, mistakes detected in CRC etc. at FEC detector
5. Gives basic **Compliance**
   No information about where failures occurred, or individual margins



Rx Impairments

Test **a.** { Added Jitter, Added Amplitude Closure

Test **b., c.** { Frequency Offset (350ppm), SSC Profile

***Beyond Compliance** – margin testing*

1. *By keeping clock domains the same, can stop aligns being added and see the effect of different stress types.*
2. *Can analyze margin in different parts of the receiver.*

PCIE Rx Compliance testing

All information in these slides are based on the PCI-Express draft 0.71

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PCI Express
Agenda

- PCIe Gen3 Receiver Testing
  - Stressed Voltage Eye
  - Stressed Jitter Eye
- Speed and Equalization Auto-Negotiation
- PLL Loop Bandwidth Testing

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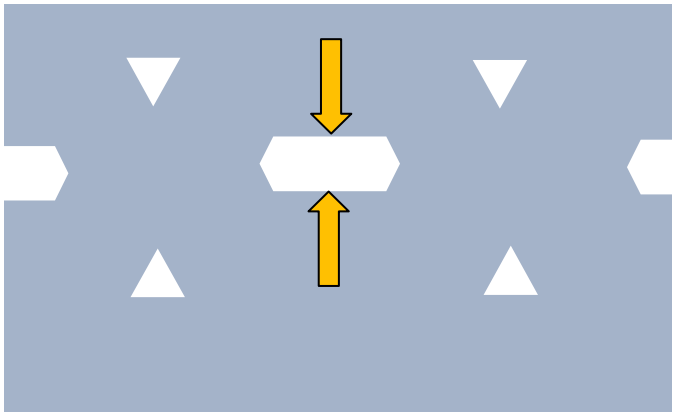
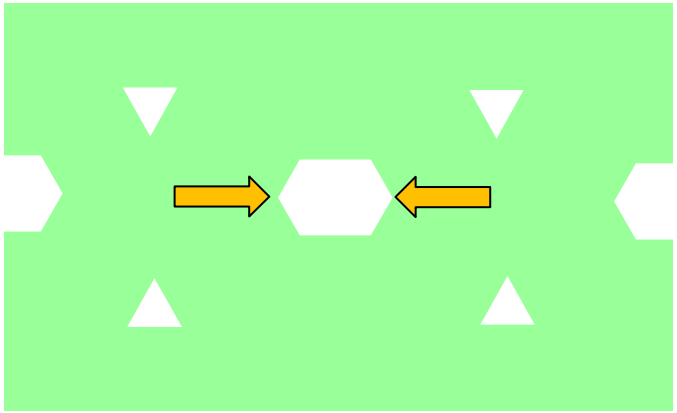
PCIe Gen3
Receiver Testing

- Split up into testing with two types of stressed eye
  1. Stressed Voltage Eye



  2. Stressed Jitter Eye



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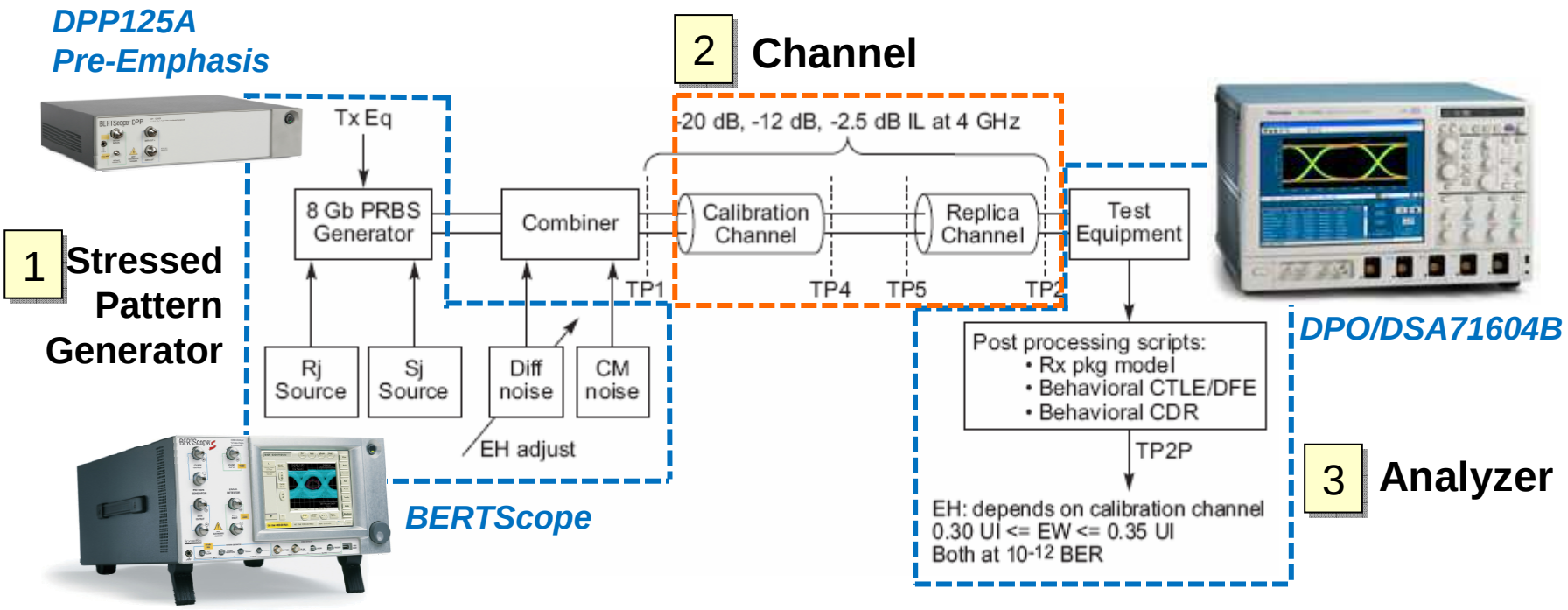
PCIE Gen3
Stressed Voltage Eye Calibration



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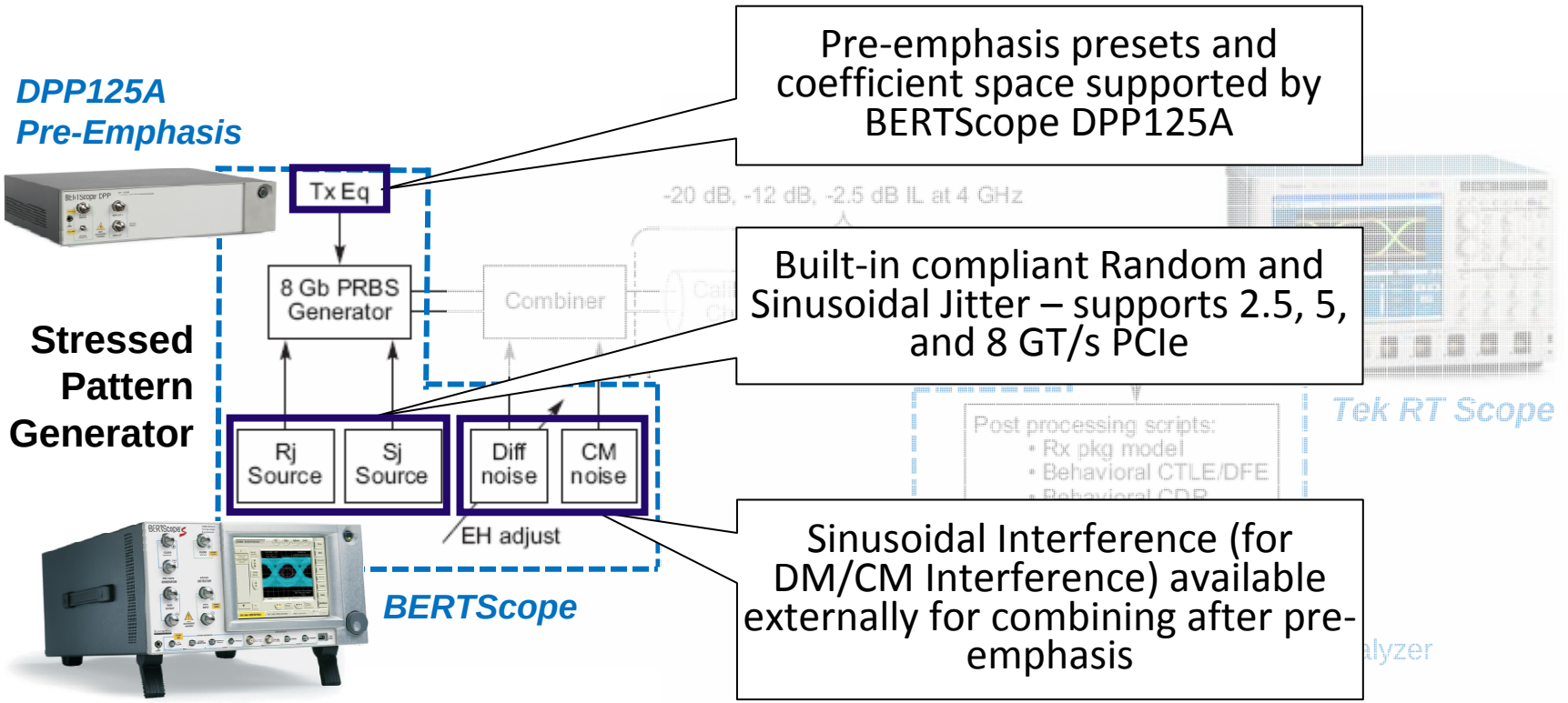
PCIE Gen3 Stressed Voltage Eye
Stressed Pattern Generation



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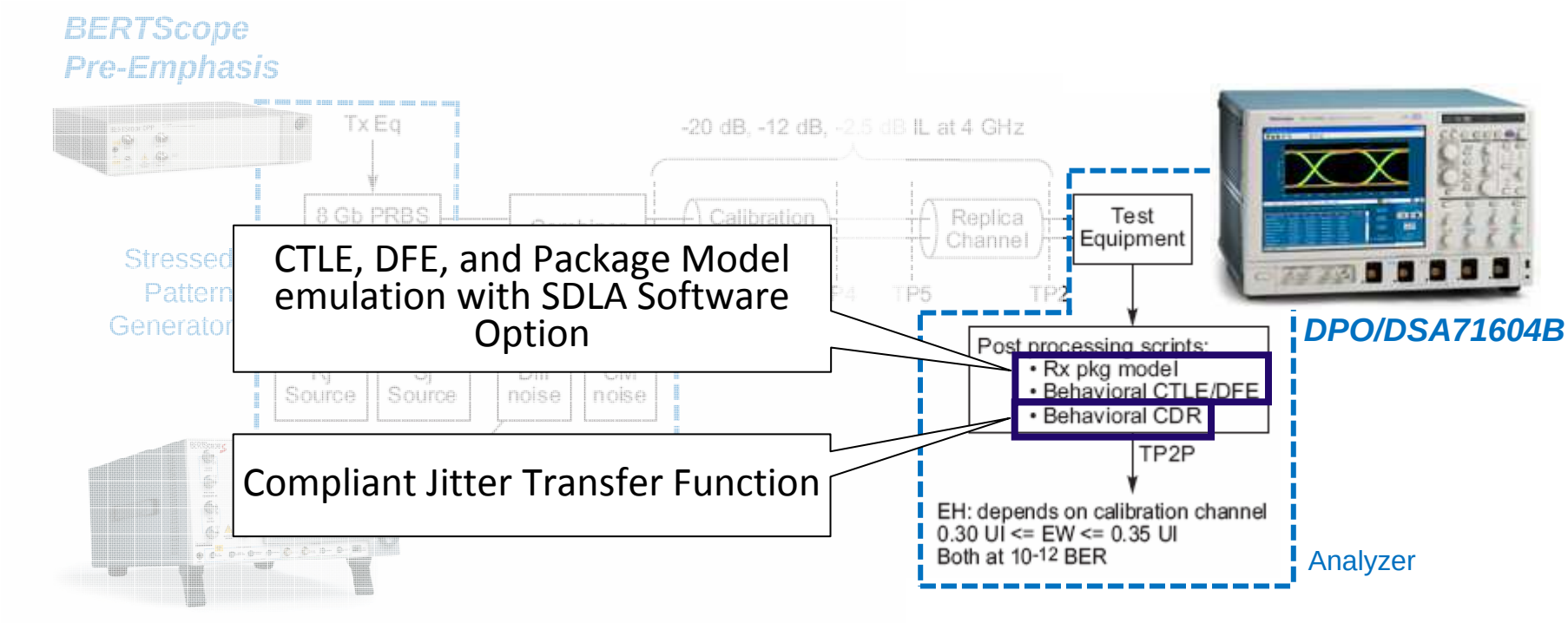
PCIE Gen3 Stressed Voltage Eye
Analyzer



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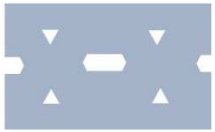
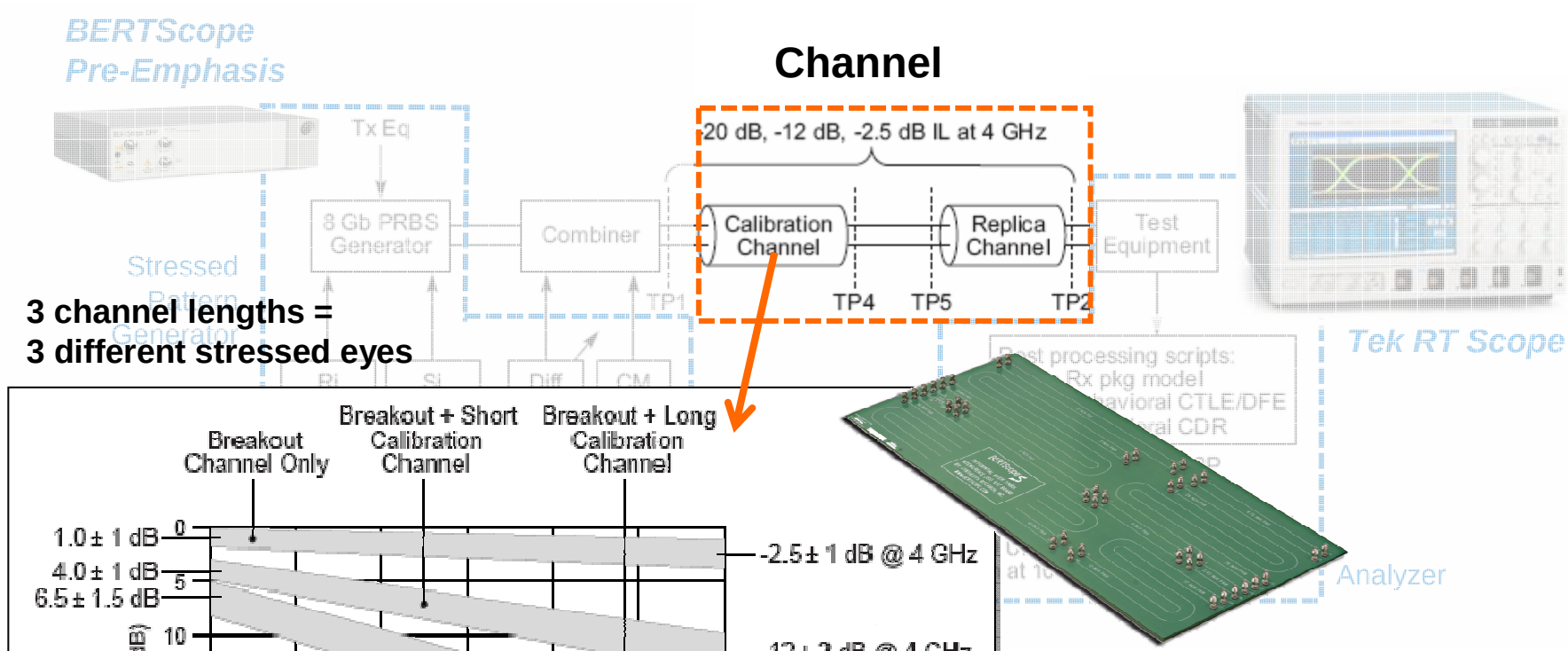
PCIE Gen3 Stressed Voltage Eye
Channel





BERTScope ISI Board
For Calibration Channel

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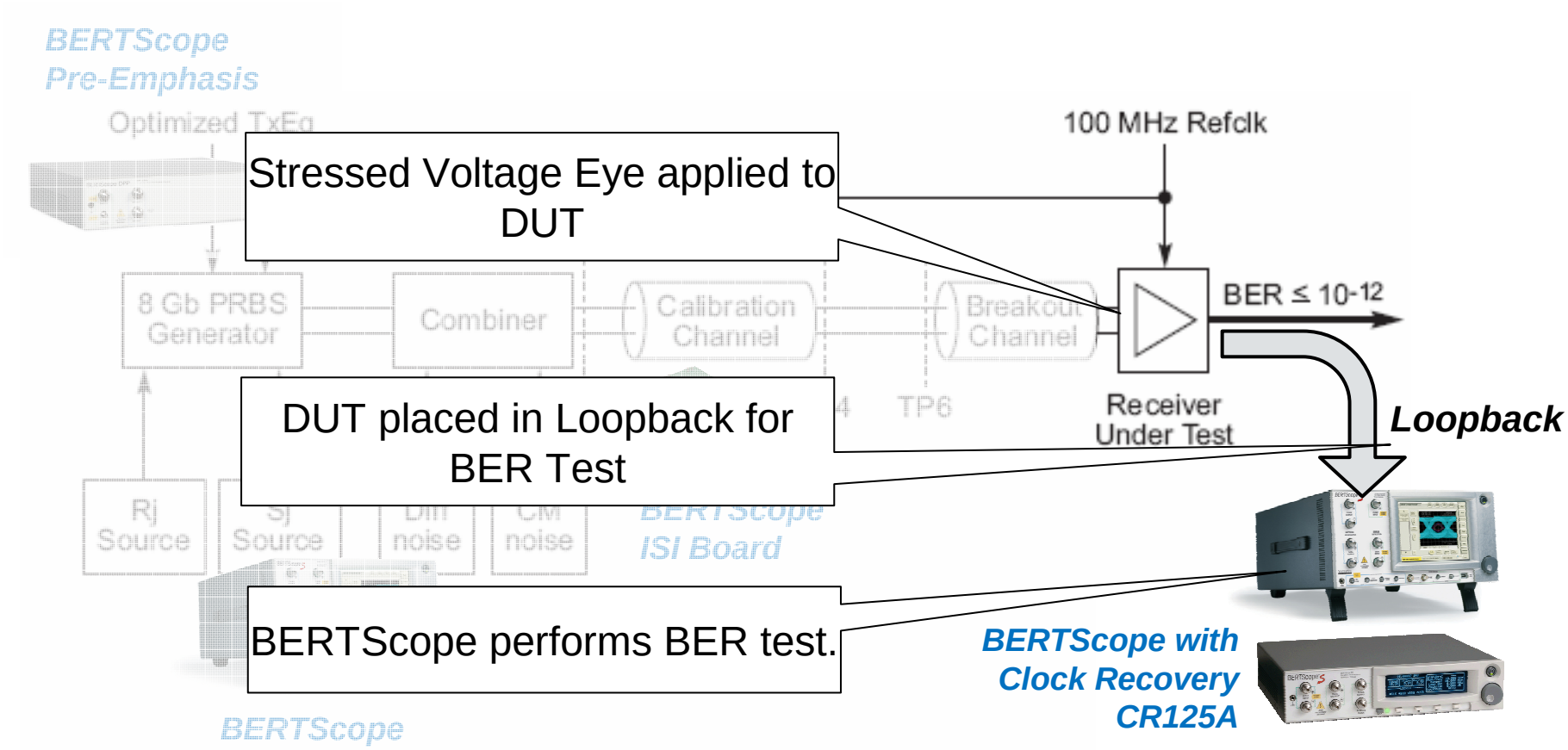
PCIE Gen3
Stressed Voltage **Test**



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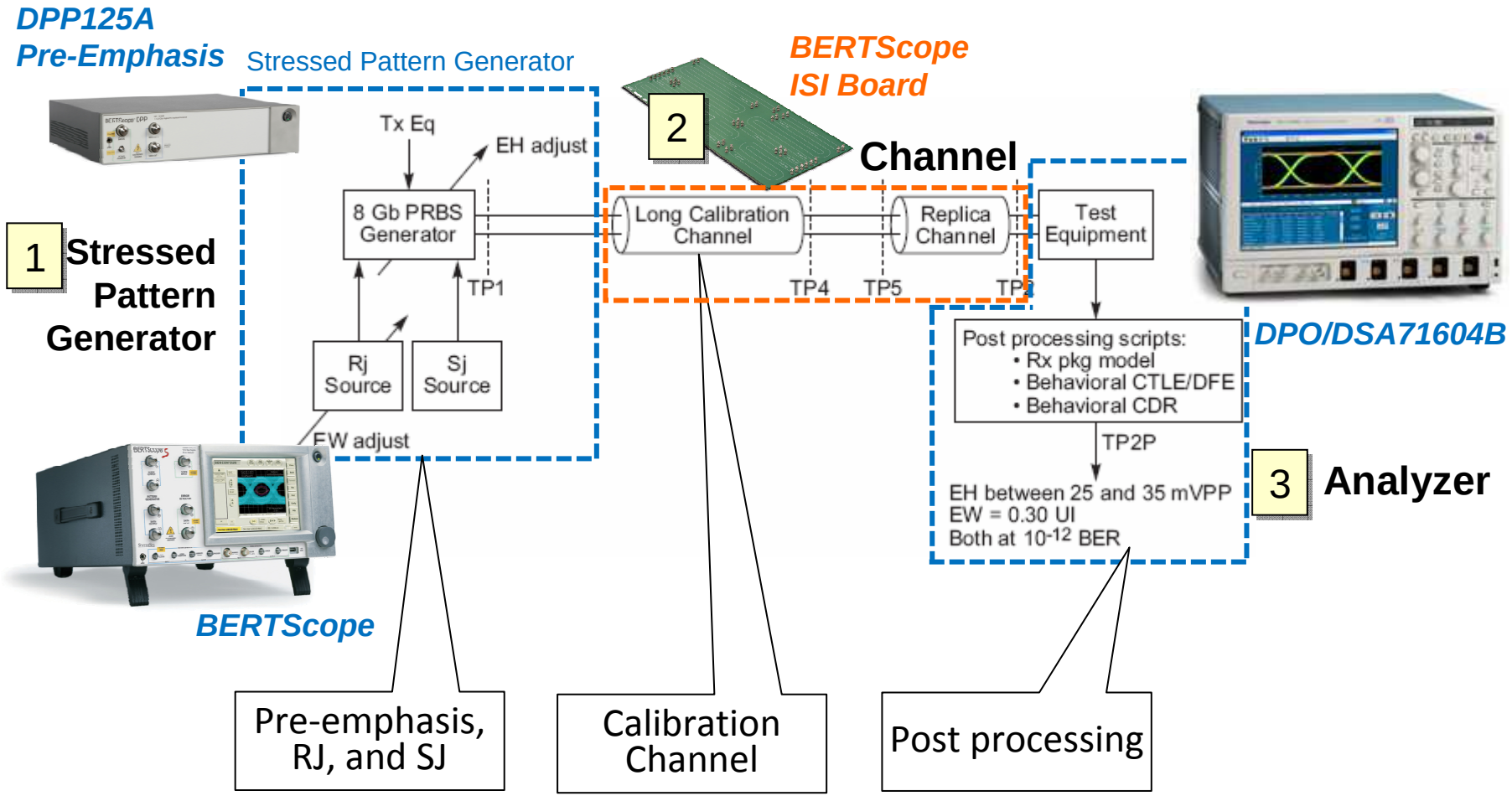
PCIE Gen3
Stressed **Jitter** Eye Calibration



Similar requirements as the Stressed Voltage Eye

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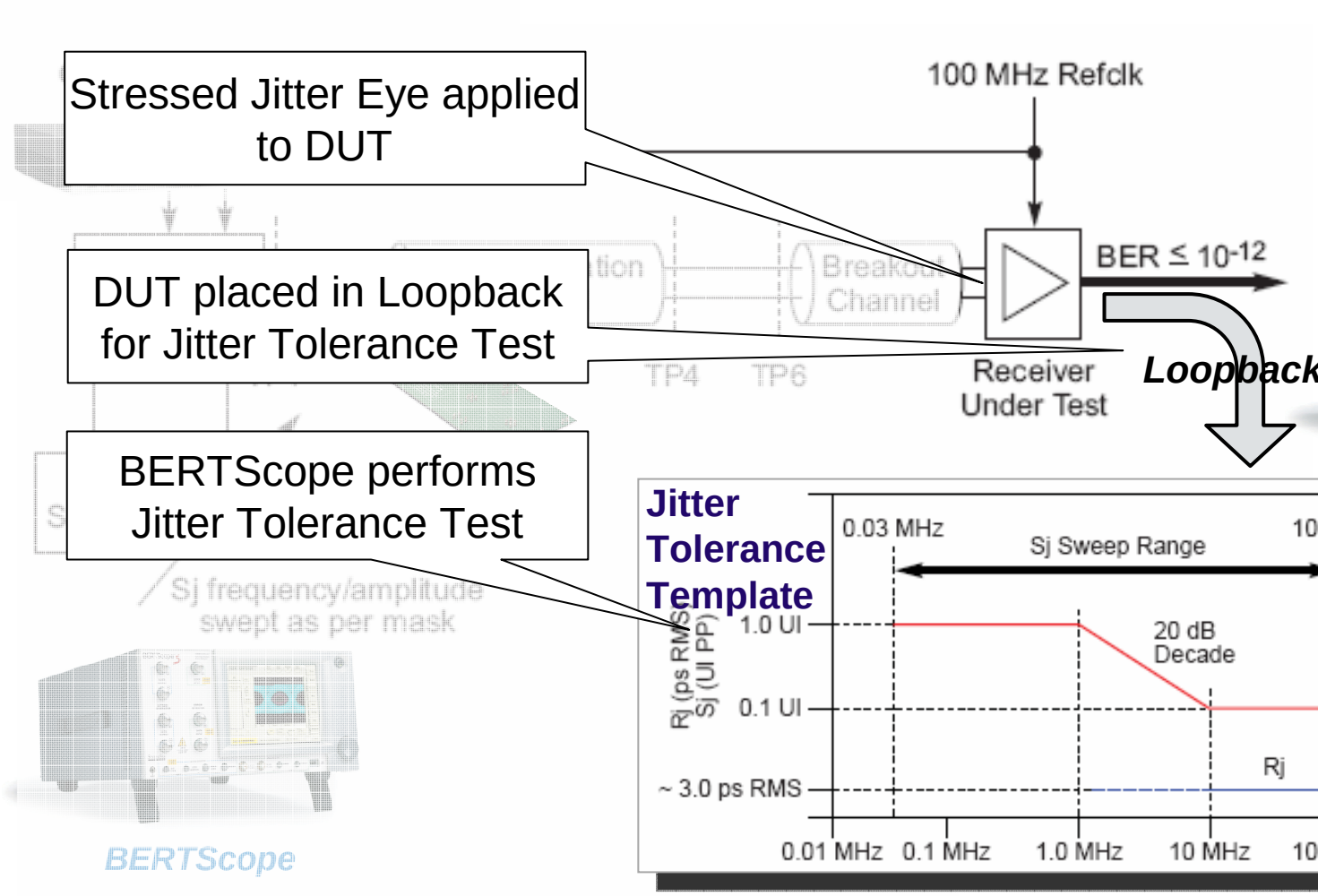
PCIE Gen3 Stressed Jitter **Test**
Jitter Tolerance

Stressed Jitter Eye applied to DUT

DUT placed in Loopback for Jitter Tolerance Test

BERTScope performs Jitter Tolerance Test



Automated Jitter Tolerance Test on the BERTScope, with Search Mode to find device limits

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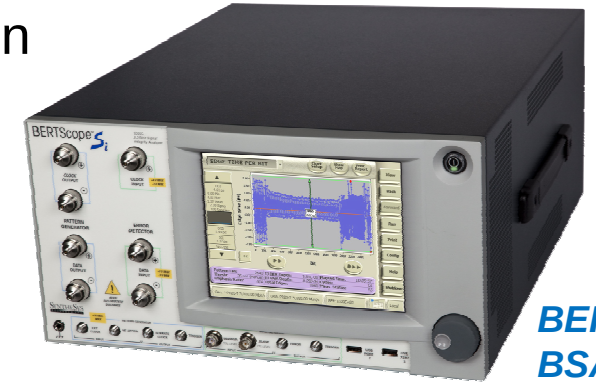
Summary of BERTScope Rx Test Capabilities for PCIe Gen3

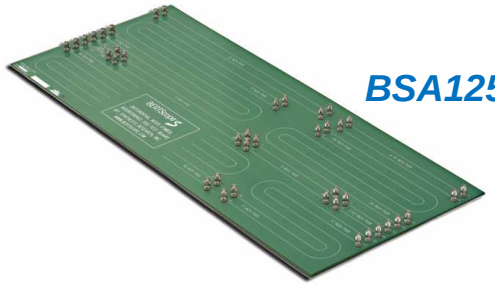
- BERTscope Stressed Pattern Generation
  - ✓ Random Jitter
  - ✓ Sinusoidal Jitter
  - ✓ Pre-emphasis (DPP125A)
  - ✓ Differential Mode Interference
  - ✓ Common Mode Interference
  - ✓ Calibration Channel (ISI Board)
- BERTScope Error Detection
  - ✓ Clock Recovery (CR125A)
  - ✓ Automated Jitter Tolerance Test
  - ✓ BER testing



BERTScope BSA85C

DPP125A

CR125A



BSA12500ISI

- **The BERTScope Family of Products provides the stresses needed for PCIe Gen3 with unrivaled ease of use, so engineers can quickly debug issues and find device margins**

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Summary of BERTScope Rx Test Capabilities for PCIe Gen3 (Continued)

- Oscilloscope (for Stressed Eye Calibration)
  - ✓ CTLE
  - ✓ DFE
  - ✓ Behavioral package emulation
  - ✓ Clock Recovery for Compliant Jitter Transfer Function

DPO/DSA71604B

- **The Tektronix DPO/DSA71604B provides compliant embedding of the Receiver equalization for accurate measurements as would be seen at the latch of the Receiver, providing the right feedback to the BERTScope Stressed Pattern Generator during Stressed Eye Calibration**

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PCIE Gen3
Agenda

- PCIe Gen3 Receiver Testing
  - Stressed Voltage Eye
  - Stressed Jitter Eye
- **Speed and Equalization Auto-Negotiation**
- PLL Loop Bandwidth Testing

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PCIE Gen3
Speed and Equalization Auto-Negotiation

- Devices must start up at 2.5 GT/s and negotiate up to 8 GT/s
- In PCIe Gen3, Receivers are expected to:
  1. Optimize their own equalization
  2. Adjust the Transmitter's pre-emphasis settings via back-channel communication

➢ **Device equalization optimization algorithm will be key to PCI-Express Gen3 success, and we are here to help you test**

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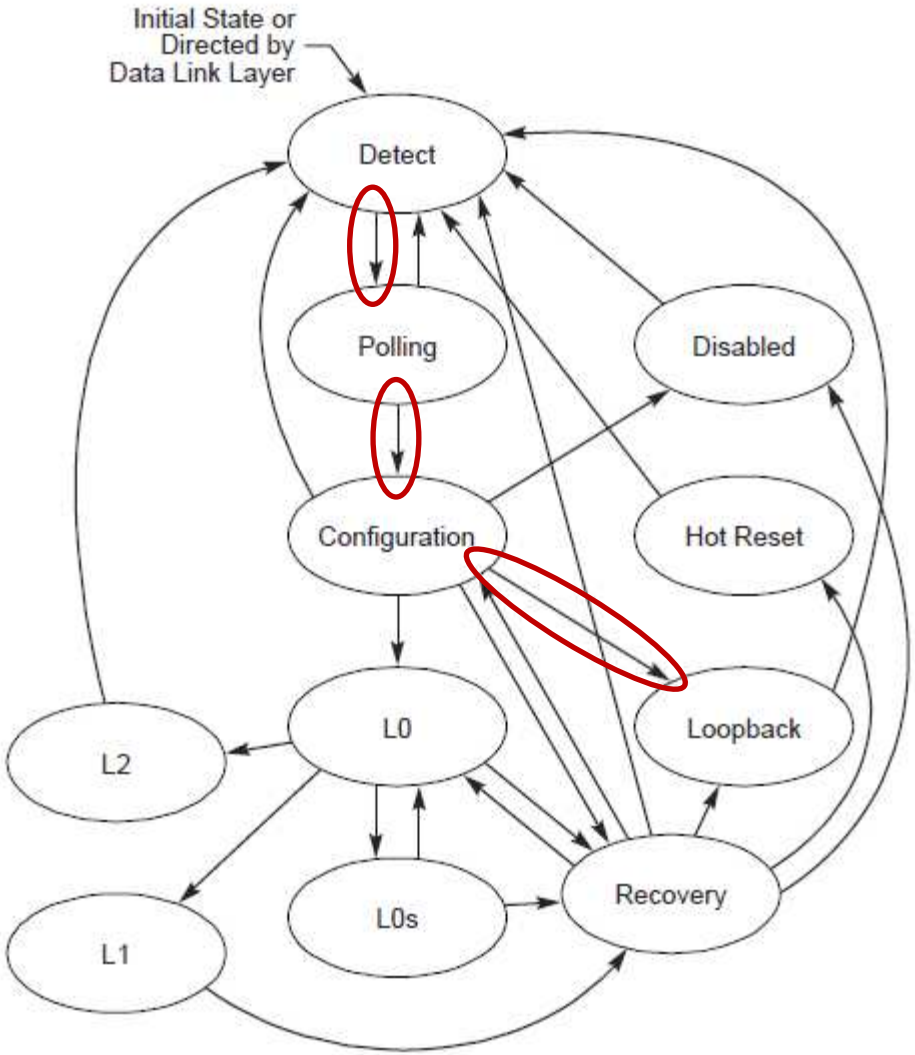
PCIE Gen3

Speed and Equalization Auto-Negotiation with the BERTScope

- Use the BERTScope for R&D testing of new Gen3 devices
  - Fixed data patterns can perform the speed negotiation to 8 GT/s and allow the user to check (manually) their DUT's equalization optimization routine
  - With a fixed pattern, can get devices into Loopback for Receiver testing of early R&D Silicon



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PCIE Gen3
Transmitter Pre-emphasis

- The DPP125A supports the allowable pre-emphasis settings (table below from draft 0.71)
- The colored fields in the table are the “pre-sets” which are easily loaded from factory created configuration files

DPP125A

Min Reduced Swing Limit

PS DE / BOOST		C_{+1} 0/24	1/24	2/24	3/24	4/24	5/24	6/24	7/24	8/24
C_{-1}	0/24	0.0 0.0 0.0	0.0 -0.8 0.8	0.0 -1.6 1.6	0.0 -2.5 2.5	0.0 -3.5 3.5	0.0 -4.7 4.7	0.0 -6.0 6.0	0.0 -7.6 7.6	0.0 -9.5 9.5
	1/24	0.8 0.0 0.8	0.8 -0.8 1.6	0.9 -1.7 2.5	1.0 -2.8 3.5	1.2 -3.9 4.7	1.3 -5.3 6.0	1.6 -6.8 7.6	1.9 -8.8 9.5	
	2/24	1.6 0.0 1.6	1.7 -0.9 2.5	1.9 -1.9 3.5	2.2 -3.1 4.7	2.5 -4.4 6.0	2.9 -6.0 7.6	3.5 -8.0 9.5		
	3/24	2.5 0.0 2.5	2.8 -1.0 3.5	3.1 -2.2 4.7	3.5 -3.5 6.0	4.1 -5.1 7.6	4.9 -7.0 9.5			
	4/24	3.5 0.0 3.5	3.9 -1.2 4.7	4.4 -2.5 6.0	5.1 -4.1 7.6	6.0 -6.0 9.5				
	5/24	4.7 0.0 4.7	5.3 -1.3 6.0	6.0 -2.9 7.6	7.0 -4.9 9.5					
	6/24	6.0 0.0 6.0	6.8 -1.6 7.6	8.0 -3.5 9.5						

Full Swing Limit or
Max Reduced Swing Limit

A-0816

Figure 4-514-504-504-50: TxEQ Coefficient Space Triangular Matrix Example

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PCIE Gen3
Agenda

- PCIe Gen3 Receiver Testing
  - Stressed Voltage Eye
  - Stressed Jitter Eye
- Speed and Equalization Auto-Negotiation
- **PLL Loop Bandwidth Testing**

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PCIE Gen3
PLL Loop Bandwidth Test

- The BERTScope CR125A-PCIE is the test instrument used for PCI-Express Gen2 PLL Loop Bandwidth testing (2.5 and 5 GT/s) at the Compliance Workshops
- Clock recovery capability at 8 GT/s facilitates testing of Gen3 devices
- Higher speed models support 16 GT/s for future PCIe Gen4

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PCIE Gen3 Summary

- Receiver testing is expected to be mandatory and will include testing with a Stressed Voltage and Stressed Jitter Eye

- Equalization auto-negotiation controlled by the Receiver is new for Gen3

- Tektronix can provide solutions for many aspects of receiver testing to PCIe Gen3 today
  - **Tektonix, including the BERTScope, has a strong history providing test solutions for PCI-Express – one that we plan to continue**
  - The BERTScope supports data rates to 8.5G, 12.5G, and 17.5G for current and future PCIe projects
  - Contact us for further details on our plans for Gen3 support

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One Stop Shopping For HSSD From Tektronix

Transmitter Tests Transmitter jitter and timing measurements.	**DSA/DPO/MSO 71254B / MSO71254 or higher bandwidth** Opt. USB-TX (TekExpress Automation and DPOJET Measurements) Opt. DPOJET Jitter and Eye Diagram Analysis Tool TF-USB3-AB-KIT (Host and Device Test) or TF-USB3-A-P (Host Test) or TF-USB3-A-R (Device Test) Test Fixture	
Receiver Tests: Signal Generation / Error Detection Receiver Jitter Tolerance Tests for Customers working with HDMI, DP, MIPI Flexible channel Emulation	**AWG7122B w/ Opt. 6 and Opt. 8 and DSA/DPO/MSO 71254B / MSO71254 or higher bandwidth w/ Opt. STU and ERRDT** SerialXpress SDX100 opt. ISI and SSC TEKEXP USB-RMT for Full Automation TF-USB3-AB-KIT Test Fixture Kit	
Receiver Tests: Error Detection Receiver Jitter Tolerance Test and Debug and Analysis Tools	**BERTScope BSA85C w/Opt. STR&PVU** DPP125 CR125A with Opt XLBW & Opt CR125ACBL (Precision delay-matched cable set for use with BSA & CR in SSC applications)	
Interconnect/Cable Tests Cable skew, Far End Noise, Near End Noise, cable and connector impedance, Insertion loss, and return loss measurements.	**DSA8200** 80E08 TDR Sampling Module for DSA8200 2 per scope IConnect TDR and S-Parameter measurement software (80SSPAR) TF-USB3-AB-KIT Test Fixture Kit for Cable Test	

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Thank You

Application Information at:
www.bertscope.com

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