Explore BERTScope’s Benefit In High Speed Serial Data
Agenda

- BERTScope In High Speed Serial Data
- USB 3.0 Compliance Testing
- SATA Compliance Testing
- PCIE Rx & PLL Loop bandwidth Testing
- One Stop Shopping for HSSD from Tektronix
BERTScope’s Applications In High Speed Serial Data

**Different model for different applications**

- BSA85C for USB3.0, SATA, PCIe, Displayport...etc PC IOs
- BSA125C/175C for 10GbE, SAS, FC...etc server and storage
- BSA260C for 40/100GbE
USB 3.0 Rx Compliance Testing
USB 3.0 Receiver Test Flowchart

Create worst case signal to test the receiver

Only needs to be performed once per setup

Test receiver with stressed eye and added sinusoidal jitter (SJ) in Jitter Tolerance template

Jitter Tolerance
1. Setup Equipment
2. Loopback Initiation
3. Jitter Tolerance

Stressed Eye Calibration
1. Setup Equipment
2. Adjust RJ
3. Adjust SJ
4. Measure TJ
5. Adjust Eye Height
USB 3.0 Stressed Eye Calibration Equipment Setup

1. Equipment
2. Adjust RJ
3. Adjust SJ
4. Measure TJ
5. Adj. Height

Pattern Generator

Must act as USB 3.0 transmitter – compliant data patterns, SSC, de-emphasis, in addition to stressed eye

Analyzer

3 m Reference Cable

Reference Channel

Calibrate here

Host Fixture-1

DUT will go here

Anlzr EQ

PG Channel

Adapt.
USB 3.0 Stressed Eye Calibration
Jitter and Eye Height

- Adjust RJ
- Adjust SJ
- Measure TJ
- Adjust Eye Height

Adjust RJ
2.42 +/- 10% ps-rms

Adjust SJ
All points on Jitter Tolerance Template (SJ amplitudes w/in +0/-10%)

Adjust Eye Height
128* mV +10/-0% (at 10^-6 BER)

* Recent changes

* Verify only*
USB 3.0 Receiver Test Flowchart

Setup Equipment
Adjust RJ
Measure TJ
Adjust Eye Height

Stressed Eye Calibration

Create worst case signal to test the receiver

DONE

Test receiver with stressed eye and added sinusoidal jitter (SJ) in Jitter Tolerance template

Jitter Tolerance

Setup Equipment
Loopback Initiation
Jitter Tolerance

Only needs to be performed once per setup
USB 3.0 Jitter Tolerance Testing Equipment Setup

Must be able to detect errors for BER (bit error ratio) measurement

Host Jitter Tolerance Test Setup

Pattern Generator

Reference Channel

3 m Reference Cable

Error Detector

Equipment

Loopback

Jitt. Tol.
USB 3.0 Jitter Tolerance Testing
Loopback Initiation

A series of **handshakes** between the Pattern Generator and DUT initiate loopback.

**Notes:**
1. Once in loopback, the DUT should not exit loopback unless directed.
2. “Loopback BER”, where the DUT keeps track of its own BER, is not required for compliance testing.
USB 3.0 Jitter Tolerance Testing
Asynchronous BER Testing

**Clock compensation symbols (SKPs)** are used to adjust for the differing clock frequencies in the received data vs. the transmitter (common in 8b/10b systems).

ED must maintain sync in spite of non-deterministic number of SKPs.

Inserted SKPs (Recovered clock slower than local clock).

DUT in Loopback mode

Recovered Clock = PG Clock
USB 3.0

Run Jitter Tolerance

Test each point with $3 \times 10^{10}$ bits. The DUT fails if one or more errors is found or if it loses bit lock.
USB 3.0
BERTScope Instrumentation

**BERTScope DPP** (3 and 4 tap) for compliant 3 dB de-emphasis

**BERTScope CR 125A** with Extended Loop Bandwidth Option for compliant JTF

**BERTScope 85C** for integrated stressed pattern generation (RJ, SJ, and SSC) and BER analysis including jitter, eye height, CTLE emulation, asynchronous BER testing and automated Jitter Tolerance testing.
USB 3.0 Host DUT

- Equipment
- Stressed Eye
- Loopback
- Jitter Tol.

Example – Rx Test

To Error Detector

From Pattern Generator

Type A Port

PG Ana/ED

Channel

DUT

PCI Express Interface Card

Host Fixture 1
USB 3.0 Stressed Eye Calibration

Jitter

For **Stressed Eye Calibration**, we need to **inject jitter from the PG** and **measure jitter in the Analyzer**.

**Jitter Map** tool performs **BER-based Jitter Decomposition** and quickly measures to depths lower than $10^{-6}$.

**Example – Rx Test**

Stress Pattern Generator control shows RJ and SJ injection.
USB 3.0 Stressed Eye Calibration
Eye Height

Example – Rx Test
1. Equipment
2. Stressed Eye
3. Loopback

Eye height should be measured at $10^{-6}$ depth – the BERTScope quickly measures deeper than this.
USB 3.0 Stressed Eye
CTLE Equalization Emulation

1. Measure difference in eye height and jitter
2. Subtract from measured eye height and TJ from previous slides

Equipment

Loopback

Jitter Tol.

Example – Rx Test

1. Equipment
2. Stressed Eye
3. Loopback

Averaged waveforms show only data dependent effects, shown on CP3

Without EQ: CTLE

With EQ: CTLE

1. Measure difference in eye height and jitter
2. Subtract from measured eye height and TJ from previous slides
USB 3.0
Final Stressed Eye

Stressed Eye Calibration only needs to be performed once per setup

(Setup is different for Hosts and Devices)
USB 3.0
Loopback Initiation

Patterns available at www.bertscope.com

Equipment
Stressed Eye
Loopback
Jitter Tol.

Example – Rx Test

Use flexible two-page pattern memory to flip between loopback initiation sequence and test data pattern

Patterns available at www.bertscope.com
USB 3.0 Loopback Confirmation

1. Equipment
2. Stressed Eye
3. Loopback

a. Confirm that the DUT is in loopback
b. Enable Symbol Filtering to get ED in sync
c. Inject an Error from the Generator
d. Watch the Errors Increment in the Detector
USB 3.0
Jitter Tolerance Test

Example – Rx Test
1. Equipment
2. Stressed Eye
3. Loopback

Test 3x10^10 bits for each test point

Use stressed eye plus calibrated SJ amplitudes

Test for compliance

Use Search mode to find device limits

[Graphs showing Jitter Tolerance Margin]
USB 3.0 Automation Software

- Automated stressed eye calibration
- Fast automated receiver testing
- Easy loopback initiation
- Database back-end for fast report generation
SATA Rx Compliance Testing
SATA Frame Error Count

1. Monitor FEC with a protocol analyzer to check CRC etc.

2. Grab a reference frame & count number of resynchronizations

SATA receiver testing requires use of Frame Error Count

Methods 1 & 2 are accepted as equivalent.
SATA
Grab Mode (Running Disparity)

Allows visibility of sources of errors, or highlights abnormal behavior, rather than just giving a blind number.
SATA Testing Decision Circuit

“Analog” input waveform → Receiver → 101001011100 → FIFO

Data matching Local Clock Domain

Receiver → Decision Circuit → CDR

101001011100
Count mistakes (Measure FEC)
Resyncs 8

Testing uses an incoming waveform that is impaired in timing (jitter) and amplitude.
SATA Testing CDR

Testing uses an incoming SSC waveform, looks for mistakes when lock is lost.
SATA Testing FIFO (+-350ppm timing offset)
SATA Compliance and beyond

Receiver Testing:
1. Generate stressed framed COMP pattern
2. Received pattern retimed and looped back to output of transmitter
3. If clock domains differ between received signal and system clock, aligns inserted.
4. Increase impairments, mistakes detected in CRC etc. at FEC detector
5. Gives basic **Compliance**
   - No information about where failures occurred, or individual margins

**Beyond Compliance – margin testing**
1. By keeping clock domains the same, can stop aligns being added and see the effect of different stress types.
2. Can analyze margin in different parts of the receiver.
PCIE Rx Compliance testing

All information in these slides are based on the PCI-Express draft 0.71
PCI Express Agenda

- PCIe Gen3 Receiver Testing
  - Stressed Voltage Eye
  - Stressed Jitter Eye

- Speed and Equalization Auto-Negotiation

- PLL Loop Bandwidth Testing
PCle Gen3 Receiver Testing

- Split up into testing with two types of stressed eye
  1. Stressed Voltage Eye
  2. Stressed Jitter Eye
PCIE Gen3
Stressed Voltage Eye Calibration

1. Stressed Pattern Generator
   - 8 Gb PRBS Generator
   - RJ Source
   - Sj Source
   - Diff noise
   - CM noise
   - EH adjust

2. Channel
   - Calibration Channel
   - Replace Channel
   - Test Equipment
   - Post processing scripts:
     - Rx p/kg model
     - Behavioral CTLE/DFE
     - Behavioral CDR

3. Analyzer
   - DPO/DSA71604B
   - EH: depends on calibration channel
     - 0.30 UI <= EW <= 0.35 UI
     - Both at 10^-12 BER

DPP125A
Pre-Emphasis
PCIE Gen3 Stressed Voltage Eye

Stressed Pattern Generation

Pre-emphasis presets and coefficient space supported by BERTScope DPP125A

Built-in compliant Random and Sinusoidal Jitter – supports 2.5, 5, and 8 GT/s PCIe

Sinusoidal Interference (for DM/CM Interference) available externally for combining after pre-emphasis
PCIE Gen3 Stressed Voltage Eye Analyzer

CTLE, DFE, and Package Model emulation with SDLA Software Option

Compliant Jitter Transfer Function

BERTScope Pre-Emphasis

Test Equipment

Post-processing scripts:
- Rx pkg model
- Behavioral CTLE/DFE
- Behavioral CDR

EH: depends on calibration channel
0.30 UI <= EW <= 0.35 UI
Both at 10^-12 BER

Taktronix

DPO/DSA71604B
PCIE Gen3 Stressed Voltage Eye

Channel

3 channel lengths = 3 different stressed eyes

BERTScope ISI Board For Calibration Channel
PCIE Gen3
Stressed Voltage Test

BERTScope performs BER test.

Stressed Voltage Eye applied to DUT

DUT placed in Loopback for BER Test

Loopback

BERTScope with Clock Recovery CR125A
PCIE Gen3
Stressed Jitter Eye Calibration

Similar requirements as the Stressed Voltage Eye
PCIE Gen3 Stressed Jitter Test

Jitter Tolerance

Stressed Jitter Eye applied to DUT

DUT placed in Loopback for Jitter Tolerance Test

BERTScope performs Jitter Tolerance Test

Automated Jitter Tolerance Test on the BERTScope, with Search Mode to find device limits
Summary of BERTScope Rx Test Capabilities for PCIe Gen3

- **BERTscope Stressed Pattern Generation**
  - Random Jitter
  - Sinusoidal Jitter
  - Pre-emphasis (DPP125A)
  - Differential Mode Interference
  - Common Mode Interference
  - Calibration Channel (ISI Board)

- **BERTScope Error Detection**
  - Clock Recovery (CR125A)
  - Automated Jitter Tolerance Test
  - BER testing

- **The BERTScope Family of Products**
  provides the stresses needed for PCIe Gen3 with unrivaled ease of use, so engineers can quickly debug issues and find device margins
Summary of BERTScope Rx Test Capabilities for PCIe Gen3 (Continued)

- Oscilloscope (for Stressed Eye Calibration)
  - CTLE
  - DFE
  - Behavioral package emulation
  - Clock Recovery for Compliant Jitter Transfer Function

- The Tektonix DPO/DSA71604B provides compliant embedding of the Receiver equalization for accurate measurements as would be seen at the latch of the Receiver, providing the right feedback to the BERTScope Stressed Pattern Generator during Stressed Eye Calibration
PCIE Gen3 Agenda

- PCIe Gen3 Receiver Testing
  - Stressed Voltage Eye
  - Stressed Jitter Eye
- Speed and Equalization Auto-Negotiation
- PLL Loop Bandwidth Testing
PCIE Gen3
Speed and Equalization Auto-Negotiation

- Devices must start up at 2.5 GT/s and negotiate up to 8 GT/s
- In PCIe Gen3, Receivers are expected to:
  1. Optimize their own equalization
  2. Adjust the Transmitter’s pre-emphasis settings via back-channel communication

- Device equalization optimization algorithm will be key to PCI-Express Gen3 success, and we are here to help you test
PCIE Gen3
Speed and Equalization Auto-Negotiation with the BERTScope

- Use the BERTScope for R&D testing of new Gen3 devices
  - Fixed data patterns can perform the speed negotiation to 8 GT/s and allow the user to check (manually) their DUT’s equalization optimization routine
  - With a fixed pattern, can get devices into Loopback for Receiver testing of early R&D Silicon
PCIE Gen3 Transmitter Pre-emphasis

- The DPP125A supports the allowable pre-emphasis settings (table below from draft 0.71)
- The colored fields in the table are the “pre-sets” which are easily loaded from factory created configuration files

![DPP125A](image)

**Figure 4-514-504-504-50: TxEQ Coefficient Space Triangular Matrix Example**
PCIE Gen3
Agenda

- PCIe Gen3 Receiver Testing
  - Stressed Voltage Eye
  - Stressed Jitter Eye
- Speed and Equalization Auto-Negotiation
- PLL Loop Bandwidth Testing
PCIE Gen3 PLL Loop Bandwidth Test

- The BERTScope CR125A-PCIE is the test instrument used for PCI-Express Gen2 PLL Loop Bandwidth testing (2.5 and 5 GT/s) at the Compliance Workshops.
- Clock recovery capability at 8 GT/s facilitates testing of Gen3 devices.
- Higher speed models support 16 GT/s for future PCIe Gen4.
PCIE Gen3
Summary

- Receiver testing is expected to be mandatory and will include testing with a Stressed Voltage and Stressed Jitter Eye

- Equalization auto-negotiation controlled by the Receiver is new for Gen3

- Tektronix can provide solutions for many aspects of receiver testing to PCIe Gen3 today
  - Tektonix, including the BERTScope, has a strong history providing test solutions for PCI-Express – one that we plan to continue
  - The BERTScope supports data rates to 8.5G, 12.5G, and 17.5G for current and future PCIe projects
  - Contact us for further details on our plans for Gen3 support
## One Stop Shopping For HSSD From Tektronix

<table>
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<tr>
<th><strong>Transmitter Tests</strong></th>
<th><strong>DSA/DPO/MSO 71254B / MSO71254 or higher bandwidth</strong></th>
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<td>Transmitter jitter and timing measurements.</td>
<td>Opt. USB-TX (TekExpress Automation and DPOJET Measurements)</td>
<td><img src="image1.png" alt="Image" /></td>
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<tr>
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<td>Opt. DPOJET Jitter and Eye Diagram Analysis Tool</td>
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<td>TF-USB3-AB-KIT (Host and Device Test) or TF-USB3-A-P (Host Test) or TF-USB3-A-R (Device Test) Test Fixture</td>
<td></td>
</tr>
</tbody>
</table>

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<th><strong>Receiver Tests: Signal Generation / Error Detection</strong></th>
<th><strong>AWG7122B w/ Opt. 6 and Opt. 8 and DSA/DPO/MSO 71254B / MSO71254 or higher bandwidth w/ Opt. STU and ERRDT</strong></th>
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<td>Receiver Jitter Tolerance Tests for Customers working with HDMI, DP, MIPI</td>
<td>SerialXpress SDX100 opt. ISI and SSC</td>
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<td>Flexible channel Emulation</td>
<td>TEKEXP USB-RMT for Full Automation</td>
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<td>TF-USB3-AB-KIT Test Fixture Kit</td>
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<th><strong>Receiver Tests: Error Detection</strong></th>
<th><strong>BERTScope BSA85C w/Opt. STR&amp;PVU</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Receiver Jitter Tolerance Test and Debug and Analysis Tools</td>
<td>DPP125</td>
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</tr>
<tr>
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<td>CR125A with Opt XLBW &amp; Opt CR125ACBL (Precision delay-matched cable set for use with BSA &amp; CR in SSC applications)</td>
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<th><strong>Interconnect/Cable Tests</strong></th>
<th><strong>DSA8200</strong></th>
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<td>Cable skew, Far End Noise, Near End Noise, cable and connector impedance, Insertion loss, and return loss measurements.</td>
<td>80E08 TDR Sampling Module for DSA8200 2 per scope</td>
<td><img src="image4.png" alt="Image" /></td>
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<td>IConnect TDR and S-Parameter measurement software (80SSPAR)</td>
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<tr>
<td></td>
<td>TF-USB3-AB-KIT Test Fixture Kit for Cable Test</td>
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Questions?
Thank You

Application Information at: www.bertscope.com