CENTELLAX

SPEED INNOVATION

Centellax Optical Communication Seminar

ShangHai

2010-03-31

www.centellax.com

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Centellax Background

Centellax delivers low-cost, high-performance test instruments, test accessories, and electronic components for high-speed communication and signal integrity applications

Test and Measurement

Telecom

Microwave

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Centellax Company

- *2001: Incorporated in Santa Rosa, CA.*
- *2002: First products for 40G telecom*
  - *Optical modulator drivers, SerDes*
- *2003: Introduced microwave products*
  - *Amplifier ICs, amplifier modules, programmable frequency dividers*
- *2005: Developed test product suite*
  - *Phy-level signal integrity focus*
  - *10G & 40G PRBS generators, BER Testers, CRUs, Synth, Amps*
- *2006: Introduced test systems*
  - *Jitter tolerance/transfer testing*
- *2009: Next generation instruments*
- *2010: Strong Product Roadmap and 3 new products to Market*

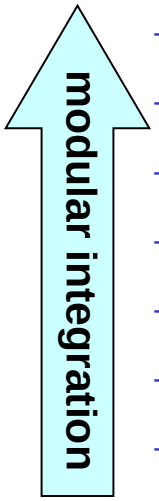
Centellax Know-how

Centellax core competency
- Analog & digital IC design
- Module design
- Instrument design
- Broad bandwidth / high-speed

Centellax value proposition
- High performance
- Low cost

Centellax product focus
- Test instruments & systems

Centellax technology portfolio
- Test systems
- Test instruments
- Test accessories
- Connectorized modules
- PC boards
- QFN packaged ICs
- GaAs and SiGe MMICs

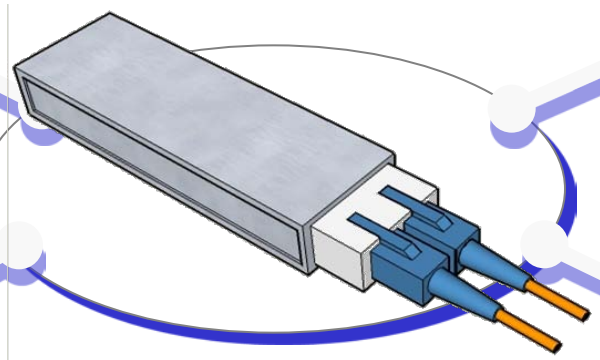


•Many 10G and 40G products are based on single-chip solutions!

Agenda

1. Introduction

2. Transmitter Testing



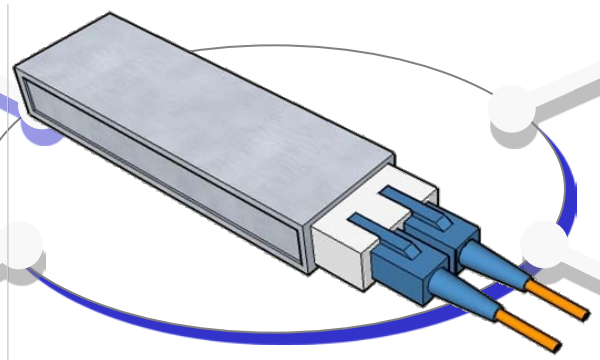
3. Receiver Testing

4. Practical BER Test Solutions

Agenda

1. **Introduction**

2. Transmitter Testing



3. Receiver Testing

4. Practical Solutions

Types of Transceivers

Type	Form Factor	Optical Data Rate	Electrical Data Rate	Standard/ Application	Notes
XFP		10 Gb/s	Same	10GbE, SONET/SDH	Widely deployed, low cost, mainly shorter distance applications.
SFP QSFP		1.25, 2.12, 4.25 Gb/s 4x5/10Gb/s	Same	Ethernet, Fibre Channel 1x, 2x, 4x Infiniband, QDR	Smaller than XFP, low cost, low data rates. 30% bigger size than SFP, 4 channel parallel.
SFP+		8.5, 10, 14 Gb/s	Same	Fibre Channel 8x,10x, 16x, 10GbE LRM	New, smaller than XFP for higher density 10Gb/s. 2 Variants, Limited & linear.
Xenpak/ X2		10 Gb/s	4x 3.125 Gb/s	10GbE	Older incarnation for 10GbE, larger than XFP, little R&D now.
300 Pin MSA		10 Gb/s 40Gb/s	16x 622M 16x2.488 Gb/s	SONET/SDH	Telecom transceiver for longer range applications. Higher quality/cost.

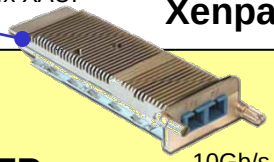
Transceiver Evolution Timeline

Enterprise

For architectures based on 4x 3.125 Gb/s shipping data around.

4x XAUI

Xenpak/X2



10Gb/s

QSFP

4 x 5/10Gb/s

Gb/s in = Gb/s out

SFP

1x FC, GbE

SFP

2x, 4x FC etc

XFP

10Gb/s

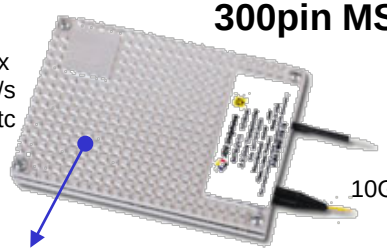
SFP+

8.5, 10, 14Gb/s

Telecom

300pin MSA

16x 622Mb/s etc



10Gb/s

For architectures based on 16 wide data

40Gb/s

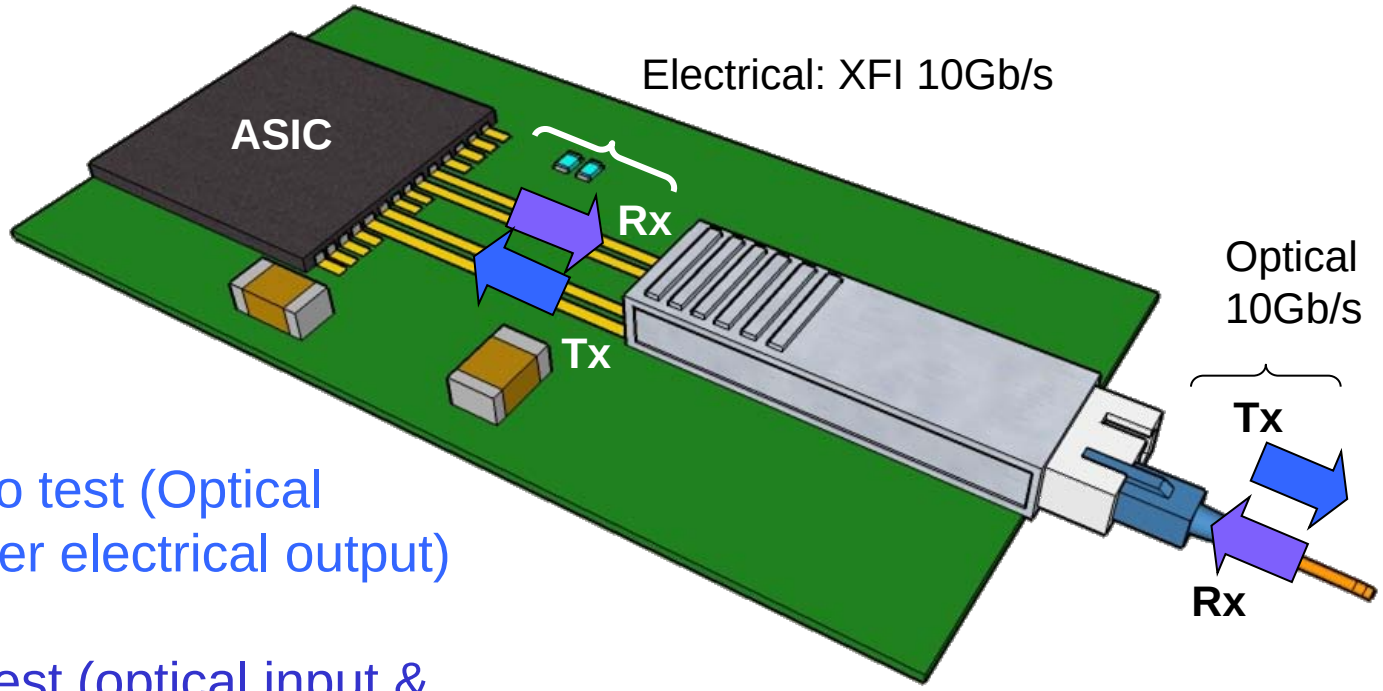
16 x 2.488b/s etc

300pin MSA

2000

2010

What Needs to be tested? XFP Example



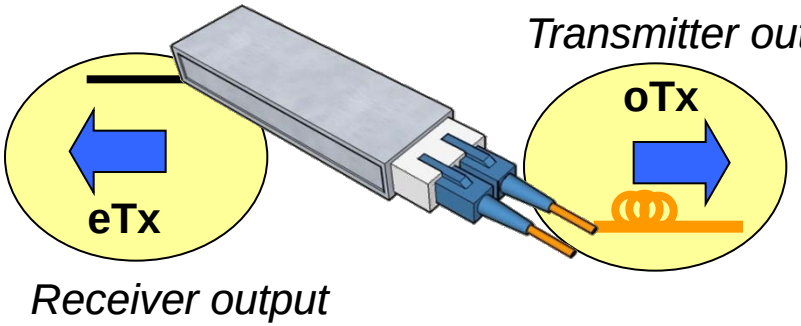
Transceiver has:

- 2 transmitters to test (Optical output & receiver electrical output)
- 2 receivers to test (optical input & transmitter electrical input)

Same principles apply for SFP (1.25, 2.12, 4.25 Gb/s)
Same for SFP+ (8.5, 10, 14 Gb/s)
Similar for 300 pin (electrical side has more low speed lanes that add up to 10 Gb/s)

How are Transmitter & Receivers Tested?

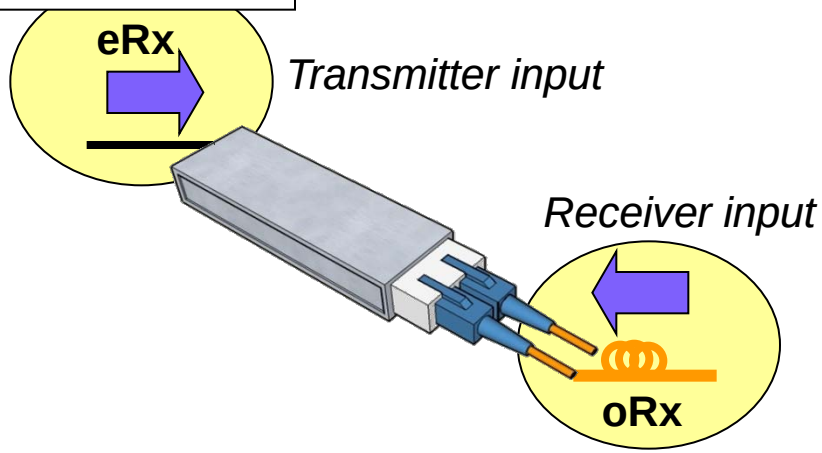
Transmitters



Mainly eye diagram based

- Quick
- Intuitive
- Usually involves testing against a mask.

Receivers



BER based*:

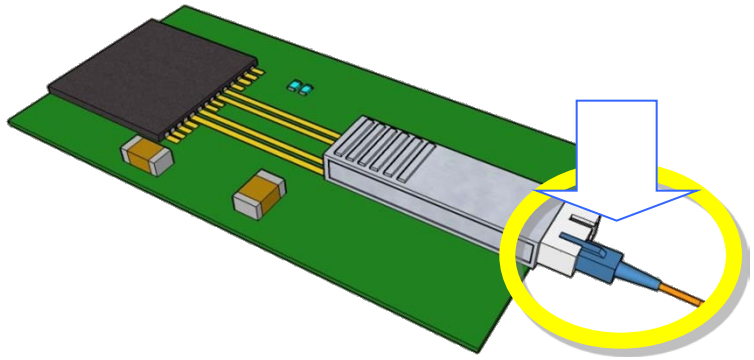
- Measuring that correct decisions were made
- Frequently also how well clock recovery is performing
- Output waveform of receiver gives no clue about whether errors were made.
- Less intuitive

**(SFP+ linear variant is different, with no decision circuit inside)*

The Remainder of the Presentation….

- Going to talk about:
  - Testing transmitters
  - Testing receivers

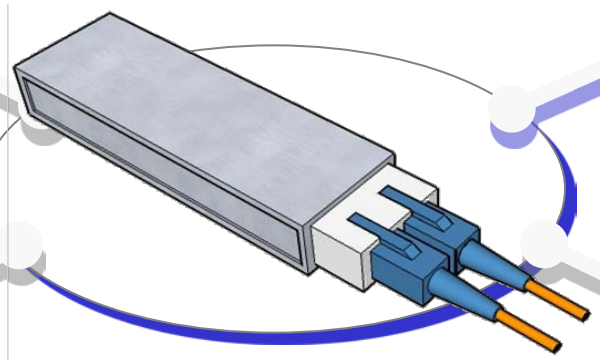
- We will focus on optical interfaces, although the same principles will apply to electrical interfaces such as XFI.
  See references at the end for information on testing XFI.



Agenda

1. Introduction ✓

2. **Transmitter Testing**



3. Receiver Testing

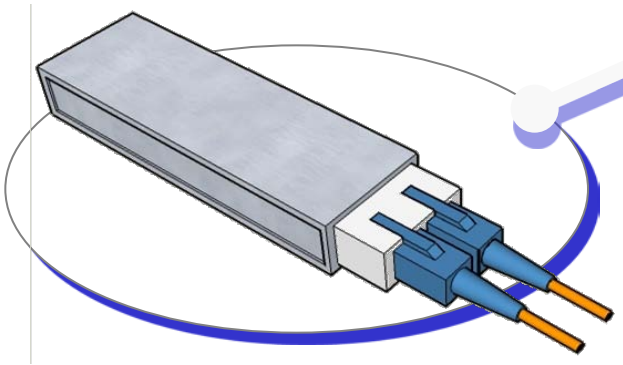
4. Practical Solutions

Agenda

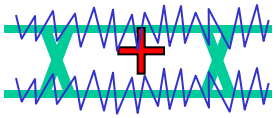
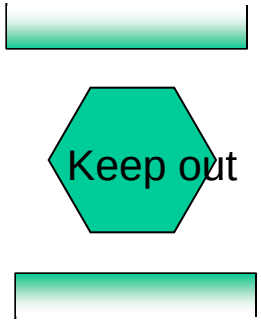
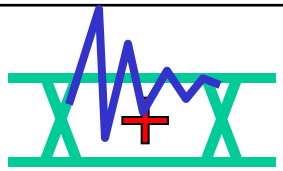
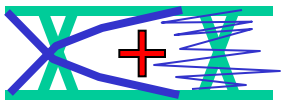
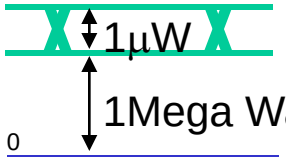
1. Why test transmitters?
2. Why use Clock Recovery?

2.

Transmitter Testing



Why Test Transmitters?

	Need	What can go wrong?	Resulting Parameter	Comment
1.	Verify that there is enough signal to be received at the other end.	Receiver errors because of signal to noise.	Power	Usually accomplished through mask specified in relevant standard.
2.	Need to know that there is enough difference between a 1 and 0 power level for a receiver to make the right decision*.		Vertical eye opening	
3.	Verify that overshoot and undershoot won't cause long distance eye closure from dispersion, AGC setting issues at the receiver.		Upper & lower limit regions of mask	
4.	Verify that there is enough eye opening in time for the receiver to make the right decision.		Rise time & jitter	
5.	Need to know that the transmitter is working efficiently and not wasting power.		Extinction ratio	Tricky measurement, difficult to get consistent results.

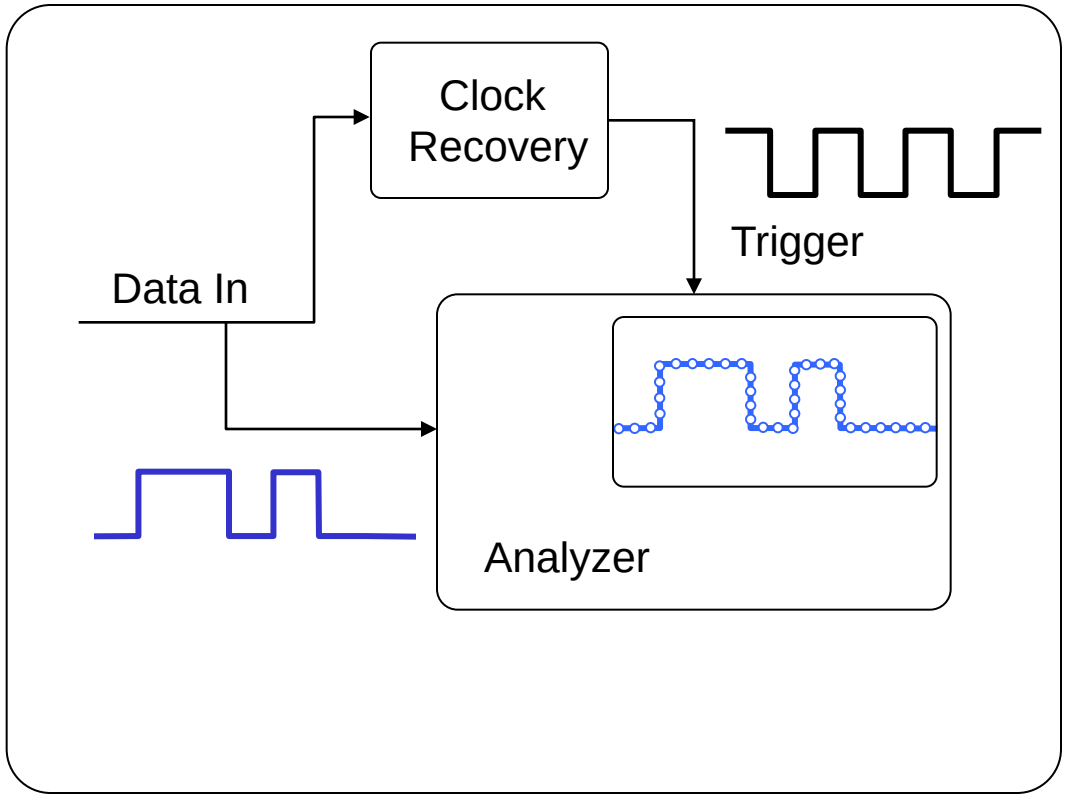
** Recent standards such as LRM use TWDP – more on this later*

Why Use Clock Recovery? (1)

- BERTs & Sampling Scopes require a synchronous trigger.

1. Some systems have ***no clock available*** (e.g. some 300 pin transceivers)

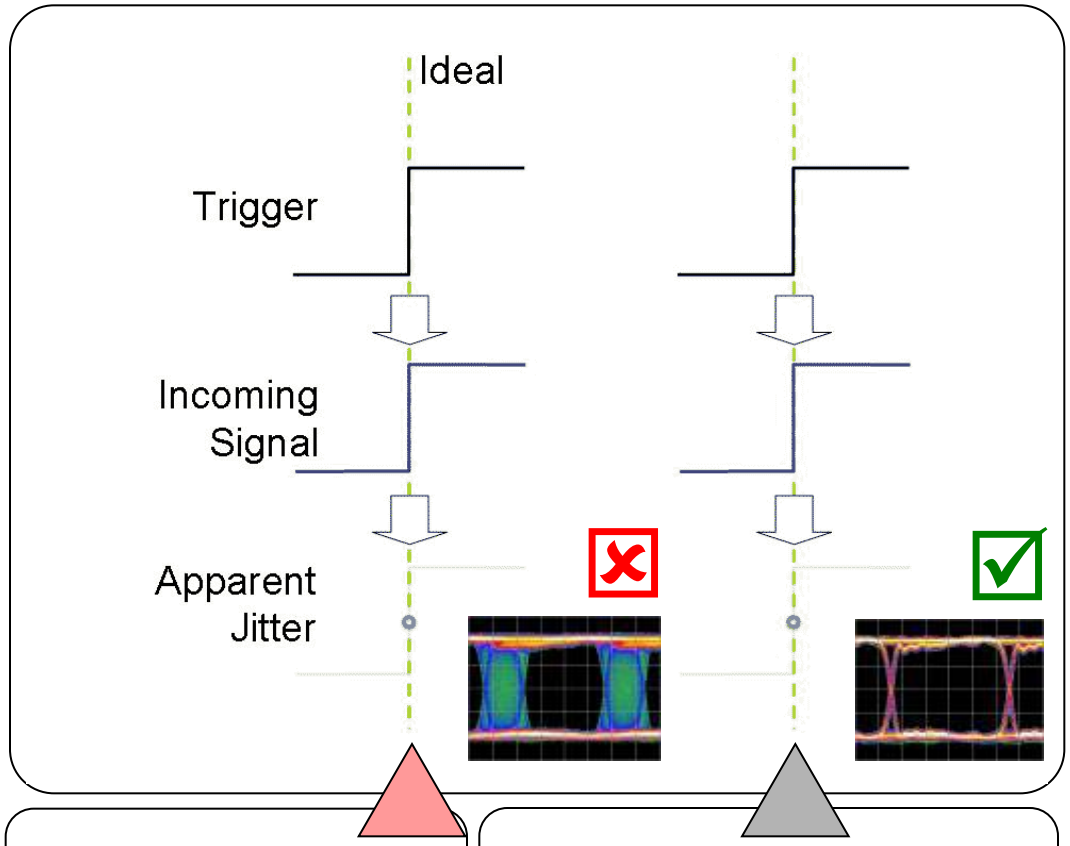
2. Often with systems or experiments using long fiber runs, effects such as polarization mode dispersion (PMD) ***destroy the relationship between the transmitter clock & arriving data.***



Why Use Clock Recovery? (2)

3. More subtle: **Handling of Jitter** in transmitter testing.

- Incoming data likely to have jitter on it.
- Up to a certain jitter frequency (~few MHz), jitter would be tracked by clock recovery in the system receiver.
- For transmitter test, don't want this to appear in the measurement – **only care about jitter that won't be tracked out by a receiver**. Hence use of clock recovery.



- Data is jittered.
- Trigger is not.
- Measurement samples appear jittered.

- Data is jittered.
- Trigger is jittered the same.
- Measurement samples don't show jitter within the CR loop bandwidth.

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Why Use Clock Recovery? (3)

- Mandated in many standards.

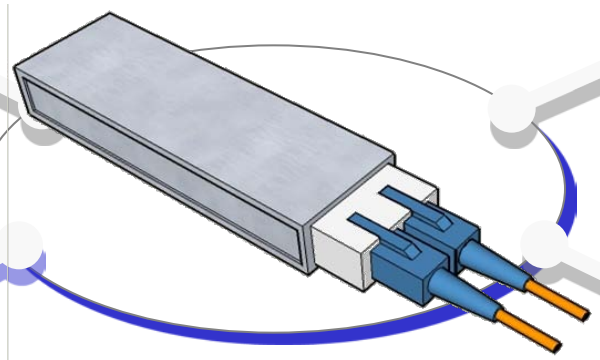
Standard			Data Rate (Gb/s)	Common Clock Divide Ratios	Loop Bandwidth (MHz)	Peaking (dB)	Slope	Clock Type	Spread Spectrum Clocking
Ethernet [4]	10 Gb/s Ethernet Transmitter Test		10.3125		≤4		–20 dB/ decade	Embedded	No
	XAUI		3.125		1.875				
Fibre Channel [5]	1X		1.063	10	0.638	0.3 max	–20 dB/ decade	Embedded	No
	2X		2.12	20	1.275	0.3 max			
	4X		4.25	40	2.550	0.3 max			
	8X		8.5	80	5.100	0.3 max			
SONET/SDH [8,9]	OC-12/STM-4		0.622		0.250		–20 dB/ decade	Embedded	No
	OC-48/STM-16		2.488		1.000				
	OC-192/STM-64		9.95		4.000				
XFP/XFI [10]	XFP/XFI	Receiver Test	9.95 - 11.2	64	8.000	0.1 max		Embedded	No
		Transmitter Test			4.000	0.1 max	–20dB/decade		

(Information applying to transmitter testing and receiver stress calibration.)

Agenda

1. Introduction ✓

2. ✓ Transmitter Testing

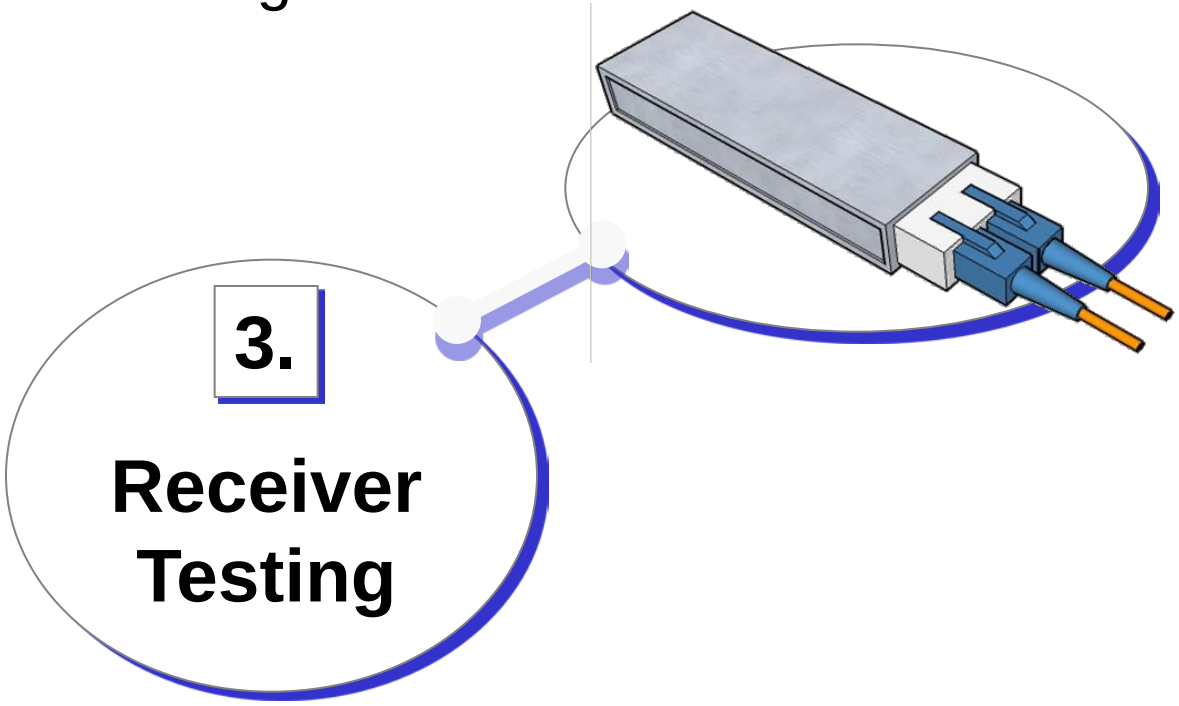


3. Receiver Testing

4. SONET/SDH Jitter Testing

Agenda

1. Why test a receiver?
2. Receiver Sensitivity
3. Testing Clock Recovery for Jitter Tolerance
4. Testing Receiver Tolerance with Stresses



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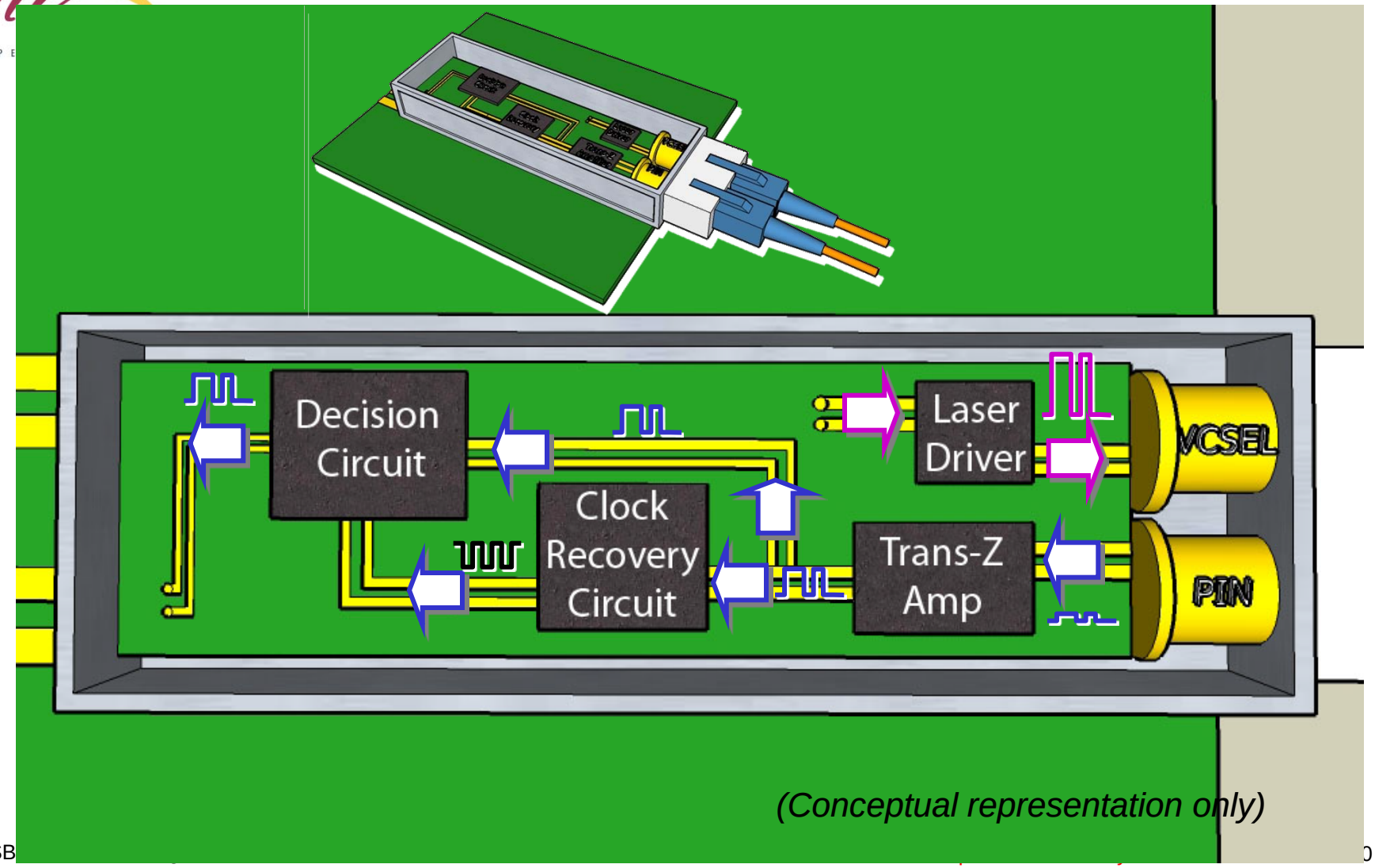
Inside Imaginary Transceiver



(Conceptual representation only)

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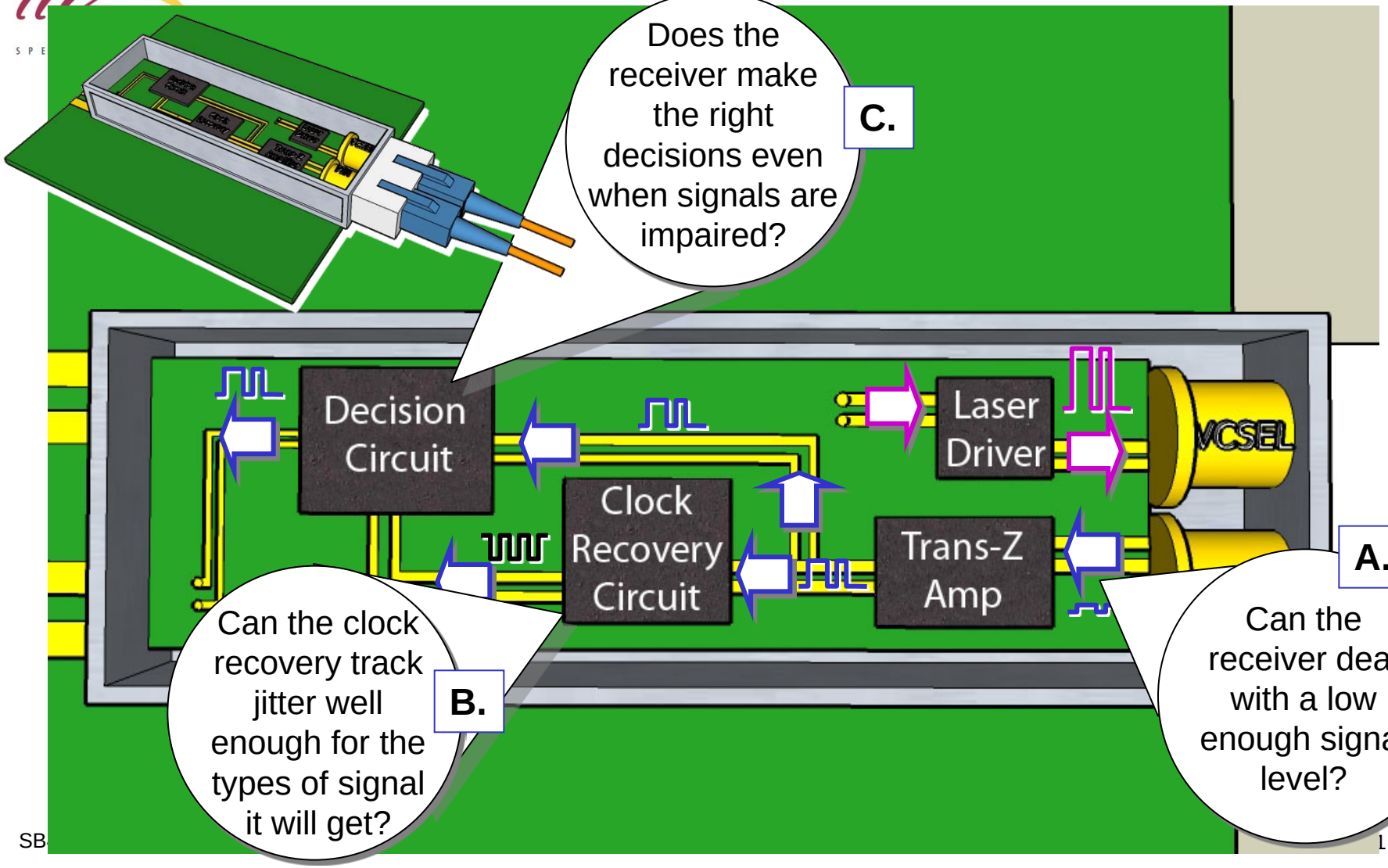
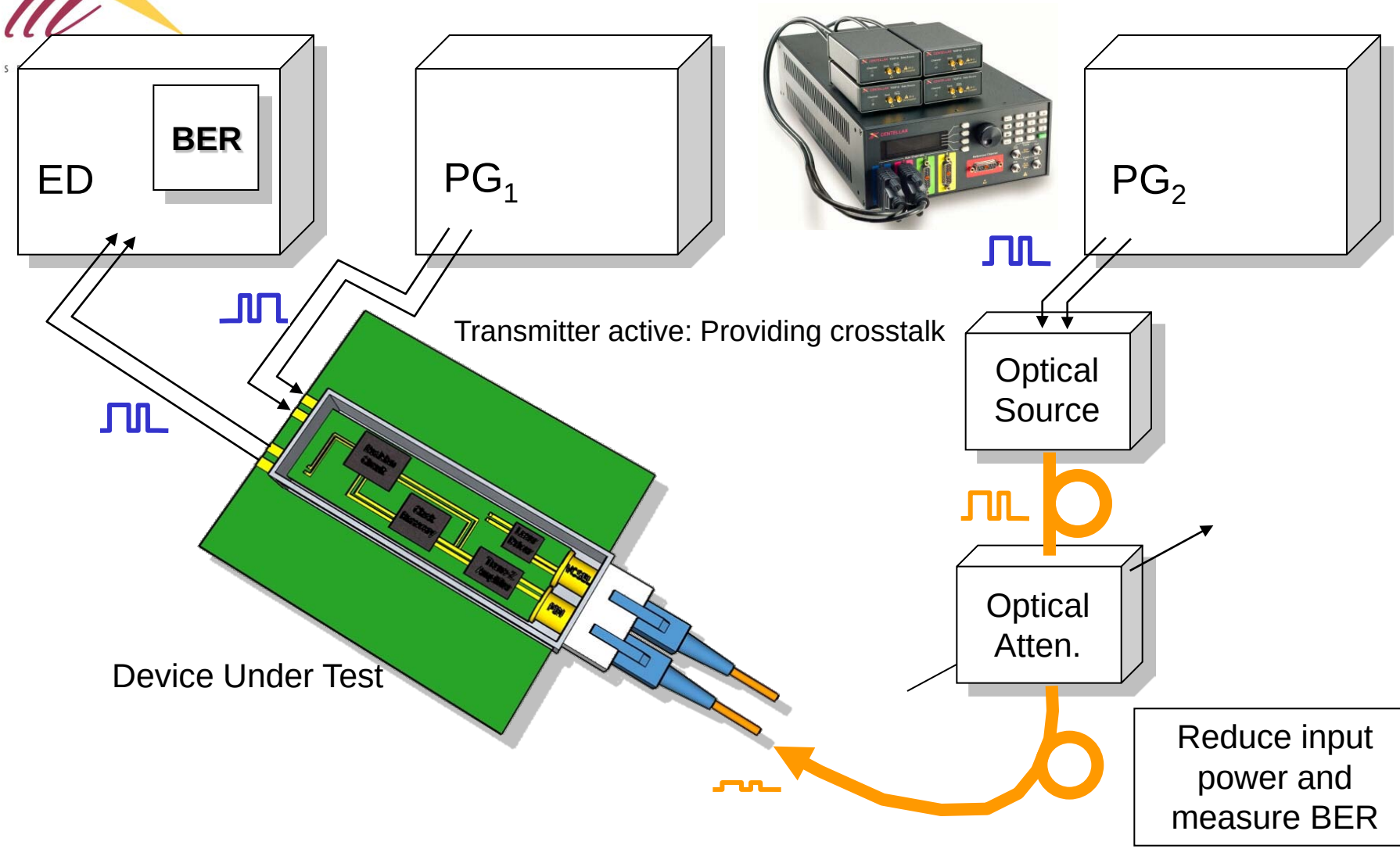
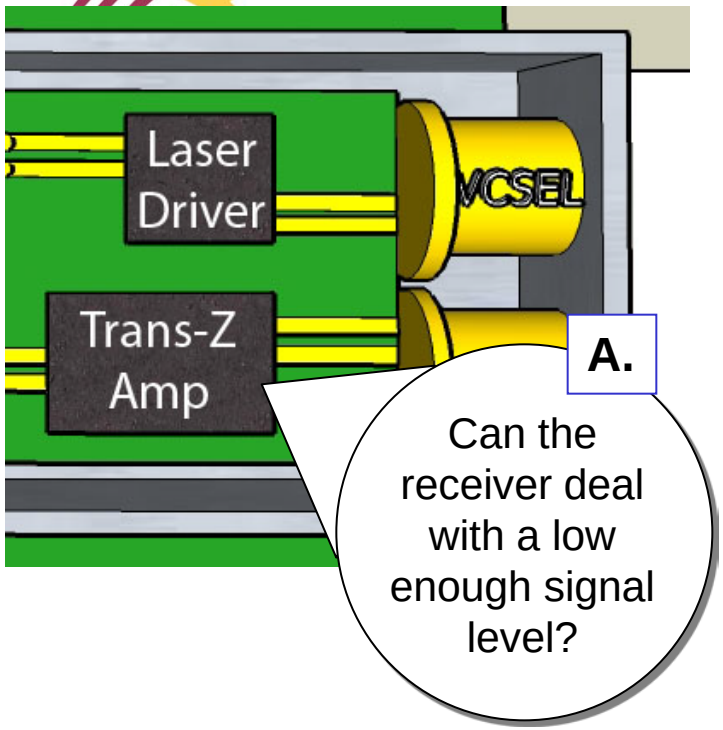
Why Test a Receiver?

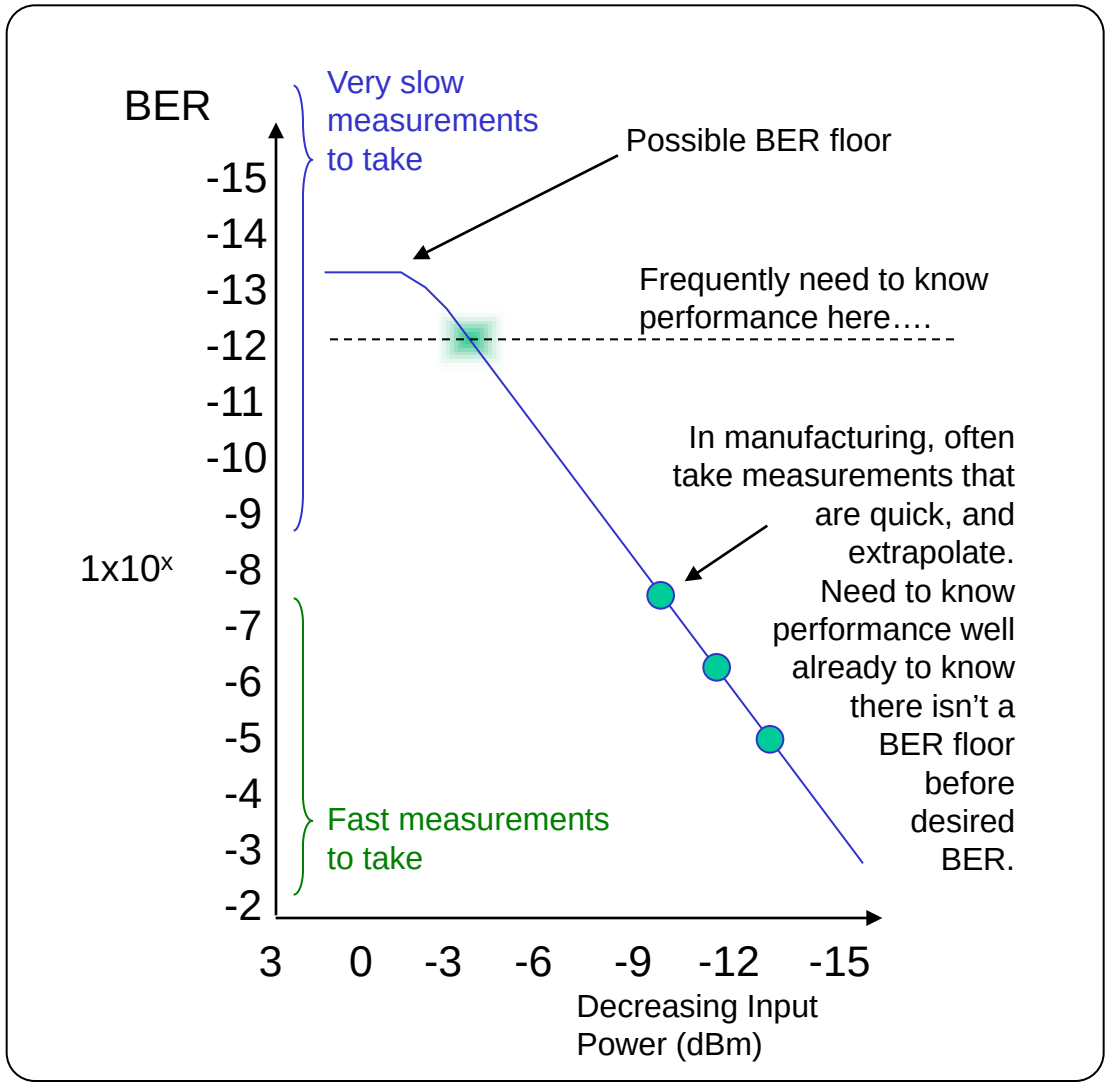


Receiver Sensitivity (Need A) (1)

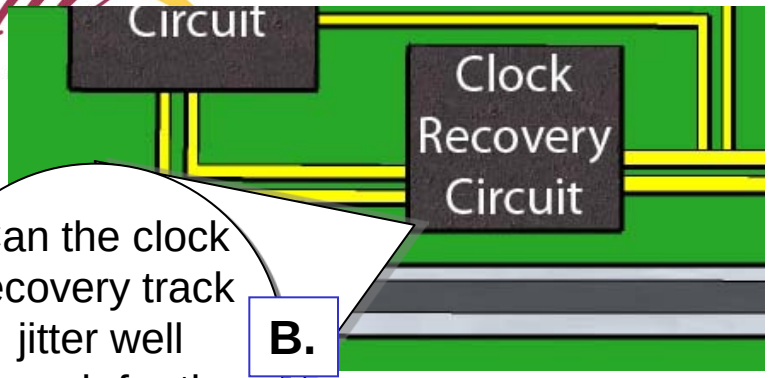


Receiver Sensitivity (2)





Testing Clock Recovery (Need B) "Jitter Tolerance Measurement"

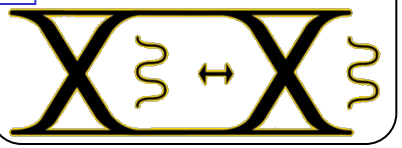


Can the clock recovery track jitter well enough for the types of signal it will get?

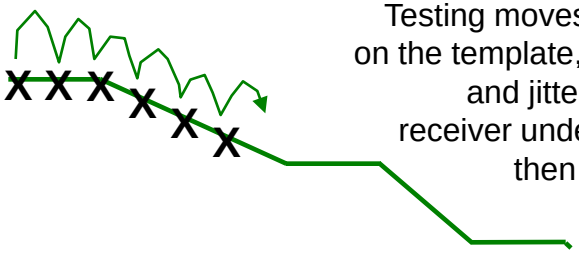
B.

1. Traditionally testing uses SJ (Sinusoidal Jitter) to exercise clock recovery.

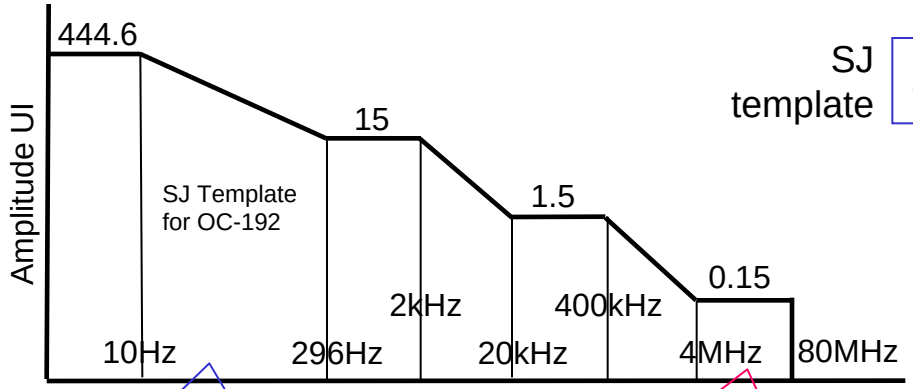
2. Data edges are modulated in time with a sine wave.

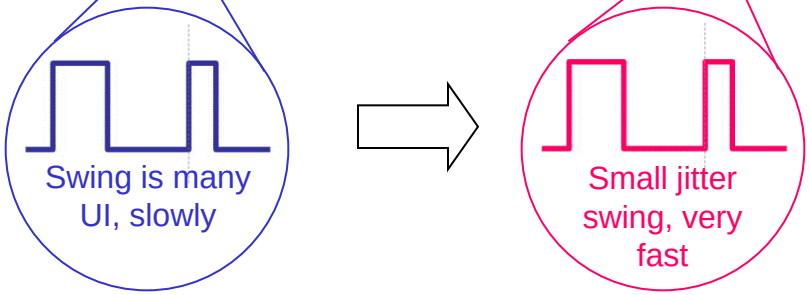


4. Testing moves from point to point on the template, sets the frequency and jitter amplitude, checks receiver under test for bit errors, then steps to next point.

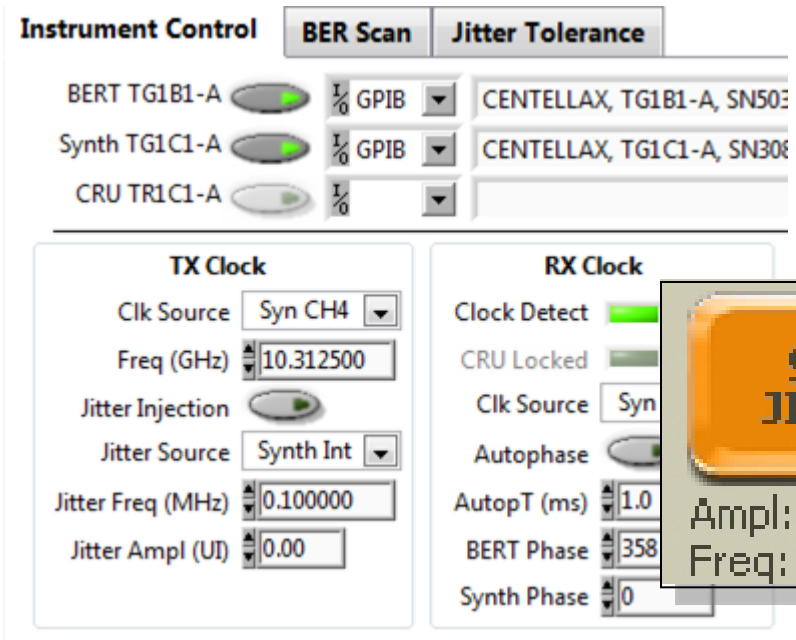


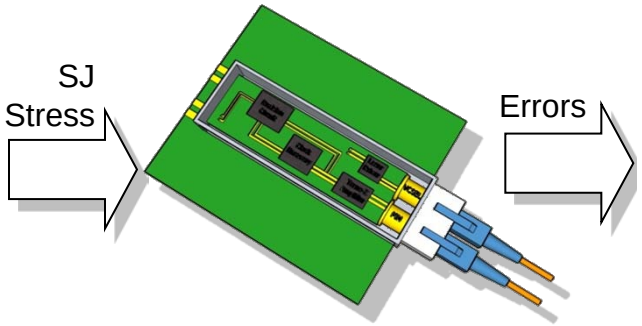
3. SJ template

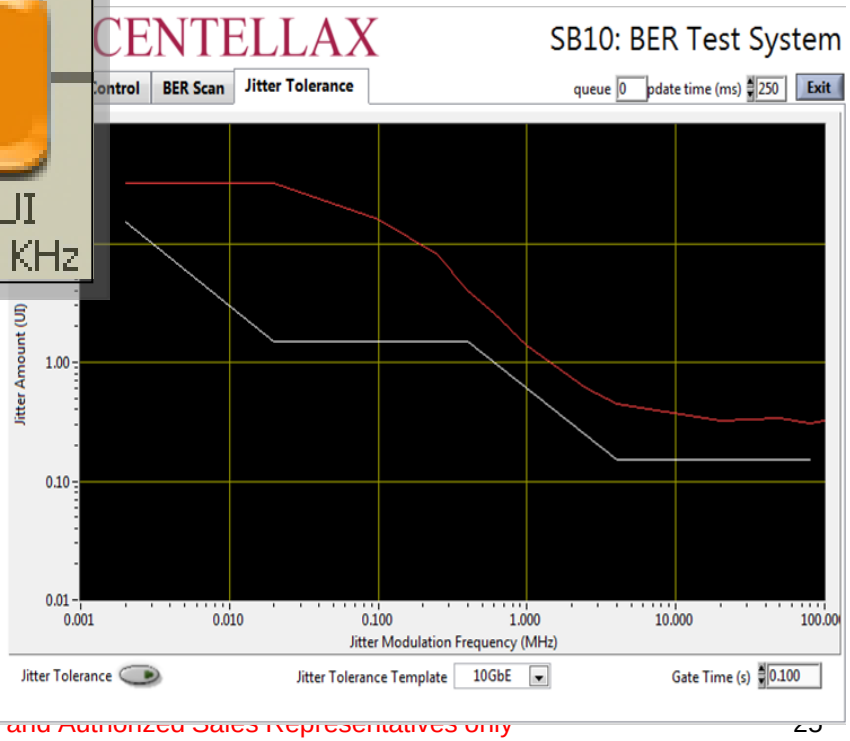




Jitter Tolerance Measurement







Typically, **automated template** software is built into test equipment to set the frequencies and amplitudes and to step through the template and analyze the errors

(Same physical setup as for sensitivity)

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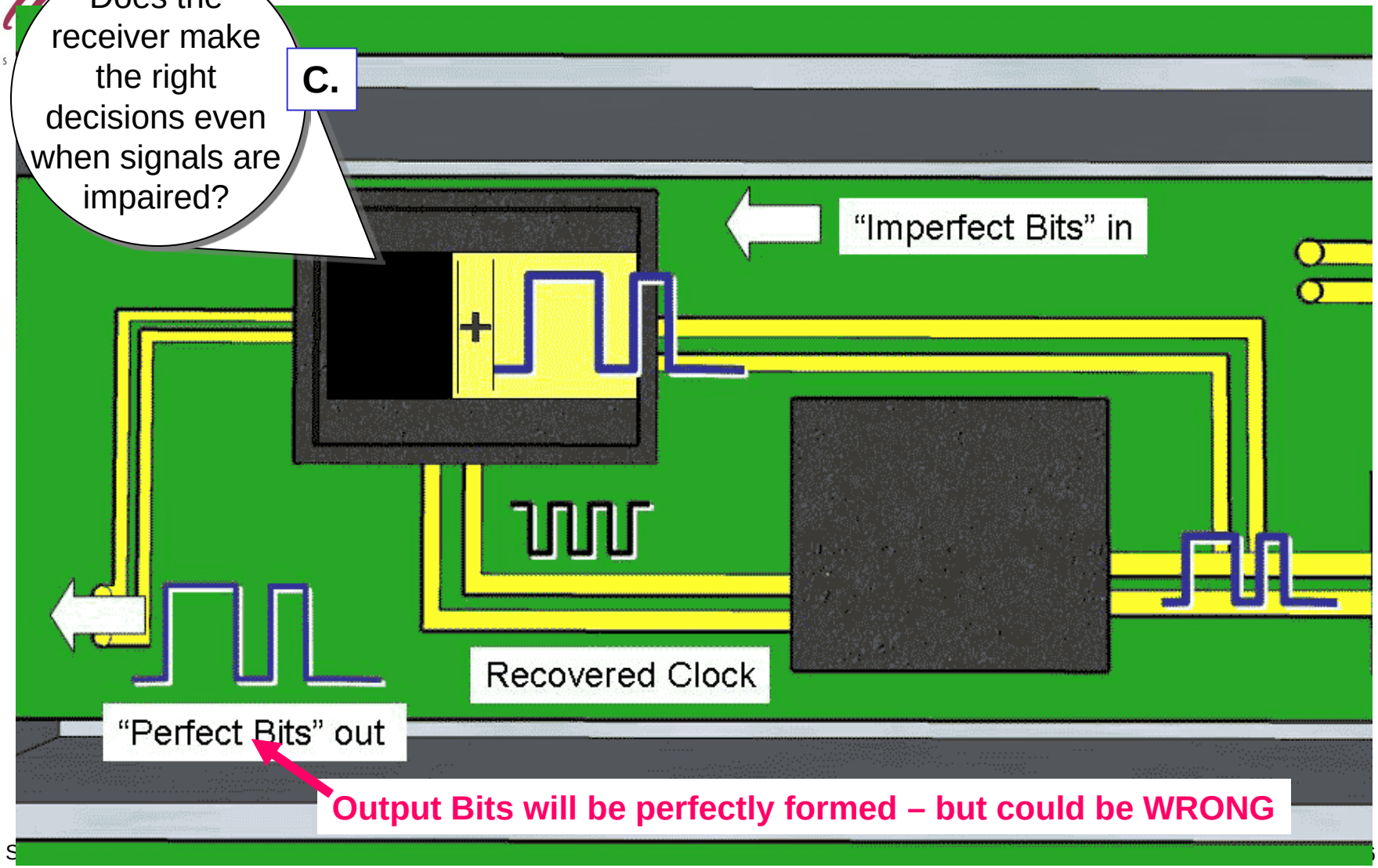
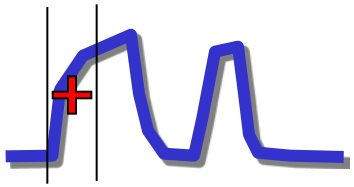
Testing the Receiver's Tolerance to Impairments (Need C)

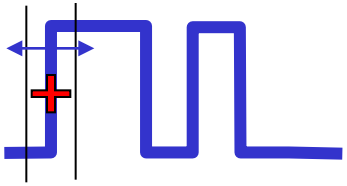


So What Can Go Wrong?

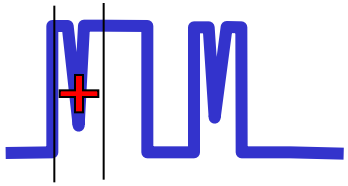
Example System Issues



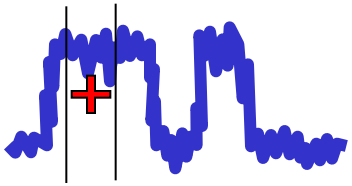
Circuit Board Dispersion
Fiber Dispersion
PMD



Edge Movement:
Frame slips
Frame overhead repetition
Pattern Sensitivity



External interference
Crosstalk



Low signal level
Other random effects

Test signal stress elements for receivers

Stresses Used by Different Standards

PRBS Jitter (BUJ)

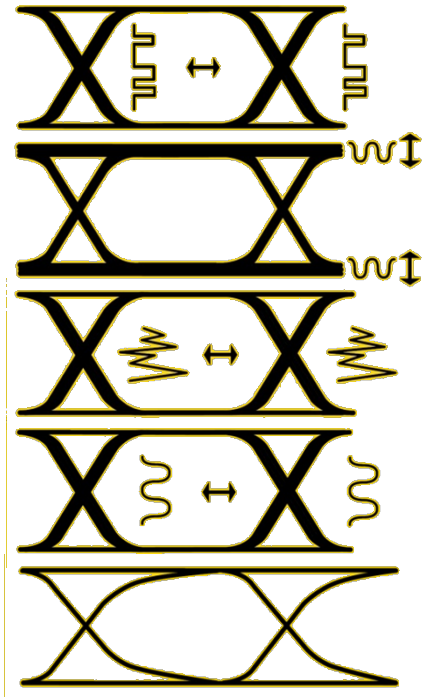
Sine Interference (SI)

Random jitter (RJ)

Sine Jitter (SJ)

Dispersion (ISI)

Dispersion (LRM)



(not discussed further here)

Receiver Tolerance Testing is now more than just Jitter Tolerance….

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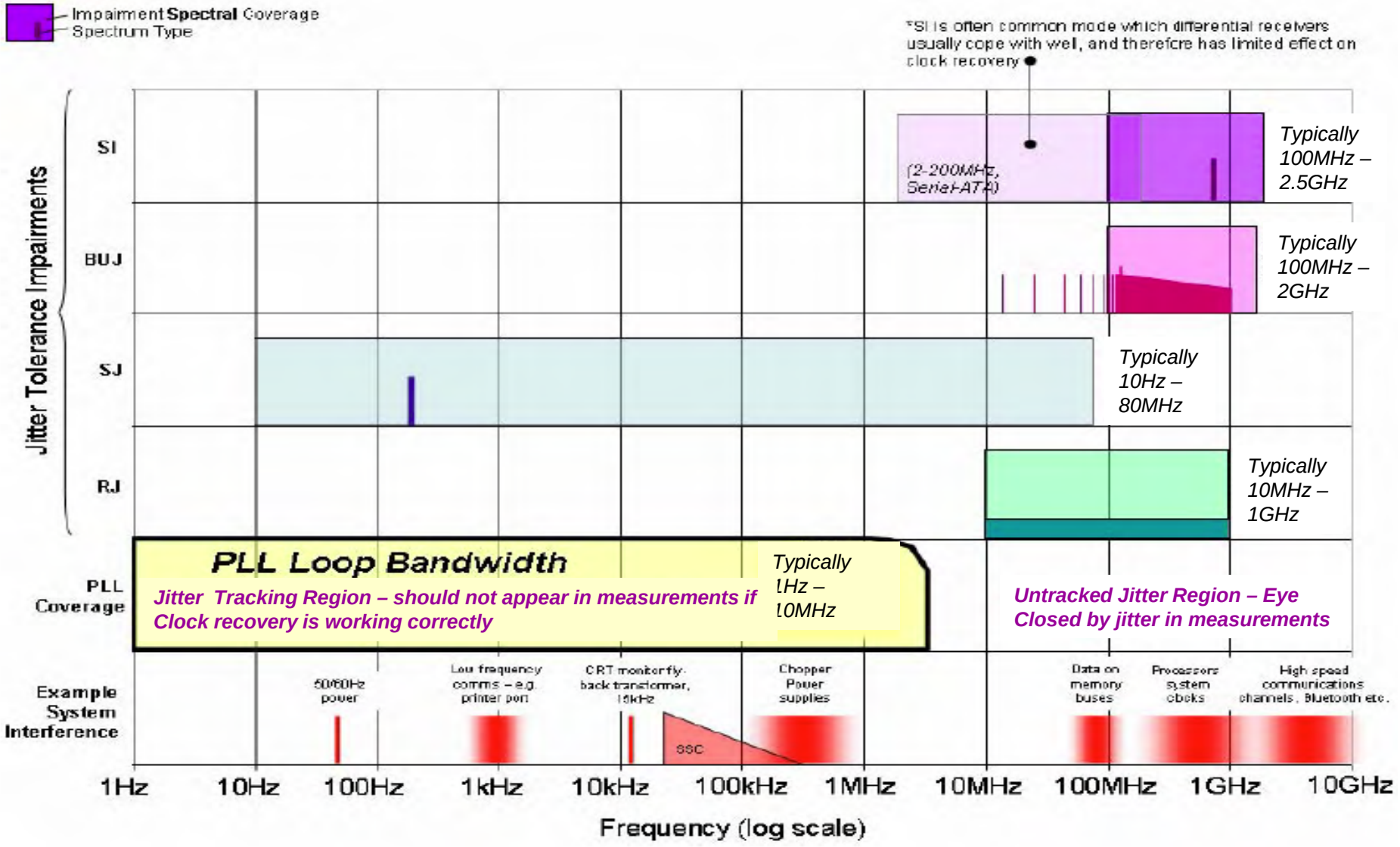
Rx Stress Spectral Coverage

Crosstalk is a headache problem!



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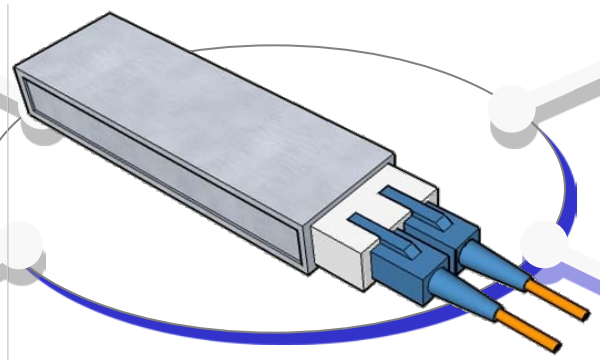
2. ✓ Transmitter Testing

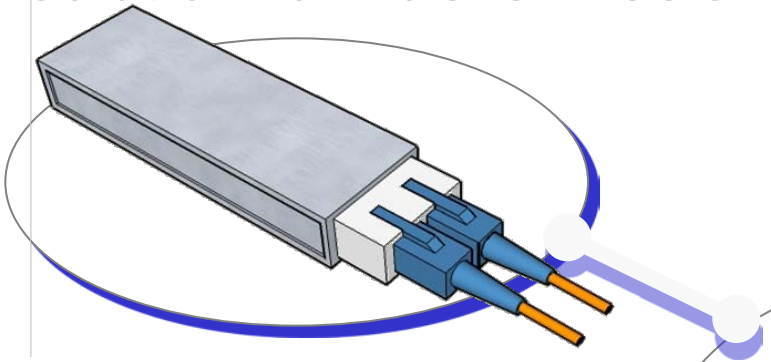


3. ✓ Receiver Testing

4. Practical BER Test Solutions

Agenda

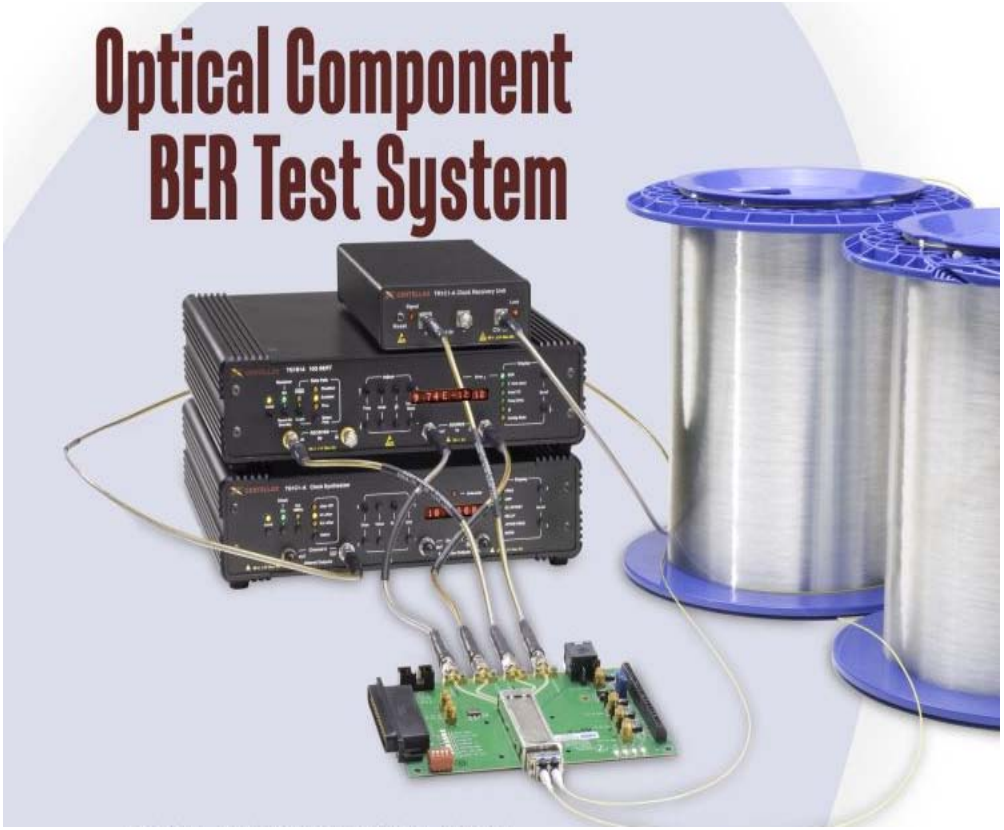
1. 500M-12.5Gb/s BERT solution for TOSA,ROSA, XFP,SFP,etc
2. 10GE SFP+ BERT solution
3. Parallel Channel BERT solution for QSFP, Crosstalk testing
4. 22G-40Gb/s BERT solution for 40G SDH/SONET, 100GE



4.

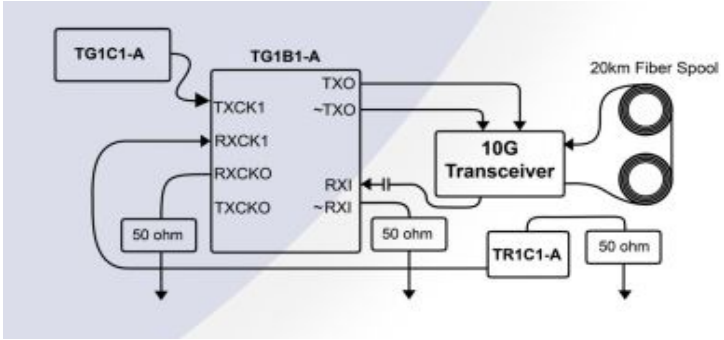
Practical BER Test Solutions

Optical Component BER Test System
-ROSA,TOSA, XFP,SFP,lasers,diodes,etc



OPTICAL COMPONENT BER TEST SYSTEM

- 500Mbps to 12.5Gbps AnyRate BER test solution for physical-layer testing
- Ideal for optical components: ROSA, TOSA, XFP, SFP, lasers, diodes, etc.
- Clock Recovery Unit handles PMD and other optical dispersion
- System shown: SB10+OPTC13+OPTS13, which includes 10G BERT, 13G Clock Recovery Unit, and 13G Clock Synthesizer
- Affordable price



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SFP+ Block Diagrams

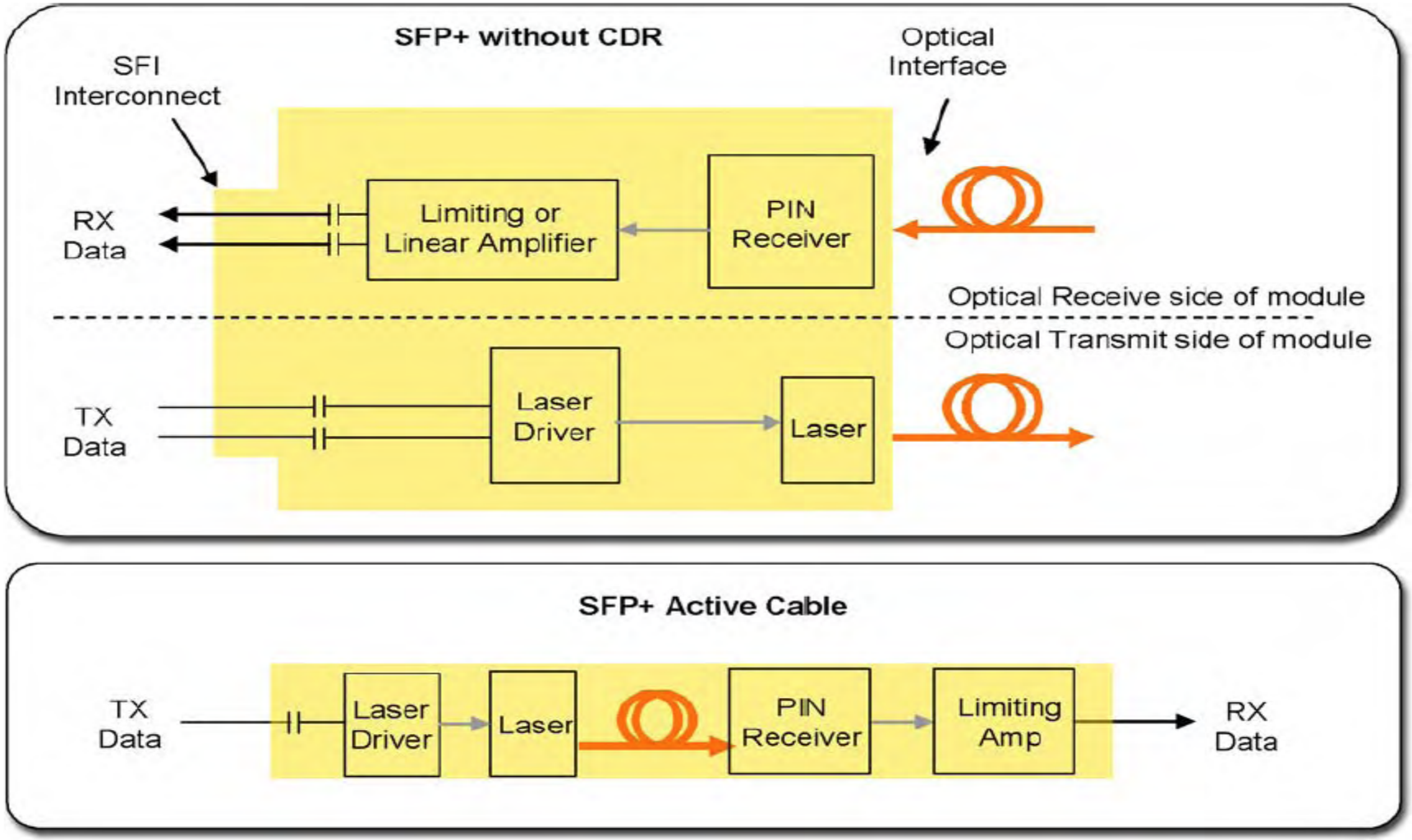
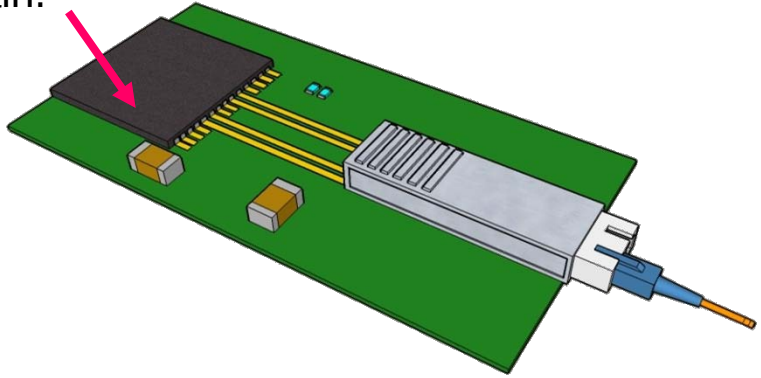


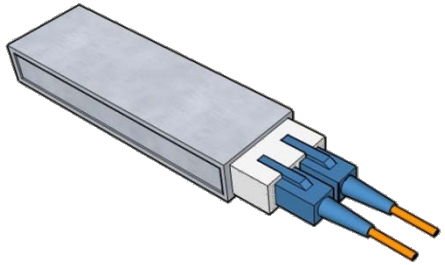
Figure 1. *SFP+ Transceiver and Active Cable (internal optical example, could also be copper with pre-emphasis and equalization) Simplified Block Diagrams*

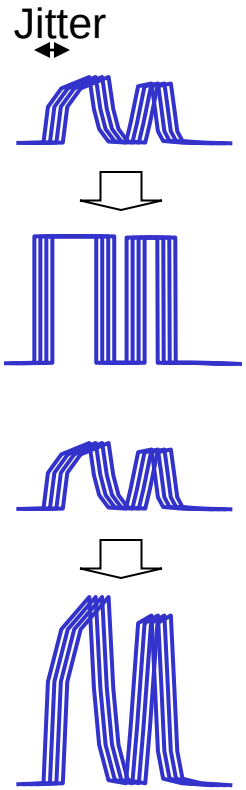
Brief Notes on SFP+

Notes:

- **SFP+** is intended to be smaller and cheaper than XFP, with lower power dissipation
- Same form factor as SFP (lower speed transceiver design)
- Many of the gains come from the receive side, having **some of the circuitry not included in the transceiver** – intention is that power hungry functions such as electronic dispersion compensation (EDC) etc. are performed on the next chip in the chain.





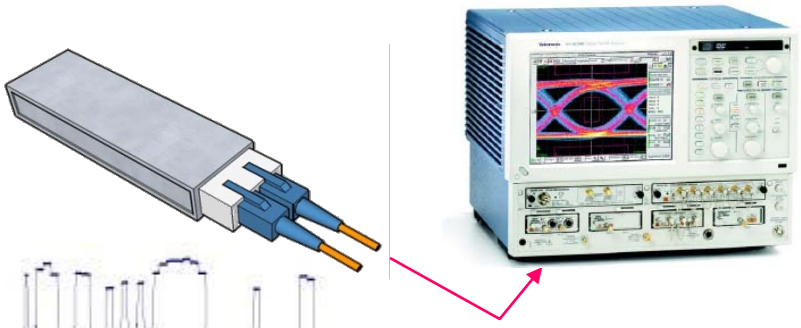


Two receiver designs:

- **Limiting**: No decision circuit, but the signal passes through a limiting amplifier. Some parametric information is lost.
- **Linear**: No decision circuit, only a linear amplifier with AGC. Output is amplified version of input, EDC can be applied later.
- Linear receivers is tested differently, not by BER. Need to measure Waveform Dispersion Penalty.

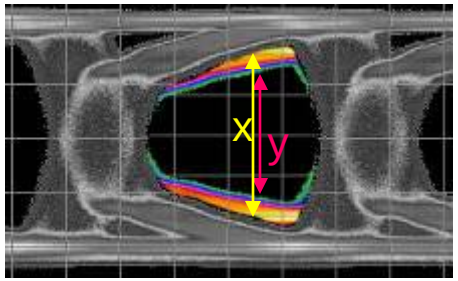
TWDP

- LRM (Long Reach Multimode, IEEE 802.3aq) is a 10GbE standard intended to allow 10Gb/s over older multimode fiber (220m).
- The biggest headache is multimode fiber dispersion
- Signal shape at a receiver can be difficult to predict.
- Transmitter performance not measured with an eye diagram directly: **T**ransmitter **W**aveform **D**ispersion **P**enalty (TWDP).
- **Output is a number.**



Long waveform capture

Math processing to simulate a standard set of fiber dispersion, a simulated receiver and the effect of electronic dispersion compensation (EDC)



Calculates a dispersion penalty: eye should be open x, is only open y, so penalty is x-y.

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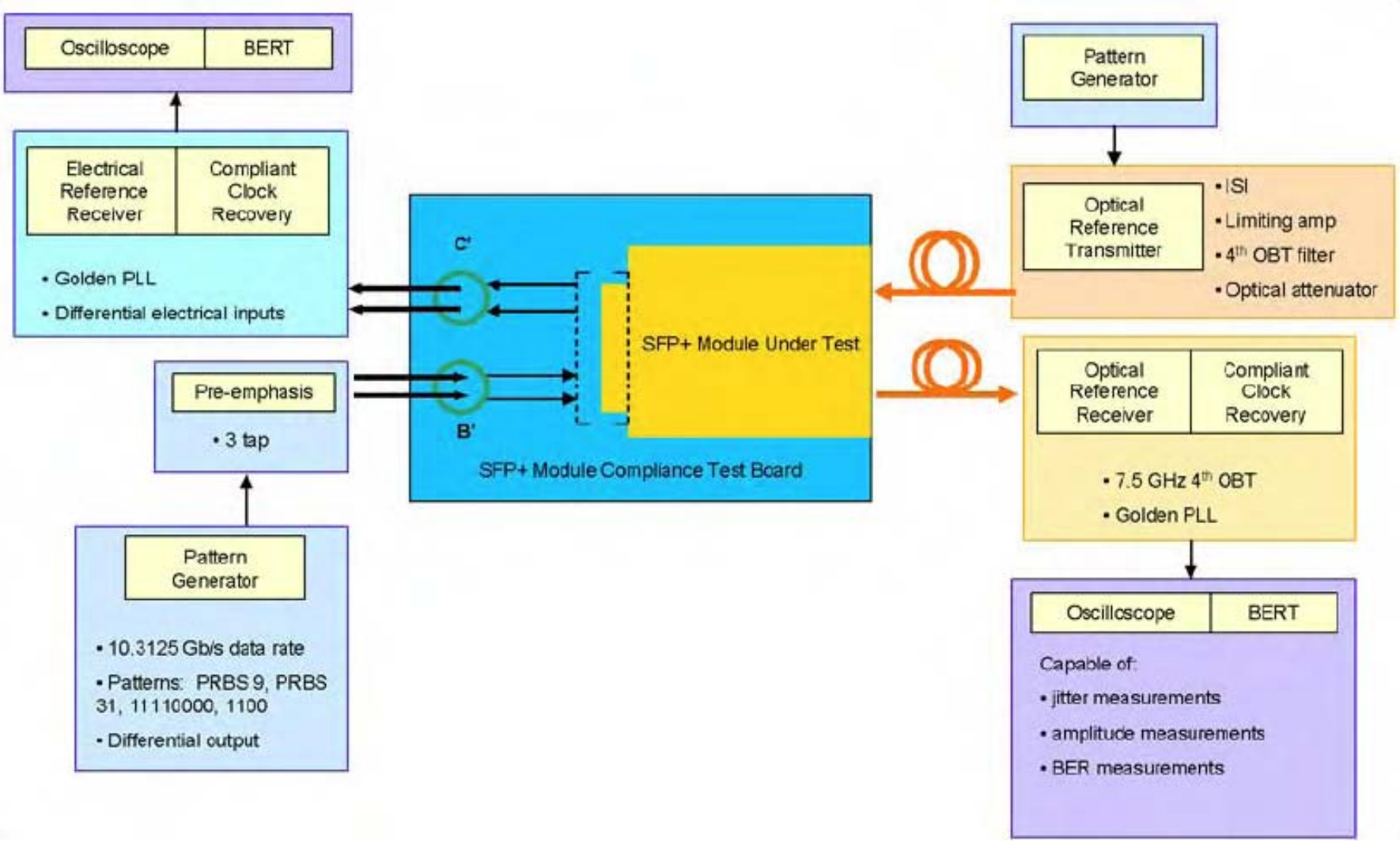
10GE SFP+ Module Test Setup



10GE SFP+ Active Cable Test Setup

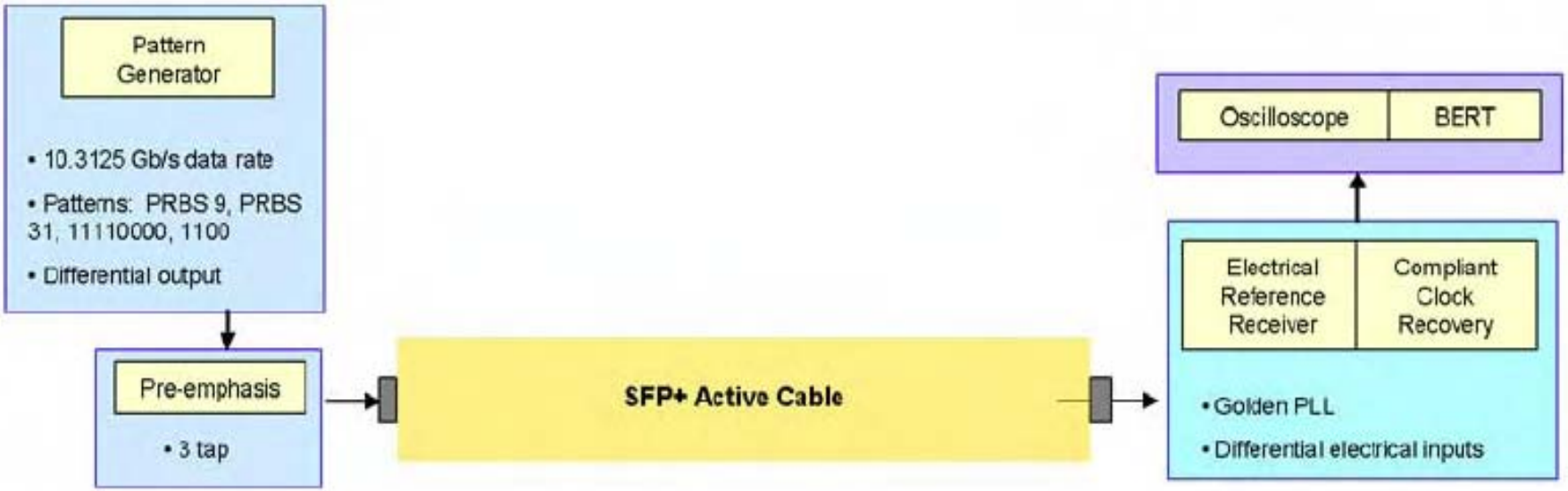
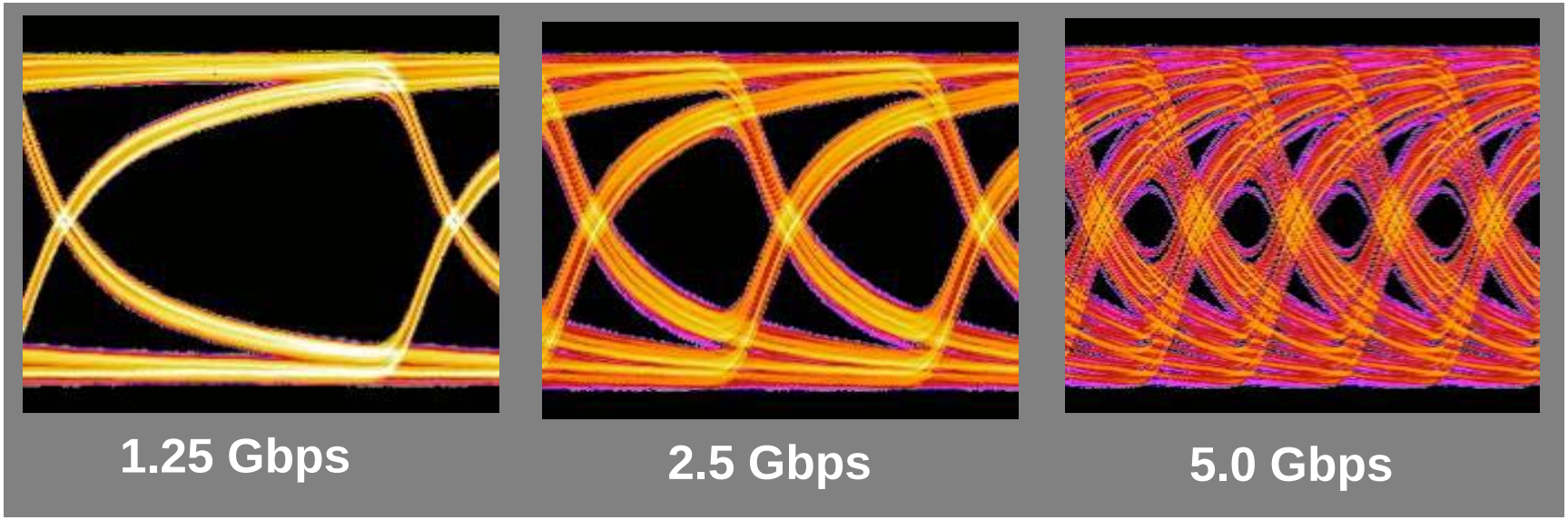


Diagram showing key voltage level, skew, wavelength coverage, and sensitivity requirements necessary to drive and test an SFP+ device for 10GbE compliance

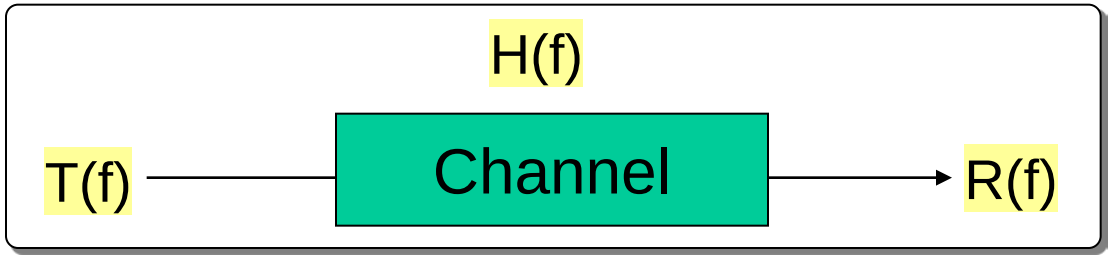
Need for Equalization

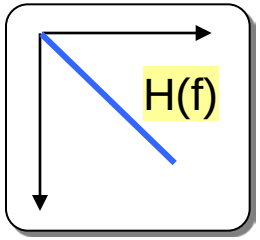
- At higher data rates, frequency dependent losses in channel lower transition speed, closing the eye at the receiver.

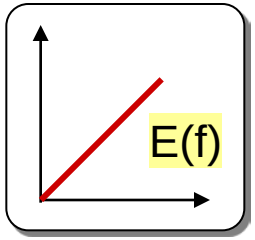


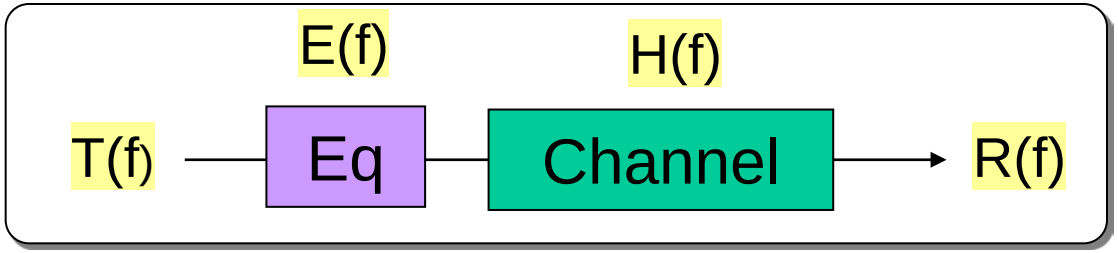
Applying Equalization

- Boosting (peaking) the signal with an equalization filter response which is the inverse of the channel loss restores the wave shape and eye opening at the receiver









If E(f) = 1/H(f),
then R(f) = T(f)

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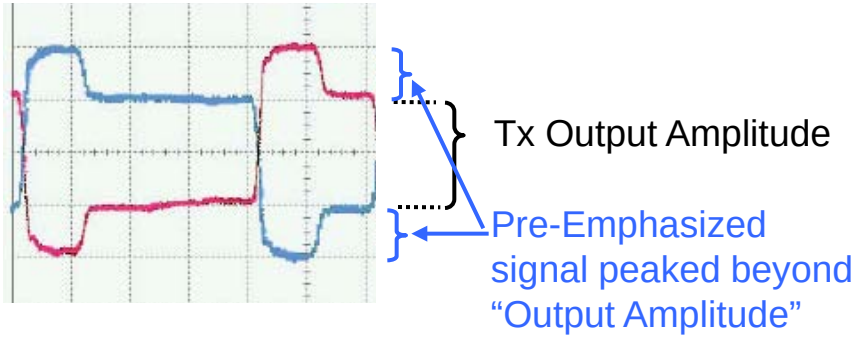
Equalizer Implementation

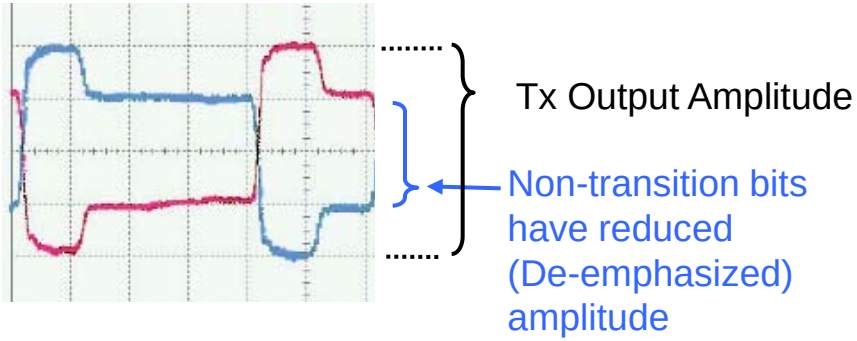
- Equalization can be located at Tx output or Rx input
  - Rx side boosts HF noise along with the signal, but Tx has limited voltage swing.
  - Tx side equalization is referred to as “Emphasis”
- Implementation can be either analog (linear) or digital
  - Linear gives more design resolution of response, but requires more chip area to implement
  - Response resolution of digital filters is determined by number of “taps”, each tap boosts or reduces response over 1 time interval

Pre-Emphasis versus De-Emphasis

- Both have the same wave shape, but amplitude specified differently
- Pre-Emphasis boosts the amplitude of the transition bit above the ongoing output amplitude



- With De-Emphasis, the specified amplitude refers to the transition bit, with the remaining bits reduced in amplitude

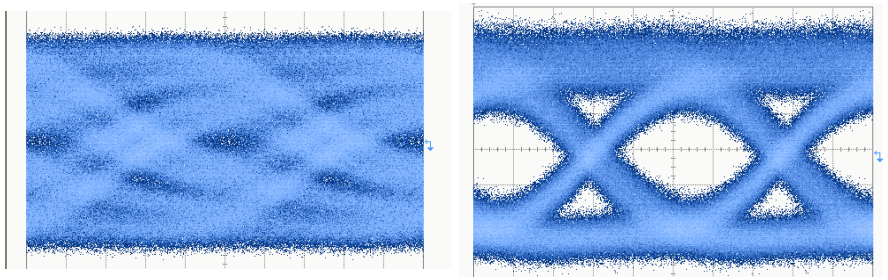


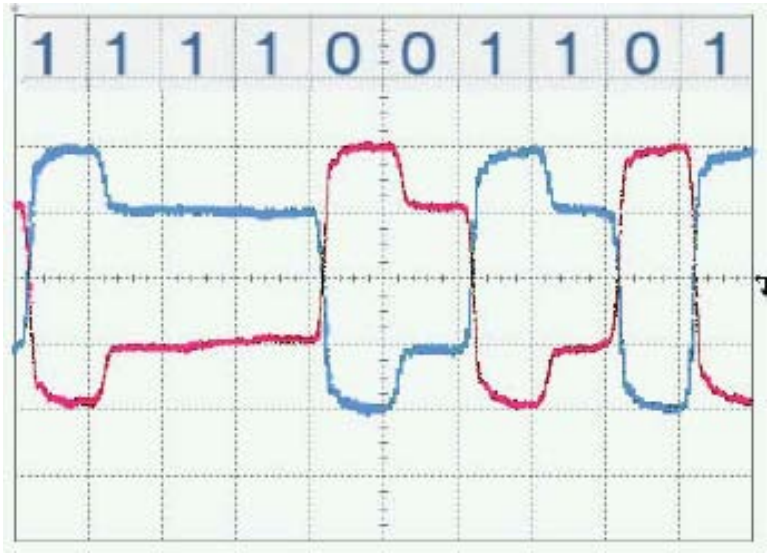
PPG12500: Programmable Pattern Generator

- *Includes many Telecom and Serial Data preloaded RAM patterns*
  - *Examples: CRPAT, CJPAT, K28-3, K28-5, K28-7, and PRBS 2N [N = 7, 9,10, 11, 13, 15, 23, 29, 31] , 1100,1010, etc.*
- *Create custom patterns in binary or hexadecimal format*
- *Check syntax of custom patterns to ensure file integrity*
- *Save pattern files to PC disk drive*
- *Upload custom patterns to a PPG*

Integrated De-Emphasis

- Used in higher data rate systems to open closed eyes at receiver
  - HF peaking at transmitter to counteract the HF loss in channel
- 2-Tap (acts on consecutive bit or bits of same logic state after transition)





Differential data signal Blue = D+, Red = D-

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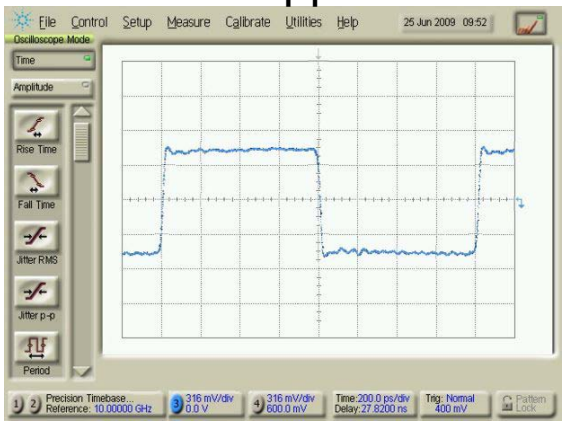
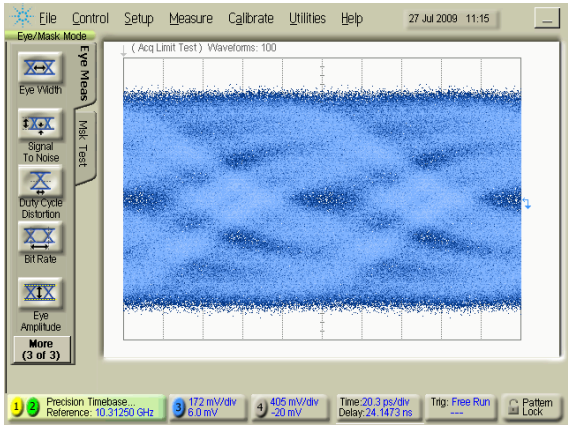
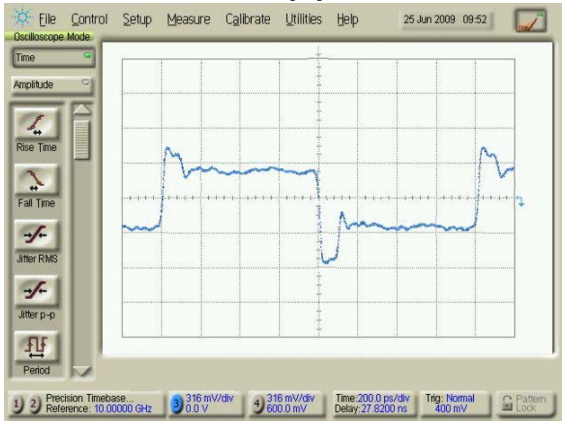
Effect of De-Emphasis on Eye Opening

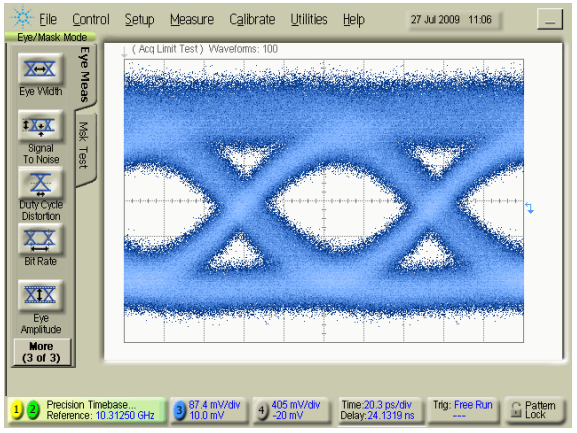
0db applied





6db applied





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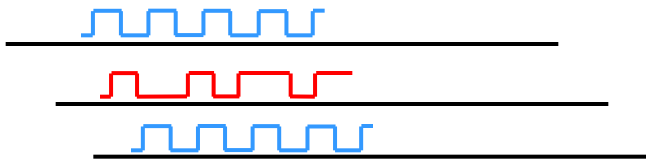
SPEED INNOVATION

PPG12500: Summary

- *Flexible and Low Cost PG solution for TX generation*
- *Supports Programmable Patterns and PRBS generation*
- *Built-in 2-tap De-emphasis (0-20db),* ***4-tap is coming in June!***
- *Jitter Tolerance Measurement when combined with Centellax Clock Synthesizer with Sinusoidal jitter injection capability*
- *BER testing with Centellax Programmable Error Detector*

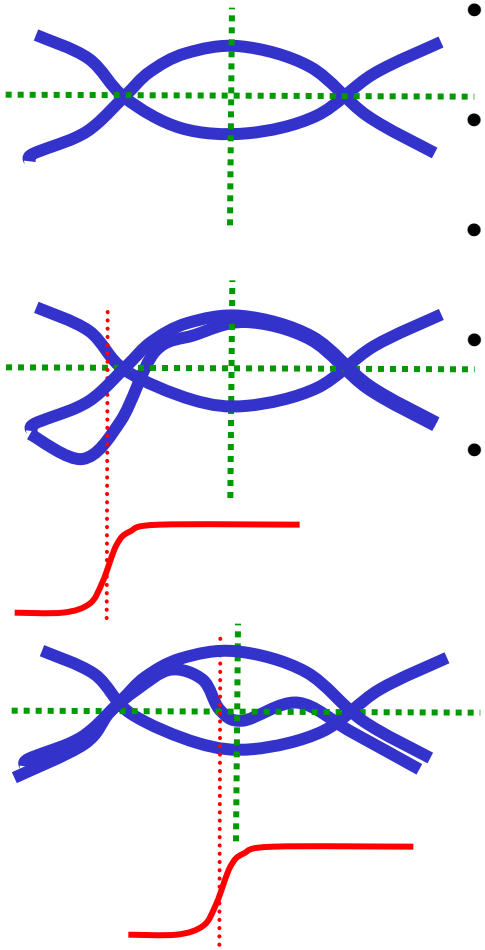
PCB12500: Parallel Channel BERT for Cross Talk Testing

- Test channel with cross talk in adjacent channels/lanes (victim – aggressor testing)

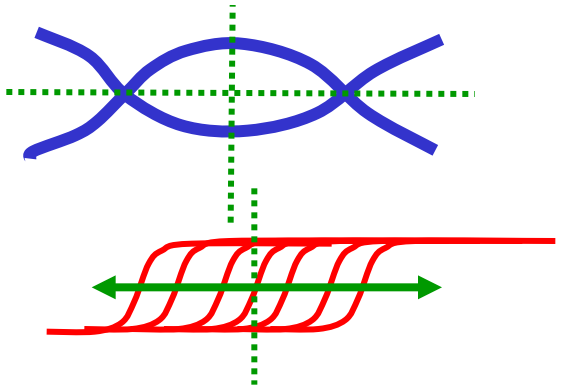


  - Multi lane standards – QSFP
  - Backplanes

Delay Sweep Phase Interference



- Victim is most susceptible to crosstalk induced errors at receiver sample point – near center of eye.
- Use of 1010 clock for aggressor signal does not guarantee edge at sample point – cable phase delay variations
- Effective crosstalk testing requires varying the phase of aggressor.
- Phase Interference sweeps phase relative to clock ±½, 1, or 2 UI, user selectable
- Triangular modulation, unique low frequency on each channel (7 - 19 Hz)



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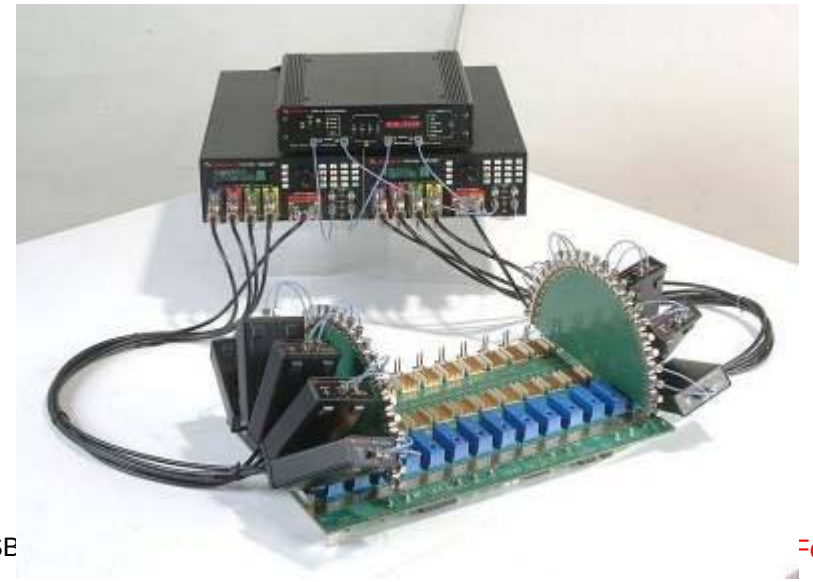
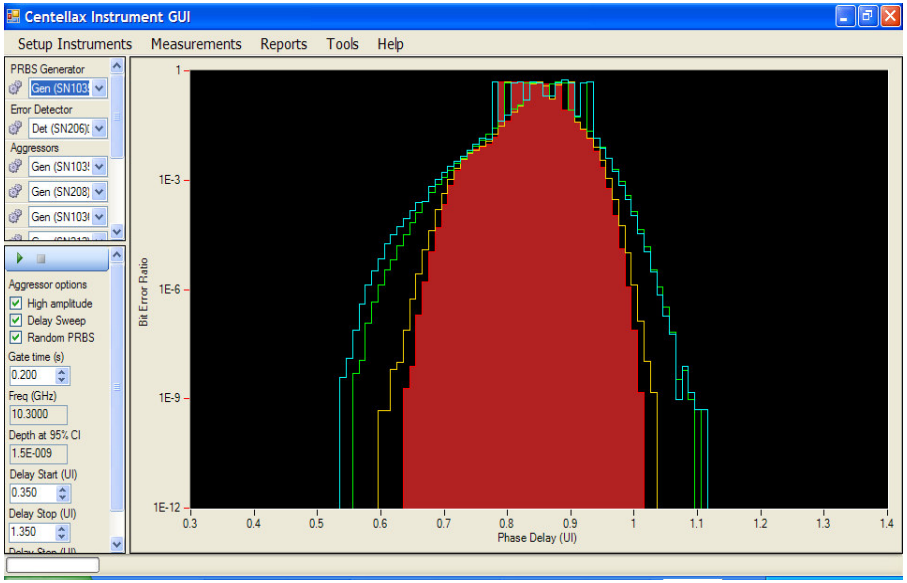
How is crosstalk measured?

– Time-domain measurement of victim channel jitter

1. Measures the increase of jitter on a victim channel
2. Requires pattern generator(s) and oscilloscope/BERT
3. This method accounts for multiple aggressors and measures the most important metric of a datacom link: the eye opening





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SPEED INNOVATION

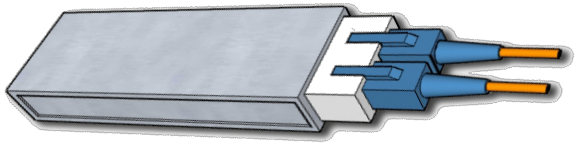
Key Messages / Value Proposition

- Cost Effectiveness
  - “Half the price with no sacrifice in signal quality”
  - Independent control of heads can eliminate signal switching
- Ease of system integration
  - Single control point for pattern generation, error detection
  - Less cabling, no external mixers or modulators
- Generator Integrated De-Emphasis
  - (cost effective and simpler integration) + no loss from extra cable lengths.

SB40 Overview

- Single channel serial Bit Error Rate Tester (BERT)
- Supports very high data rates (40, 28 & 25 Gb/s)
- Modular System comprised of 3 instruments
- Very cost effective compared to competitive systems

Opto-Electronic Devices



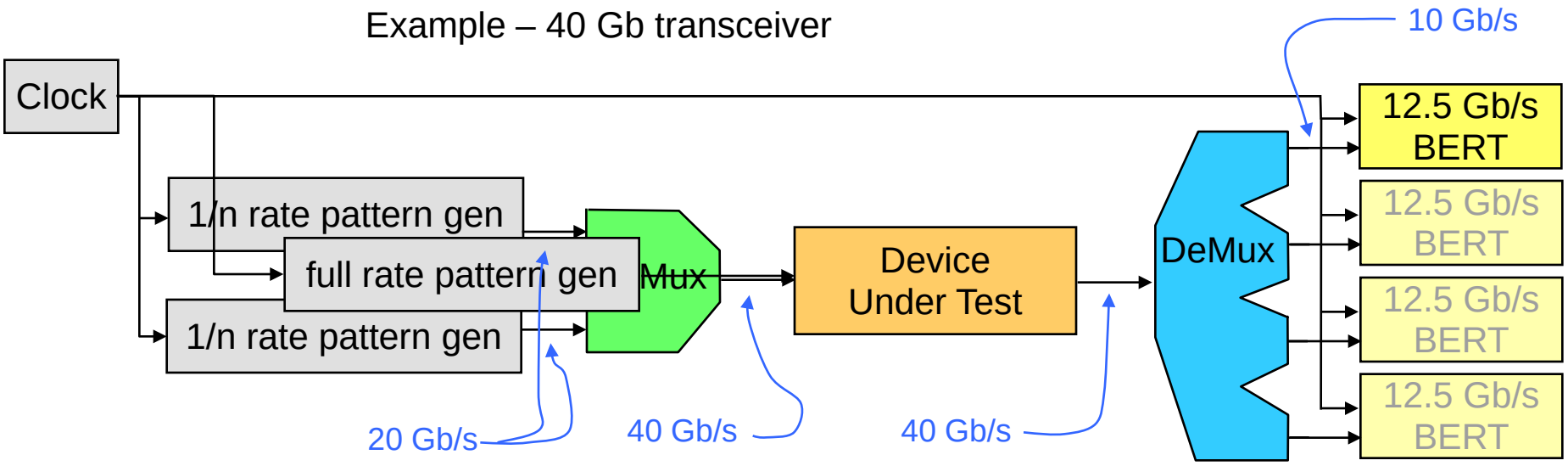
- Shift from 10 G to 40 G systems
  - Enabling technologies in long haul optical components make 40 Gb/s practical for telecom use
  - Great reduction on costs allow 40 Gb/s use in datacom / server farm applications
- Device terminology:
  - Transceivers = optical transmitter and receiver with straight full-rate OE and EO conversion. Need 25 and 40Gb/s BERTs
  - Transponders = optical transmitter and receiver with clock recovery, framing, mux/demux in same package. I/O is multiple lower data rate electrical signals. (e.g. 4 X10G, 16 X 2.5G)
    - Can use lower speed BERTs

Overview of high data rate BERTs

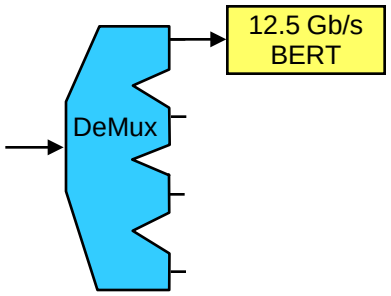
- The pattern generator (PG) and error detector (ED) in low to intermediate speed BERTs usually operate at the full data rate.
- Both the PG and ED are often in the same housing (“single box”)
- Logic to support high data rates (>13 Gb/s) is limited to simple implementations
  - Dissipates high power & requires transmission line interconnection
  - Practically limited to a few gates or flip-flops / package (Low level of integration)
- High data rate O/E transponders mux / demux optical data into several slower electrical streams in same package
- Same limitations apply to instrumentation – complex measurements performed on divided lower data rate streams

High Data Rate BERT Topology

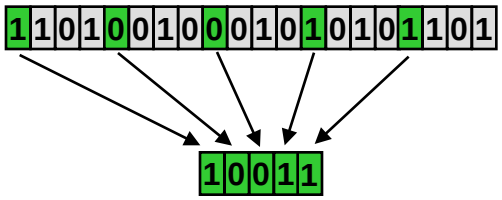
- Streams from fractional rate pattern generators are multiplexed together to full rate to drive DUT
  - Some implementations use full rate pattern generators
- Full rate output passes through demultiplexer to feed lower rate BERT (single or multiple)



Pattern Requirements for Sub- Rate BER Measurement



Full Rate Pattern

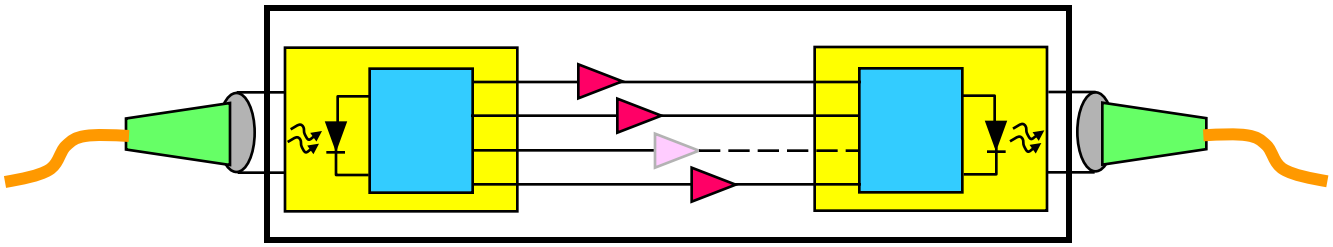


BERT ED Pattern
(1/4 data rate)

- Because BERTs sample sub-rate data, in general error detector pattern ≠ full rate pattern
- ED pattern is the decimated version of full rate pattern (retain every *n*th bit)
- PRBS patterns decimated to a binary divisor automatically produce the same PRBS pattern at lower rate
  - i.e. every 4th bit of a PRBS-7 pattern is the same PRBS-7 pattern.

Do I need a BERT on all DeMux outputs?

- Ideally – YES, however a single BERT can work, if:
  - Random events will equally disperse on all DeMux outputs.
  - Pattern lengths not an even multiple of demultiplexer ratio will circulate through all outputs.
    (will measure pattern dependent errors)
- Math works – subrate BERTs count 1/*n* errors on 1/*n* bits
- Measuring a single demultiplexer output will not count subrate clock related errors
  - Possible if the DUT uses Mux and DeMux sub-rate data streams



Notes when using multiple BERTs

- Possible to use single BERT with switching to monitor each demultiplexer output sequentially
- Do not interrupt demultiplexer when switching BERT to next output.
  - Individual output offset to full rate clock may change if test is interrupted
- To calculate total BER, don’t use individual BER measurements from each demultiplexer output
  - Combine total bit count and total error count, then divide these totals

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SPEED INNOVATION

SB40 Key Features

22 – 44 Gbps Operation

- One system covers 40, 28 and 25 Gb/s standards
  - Broadband option in the pattern generator is required to support the lower speeds (22-37Gb/s)
- Additional speed to accommodate headroom for data encoding and Forward Error Correction (FEC)
- De-multiplexer operates in either 1:4 or 1:2 modes to optimize configuration for data rate
- Flexible clock dividers support virtually any configuration

Flexible Source Capability

- Built in 39.8 Gb/s clock oscillator for 40 Gb/s applications
  - Options for 25 and 28GHz oscillators
  - Operation at other bit rates requires an external synthesizer
- True hardware PRBS generation with PRBS-7, PRBS-15, and PRBS-31 patterns
- Operates in differential or single ended configurations
- Optional output drivers amplifiers for Lithium Niobate or Electro Absorption laser modulator applications
- Pattern trigger and divided clock outputs for scope trigger.

Choice of BERTs

- TG1B1-A 10 G BERT cost effective for monitoring one Demultiplexer output
  - Can add additional TG1B1-A to measure all data

- PCB12500 with TR2P1A Error Detector heads – compact, low cost method to measure all data
  (coming soon)

SB40 System Components

- TG1P4A 22 – 44 Gb/s PRBS Source
  - Built in 39.8 Gb/s oscillator
  - Options for 25G and 28G operation
- TR1D4A 40 G Clock and Data Demultiplexer
  - Configurable as 1:4 or 1:2 demultiplexer

- TG1B1-A 10 G BERT (1, 2 or 4)

or

- PCB12500 TR2P1A Parallel Channel BERT with Error Detector Heads (1, 2, or 4)

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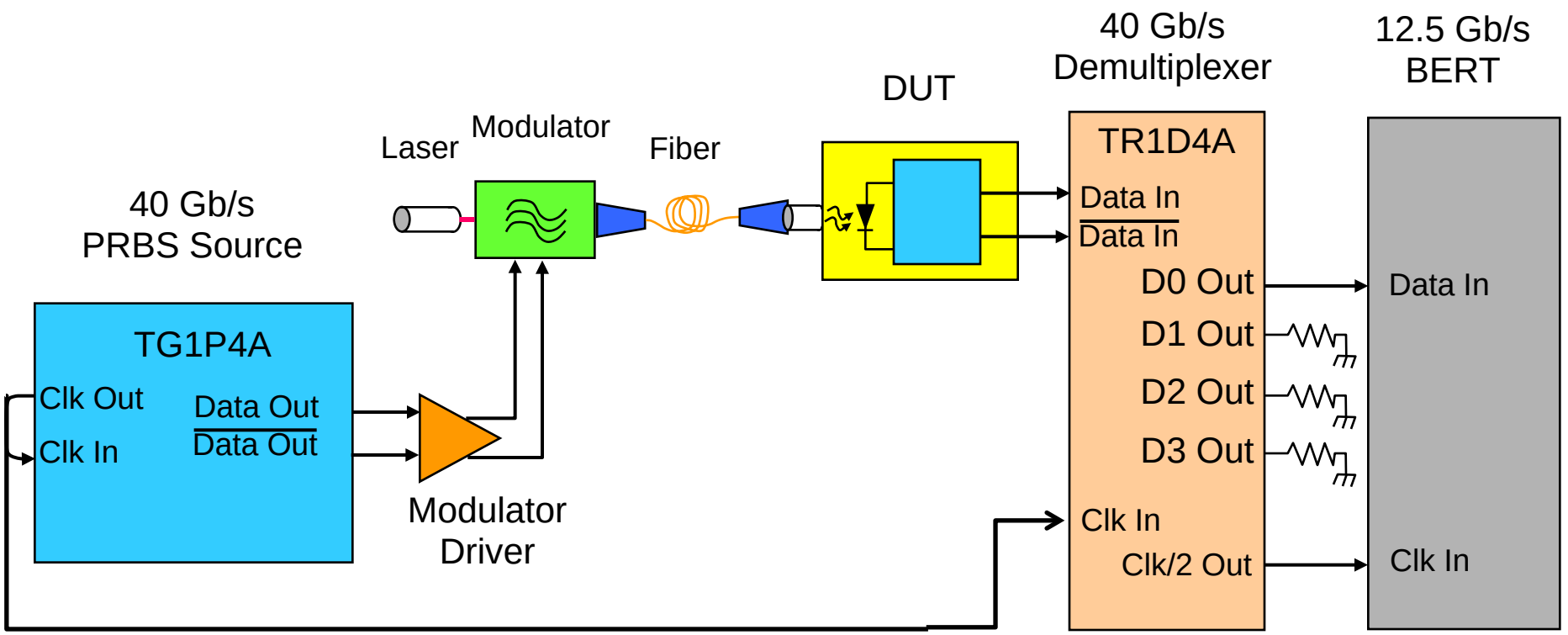
SPEED INNOVATION

SB40 Configurations

SB40 System with
1x TG1B1-A 10G BERT

SB40 System with
PCB12500 and
4x TR2P1A
Error Detector Heads

Typical Configuration: 40 Gb/s receiver application



User Control Interface

PRBS Source and Demultiplexer are manually configured

- Switch selection and cable connections used to configure system

- BERTs have front panel controls as well as remote program control
  - TG1B1-A has dedicated pushbutton controls
  - PCG12500 uses display defined buttons, numeric keypad and knob for parameter entry and editing

LabView Drivers and GUI

- LabView drivers on the web site for TG1B1-A and SB40 configuration
  - SB40 configuration allows gated BER measurements on 4x TG1B1-A
  - Version with PCB12500/TR2P1A available soon
- Provide GUI which shows all control parameters at once
- Driver only and self executable versions available
- Set up guide for installing LabView libraries and run time engine
- SCPI Command Set documented in TG1B1A manual for users who need to program outside of LabView environment

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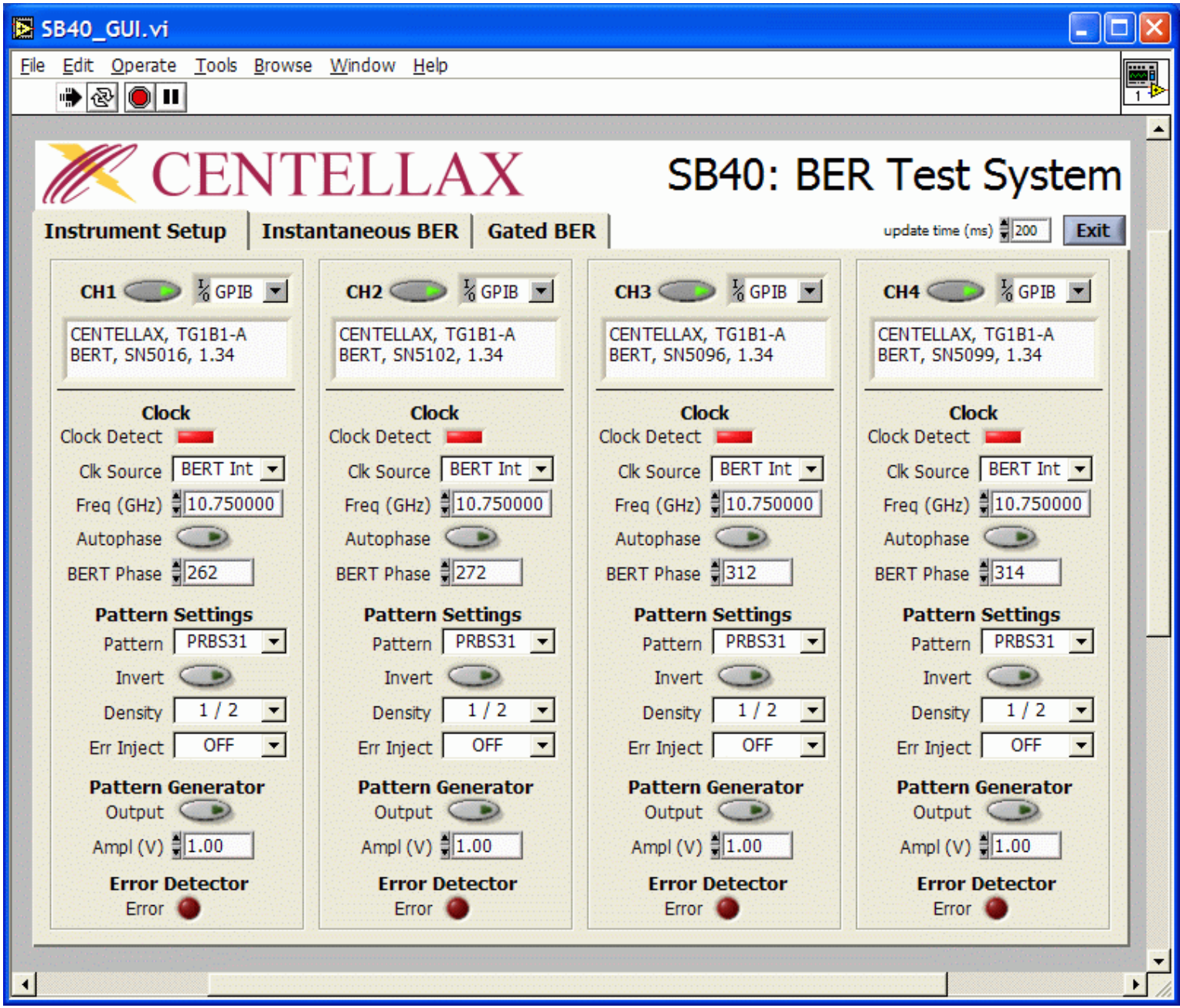
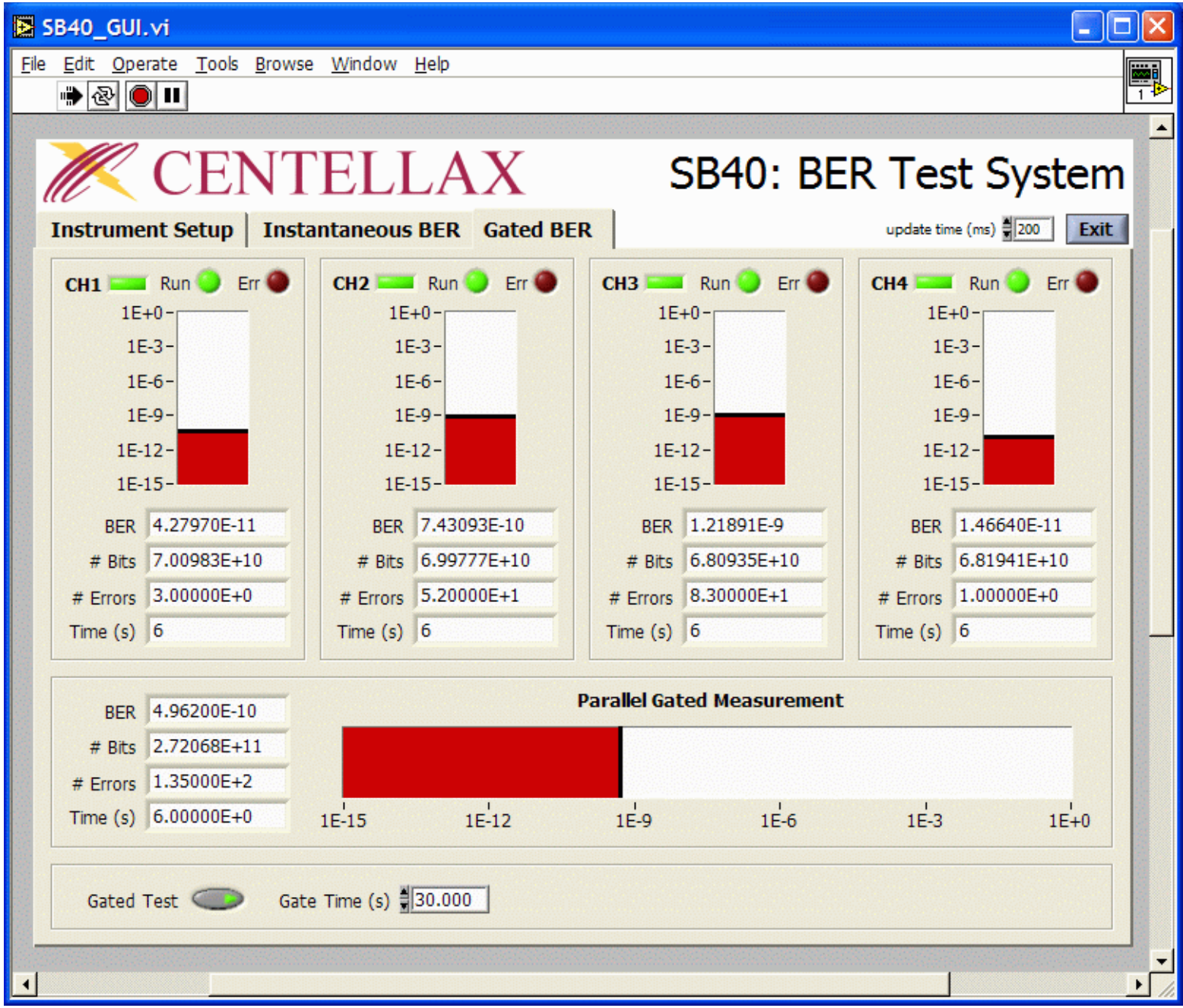
SPEED INNOVATION




SB40_GUI.vi
File Edit Operate Tools Browse Window Help
CENTELLAX
SB40: BER Test System
Instrument Setup
Instantaneous BER
Gated BER
update time (ms) 200
Exit
CH1 Run Err
1E+0
1E-3
1E-6
1E-9
1E-12
1E-15
BER 4.27970E-11
Bits 7.00983E+10
Errors 3.00000E+0
Time (s) 6
CH2 Run Err
BER 7.43093E-10
Bits 6.99777E+10
Errors 5.20000E+1
Time (s) 6
CH3 Run Err
BER 1.21891E-9
Bits 6.80935E+10
Errors 8.30000E+1
Time (s) 6
CH4 Run Err
BER 1.46640E-11
Bits 6.81941E+10
Errors 1.00000E+0
Time (s) 6
BER 4.96200E-10
Bits 2.72068E+11
Errors 1.35000E+2
Time (s) 6.00000E+0
Parallel Gated Measurement
1E-15 1E-12 1E-9 1E-6 1E-3 1E+0
Gated Test
Gate Time (s) 30.000

SB40 Product Positioning (Customer Screening)

- SB40 is a cost effective tool for characterizing of components and systems used at high data rates
  - 40 Gb/s – OC 768, STM 256
  - 25 Gb/s – 100 GBase LR4/ER4 (4 X 25G)
  - 28 Gb/s – 100 Gbase with FEC (4 x 28G)
- Anyone who works with the electrical signal at these data rates is a candidate for a BERT

Key Messages / Value Proposition

- Cost Effectiveness
  - Lowest cost BERT operating at these data rates
  - Flexible BERT options for measuring one or all sub-rate demultiplexer outputs
  - Even lower cost for measuring all data with PCB12500 BERT
- Simpler Configuration
  - Internal oscillator and full operation in the PRBS source eliminate external clock synthesizers and data multiplexers
- Compact Size
  - Smaller components in modular system require less bench or rack space – Important in production test environments

Centellax Support

If you have questions or need more assistance with this product, please contact us:

sales@centellax.com for pricing and availability

support@centellax.com for technical assistance

marketing@centellax.com for materials and demos

SB40 webpage http://www.centellax.com/products/testmeas/40g_bert.shtml

TG1P4A PRBS generator webpage http://www.centellax.com/products/testmeas/40g_prbs.shtml

TR1D4A De-multiplexer webpage http://www.centellax.com/products/testmeas/accessories/TR1D4A.shtml

10G BERT webpage http://www.centellax.com/products/testmeas/10g_bert.shtml

PCB12500 webpage http://www.centellax.com/products/testmeas/PCB12500

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Thank You